TG12864R-04 VER:00

Specification For Approval

Customer Approval:_____ Date:_____

Prepared:_____Check:_____Approval:_____

Date:_____Date:_____Date:_____

Description

REV.	DESCREPTION	DATE
V00	First issue	Nov-16-2006

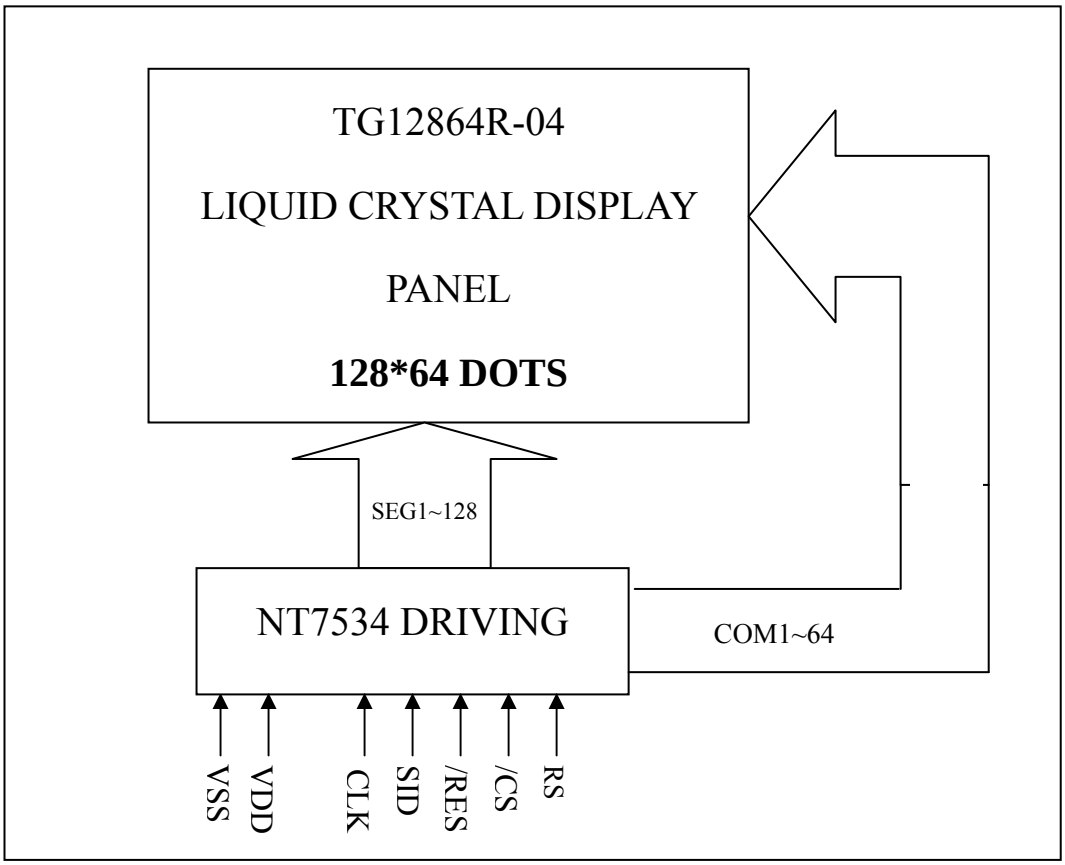
CONTENTS

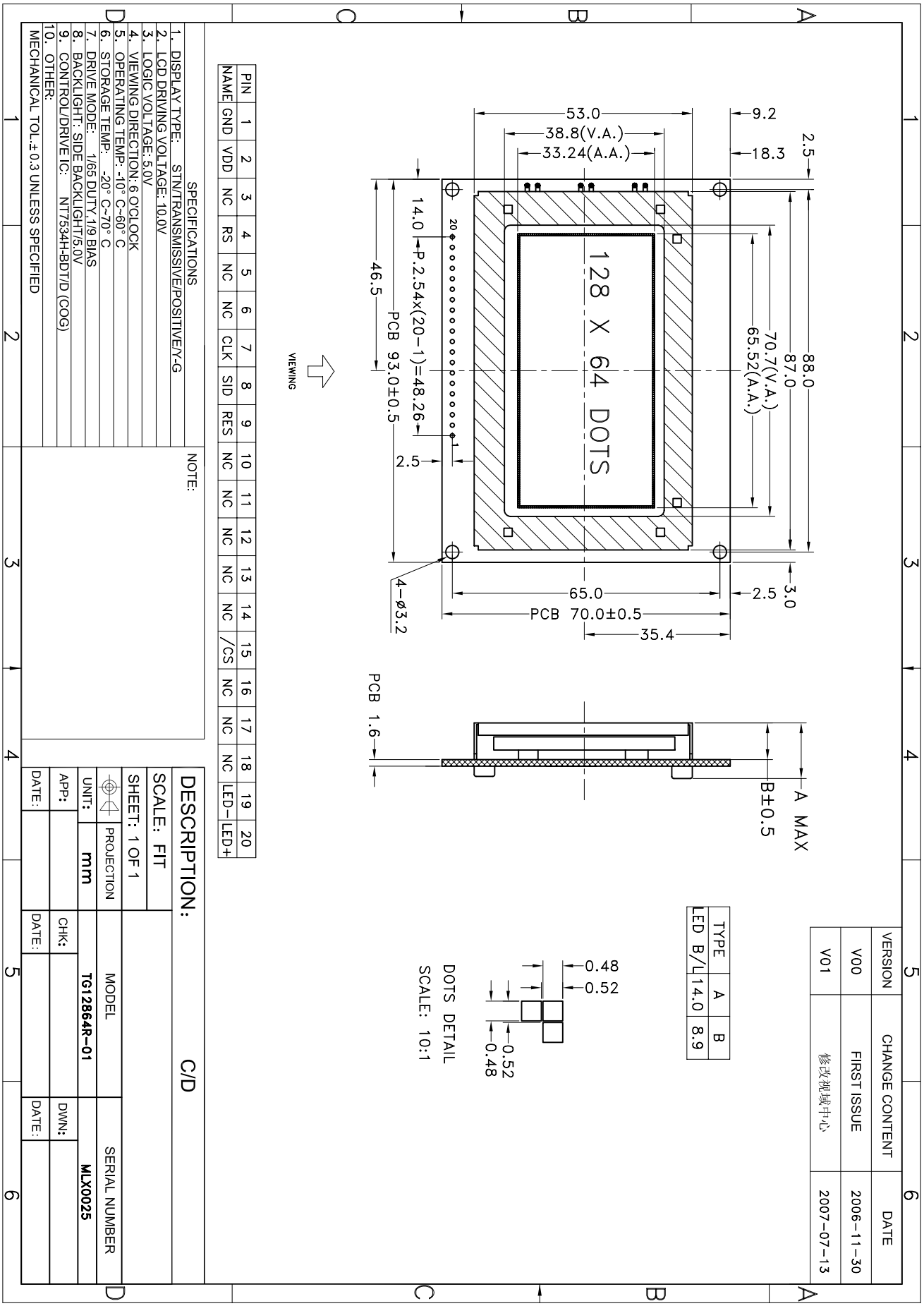
1 . SPECIFICATIONS

1.1 FEATURES

Item	Contents	Unit
LCD type	STN/Transmissive/Negative/Blue	--
LCD duty	1/65	--
LCD bias	1/9	--
Viewing direction	6	o'clock
Module size(W x H x T)	93.0 X 70.0 X 13.5	mm
Viewing area(W x H)	70.7 X 38.8	mm
Number of dots	128 X 64	dots
Dots size(W x H)	0.48 X 0.48	mm
Dots pitch(W x H)	0.52 X 0.52	mm

1.2. BLOCK DIAGRAM





VERSION	CHANGE CONTENT	DATE
V00	FIRST ISSUE	2006-11-30
V01	修改视域中心	2007-07-13

TYPE	A	B
LED B/L	14.0	8.9

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NAME	GND	VDD	NC	RS	NC	NC	CLK	SID	RES	NC	NC	NC	NC	NC	/CS	NC	NC	NC	LED-	LED+

SPECIFICATIONS

1. DISPLAY TYPE: STN/TRANSMISSIVE/POSITIVE/Y-G
2. LCD DRIVING VOLTAGE: 10.0V
3. LOGIC VOLTAGE: 5.0V
4. VIEWING DIRECTION: 6 O'CLOCK
5. OPERATING TEMP: -10° C~60° C
6. STORAGE TEMP: -20° C~70° C
7. DRIVE MODE: 1/65 DUTY,1/9 BIAS
8. BACKLIGHT: SIDE BACKLIGHT/5.0V
9. CONTROL/DRIVE IC: NT7534H-BDT/D (COG)
10. OTHER:

MECHANICAL TOL.±0.3 UNLESS SPECIFIED

NOTE:

DESCRIPTION: C/D

SCALE: FIT

SHEET: 1 OF 1

PROJECTION

UNIT: mm

APP: DATE:

CHK: DATE:

DWN: DATE:

MODEL	SERIAL NUMBER
TG12864R-01	MLX0025

1.4 ABSOLUTE MAXIMUM RATINGS

(T_A = 25ºC , VSS =0 V)

Parameter	Symbol	Min	Max	Unit
Supply voltage for module	V_{DD}	-0.3	5.5	V
Supply voltage for LCD	V_o	-0.3	14.5	V
Input voltage	V_I	-0.3	V_{DD} +0.3	V
Normal Operating temperature	T_{OP}	-10	+60	℃
Normal Storage temperature	T_{ST}	-20	+70	℃

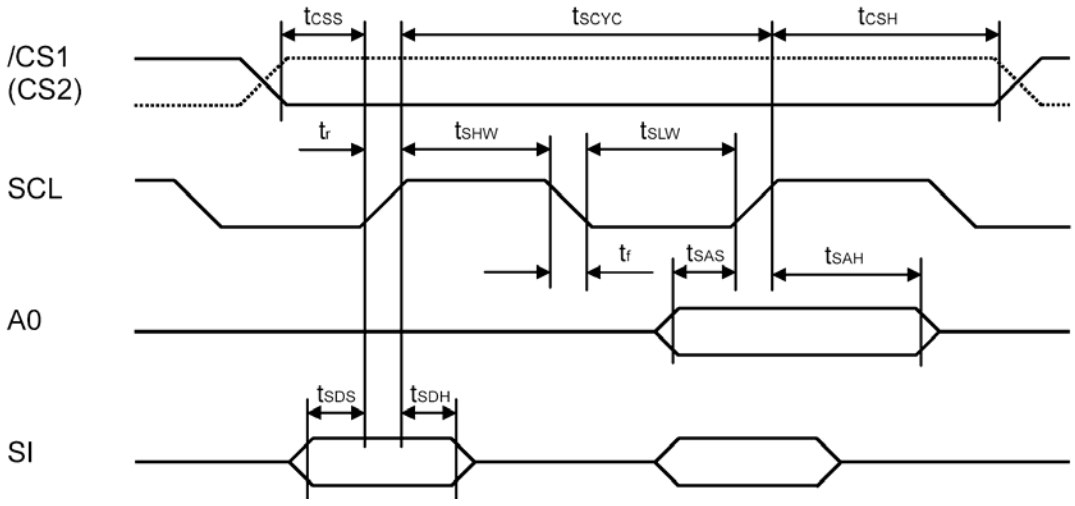
1.5 DC ELECTRICAL CHARACTERISTIC

(T_A = 25ºC , VSS =0 V)

Parameter	Symbol	Condition	Min	Type	Max	Unit
Supply voltage for module	VDD	--	4.8	5.0	5.2	V
Supply current for logic	IDD	--	--	--	4.5	mA
Operating voltage for LCD	V0	25℃	10.0	10.2	10.4	V
Input voltage “ H ” level	VIH	--	0.8VDD	--	VDD	V
Input voltage “L” level	VIL	--	0	--	0.2VDD	V

1.6 AC CHARACTERISTIC

Serial Interface Timing

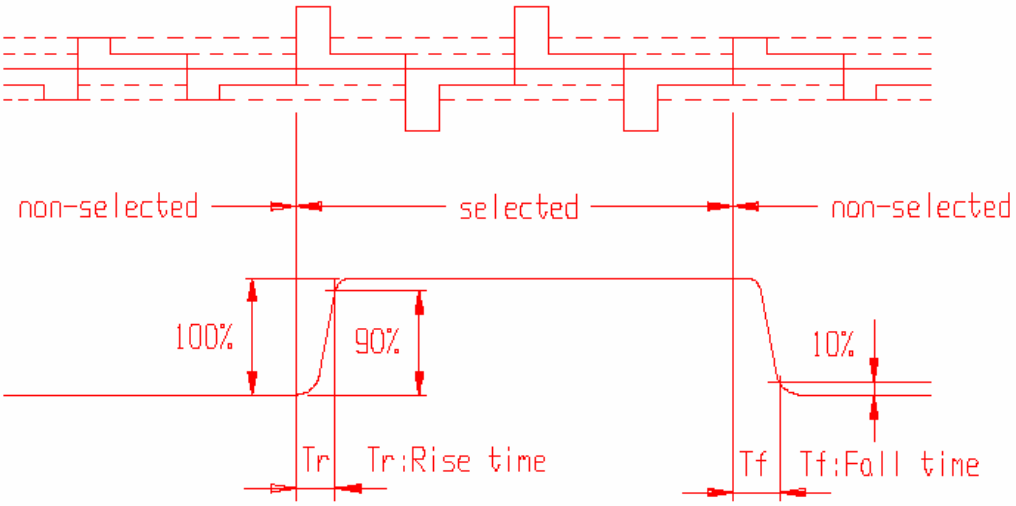


(Ta = -10 ~ +60 ° C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tscyc	Serial clock cycle	120	-	-	ns	SCL
tshw	Serial clock H pulse width	60	-	-	ns	SCL
tslw	Serial clock L pulse width	60	-	-	ns	SCL
tsas	Address setup time	30	-	-	ns	A0
tsah	Address hold time	20	-	-	ns	A0
tsds	Data setup time	30	-	-	ns	SI
tsdh	Data hold time	20	-	-	ns	SI
tcss	Chip select setup time	20	-	-	ns	/CS1, CS2
tcsh	Chip select hold time	40	-	-	ns	/CS1, CS2

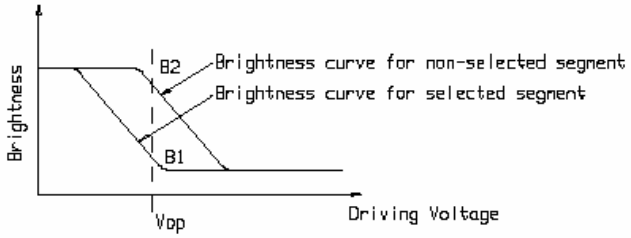
1.7 ELECTRO-OPTICAL CHARACTERISTICS

Note1: Definition of response time.

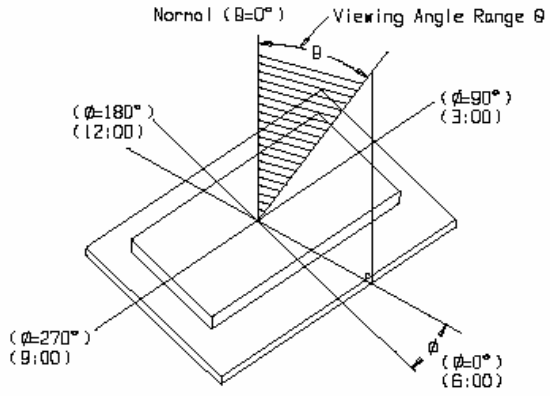


Note2: Definition of contrast ratio 'Cr' .

$$Cr = \frac{\text{Brightness of non-selected segment(B2)}}{\text{Brightness of selected segment(B1)}}$$



Note3: Definition of viewing angle range 'θ'.



1.8 BACKLIGHT CHARACTERISTIC

1.8.1 ABSOLUTE MAXIMUM RATINGS(Ta=25℃)

Item	Symbol	Conditions	Rating	Unit
Absolute maximum forward current	Ifm		75	mA
Peak forward current	Ifp	I macc 脉冲，1/10 占空比 I msec plus 10% Duty Cycle	180	mA
Reverse voltage	V_r		5.0	V
Power dissipation	P_d		240	mW
Operating Temperature Range	T_{OPr}		-20~+60℃	℃
Storage Temperature Range	Tstg		-30~+70℃	℃

1.8.2 ELECTRICAL –OPTICAL CHARACTERISTICS(Ta=25℃)

Color: White

Item	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	vr	3.0	3.2	3.4	V	If = 45mA
Reverse Current	I_r	--	--	40	uA	Vr = 5.0 V

2. MODULE STRUCTURE

2.1 INTERFACE PIN DESCRIPTION

Pin	Symbol	Level	Description
1	**GND**	0V	Ground
2	**VDD**	+5.0V	Power supply for logic operating.
3	**NC**	--	No connection.
4	**A0(RS)**	H/L	A0 = "H": Indicates that SID is display data. A0 = "L": Indicates that SID is control data.
5	**NC**	--	No connection.
6	**NC**	--	No connection.
7	**CLK**	H/L	This is a serial clock.
8	**SID**	H/L	This is a serial data.
9	**RES**	H/L	When /RES = L, the settings are initialized.
10	**NC**	--	No connection.
11	**NC**	--	No connection.
12	**NC**	--	No connection.
13	**NC**	--	No connection.
14	**NC**	--	No connection.
15	**/CS**	H/L	This is the chip select signal. When /CS1 = L, then the chip select becomes active.
16	**NC**	--	No connection.
17	**NC**	--	No connection.
18	**NC**	--	No connection.
19	**K**	0V	The backlight.
20	**A**	+5.0V	Power Supply for backlight.

2.2. COMMAND TABLE

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation

Command table(continue)

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

***Note: Do not use any other command, or system malfunction may result.**

2.3. COMMAND DETAIL EXPLAIN

2.3.1. Display ON/OFF

Alternatively turns the display on and off.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**Display on**
										0	**Display off**

When the display OFF command is executed when in the display all points ON mode, the power save mode is entered. See the section on the power saver for details.

2.3.2 . Set Display Start Line

Specifies line address to determine the initial display line, or COM0. The RAM display data becomes the top line of the LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. This command changes when the line address, smooth scrolling or a page change take place.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**0**	**0**	**1**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

2.3.3. Set Page Address

Specifies the page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	**/RD**	**/WR**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	**1**	**0**	**1**	**0**	**1**	**1**	**A3**	**A2**	**A1**	**A0**

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

2.3.4. Set Column Address

It specifies column address of display RAM. It divides the column address into 4 higher bits and 4 lower bits. Set each of them in succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental during each access until address 132 is accessed. The page address is not changed during this time.

A0	**/RD**	**/WR**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**	
0	**1**	**0**	**0**	**0**	**0**	**1**	**A7**	**A6**	**A5**	**A4**	Higher bits
0	**1**	**0**	**0**	**0**	**0**	**0**	**A3**	**A2**	**A1**	**A0**	Low bits

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

2.3.5. Read Status

A0	**/RD**	**/WR**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	**0**	**1**	**busy**	**ADC**	**On/off**	**reset**	**0**	**0**	**0**	**0**

Busy: When high, the NT7534 is busy due to the internal operation or reset. Any command is rejected until BUSY becomes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address "131-n" corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command

RESET: Indicates that the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is reset.

2.3.6. Write Display Data

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	Write data							

2.3.7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after the column address setup. Refer to the display RAM section of the FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Read data							

2.3.8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of following. When display data is written or read, the column address is incremented by 1 as shown in following:

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	0	0	D

When D is low, rotation is to the right (normal direction)

When D is high, rotation is to the left (reverse direction)

2.3.9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display)

When D is high, the RAM data is low, being LCD ON potential (reverse display)

2.3.10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

2.3.11. Set LCD Bias

This command selects the voltage bias ratio required for the liquid crystal display.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	1	0	D

When D is low, 1/9 bias is selected.
When D is high, 1/7 bias is selected.

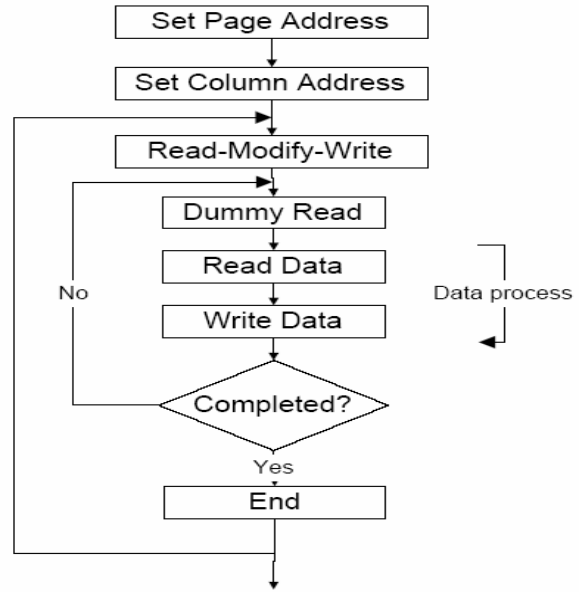
2.3.12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, the column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until the End command is issued. When the End is issued, the column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed when the cursor is blinking or other events.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

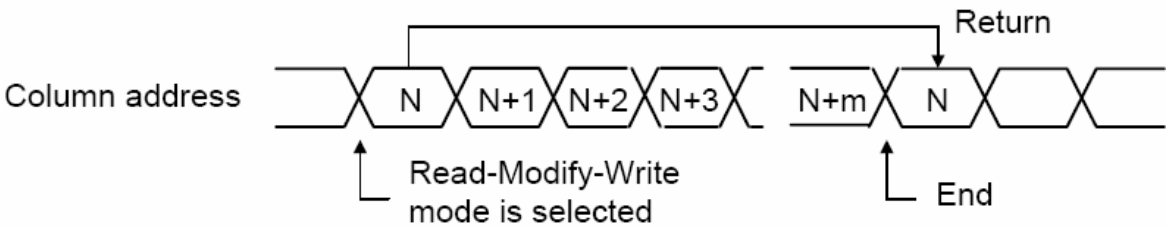
Cursor display sequence



2.3.13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued).

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	1	1	1	0



2.3. 14. Reset

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize the LCD power supply. Only the Reset signal to the /RES pad can initialize the supplies.

2.3.15 Output Status Select Register

Applicable to the NT7534. When D is high or low, the scan direction of the COM output pad is selectable. Refer to

Output Status Selector Circuit in Function Description for details.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pad

D = 0: Normal (COM0 → COM63)

D = 1: Reverse (COM63 → COM0)

*: Invalid bit

2.3.16. Set Power Control

Selects one of eight-power circuit functions using a 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to the Power Supply Circuit section of the FUNCTIONAL DESCRIPTION for details.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 is low, the voltage follower turns off. When A0 is high, it turns on.

When A1 is low, the voltage regulator turns off. When A1 is high, it turns on.

When A2 is low, the voltage booster turns off. When A2 is high, it turns on.

2.3.17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under “The Power Supply Circuits”

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb / Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									:		:
								1	1	0	
								1	1	1	Large

2.3.18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a double byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume

register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	V0
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
0	1	0	*	*			:				:
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

2.3.19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands. This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes. The static indicator ON command is a double byte command paired with the static indicator registers, and these commands must be executed one after the other. (The static indicator OFF command is a single byte command.)

(1) Static Indicator ON/OFF When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command

A0	**/RD**	**/WR**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	**1**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**D**

D = 0: Static Indicator OFF

D = 1: Static Indicator ON

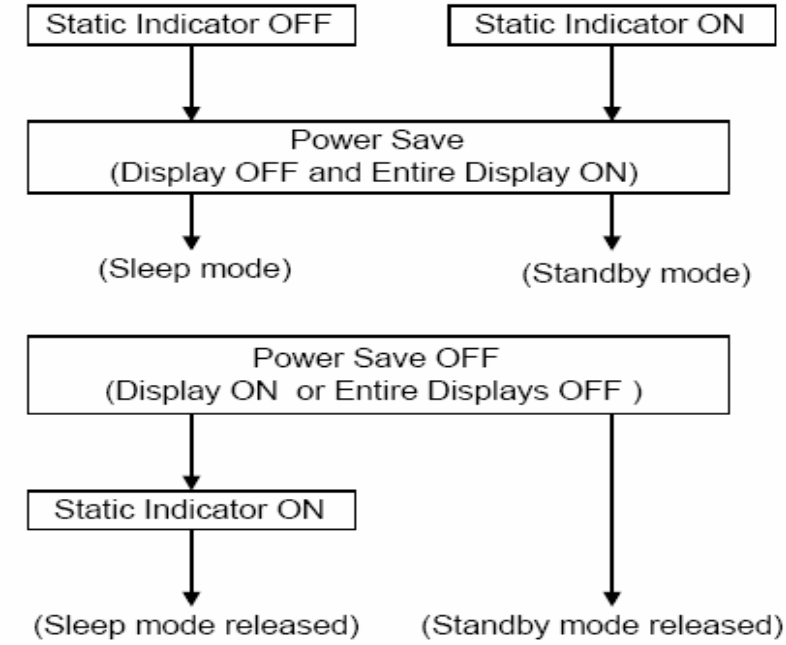
(2) Static Indicator Register Set

These commands set two bits of data into the static indicator register and are used to set the static indicator into a blinking mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately 0.5 second intervals
									1	0	ON (blinking at approximately 1 second intervals
									1	1	ON (constantly on)

2.3.20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption. If the static indicators are off, the Power Save command makes the system enter sleep mode. If it is on, this command makes the system enter standby mode. Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.

(2) Stops the LCD drives and outputs the Vss level as the segment/common driver output.

(3) Holds the display data and operation mode provided before the start of the sleep mode.

(4) The MPU can access the built-in display RAM.

Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for the static drive. The ON operation of the static drive system indicates that the NT7534 is in standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.

(2) Stops the LCD drive and outputs the Vss level as the segment / common driver output. However, the static drive system still operates.

(3) Holds the display data and operation mode provided before the start of the standby mode.

(4) The MPU can access the built-in display RAM. When the RESET command is issued in the standby mode, the sleep mode is set.

- When an external resistive driver gives the LCD driving voltage level, the current of this resistor must be cut so that it may be fixed to floating or Vss level, prior to or concurrently with causing the NT7534 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or Vss level, prior to or concurrently with causing the NT7534 to go into sleep mode or standby mode.

2.3.21. NOP

Non-Operation Command

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	1	1

2.3. 22. Test Command

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued inadvertently set the /RES input to low or issue the Reset command to release the test mode.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**0**	**1**	**1**	**1**	**1**	*****	*****	*****	*****

Cautions: The NT7534 maintains an operation status specified by each command. However, a high level of ambient noise may change the internal operation status. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended. The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

2.3. 23. Oscillation Frequency Select

This command is to select the oscillation frequency of driver IC as below.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Oscillation Frequency
0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	Typical 31.4 KHz
										1	Typical 26.3 KHz

2.3. 24. Partial Display Mode Set

This command enables to select the display mode. When D0 is low, the IC is in normal display mode, the maximum display duty ratio is decided by pin connection of DUTY0 and DUTY1 and the command LCD Bias Set decides the LCD bias ratio. The IC enters into partial display mode when D0 is high, then the commands Partial Display Duty Set and Partial Display Bias Set decide the LCD display duty and bias ratios.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Display Mode
0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	Normal Display
										1	Partial Display

2.3. 25. Partial Display Duty and Bias Set

These two commands set the LCD display duty and bias ratios when the IC is in partial display mode. They are invalid when the IC is in normal display mode. When the partial display duty is set, the LCD bias for partial display is set simultaneous as below. The partial display duty will be kept at maximum duty (decided by pins DUTY0 and DUTY1) when setting duty is larger than maximum duty.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Duty	Scanning Line
0	1	0	0	0	1	1	0	0	0	0	30h	1/9 duty	Line [0:7], COMS
								0	0	1	31h	1/17 duty	Line [0:15], COMS
								0	1	0	32h	1/33 duty	Line [0:31], COMS
								0	1	1	33h	1/49 duty	Line [0:47], COMS
								1	0	0	34h	1/65 duty	Line [0:63], COMS
								1 1	0 1	1 *	35h 37h	Reserved	No effect

Using Partial Display Bias Set command to change the LCD bias in partial display mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	LCD Bias
0	1	0	0	0	1	1	1	0	0	0	38h	1/4
								0	0	1	39h	1/5
								0	1	0	3Ah	1/6
								0	1	1	3Bh	1/7
								1	0	0	3Ch	1/8
								1	0	1	3Dh	1/9
								1	1	0	3Eh	Reserved
								1	1	1	3Fh	Reserved

Note: The COM waveform of no display area is non-select waveform.

2.3. 26. Partial Start Line Set (Double Byte Command)

This command makes it possible to set the partial start line for partial display. It is a two-byte command used as a pair and the Number of Start Line Set command must be issued after the Partial Start Line Set command.

(1) **Partial Start Line Set**

When this command is input, no other command except for the Number of Start Line Set command can be used.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**1**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**1**

(2) **Number of Start Line Set**

By using this command to set six bits of data to the Partial Start Line register. Once the Number of the Start Line Set command has been used to set data into the register, then the partial start line will affect on the LCD display. The number of partial start line is always equal to zero when the partial start line is larger than maximum duty ratio

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Start Line
0	1	0	*	*	0	0	0	0	0	0	XX	0 line
					0	0	0	0	0	1	XX	1 line
					0	0	0	0	1	0	XX	2 line
								:			:	:
					1	1	1	1	1	0	XX	62 line
					1	1	1	1	1	1	XX	63 line

2.3. 27. The N-Line Inversion (Double Byte Command)

This command makes it possible to adjust the number of scan lines for liquid crystal display inversion. It is a two-byte command used as a pair and the Number of Line Set command must be issued after the N-Line Inversion Set command.

(1) **N-Line Inversion Set**

When this command is input, no other command except for the Number of Line Set command can be used.

A0	**/RD**	**/WR**	**DB7**	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**1**

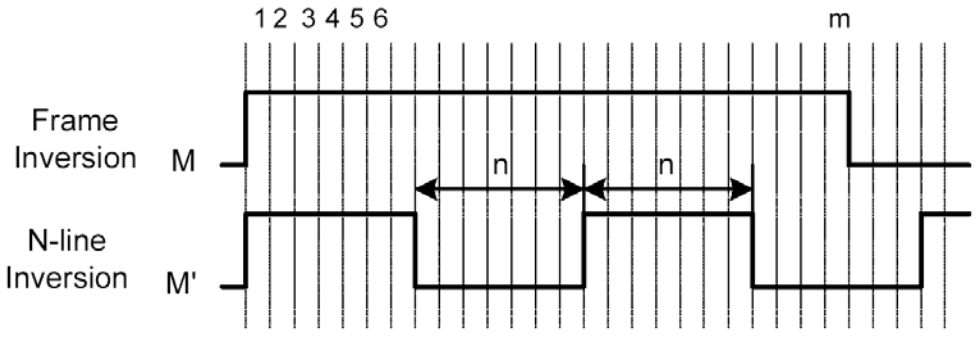
(2) **Number of Line Set**

By using this command to set five bits of data to the N-Line inversion register. Once the Number of Line Set command has been used to set the data into the register, then the N-Line inversion will affect on the LCD display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Line Inversion
0	1	0	*	*	*	0	0	0	0	0	XX	1 line
						0	0	0	0	1	XX	2 line
								:			:	:
						1	1	1	1	1	XX	32 line

Note 1: The number of inversed scan line = register setting value + 1.

Note 2: When Partial Duty = 1/9 or 1/17, the N-line inversion function release and the LCD display scan line is back to frame inversion status.



2.3. 28. Release N-Line Inversion

This command is used to exit the N-Line inversion function. The N-Line inversion function is released and the LCD display is set back to frame inversion status once this command is executed.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	0	0	0	1	0	0

2.3. 29. DC/DC Clock Frequency (Double Byte Command)

This command makes it possible to adjust the frequency for DC/DC clock. It is a two-byte command used as a pair and the DC/DC Frequency Division Set command must be issued after the DC/DC Clock Set command.

(1) **DC/DC Clock Set**

When this command is input, no other command except for the DC/DC Frequency Division Set command can be used.

A0	/RD	/WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	1	1	0

(2) **DC/DC Frequency Division Set**

By using this command to set five bits of data to the frequency division register.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Division
0	1	0	*	*	*	*	0	0	0	0	XX	fOSC
							0	0	0	1	XX	fOSC/2
							0	0	1	0	XX	fOSC/4
							0	0	1	1	XX	fOSC/6 (default)
							0	1	0	0	XX	fOSC/8
							0	1	0	1	XX	fOSC/10
							0	1	1	0	XX	fOSC/12
							0	1	1	1	XX	fOSC/14
							1	0	0	0	XX	fOSC/16
							1	0	0	1	XX	fOSC/18
							1	0	1	0	XX	fOSC/20
							1	0	1	1	XX	fOSC/22
							1	1	0	0	XX	fOSC/24
							1	1	0	1	XX	fOSC/26
							1	1	1	0	XX	fOSC/28
							1	1	1	1	XX	fOSC/30

2.4. DISPLAY DATA RAM

2.4.1. Chip Select Inputs

The NT7534 has two chip select pads. /CS1and CS2 can interface to a microprocessor when /CS1 is low and CS2 is high. When these pads are set to any other combination. D0 to D7 are high impedance and A0, E (/RD) and R/W (/WR) inputs are disabled. (When serial input interface is selected. the shift register and counter are reset.)

2.4.2. Access to Display Data RAM and Internal Registers

The NT7534 can perform a series of pipeline processing between LSI's using the bus holder of the internal data bus in

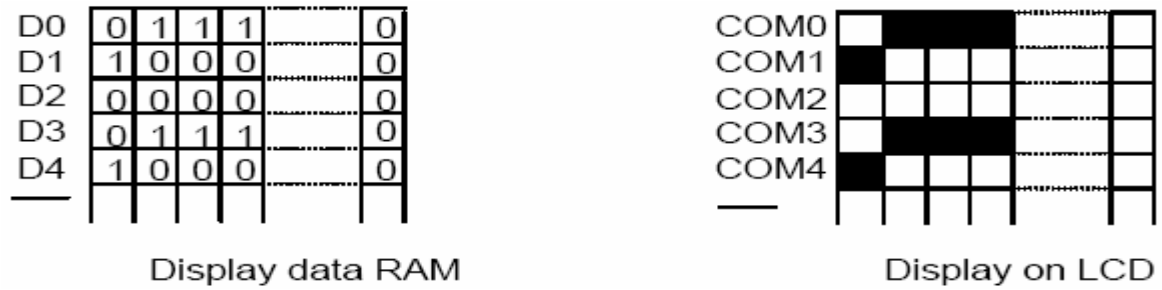
order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in the bus holder, and outputs it onto the system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in the bus holder, and stores it in display RAM until the next data write cycle starts. When viewed from the microprocessor, the module access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}).
This view shows the data transfer speed to / from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output immediately following the read instruction. The address data is output during the second data read. A single dummy read must be inserted after the address setup and after the write cycle..

2.4.3. Busy Flag

When the busy flag is "1" it indicates that the NT7534 chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pad with the read instruction. If the cycle time (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

2.4.4. Display Data RAM

The display data RAM is RAM that stores the dot data for the display. It has a 65(8 page * 8 bit+1)*132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in the following figure, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, and there are few constraints at the time of display data transfer when multiple NT7534 chips are used, thus display structures can be created easily and with a high degree of freedom. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during the liquid crystal display, it will not cause adverse effects on the display (such as flickering).



2.4.5. The Page Address Circuit

As shown in Figure 4, the page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address8 (D3, D2, D1, D0 = 1, 0, 0, 0,) is the page for the RAM region used; only display data D0 is used.

2.4.6. The Column Address

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read / write command. This allows the MPU display data to be accessed continuously. Moreover, the incrimination of column addresses stops with 83H, because the column address is independent of the page address. Thus, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address. Furthermore, as shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

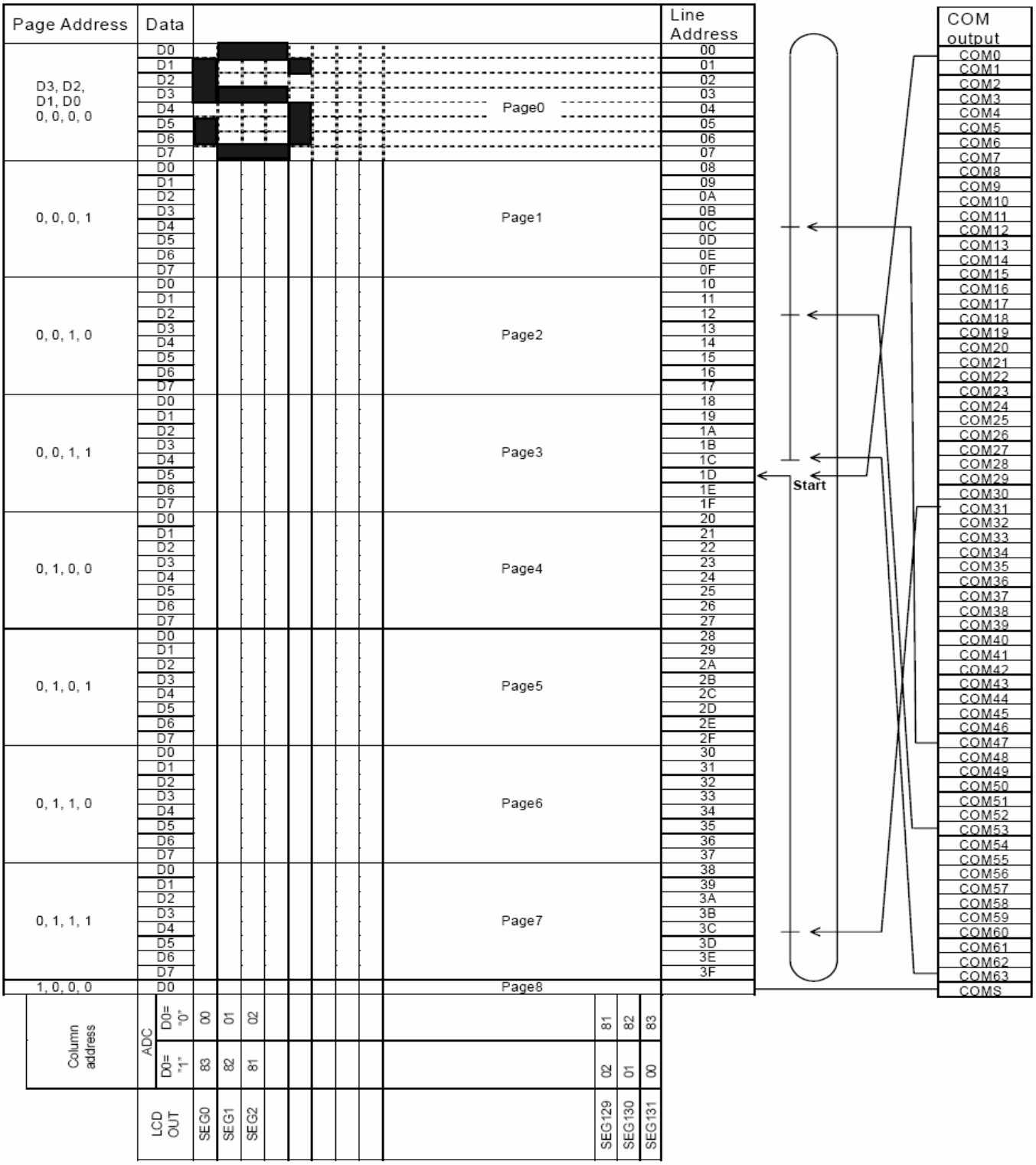
TABLE

SEG Output	SEG0		SEG131
ADC = "0"	0 (H)→	Column Address	→83 (H)
ADC = "1"	83 (H)←	Column Address	←0 (H)

2.4.7 The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for module, when the common output mode is reversed. The display area is a 65-line area for the module from the display start line address. If the line addresses are changed dynamically using the display start line address set command, then screen scrolling, page swapping, etc. can be performed.

2.4.8. Relationship between display data RAM and address (if initial display line is 1DH)

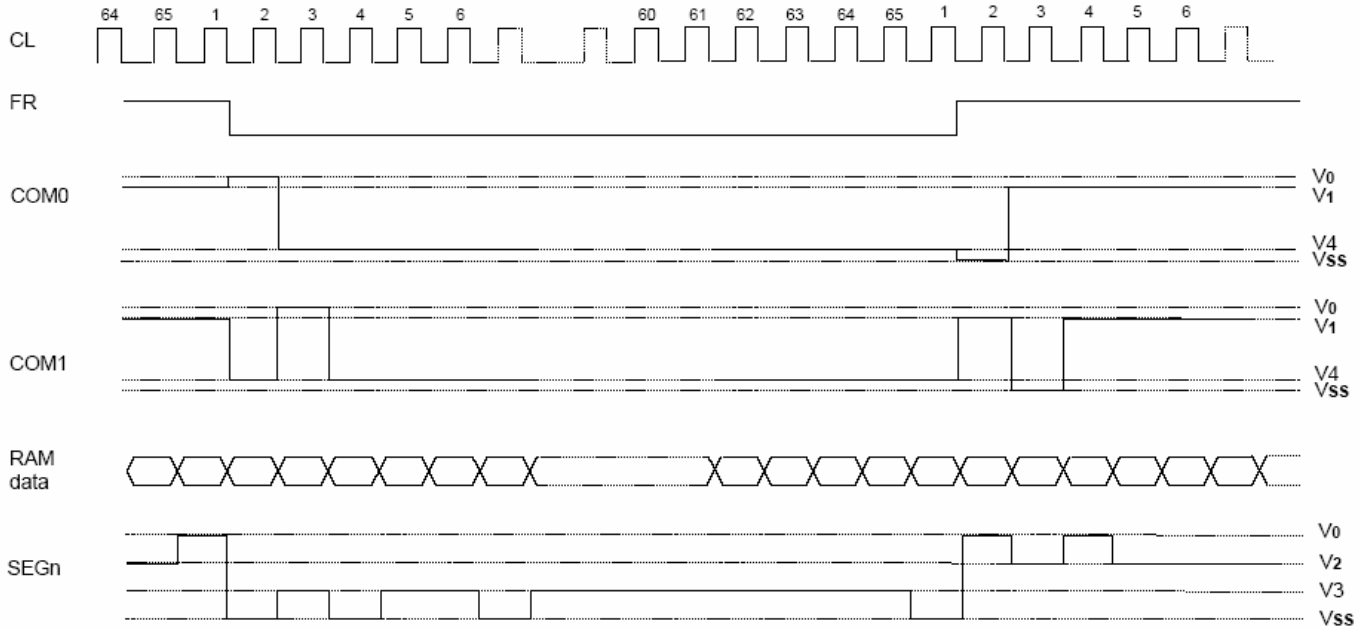


2.4.9. The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM themselves.

2.4.12. Display Timing Generator Circuit

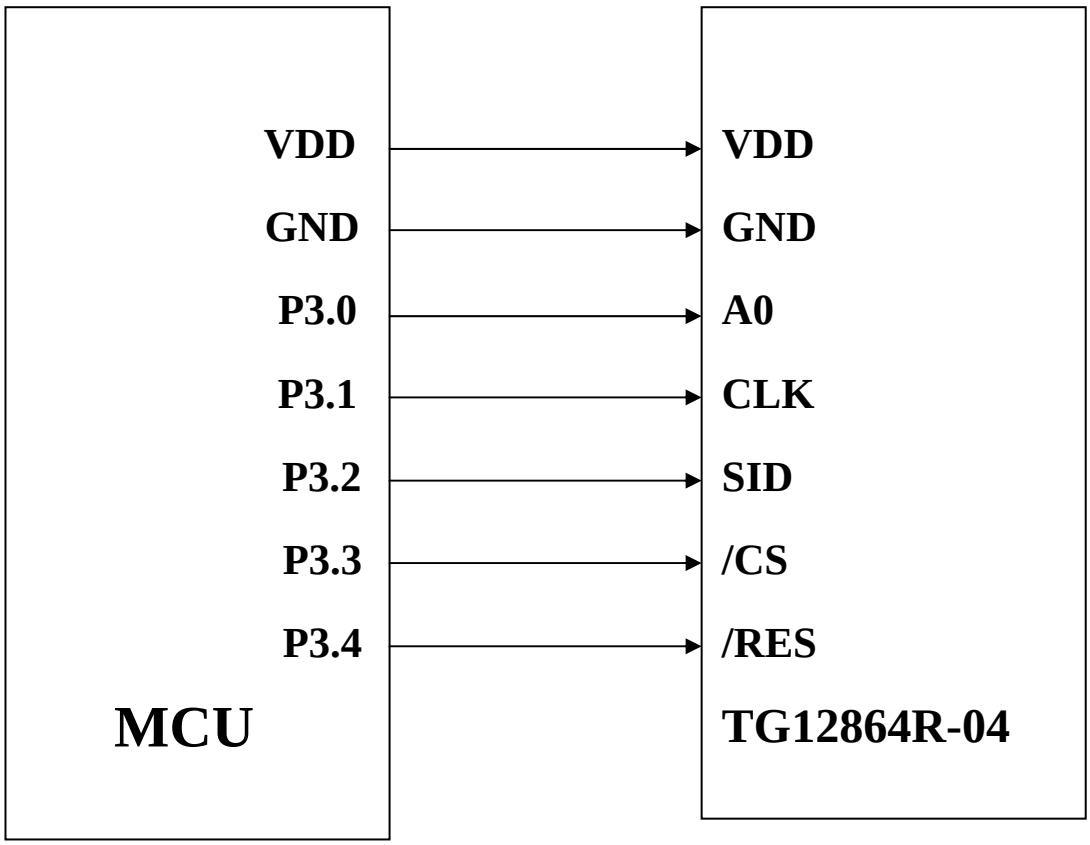
The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there are absolutely no adverse effects (such as flickering) on the display. Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a driving waveform using a 2-frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.



When multiple NT7534 chips are used, the slave chips must be supplied with the display timing signals (FR, CL,/DOF) from the master chip. Table 5 shows the status of the FR, CL, and /DOF signals.

2.5. CIRCUIT CONNECTION BLOCK

The MCU interface

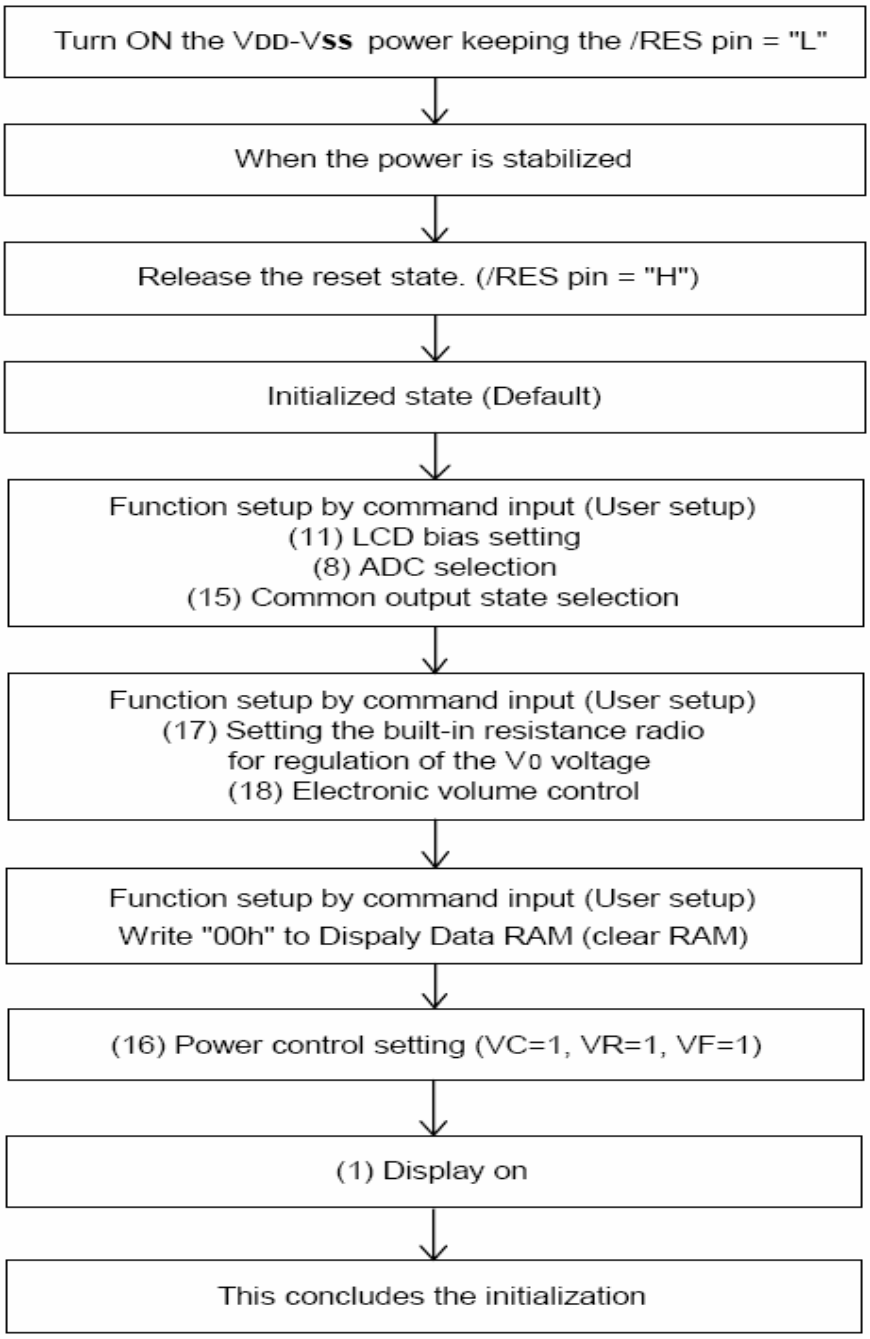


2.6. INITIAL THE MOFULE

Instruction Setup: Reference

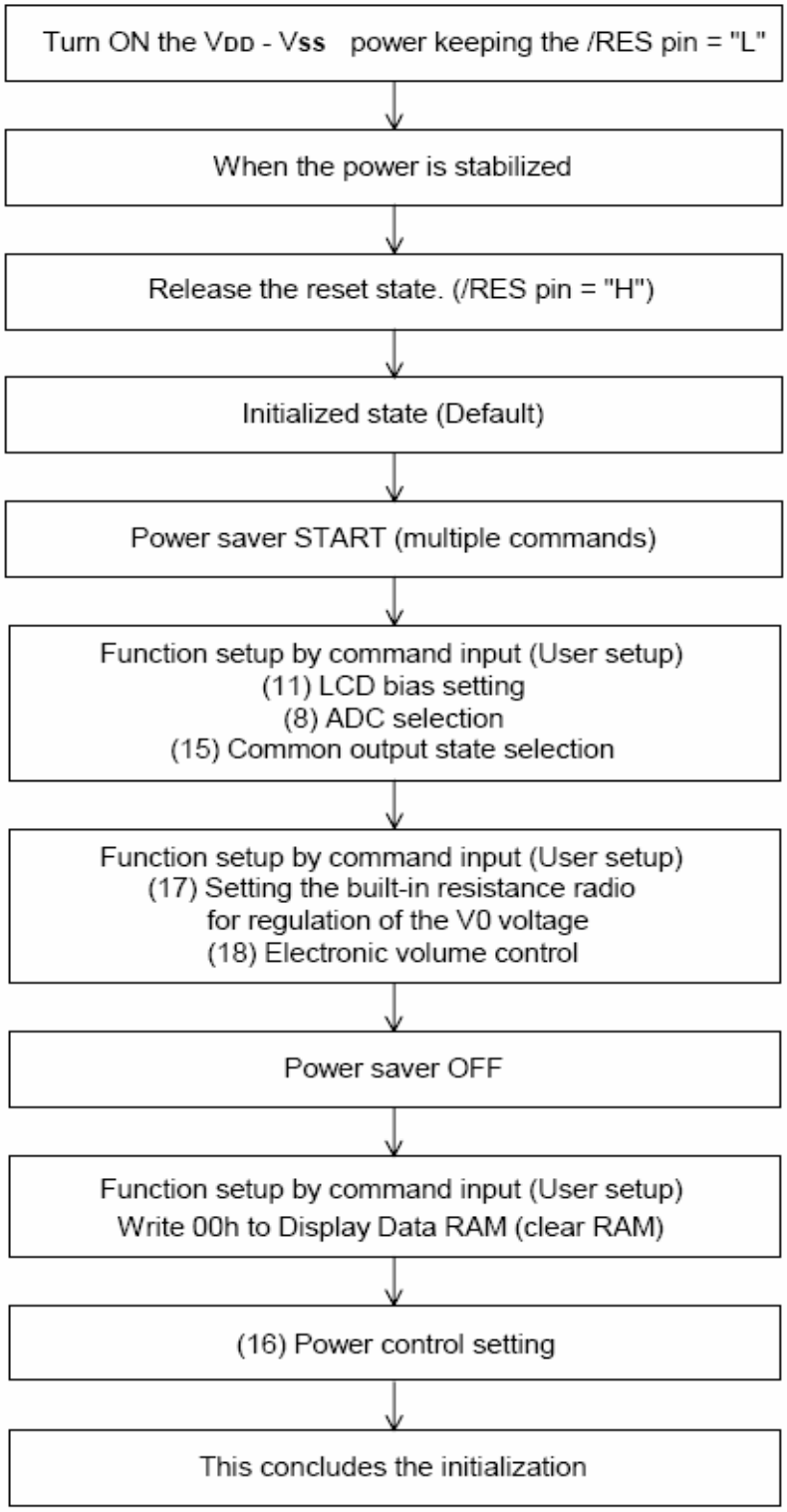
2.6.1. Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 - V4) and the V_{DD} pin, the picture on the display may instantaneously become totally dark when the power is turned on. To avoid such failure, we recommend the following flow sequence when turning on the power. 1.1. When the built-in power is being used immediately after turning on the power.



The time of initialization will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

2.6..2. When the built-in power is not used immediately after turning on the power



The target time of 5ms will vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you conduct an operation check using the actual equipment.

3. RELIABILITY TEST AND QUALITY

3.1. RELIABILITY TEST CONDITION

No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	60 °C 200 hrs	------
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-10 °C 200 hrs	------
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50 °C 200 hrs	------
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	0 °C 200 hrs	------
5	High temperature / Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	60 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
6	High temperature / Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40 °C , 90 %RH 96 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. -10°C 30min ⇌ 25°C 5min. ⇌ 60°C 30min 1 cycle	-10°C / 60°C 10 cycles	------

Supply voltage for logic system = 5V. Supply voltage for LCD system = Operating voltage at 25 C.

Mechanical Test

Vibration test	Endurance test applying the vibration during transportation and using	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hour	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 11 msede 3 times of each direction	MIL-202E-213B
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air	115mbar 40hrs	MIL-202E-105C
Static electricity test	Endurance test applying the electric stress to the terminal	VS=800V,RS-1.5KΩ CS=100pF, 1 time	MIL-883B-3015.1

Failure Judgment criterion

Criterion Item	Test Item No.											Failure Judgment Criterion
	1	2	3	4	5	6	7	8	9	10	11	
Basic specification												Out of the Basic specification
Electrical characteristic												Out of the DC and AC characteristic
Mechanical characteristic												Out of the Mechanical specification Color change: out of Limit Appearance Specification
Optical characteristic												Out of the Appearance Standard

3.2. QUALITY GUARANTEE

Acceptable Quality Level, Each lot should satisfy the quality level defined as follows.
-Inspection method: MIL-STD-105E LEVEL II Normal one time sampling

AQL

Partition	AQL	Description
A: Major	0.4%	Functional defective product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

Definition of 'LOT'

One lot means the delivery quality to customer at once time.

Conditions of Cosmetic Inspection

. Environmental condition

The inspection should be performed at the 1metre height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃ and normal humidity 60±15%RH).

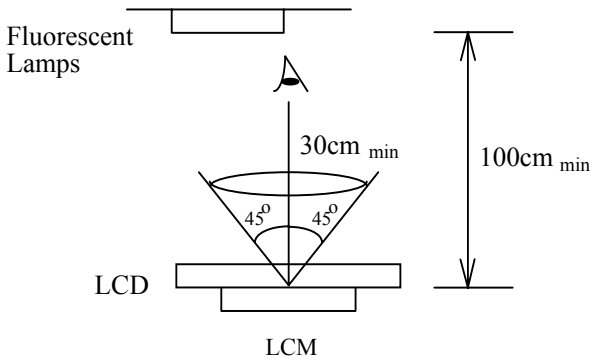
Driving voltage

The Vo value which the most optimal contrast can be obtained near the specified Vo in the specification (Within of the typical value at 25℃.).

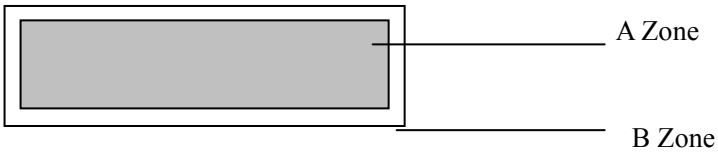
3.3. INSPECTION METHOD

The visual check should be performed vertically at more than 30cm distance from the LCD panel

Viewing direction for inspection is 45° from vertical against LCM.



Definition of zone:

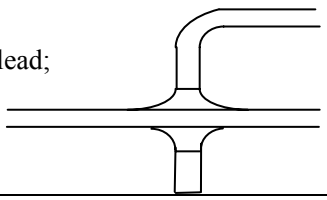
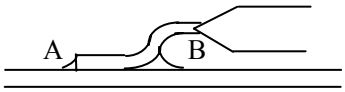
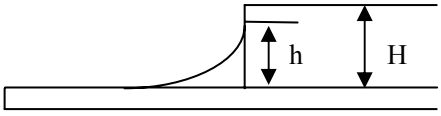


A Zone: Active display area (minimum viewing area).

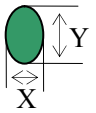
B Zone: Non-active display area (outside viewing area).

3.4. INSPECTION STANDARD FOR SOLDER

Module Cosmetic Criteria

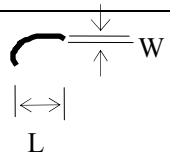
No.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern Peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
4	Resist flaw on substrate	Invisible copper foil (Φ0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceedΦ0.2㎜)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Plate discoloring 1. Lead parts	a. Soldering side of PCB Solder to form a 'Filet' all around the lead; Solder should not hide the lead form perfectly too much 	Minor
	2. Flat packages	Either "toe"(A) or "heal' (B) of The lead to be covered by 'Filet' Lead form to be assume over Solder. 	Minor
	3. Chips	(3/2) H ≥h ≥ (1/2) H 	Minor

3.5. SCREEN COSMETIC CRITERIA(APPEARANCE)

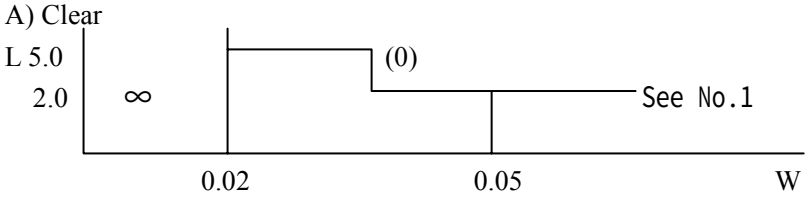
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td rowspan="8">1</td><td>Short or open circuit</td><td rowspan="8">No allow</td></tr>
<tr><td>LC leakage</td></tr>
<tr><td>Flickering</td></tr>
<tr><td>No display</td></tr>
<tr><td>Wrong viewing direction</td></tr>
<tr><td>Wrong Back-light</td></tr>
<tr><td>Wrong or missing component</td></tr>
<tr><td rowspan="2">2</td><td>Contrast defect (dim, ghost)</td><td rowspan="2">Refer to the approval sample</td></tr>
<tr><td>Background color deviation</td></tr>
<tr><td>3</td><td>Point defect, Black spot, dust (including Polarizer)
Φ=(X+Y)/2</td><td> 

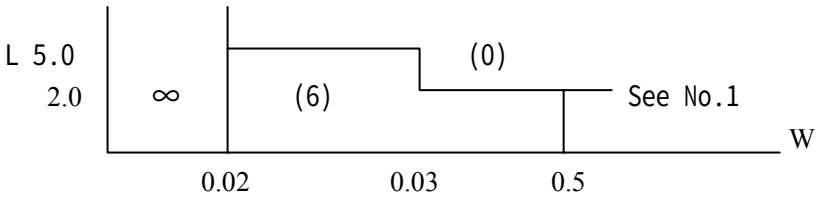
<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>$\phi \leq 0.10$</td><td>Disregard</td></tr>
<tr><td>$0.10 < \phi \leq 0.20$</td><td>6</td></tr>
<tr><td>$0.20 < \phi \leq 0.3$</td><td>2</td></tr>
<tr><td>$\phi > 0.30$</td><td>0</td></tr>
</table></td></tr>
</table>

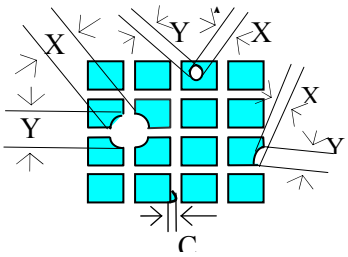
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>4</td><td>Line defect,

Scratch: In accordance with spots and lines operating cosmetic criteria. When the light reflective on the panel surface, the scratches are not to be remarkable.</td><td>


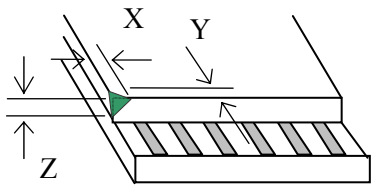
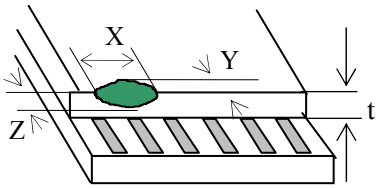
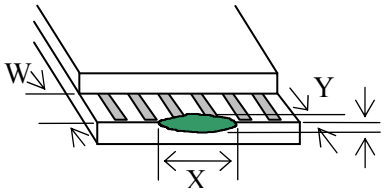
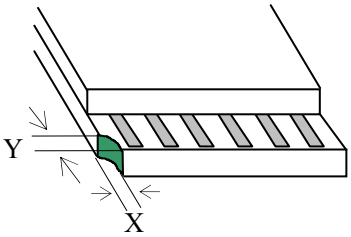
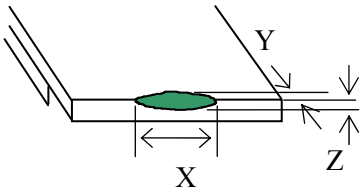
<table>
<tr><td colspan="2">Line</td><td>Acceptable Qty.</td></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.015≥W</td><td>Disregard</td></tr>
<tr><td>3.0≥L</td><td>0.03≥W</td><td rowspan="2">2</td></tr>
<tr><td>2.0≥L</td><td>0.05≥W</td></tr>
<tr><td>1.0≥L</td><td>0.1＞W</td><td>1</td></tr>
<tr><td>---</td><td>0.05<W</td><td>Applied as point defect</td></tr>
</table>
Unit: mm

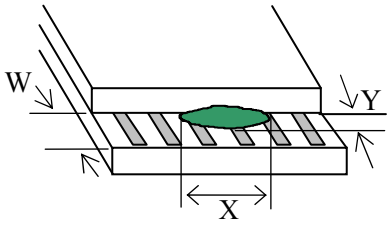
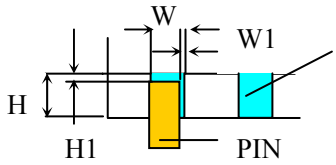
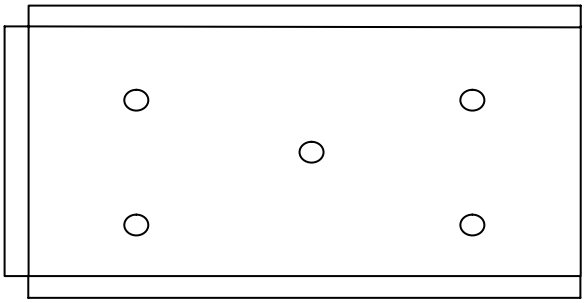
A) Clear


Note: ( ) –Acceptable Qty in active area
L –Length (mm) W –Width (mm) ∞ -Disregard
B) Unclear


</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two colors change across the viewing area</td></tr>
<tr><td>6</td><td>Dot-matrix
pattern
ϕ = (X+Y)/2</td><td>Pin hole:


<table>
<tr><td>Size</td><td>Acceptable Qty.</td></tr>
<tr><td>ϕ＜0.1</td><td>Disregard</td></tr>
<tr><td>0.10≤ϕ≤0.20</td><td>1</td></tr>
<tr><td>ϕ>0.20</td><td>0</td></tr>
</table>
C: Shall not touch other dot(s).</td></tr>
</table>

No.	Item	Criterion
7	Chip Remark: X: Length direction Y: Short direction Z: Thickness direction t: Glass thickness W: Terminal Width	 Acceptable criterion X: ≤2 | Y: 0.5mm | Z: ≤t  Acceptable criterion X: ≤2 | Y: 0.5mm | Z: ≤t/2  Acceptable criterion X: Disregard | Y: ≤0.2 | Z: ≤t  Acceptable criterion X: ≤3 | Y: ≤2 | Z: ≤t shall not reach to ITO  Acceptable criterion X: ≤5 | Y: ≤2 | Z: ≤t/3

No.	Item	Criterion
8	Total no. of acceptable Defect	A. Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.
9	Protruded W: Terminal Width	 Acceptable criteria: Y ≤ 0.4
10	PIN	Position  W1≤1/3W H1≤1/3H
11	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX/BMIN≤2 -BMAX : Max. value by measure in 5 points -BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure 
12	Allowable density	Above defects should be separated more than 10mm each other.
13	Rubbing line	Not to be noticeable.
14	Dot size	To be 95% ~ 105% of the dot size (typ.) in drawing, Partial defects of each dot (ex. Pin-hole) shold be t4reated as 'spot'.(see Screen Cosmetic Criteria (operating) No.)

No.	Item	Criterion	
15	Bubbles in polarizer	Size : d mm	Acceptable Qty in active area
		d≦0.3	Disregard
		0.3<d≦1.0	3
		1.0<d≦1.5	1
		1.5<d	0
16	Allowable density	Above defects should be sea rated more than 30mm each other	
17	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Backlit type should be judged with back-lit on state only.	
18	Contamination	Not to be noticeable.	

Note:

'Clear'= the shade and size are not changed by Vo.

'Unclear'= the shade and size are changed by V0.

Size: d=(long length + short length)/2

The limit samples for each item have priority

Completed defects are defined item by item, but if the number of defects is defined in above table, the total number should not exceed 10.

In case of ' concentration', even the spots or the lines of 'disregarded size should not allowed. Following three situations Should be treated as 'concentration'.

-7 or over defects in circle of Φ2mm

-10 or over defects in circle ofΦ10㎜

-20 or over defects in circle ofΦ20㎜

3.6. PRECAUTIONS FOR USING LCM MODULES

1. Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handing.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or Polarizer peel-off may occur with high humidity.

(2) Do not touch, push or rub the exposed polarizer with anything harder than an HB Pencil lead (Glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic, substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum Benin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

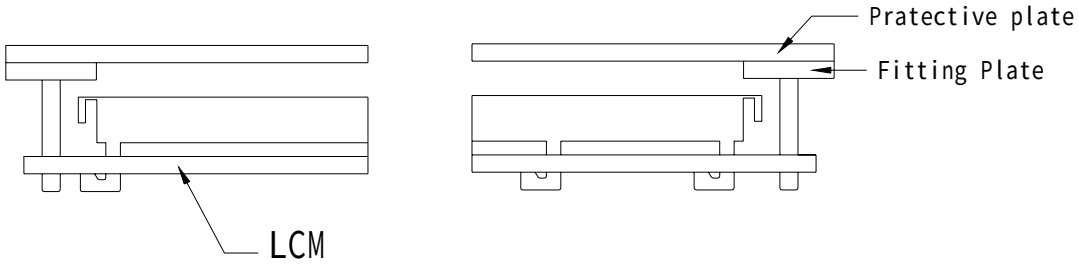
(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature the must be warmed up in a container before coming is contacting temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.
(9) Do not touch the display with bare hands. This will stain the display and degrade insulation between terminals (some cosmetics are determinate to the polarizer).
(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

3.7. INSTALLING LCM MODULES

The hole in the printed circuit board is used to if LCM as shown in the picture below. Attend to the following items when installing the LCM

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm]

3.8. PRECAUTION FOR HANDING LCM MODULE

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change shape of the tab on the metal frame
(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
(3) Do not damage or modify the pattern writing on the printed circuit board.
(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
(6) Do not drop, bend or twist LCM

3.9. ELECTRO-STATIC DISCHARGE CONTROL

Since this module uses a CMOS LSI, the same attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.
(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutation of the motor.
(5) As far as possible make the electric potential of your work clothes and that of the workbench the ground potential.
(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

3.10. PRECAUTION FOR SOLDERING TO THE LCM

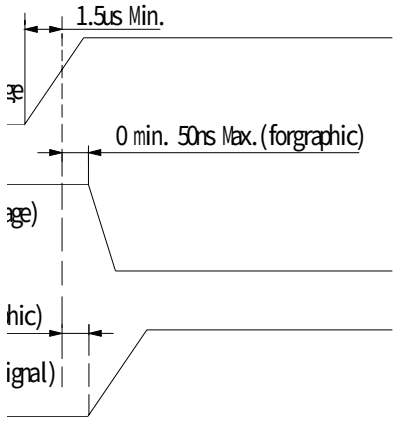
(1) Observe the following when soldering lead wire , connector cable and etc. to the LCM
-Soldering iron temperature: 280℃±10℃
-Soldering time: 3-4 seconds
-Solder: eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation.(This does not apply in the case of non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electro-luminescent panel and PC board, the panel and board should not be detached more than three times, This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
(3) When remove the electro-luminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PX board could be damaged.

3.11. PRECAUTIONS FOR OPERATION

(1) Viewing angle varies with the change of liquid crystal driving voltage (V0). Adjust Vo to show the best contrast.
(2) Driving the LCD in the voltage above the limit shortens its life.
(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD cell be out of the order. It will recover when it returns to the specified temperature range.
(4) If the display area is pushed hard during operation, the display will become abnormal, however, it will return to normal. If it is turned off and then back on. Used under the relative condition of 40℃, 50%RH.
(5) When turning the power on input each signal after the positive/negative voltage becomes stable.



3.12. STORAGE

When storing LCD as spares for some years, the following precautions are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0℃ and 35℃

(3) The polarizer surface should not come in contact with any other object.(we advise you to store them in the container in which they were shipped.)

(4) Environmental conditions:

-Don not leave them for more than 168hrs. at 60℃

-Should not be left for more than 48hrs. at -20℃.

3.13. SAFETY

(1) It is recommended to crush damaged or unnecessary LCD into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2)If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

3.14. LIMITED WARRANTY

Unless agreed between EGO LCD and customer, EGO LCD will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with TINSHAR LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to TINSHARP within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of TINSHARP limited to repair and/ or replacement on the terms set forth above. TINSHARP will not be responsible for any subsequent or consequential events.

3.15. RETURN LCM UNDER WARRANTY

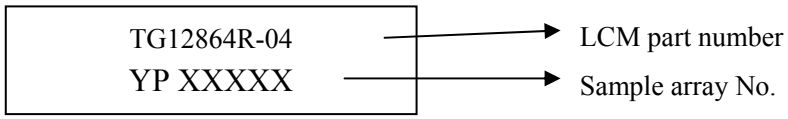
No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are:

-Broken LCD glass.
-PCB eyelet's damaged or modified.
-PCB conductors damaged.
-Circuit modified in any way, including addition of components.
-PCB tampered with by grinding, engraving or painting varnish.
-Soldering to or modifying the bezel in lay manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelets, conductors and terminals.

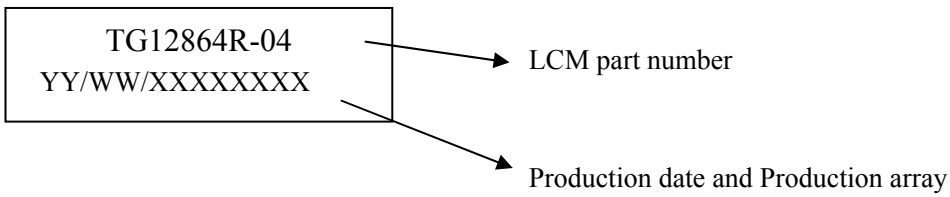
4. DATE CODE RULES

4-1. DATE CODE FOR SAMPLE



YP: meaning sample

4-2. DATE CODE FOR PRODUCTION



A. TG12864R-04 represents LCM part number

C. YY/WW represents Year, Month, and Week

YY—Year WW—Week

XXXXXXXX—Production array No.

END