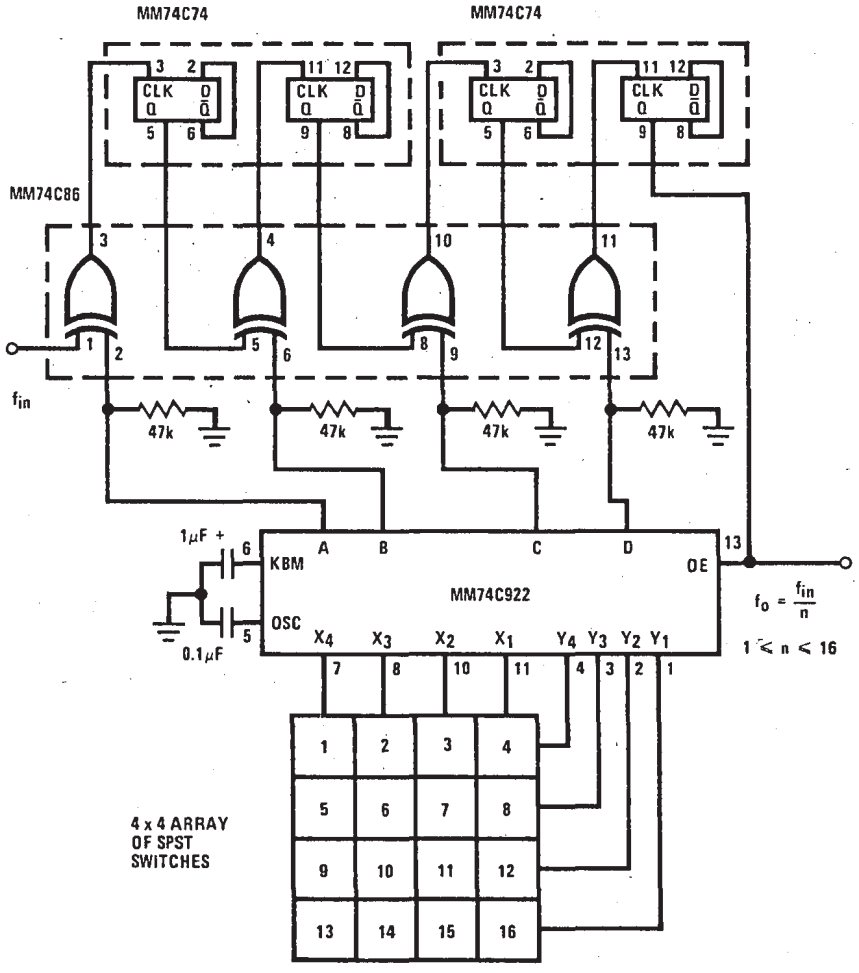
APRIL 1976
Gerald Buurma
National Semiconductor Corp.

Keyboard programmable divide-by-N counter with symmetrical output

A CMOS key encoder combines with a couple of Dual D flip-flops and an exclusive OR package to form a simple but versatile programmable divider. The input frequency can be divided by any number n between 1 and 16 by simply pressing the appropriate key. The counter output is symmetrical for both odd and even divisors.

This circuit is useful for simple frequency synthesis or as an oscilloscope triggering unit where the displayed signal is applied to the counter input and the external trigger of the oscilloscope is connected to the counter output. The trigger signal is then some submultiple of displayed signal which often results in a more stable trace. Different divisors can be easily keyed in as the input signal varies.



Simply press the key and the input frequency is divided by that number. The output frequency is symmetrical for odd and even divisors. Use it for simple frequency synthesis or as a keyboard controlled oscilloscope triggering unit.

The key encoder scans the key array which is set up so the key labeled "16" is in the matrix position which causes "0" to be encoded, the key labeled "15" causes "1" to be encoded, and so on until we find that the key position labeled "1" causes a binary "15," or all ones, at the output of the encoder. The key arrangement converts a key position so that any number n from 1 to 16 is encoded as 16 - n at the encoder output. For example, if the key labeled 5 is pressed the binary number 1011 = 11 appears at the encoder output. The MM74C922 key encoder scans the keys, detects, debounces, and encodes any entry. An internal register remembers the last key pressed and presents it to the Tri-State® outputs.

The input to the exclusive OR is a "zero" when the respective encoder output is a "zero" or when the feedback signal from the last counter stage forces the encoder outputs into Tri-State. When in Tri-State the pull down resistors feed a "zero" into the exclusive OR inputs.

When the output is an active "one," the clock signal from one flip-flop to the next is inverted by the exclusive ORs.

When the output is a "zero" or the encoder is in Tri-State, due to the feedback signal, the clock signal from one flip-flop to the next is the same phase. For every n/2 input time period, the counter output and feedback change state. Whenever the feedback signal changes state, all flip-flops programmed with a "one" by the encoder change their phases; this effectively adds a clock pulse to that stage of the counter. The addition of clock pulses to the 2^0, 2^1, 2^2 or 2^3 stages allows us to divide by any number between 1 and 16. Since the feedback changes state every n/2 input time period, the output frequency is symmetrical for any divisor.

The unit operates over the standard CMOS supply range of 3 to 15 volts and has a typical upper frequency limit of one megacycle with a 10 volt supply.

REFERENCE

1. M. V. Subba Rao, "Programmable Divide by n Counter Provides Symmetrical Outputs for all Divisors," *Electronic Design*, no. 2, January 19, 1976, p. 82.