iW3689 application note

... personal
... portable
... connected

2016.03.23

IW3689 Control chip Introduction

- Single-stage dimmable control chip, SOIC-8 packages using
- Support for buck-boost (non-isolated scheme) or flyback topology (Isolation Scheme)
- Support the dimmer, the leading edge, trailing edge dimmer operation (triac dimmer / ELV dimmers)
- No high power factor (PF> 0.9) and dimmer low THD (<20%)
- Most dimmers may support a wide dimming range 1% to 100%

typical application

- 100V, 120V or 230V AC mains input, compatible with conventional household dimmer
- 25W of LED bulbs or lamps (100W incandescent equivalent). Applications such as candle lamp, GU10, PAR lamp, BR light, R light, bulb lights,

※ For output power above 12W designs, care should be taken to verify the thermal and reliability constrains on the IC. IC temperature below 120 ° C is recommended for proper IC operation.

based on **iW3689** Dimming **led** Drive scheme

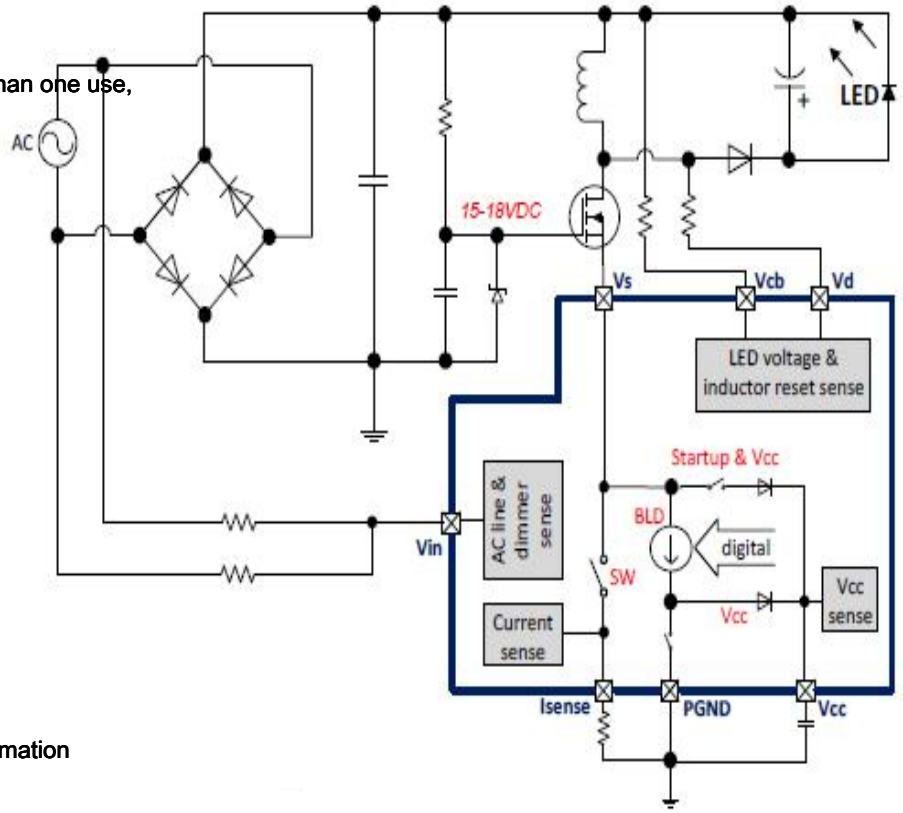
q Using a high voltage power source level control MOS Tube, the internal implementation of more than one use, I.e., switching power supply, bleeder as well as Vcc A charge sharing. Peripheral circuits are simplified and reduced BOM .

q No need 12V Driving high voltage power MOS A gate . A lower Vcc Voltage (5V) . Advantages include increased speed and less power Vcc Capacitors (ceramic capacitors may be used).

q Precise and flexible bleeder Current Control . Bleeder Current no longer Input voltage is limited: i.e., input can be provided a high voltage low bleeder Current, low input voltage can also be achieved very low bleeder impedance .

q MOS Open time of the main portion of the inductor to be charged multiplexing washed Vcc . Bleeder Current may overshoot Vcc . IC Power supply is no longer dependent on the auxiliary winding .

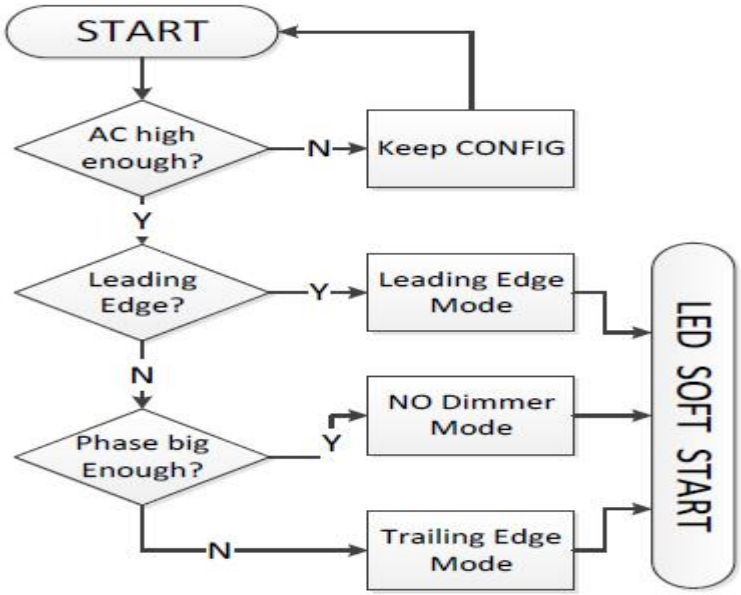
q Using differential input signals on both sides of the main inductor Reconstruction led Voltage information A main inductor and the discharge timing. You do not need attached to the auxiliary winding Obtain this information .



No special bleeder or start-up circuit ,and also Without auxiliary winding , A peripheral circuit can be simplified, requires only one high voltage power MOS, using very inexpensive single-winding inductor.

From the machine

1. AC Input is open
2. High-voltage power MOS The gate voltage of the tube RC A charging circuit and is finally clamped To zener Tube voltage (16V) ; And when the gate voltage higher than a certain, Due to the low potential source, the high voltage power MOS The tube is opened.
3. Using the internal chip enable circuit power MOS Tube filling Vcc , To charge 5V After the chip logic is activated, and immediately stops to continue to Vcc Charge.
4. Chip checks for over-temperature situation, if it is the next stop. and Vcc Will slowly down until the chip voltage shutdown, then restart.
5. enter " Dimmer learning " Phase, which checks to see if the chip dimming , A leading edge or after cutting, how much the phase angle.
6. Depending on the situation (no dimmer, or cut after the leading edge), different Control mode, and gradually increase led Until the current target current.

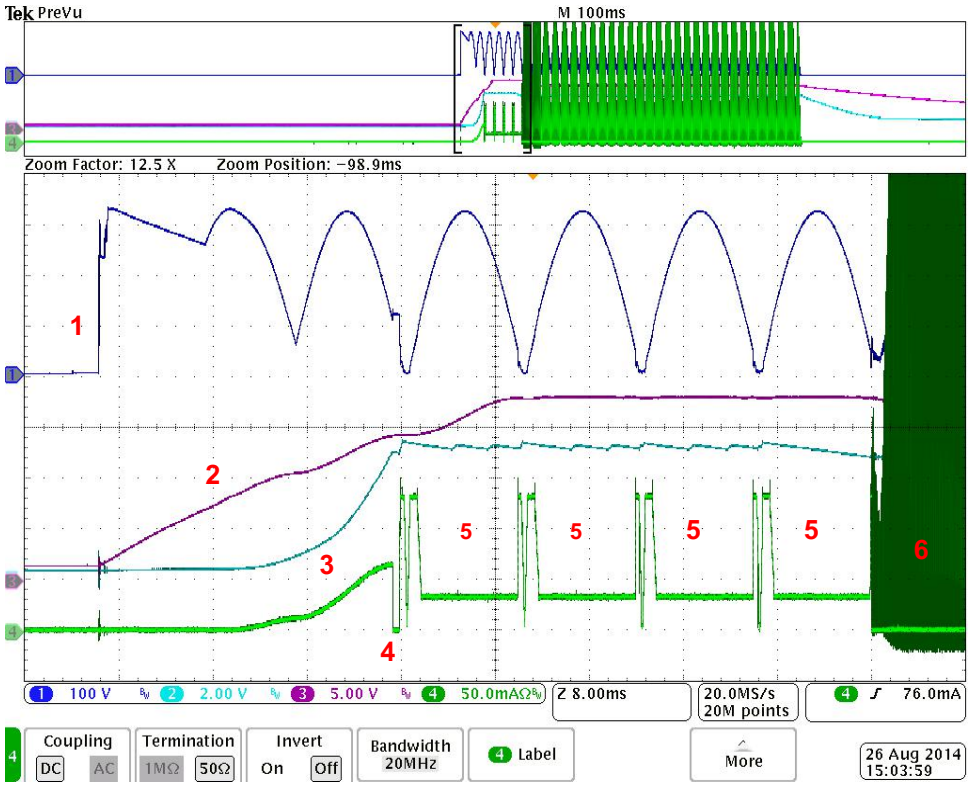


CH1: rectified input voltage;

CH2: Vcc;

CH3: gate voltage;

CH4: Current source



no dimmer Operating mode

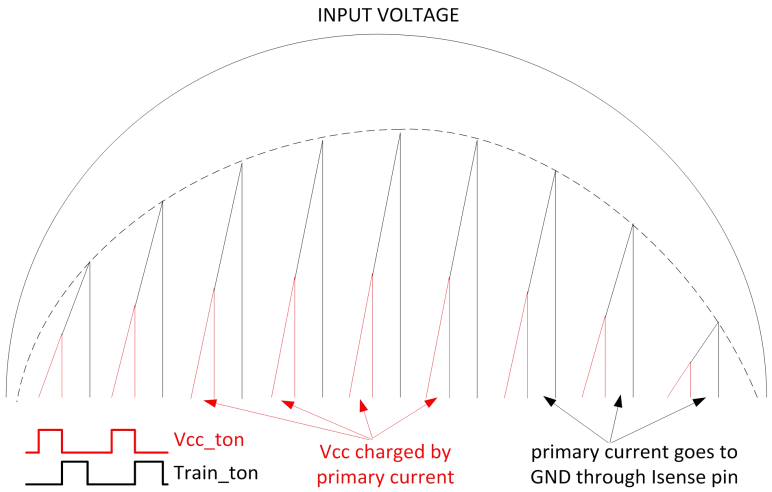
q Primary inductor peak current synchronized with the input voltage. Achieve high power factor and low THD . Equivalent to iW3608 / iW3609

q use valley-mode-switching Minimize MOS Switch tube Loss, and optimization EMI

q To limit the maximum switching frequency 90kHz , I.e., the cycle must be greater than 11us

q Beginning to use some of the primary inductor to charge the charging time while Vcc . and This period of time is charged by the chip according to the detected Vcc Voltage level automatic adjustment. Chip will Vcc Voltage stability in 5V about

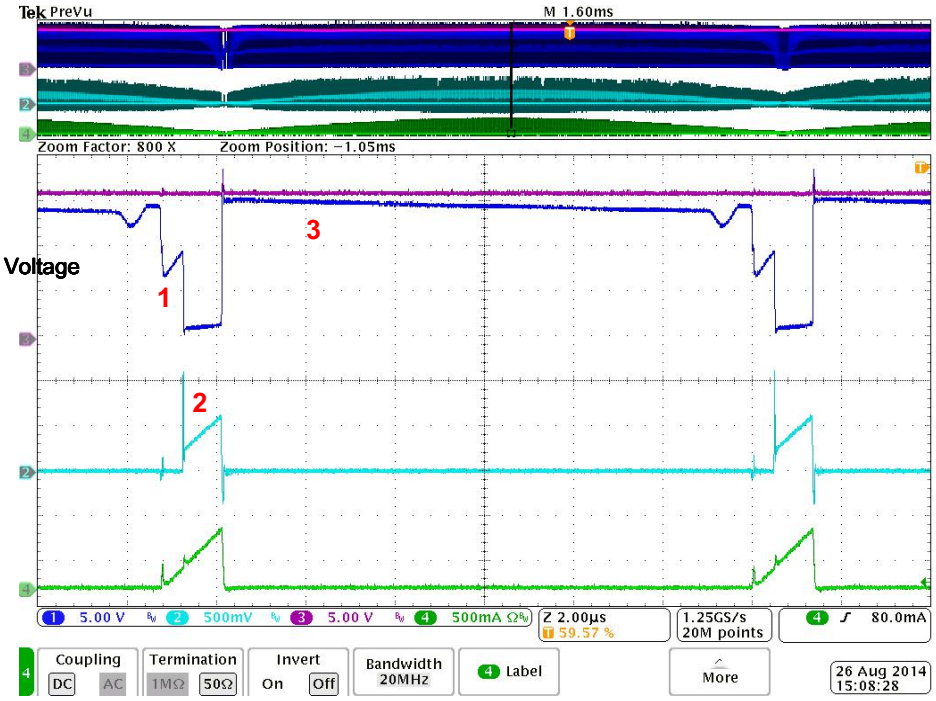
q The resulting output current chip real-time calculation, precise control of the main peak inductor flow. Achieved under different voltage input line < 3% of led Current changes, and different led Voltage is less than < 5% of led Current changes



Ivcc equation for every switching cycle:

- *Vin * Ipri * • = Pout*
- *Ivcc = Ipri * Vcc_ton / (Vcc_ton + Train_ton)*
- ***Ivcc = Pout / (Vin * •) * (Vcc_ton / (Vcc_ton + Train_ton))***

CH1: Vs; CH2: Isense; CH3: Vg; CH4: Isource



1. Vcc_ton: Charging the primary inductor current rises *Vcc* Period of time .

2. Train_ton: Vcc After charging, the external *MOS* Tube remains open, and the main inductor current is further increased, until after the target current *MOS* The tube is turned off .

3. A main inductor discharge, energy is released through the rectifying diode LED.

Before cutting dimmer Operating mode

q Using a fixed inductor peak current (Ipk) And a fixed switching frequency (fsw)

To achieve the same energy-per switching. control led Average current as smooth as possible, or to eliminate flicker in low light situations tremble .

q able to pass SDA Pull-down resistor is selected pin fixed peak inductor

flow (For details, see 25 page). When the conduction angle> 75% Time, IC At low line voltage will reduce the peak current, in order to avoid Ton + Treset> Tp.

q able to pass SCL Foot pull-down resistor to select a fixed switching frequency

(For details, see 25 page) . in case Ton + Treset> Tp , IC It will automatically increase Tp In order to avoid entering CCM . However, application design suitable switching frequency should be selected to minimize this happens.

q Breakthrough in the use of single-stage program " Thyristor conduction " control. Other words Saying, " Conduction angle " Not really all turned on. Chip intends to let off thyristor section in the middle, rather than requiring its continued conduction. Thus achieving a higher on-current and low bleeder loss.

q Bleeder Circuitry reduces led Driver output in the front tangent (thyristor

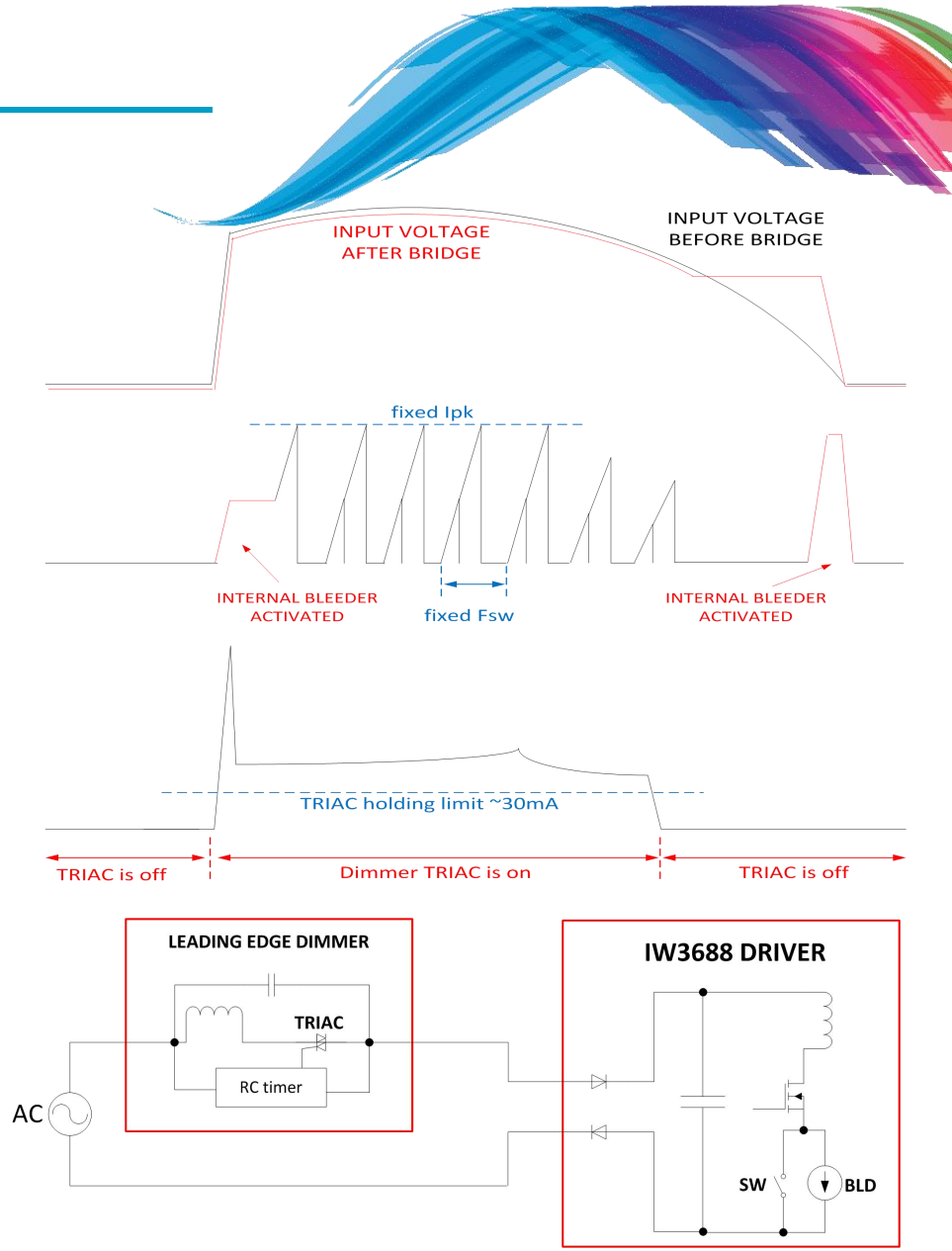
The voltage is almost zero when the input impedance), greatly enhances the ability to charge the smart dimmer.

q Export led The current percentage of the total conduction angle AC Half-wave period hundred

Related dividing ratio, rather than the average input voltage and correlation. Thus at different line voltages, adjusting almost identical clearance curve.

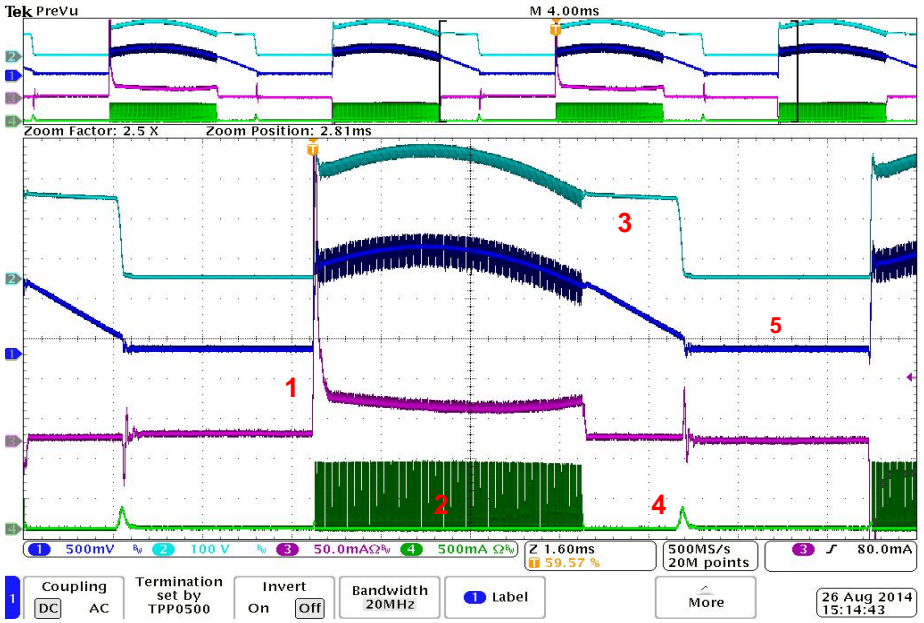
in DCM Mode, PLED = ½ * Lm * (Ipk) ^ 2 * fsw

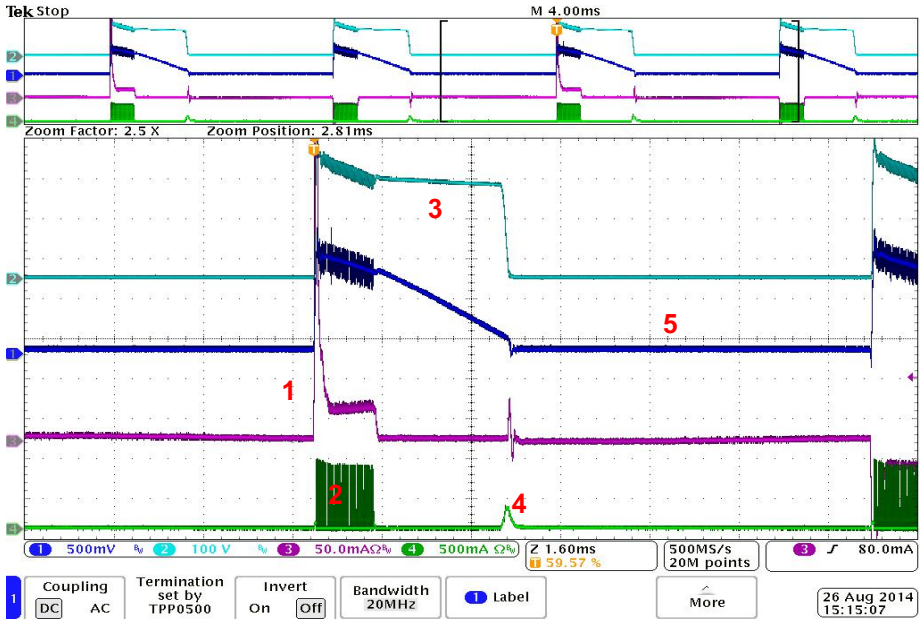
As long as each AC Half cycle switching frequency constant, a fixed peak current, fixed frequency to provide the most stable output



Before cutting dimmer Operating mode

CH1: rectified AC before bridge; CH2: rectified AC after bridge ; CH3: Input current ; CH4: Isource





1.AC Inrush current and the tangent *RC snubber* Electric current

2.Buck-boost Fixed switching frequency and fixed to a peak current converting energy *led* . Input current is comparatively high and stable, good to meet the thyristor remains conductive current requirement

3. Energy output sufficient to *led* After switching without using stop *bleeder* . SCR off naturally. Since the voltage of the bridge so no pull-down current suspension. However, before the affected voltage across the bridge is across the interior of the dimmer SCR capacitor continues to follow *AC* Line voltage drop

4. Use bridge voltage detection before zero crossing; with *bleeder* The rear axle electric voltage on the capacitor freed, and keep *bleeder* Max Open

5.Bleeder Set to the maximum current, minimum input impedance. Since there is no tangent to the input voltage, so almost no loss. Low input impedance to ensure the transfer correlator *RC* The timing function normally

After the cut dimmer Operating mode

q Using a fixed inductor peak current (Ipk) And a fixed switching frequency

Rate (fsw) To achieve the same energy-per switching. control led

Average current as smooth as possible, or to eliminate flicker in low light situations

tremble

q able to pass SDA Foot pull-down resistor to select a fixed inductor

Peak current (For details, see 25 page). When the conduction angle> 75% Time, IC

At low line voltage will reduce the peak current, in order to avoid Ton + Treset> Tp

q able to pass SCL Pull-down resistor to select a fixed pin opening

Off frequency (For details, see 25 page) . in case Ton + Treset> Tp ,

IC It will automatically increase Tp In order to avoid entering CCM . However, application

design suitable switching frequency should be selected to minimize this happens.

q In the tangent, use delivered to led The energy input to the drive

The capacitor discharge, but also to tune across capacitor discharge correlators. Until the

line voltage is low enough, only the use of bleeder Continues to discharge, the greatest

degree of reduced bleeder Loss

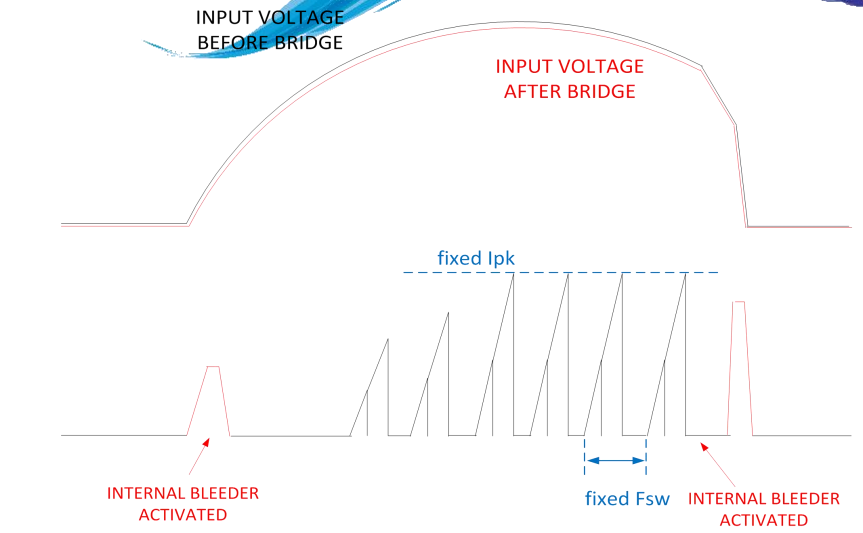
q Just " Conduction angle " In part to the time led Transport energy,

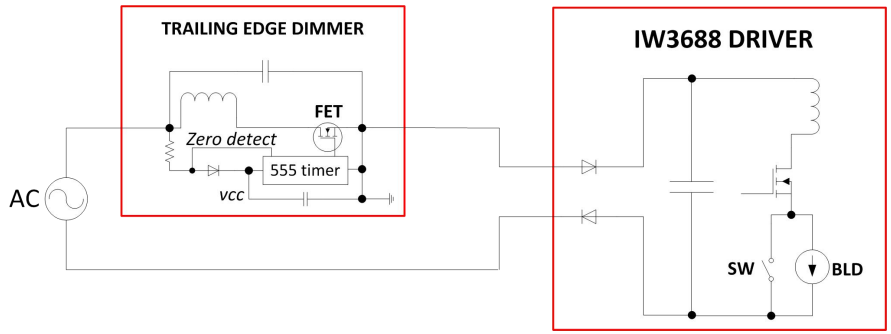
Not the entire conduction angle. Such dimming range becomes relatively wide.

q Input output led The current percentage of the total conduction angle AC Half-wave

Percentage cycle related, rather than the average input voltage and correlation. Thus at

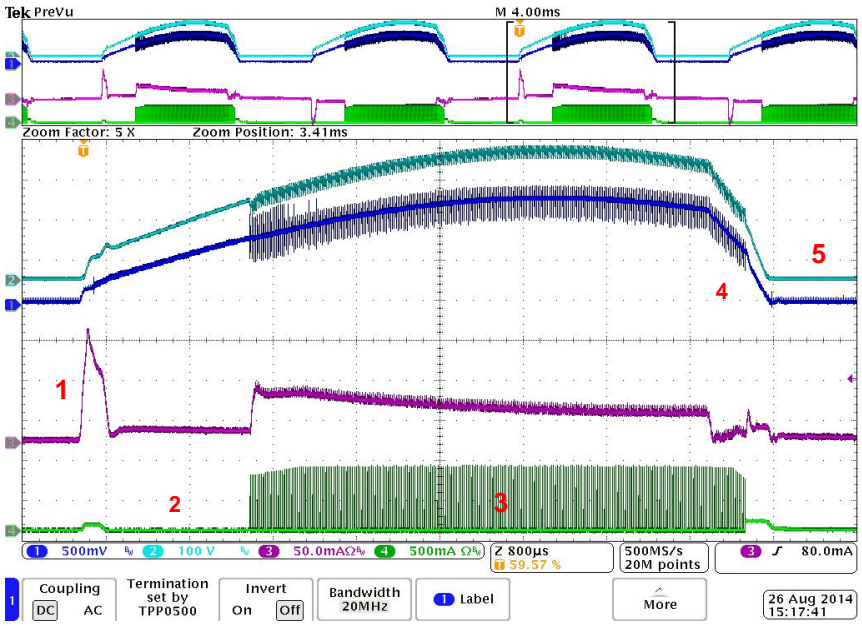
different line voltages, adjusting almost identical clearance curve.

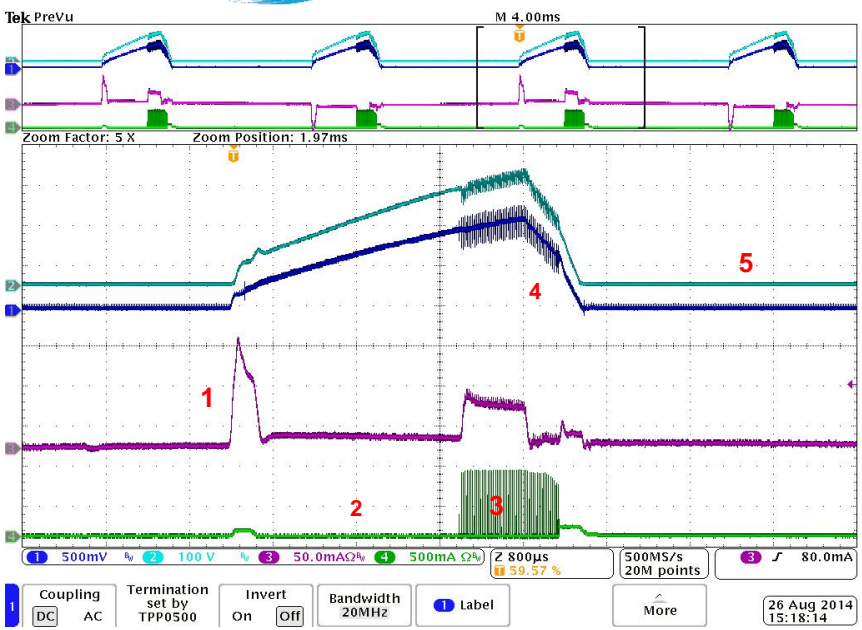




After the cut dimmer Operating mode

CH1: rectified AC before bridge; CH2: rectified AC after bridge ; CH3: Input current ; CH4: Isource





1. After detecting the line voltage is raised immediately closed *bleeder*

2.IC Silent until the forecast *buck-boost* Switch activation point

3.Buck-boost Fixed switching frequency and fixed to a peak current converting energy *led* . Input current is comparatively high and stable.

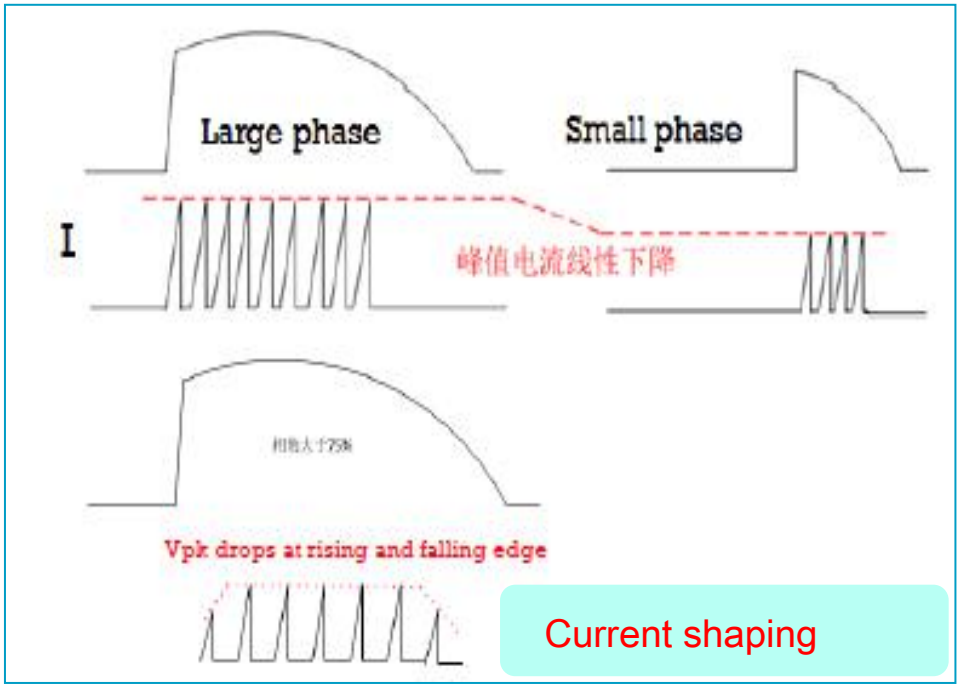
4. In the tangent, and the use of a current switch *bleeder* Current to the input capacitance of the dimmer and the capacitance discharge, *bleeder* Minimize loss

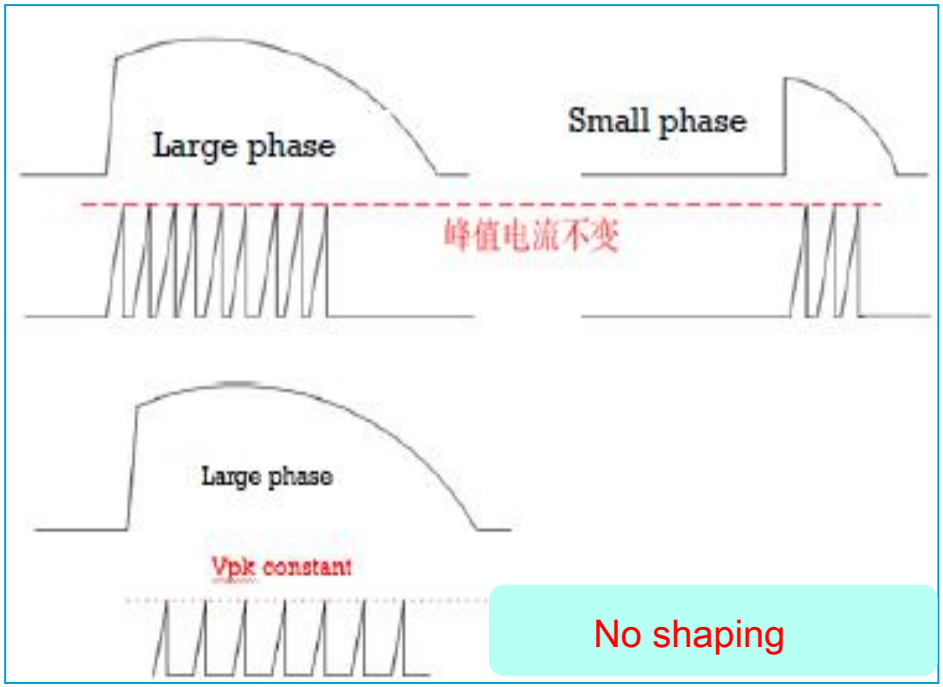
5.Bleeder Set to the maximum current, minimum input impedance. Since the tangent since almost no voltage is input, there is almost no loss. At the same time ensures a low input impedance and zero crossing detection timing adjusting clearance inside the interior of the normal operation may be

IC select

IC option

Part Number	0ption
IW3689-00	120Vac input, standard product
IW3681-10	120Vac, optimized for filament lamp, disable peak current shaping
IW3689-11	230Vac, optimized for low wattage design, disable peak current shaping
IW3689-01	230Vac input, standard product
IW3689-31	230Vac, optimized for filament lamp, disable peak current shaping





CFG Pin Value

IW3689-01, IW3689-00, IW3689-11

CFG Pin Resistor (R17 in Fig. 11.1)			No CFG Capacitor		CFG Capacitor (2.2nF)	
Min Value (kΩ)	Typical Value (kΩ)	Max Value (kΩ)	OTP Starting Point (°C)	V_{PK} at Dimmer Mode (V)	OTP Starting Point (°C)	V_{PK} at Dimmer Mode (V)
17.82	18.0		disabled	1.05	105	1.05
	0.40	0.69	105	0.95	105	0.95
1.39	1.65	1.91	105	0.85	105	0.85
2.78	3.0	3.22	105	0.75	105	0.75
4.28	4.45	4.62	115	1.05	125	1.05
5.88	6.05	6.22	115	0.95	125	0.95
7.70	7.85	8.00	115	0.85	125	0.85
9.74	9.88	10.01	115	0.75	125	0.75
12.04	12.18	12.31	135	0.95	135	1.05
14.67	14.85	15.03	135	0.75	135	0.85

Table 9.1 CFG Pin Configuration Resistor Values

IW3689-31, IW3681-10

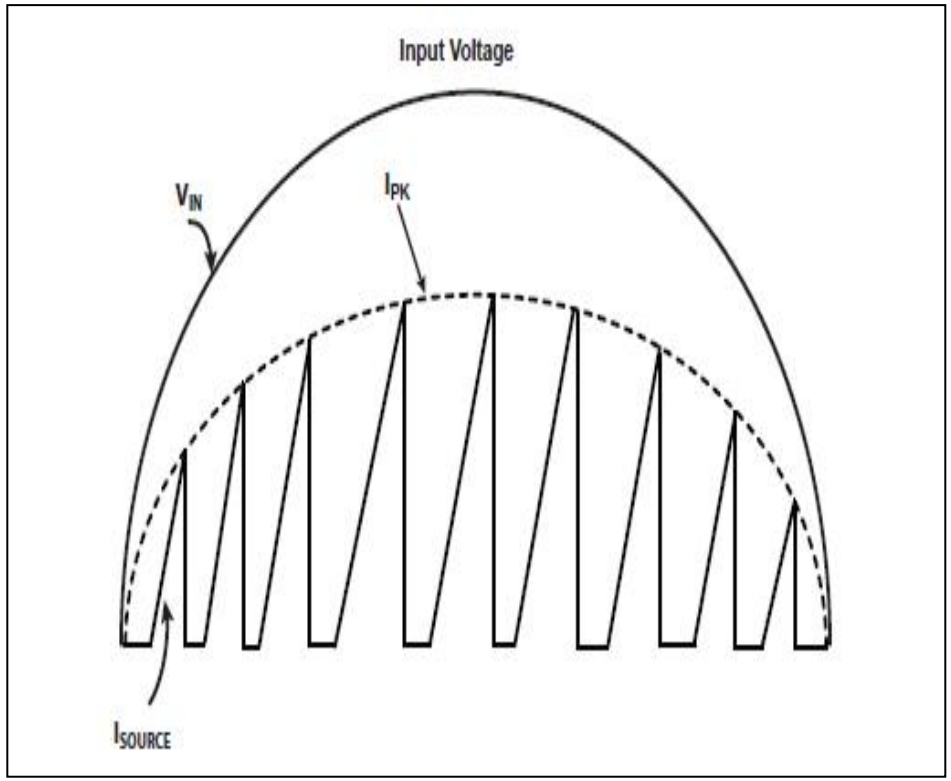
CFG Pin Resistor (R17 in Fig. 11.1)			No CFG Capacitor		CFG Capacitor (2.2nF)	
Min Value (kΩ)	Typical Value (kΩ)	Max Value (kΩ)	OTP Starting Point (°C)	V_{PK} at Dimmer Mode (V)/V_{IN} Rising Edge V_{PK} Clamp Value at No Dimmer Mode	OTP Starting Point (°C)	V_{PK} at Dimmer Mode (V)/V_{IN} Rising Edge V_{PK} Clamp Value at No Dimmer Mode
17.82	18.0		disabled	1.05/0.45	105	1.05/0.45
	0.40	0.69	105	0.95/0.4	105	0.95/0.4
1.39	1.65	1.91	105	0.85/0.35	105	0.85/0.35
2.78	3.0	3.22	105	0.75/0.3	105	0.75/0.3
4.28	4.45	4.62	115	1.05/0.45	125	1.05/0.45
5.88	6.05	6.22	115	0.95/0.4	125	0.95/0.4
7.70	7.85	8.00	115	0.85/0.35	125	0.85/0.35
9.74	9.88	10.01	115	0.75/0.3	125	0.75/0.3
12.04	12.18	12.31	135	0.95/0.4	135	1.05/0.45
14.67	14.85	15.03	135	0.75/0.3	135	0.85/0.35

Table 9.1 CFG Pin Configuration Resistor Values

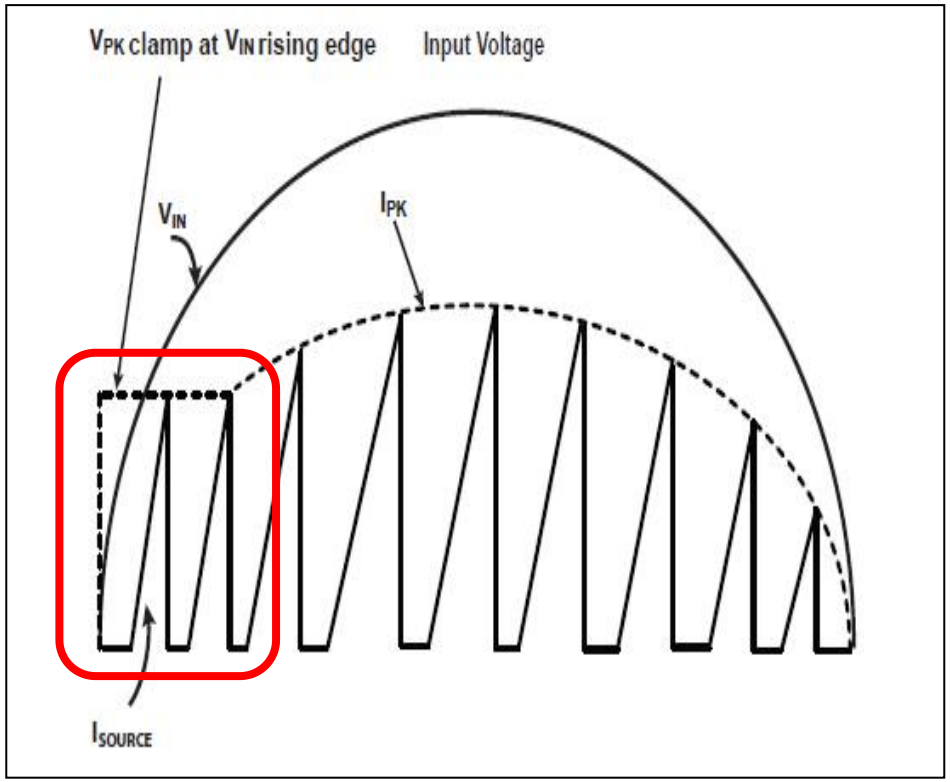
CFG The value determines the clamping voltage from the machine, Vipk and OTP Derating point; for IW3681-10 Low-voltage high-power design, please note CFG Configuration, ensure that the input current does not clamp, If the configuration is unreasonable, it will le Bleeder The duty cycle of the switching duty cycle together, the dimming process will produce once flicker phenomenon.

Peak Current Regulation in No-Dimmer Mode

IW3689-01, IW3689-00, IW3689-11



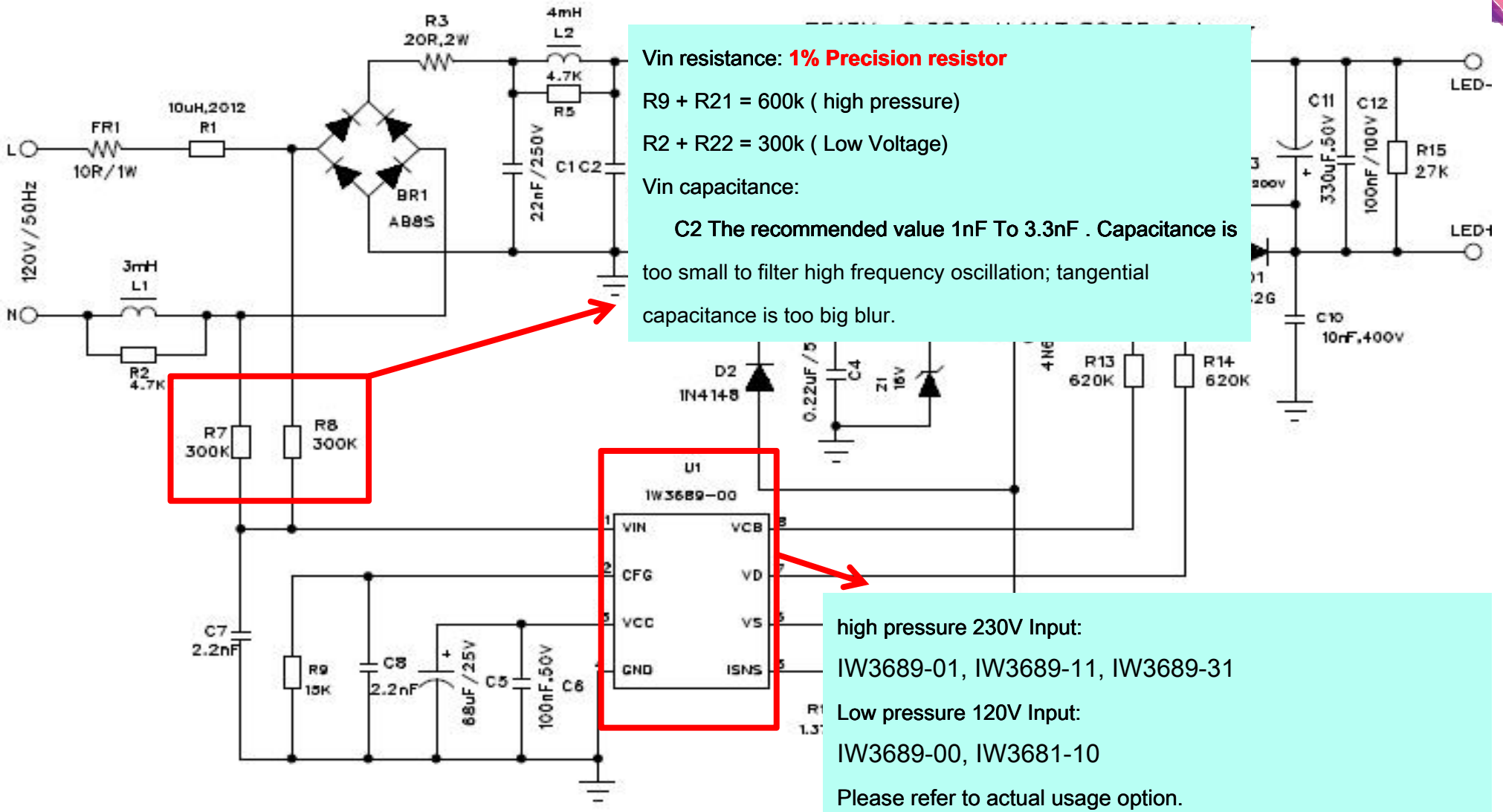
IW3689-31, IW3681-10



No dimmer State, since the difference of the motor current waveform.

Application Notes

IC versus Vin Related



Vin resistance: **1% Precision resistor**

R9 + R21 = 600k (high pressure)

R2 + R22 = 300k (Low Voltage)

Vin capacitance:

C2 The recommended value 1nF To 3.3nF . Capacitance is too small to filter high frequency oscillation; tangential capacitance is too big blur.

high pressure 230V Input:

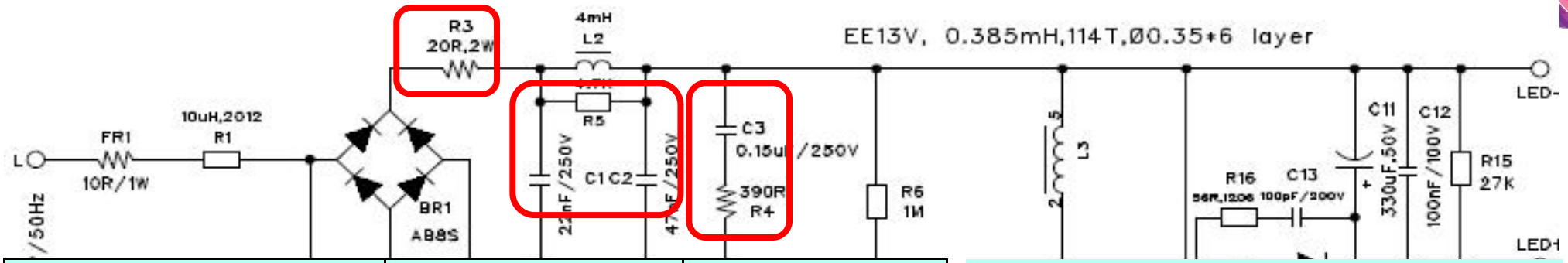
IW3689-01, IW3689-11, IW3689-31

Low pressure 120V Input:

IW3689-00, IW3681-10

Please refer to actual usage option.

Π Type capacitors, inrush , RC damping Related



application	C1 + C2	R13 (No potting)
3W-6W, 230Vac	10nF + 22nF	120R / 2W
6W-12W, 230Vac	10nF + 33nF	100R / 2W
12W-20W, 230Vac	22nF + 68nF	68R / 2W
3W-6W, 120Vac	22nF + 33nF	33R / 2W
6W-12W, 120Vac	22nF + 68nF	22R / 2W
12W-20W, 120Vac	22nF + 100nF	10R / 2W

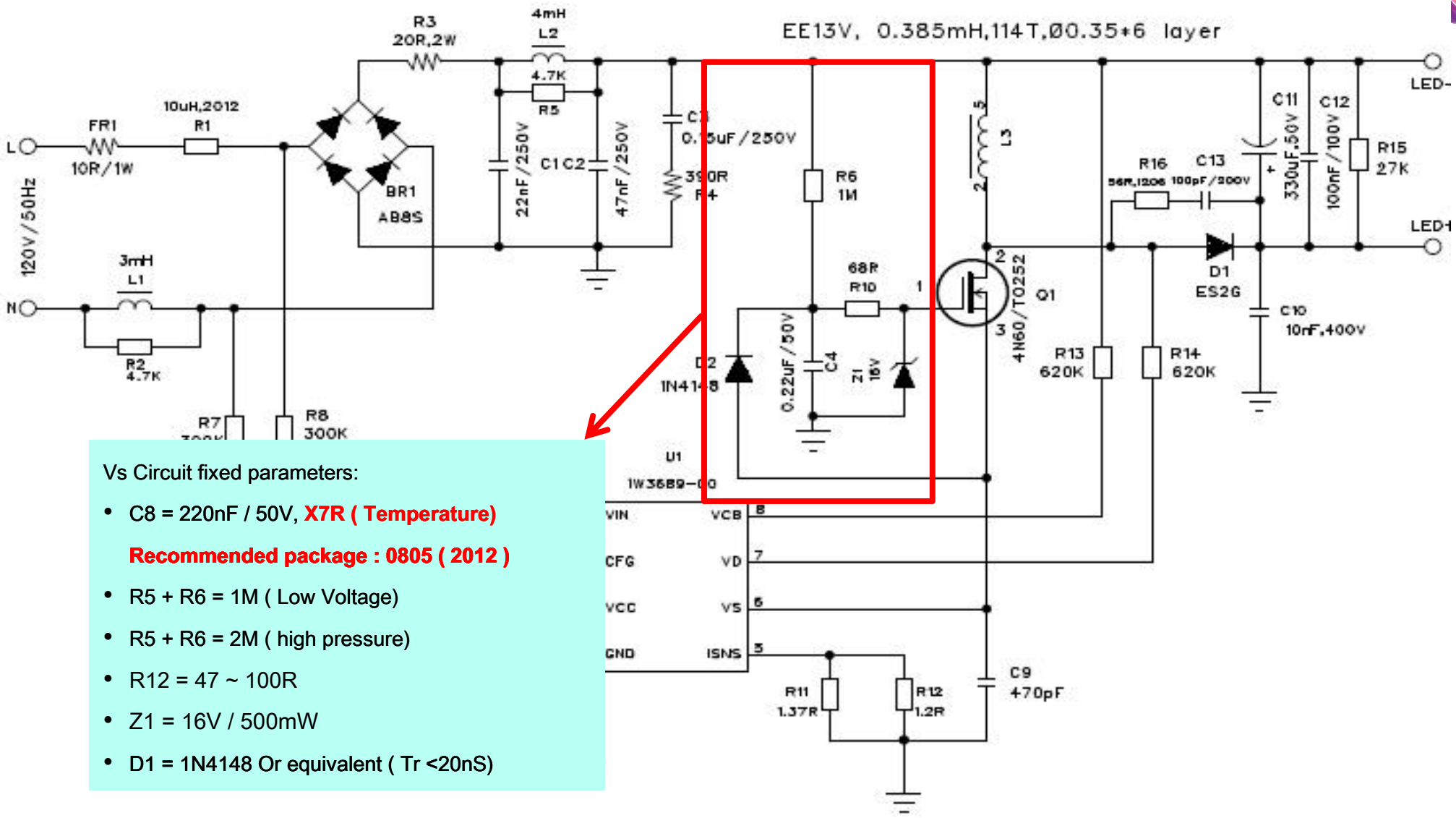
application	C3	R4
120V	0.15 ~ 0.22uF	390R / 2W
230V	0.1uF ~ 0.15uF	390R ~ 680R / 2W

External 20W About design , R3 , R4 use 3W Resistance, and the need to close cooling rack, between the body and the cooling rack increased thermal paste. Consider R3 , R4 Temperat the high voltage output **Power greater than 8W** design, C3 Consider using 0.1uF.

for GU10 design In order to achieve better dimmer Properties, the use of high pressure 150nF.

C1 versus C2 The larger the capacitance, dimmer mode under IC and MOSFET The higher the temperature. Please be adjusted according to the actual situation.

Vg Related

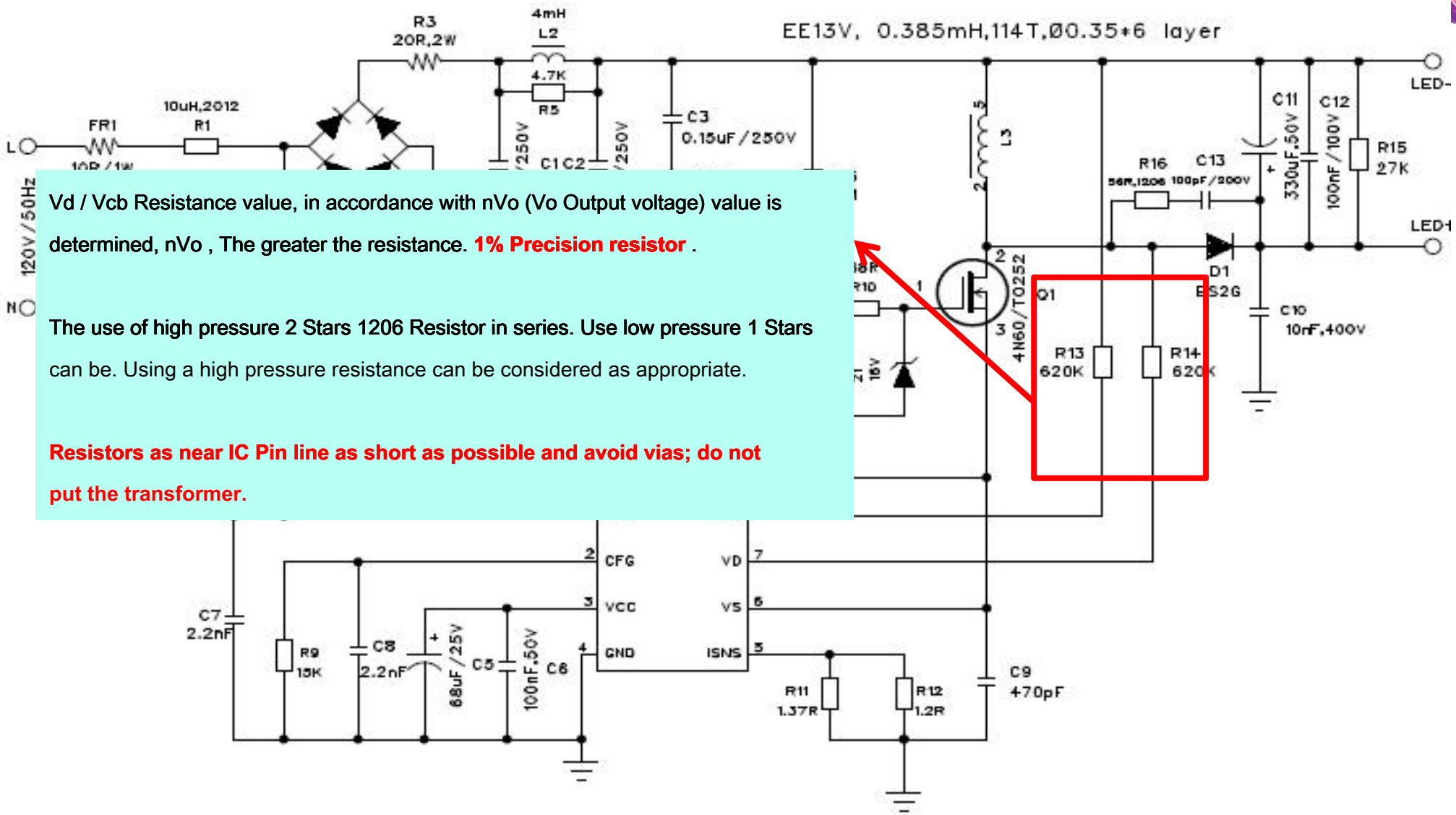


Vs Circuit fixed parameters:

- C8 = 220nF / 50V, **X7R (Temperature)**

  Recommended package : 0805 (2012)
- R5 + R6 = 1M (Low Voltage)
- R5 + R6 = 2M (high pressure)
- R12 = 47 ~ 100R
- Z1 = 16V / 500mW
- D1 = 1N4148 Or equivalent (Tr <20nS)

Vd , Vcb Related

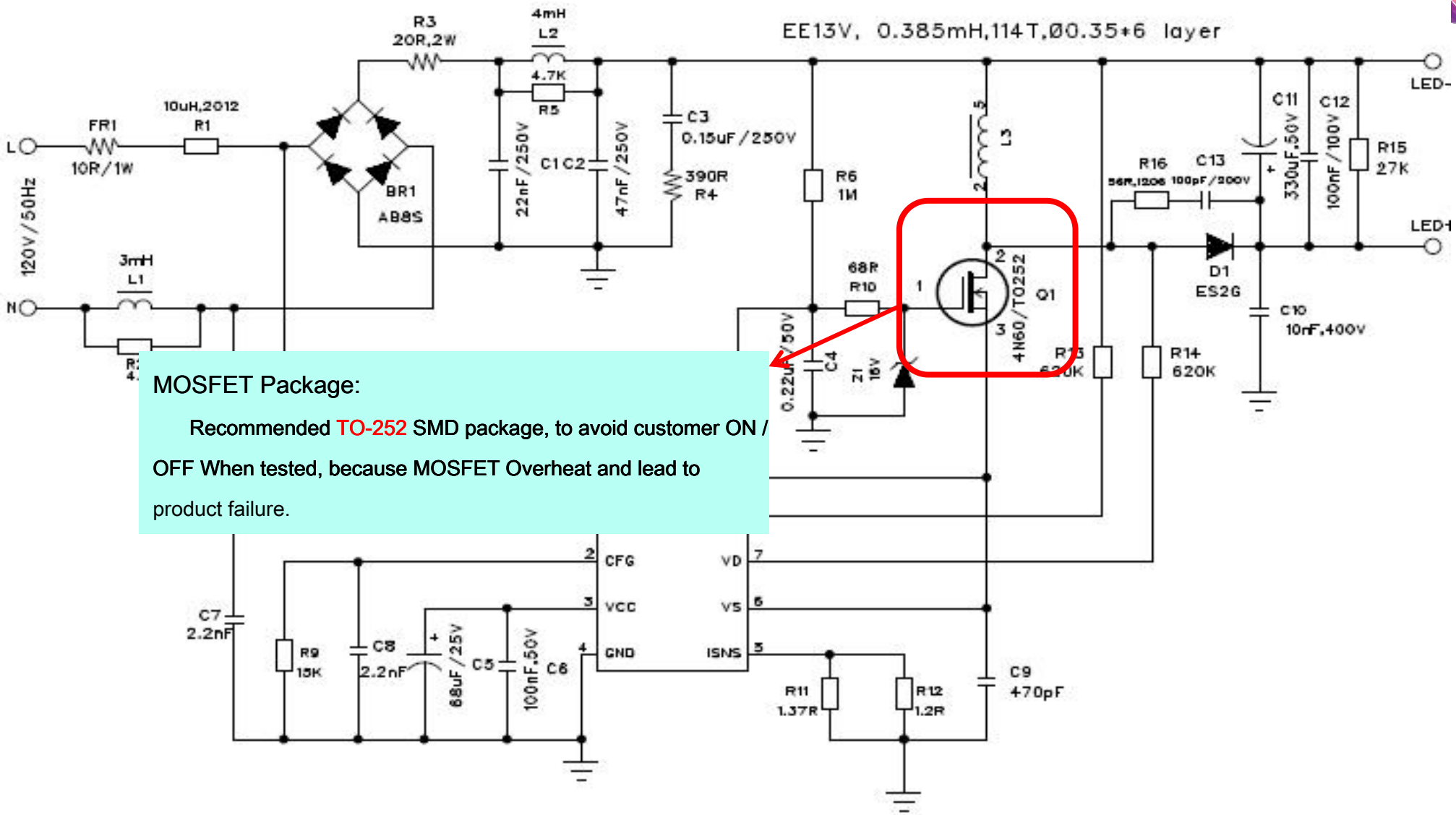


Vd / Vcb Resistance value, in accordance with nVo (Vo Output voltage) value is determined, nVo , The greater the resistance. **1% Precision resistor** .

The use of high pressure 2 Stars 1206 Resistor in series. Use low pressure 1 Stars can be. Using a high pressure resistance can be considered as appropriate.

Resistors as near IC Pin line as short as possible and avoid vias; do not put the transformer.

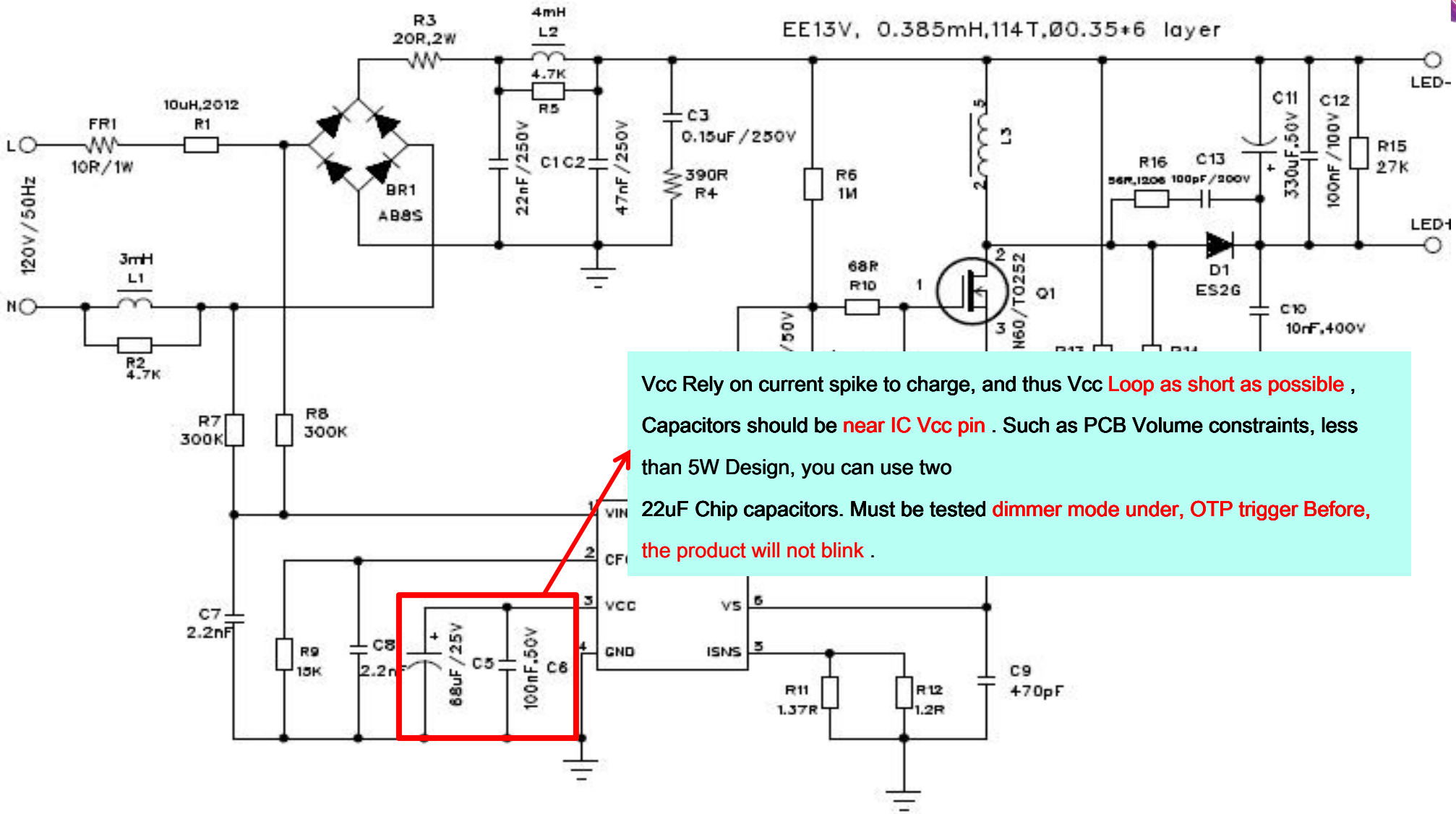
MOSFET Related



MOSFET Package:

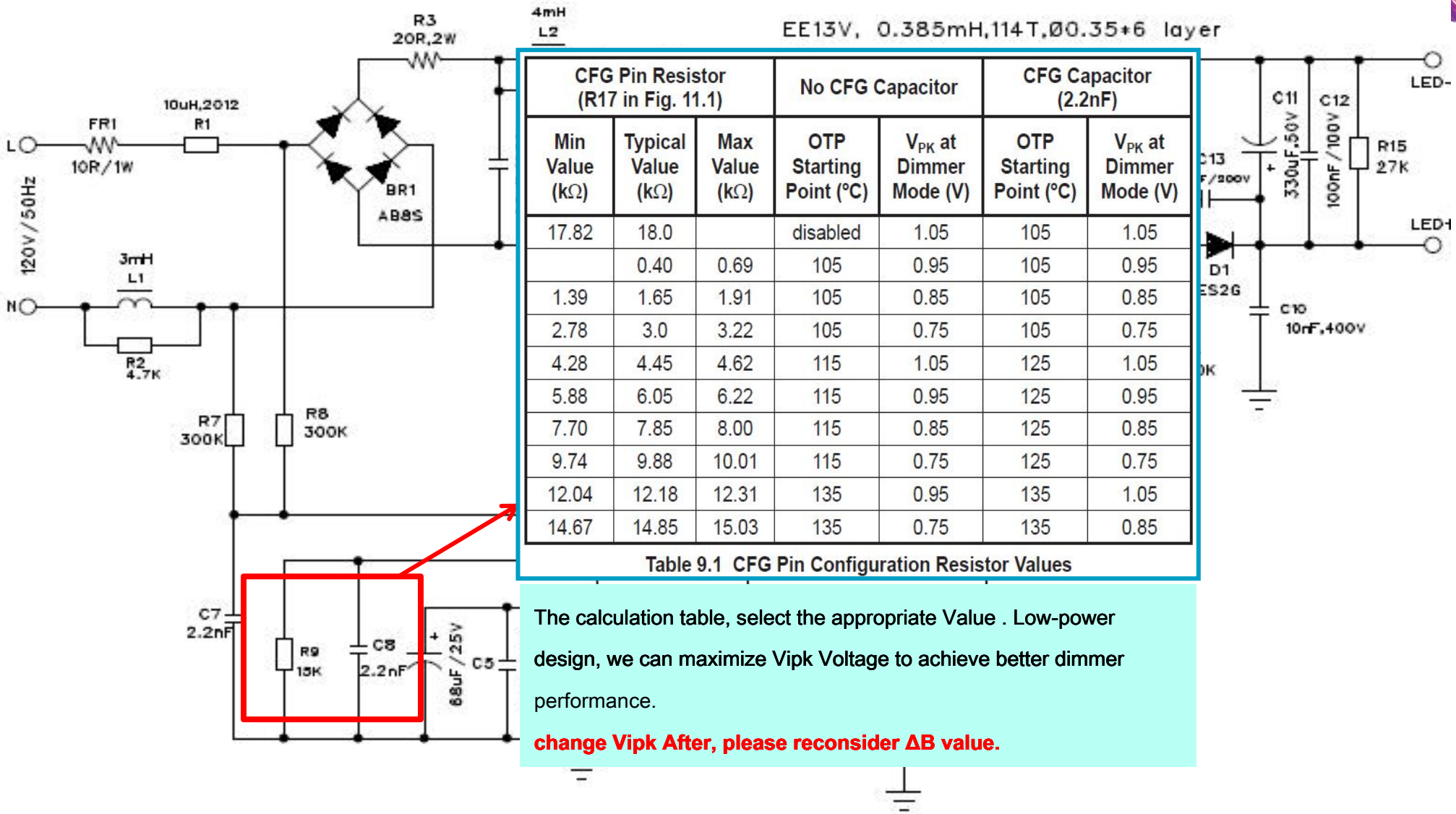
Recommended TO-252 SMD package, to avoid customer ON / OFF When tested, because MOSFET Overheat and lead to product failure.

Vcc Related



Vcc Rely on current spike to charge, and thus Vcc Loop as short as possible , Capacitors should be near IC Vcc pin . Such as PCB Volume constraints, less than 5W Design, you can use two 22uF Chip capacitors. Must be tested dimmer mode under, OTP trigger Before, the product will not blink .

CFG Related



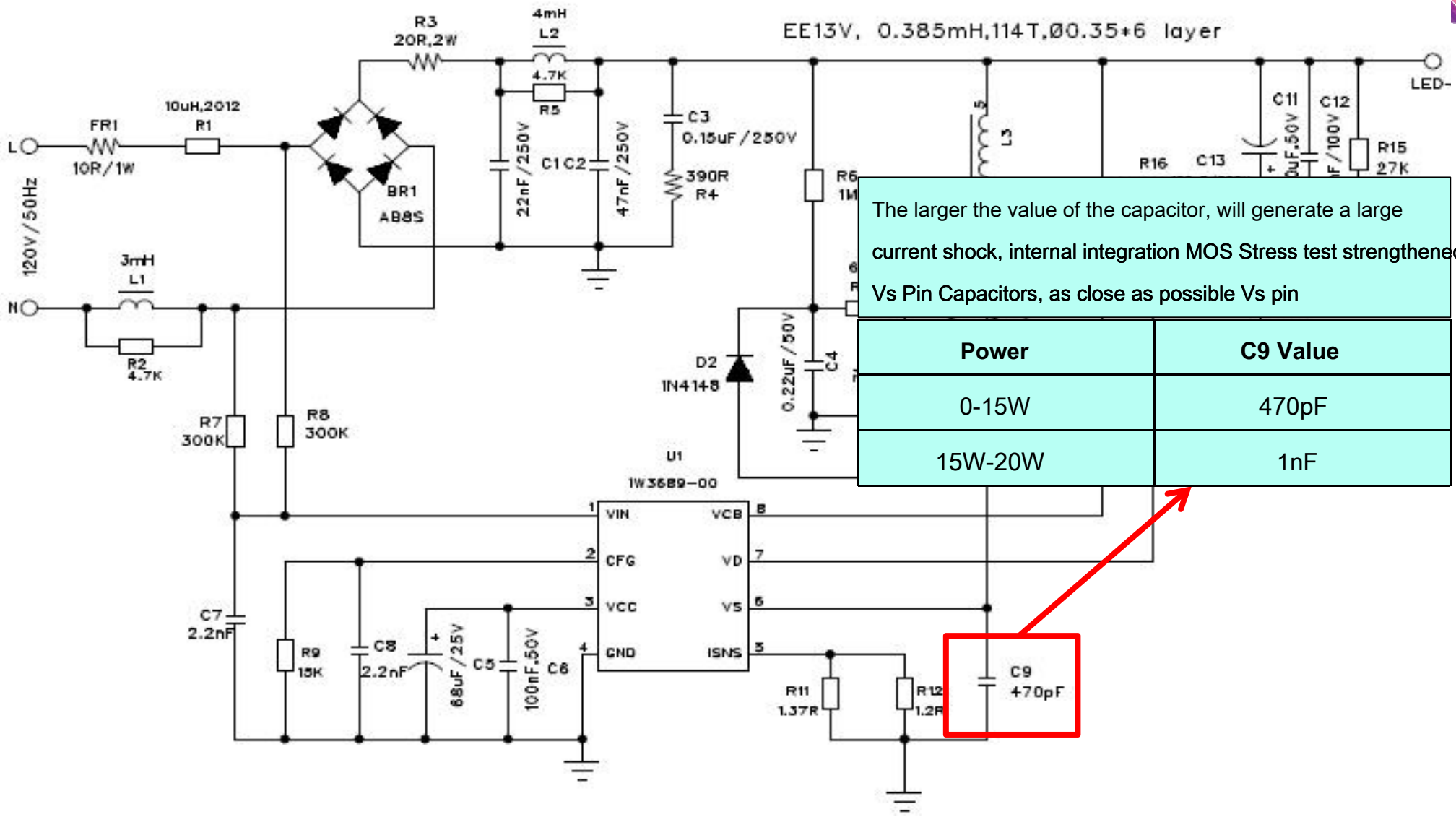
CFG Pin Resistor (R17 in Fig. 11.1)			No CFG Capacitor		CFG Capacitor (2.2nF)	
Min Value (kΩ)	Typical Value (kΩ)	Max Value (kΩ)	OTP Starting Point (°C)	V_{PK} at Dimmer Mode (V)	OTP Starting Point (°C)	V_{PK} at Dimmer Mode (V)
17.82	18.0		disabled	1.05	105	1.05
	0.40	0.69	105	0.95	105	0.95
1.39	1.65	1.91	105	0.85	105	0.85
2.78	3.0	3.22	105	0.75	105	0.75
4.28	4.45	4.62	115	1.05	125	1.05
5.88	6.05	6.22	115	0.95	125	0.95
7.70	7.85	8.00	115	0.85	125	0.85
9.74	9.88	10.01	115	0.75	125	0.75
12.04	12.18	12.31	135	0.95	135	1.05
14.67	14.85	15.03	135	0.75	135	0.85

Table 9.1 CFG Pin Configuration Resistor Values

The calculation table, select the appropriate Value . Low-power design, we can maximize Vipk Voltage to achieve better dimmer performance.

change Vipk After, please reconsider ΔB value.

Vs Pin Parallel capacitance



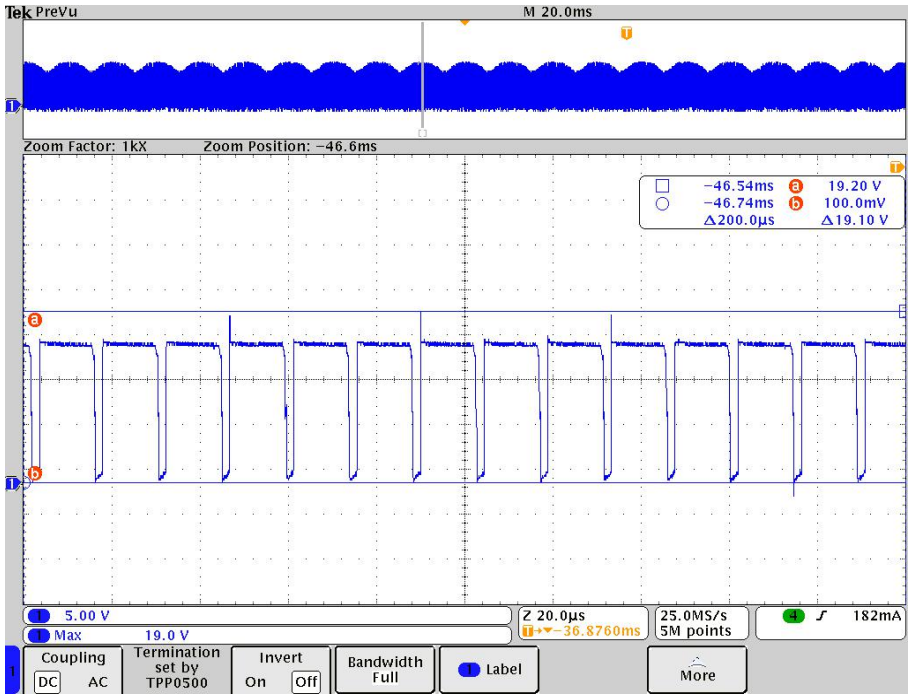
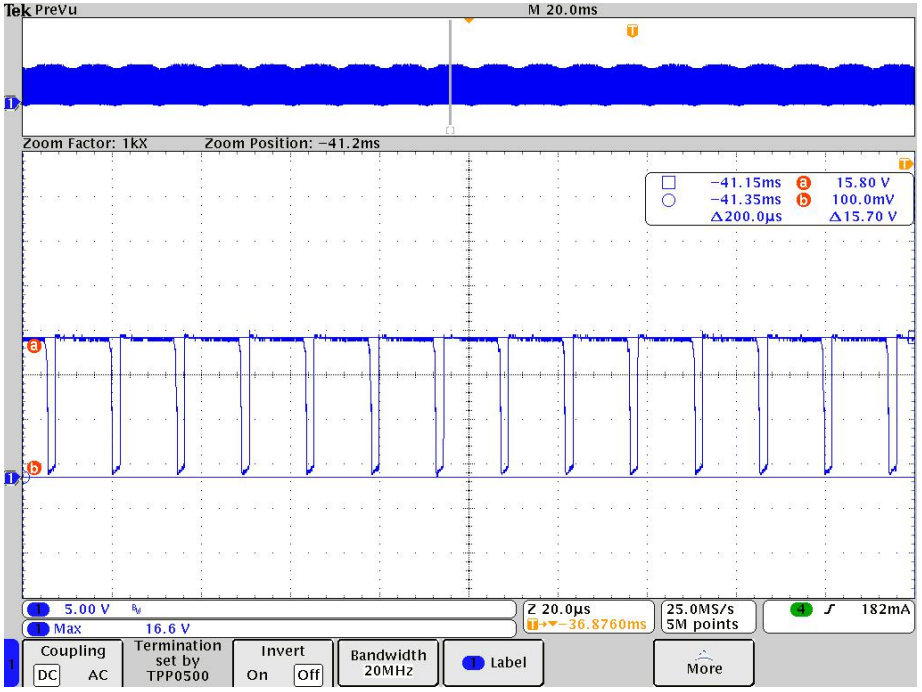
The larger the value of the capacitor, will generate a large current shock, internal integration MOS Stress test strengthened.

Vs Pin Capacitors, as close as possible Vs pin

Power	C9 Value
0-15W	470pF
15W-20W	1nF

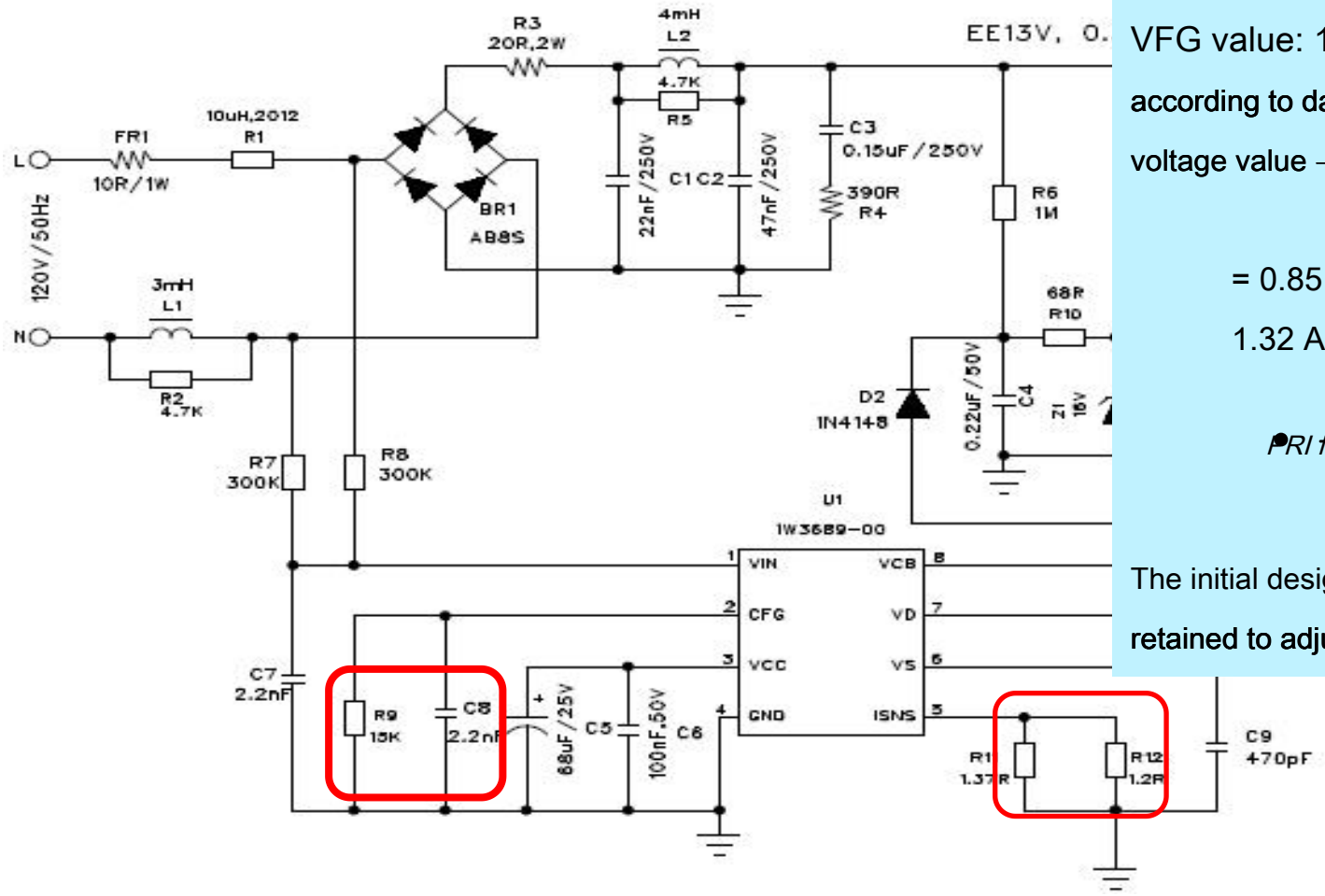
Vs Pin Voltage

When the test voltage, use oscilloscope **Full bandwidth** test. Different manufacturers MOSFET , Will lead to different test results, make sure **Vs Pin Voltage as low as possible** ! Recommended Huajing MOSFET.

Full bandwidth	20M bandwidth
	
Vs voltage: 19V	Vs voltage: 16.6V

ΔBmax Related

because dimmer mode Fixed Ipeak Current control calculation ΔB When, according to direct CFG Configured to calculate a voltage ΔB value. E.g:



VFG value: 15K and 2.2nF

according to datasheet Page 15 Table detect the voltage value → 0.85V Imax = Vipk / Risens

= 0.85 / (R11 // R12) =

1.32 A

$$\bullet\ I_{LB}$$

$$I_{PRI\ MAX} \bullet$$

$$\bullet\ A_{Ne}$$

The initial design, the appropriate margin can be retained to adjust Vipk .

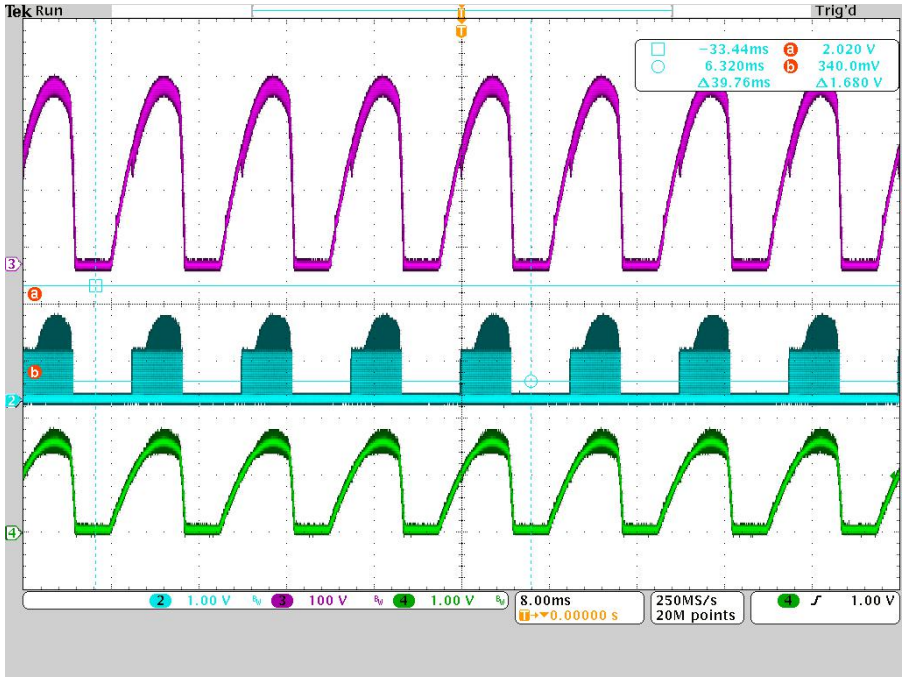
Thermal Related

Under the same condition, please test **Before cutting** Dimming state, the temperature of the product. Before cutting dimmer Mode of operation, after the end of the work cycle, CBB There is also a higher voltage, even when the capacitor light chopping Rear, bleeder This work requires some energy discharge, can cause MOSFET and IC The temperature rises.

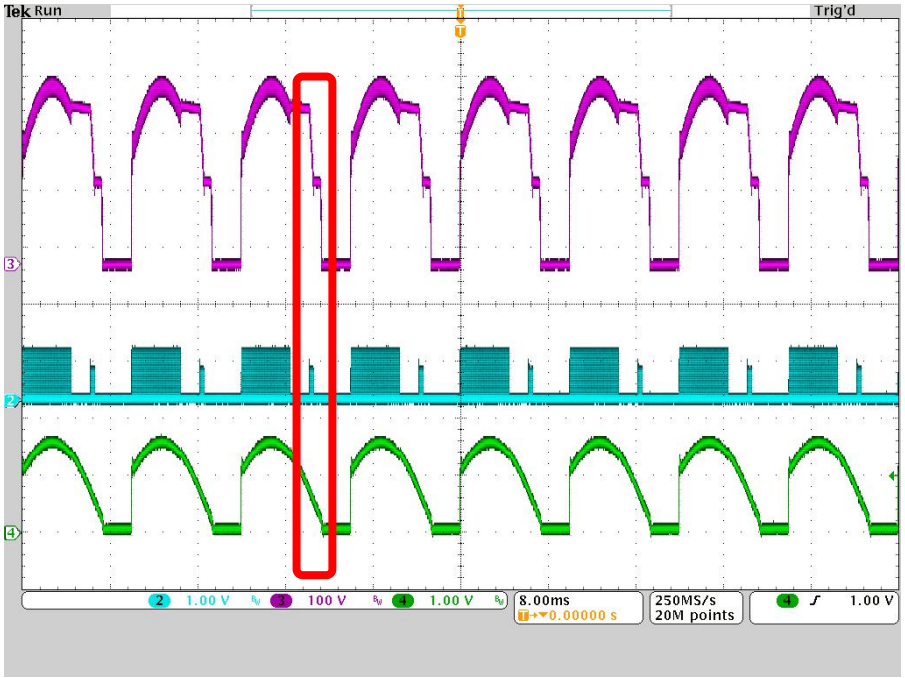
CH2 → Visens

CH3 → Vbulk CH4

→ Vin

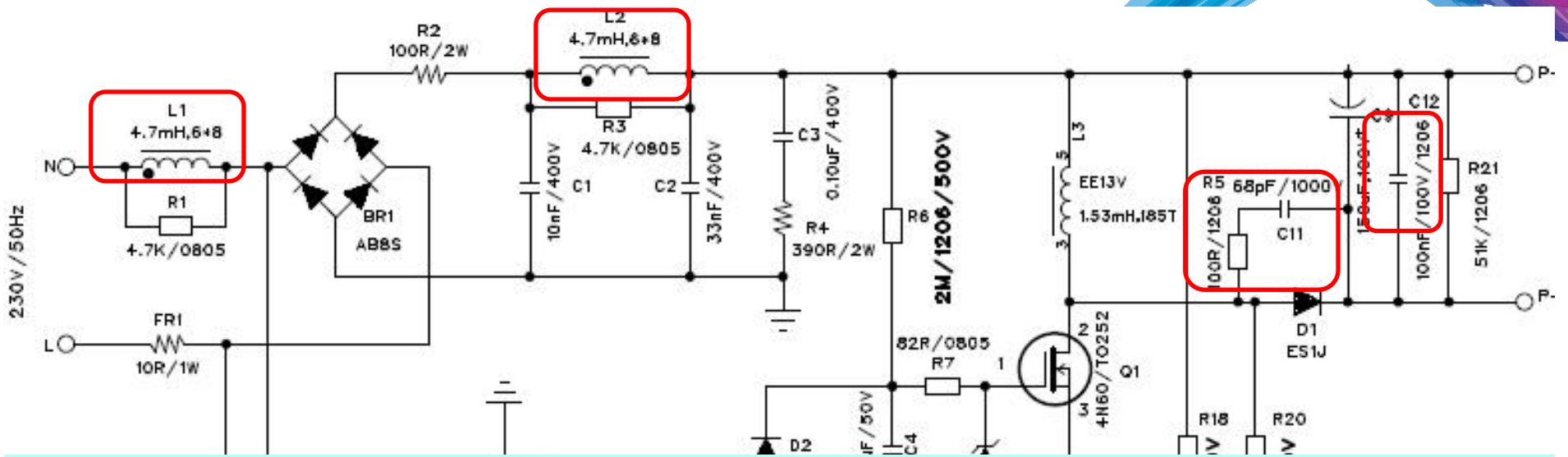


After the cut dimmer , Vbulk At the end of the work to zero



Before cutting dimmer , Was completed after light chopping Rear, bleeder Discharge.

EMI Related



For CE, Can increase the sense of the amount of differential mode inductance, if the space is large, the cost is not strict, you can use three differential mode inductance.

For RE, Non-isolated parallel design about 100nF ~ 200nF MLCC chip LED + and between the LED - (considering the withstand voltage, to select the appropriate pressure); or an increase in the capacitance between the primary and the LED +, the capacitance value of 1 ~ 4.7nF .

The output diode may absorb parallel RC.

And try to rest core transformer shield grounded.

When testing, use **Supporting the housing and lamps** .

Isolate design --- Vds

To ensure that IC Accurate sampling, ensure that the transformer frequencies below 500nS.

In isolation design, RCD Line series R26 , The resistance of the resistance can be suitably adjusted according to test results. To ensure that under extreme conditions, there is sufficient margin.