Siliconix

FET Design Catalog

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Contents

INTRODUCTION Index 1

SELECTOR GUIDES Index 2

Product Specifications

DATA SHEETS, METAL CAN (In Numeric-Alpha Order) Index 3

Refer to FET Cross Reference and Index

DATA SHEETS, PLASTIC (In Numeric-Alpha Order) Index 4

Refer to FET Cross Reference and Index

GEOMETRY CHARACTERISTICS Index 5

Refer to FET Cross Reference and Index

APPLICATION NOTES Index 6

MECHANICAL DATA & SALES OFFICES Index 7

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PARTS NOT READILY AVAILABLE IN EUROPE

The following device types are classified as *specials* (non-preferred parts). These devices are not readily available through European Sales Outlets. For further details and availability contact the Siliconix Sales Office or Franchised Distributor nearest you.

2N3368/69/70
2N3684/85/86/87
2N3909
2N4867A/68A/69A
2N5078
2N5515–24
2N5555
2N5556/57/58
2N5653/54
2N5669/70
JAN/JANTX Series
J230/31/32
K114–18
K1837–18
K210/11/12 (–18)
KK4416–18
MFE823
MPF102
MPF108
MPF109
MPF111
MPF112
PN4416
PN5163
U1837
U1994

EUROPEAN HI-REL PARTS

The Following Devices Have Been Approved to BS CECC European Standards:

Type Number	**BS CECC Specification**
2N3970/1/2	BS CECC 50 012-001 (ISSUE 1, JUNE 1978)
2N4091/2/3	BS CECC 50 012-002 (ISSUE 1, JUNE 1978)
2N4391/2/3	BS CECC 50 012-004 (ISSUE 1, APRIL 1978)
2N4856/7/8	BS CECC 50 012-005 (ISSUE 1, JUNE 1978)
2N4859/60/61	BS CECC 50 012-005 (ISSUE 1, JUNE 1978)
2N4856A/7A/8A	BS CECC 50 012-006 (ISSUE 1, JUNE 1978)
2N4859A/60A/61A	BS CECC 50 012-006 (ISSUE 1, JUNE 1978)

For Details on Other Products Submitted for Approval, Contact Your Nearest Siliconix Sales Office or Franchised Distributor.

how to use the
FET Cross Reference *and* Index

The following examples illustrate how the FET Cross Reference and Index should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3458	N JFET	2N3458

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison. **Refer to appropriate page number listed under Data Sheet or Geometry column.**

Type and classification abbreviations are described as follows:

CR (Current Limiter)	**JPAD** (Plastic Pico Ampere Diode)
D (Dual)	**N** (N-Channel)
DPAD (Dual Pico Ampere Diode)	**P** (P-Channel)
ENH (Enhancement-Mode Normally-Off)	**PAD** (Pico Ampere Diode)
G (Gate)	**VMOS** (Vertical MOSFET)

FET Cross Reference *and* Index

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
1N5283	CL N JFET	CR022	3-45	5-12
1N5284	CL N JFET	CR024	3-45	5-12
1N5285	CL N JFET	CR027	3-45	5-12
1N5286	CL N JFET	CR030	3-45	5-12
1N5287	CL N JFET	CR033	3-45	5-12
1N5288	CL N JFET	CR039	3-45	5-12
1N5289	CL N JFET	CR043	3-45	5-12
1N5290	CL N JFET	CR047	3-45	5-12
1N5291	CL N JFET	CR056	3-45	5-12
1N5292	CL N JFET	CR062	3-45	5-12
1N5293	CL N JFET	CR068	3-45	5-13
1N5294	CL N JFET	CR075	3-45	5-13
1N5295	CL N JFET	CR082	3-45	5-13
1N5296	CL N JFET	CR091	3-45	5-13
1N5297	CL N JFET	CR100	3-45	5-13
1N5298	CL N JFET	CR110	3-45	5-13
1N5299	CL N JFET	CR120	3-45	5-13
1N5300	CL N JFET	CR130	3-45	5-13
1N5301	CL N JFET	CR140	3-45	5-13
1N5302	CL N JFET	CR150	3-45	5-13
1N5303	CL N JFET	CR160	3-45	5-14
1N5304	CL N JFET	CR180	3-45	5-14
1N5305	CL N JFET	CR200	3-45	5-14
1N5306	CL N JFET	CR220	3-45	5-14
1N5307	CL N JFET	CR240	3-45	5-14
1N5308	CL N JFET	CR270	3-45	5-14
1N5309	CL N JFET	CR300	3-45	5-14
1N5310	CL N JFET	CR330	3-45	5-14
1N5311	CL N JFET	CR360	3-45	5-14
1N5312	CL N JFET	CR390	3-45	5-14
1N5313	CL N JFET	CR430	3-45	5-14
1N5314	CL N JFET	CR470	3-45	5-14
2N2386	P JFET	2N608		
2N2386A	P JFET	2N609		
2N2497	P JFET	2N3329		
2N2498	P JFET	2N3330		
2N2499	P JFET	2N3331		
2N2500	P JFET	2N3332		
2N506	P JFET	2N2608		
2N2606JAN	P JFET	2N2608JAN		
2N2607	P JFET	2N2608		
2N2607JAN	P JFET	2N2608JAN		
2N2608	P JFET	2N2608	3-1	5-36
2N2608JAN	P JFET	2N2608JAN		
2N2609	P JFET	2N2609	3-1	5-37
2N2609JAN	P JFET	2N2609JAN		
2N2841	P JFET	2N2843		
2N2842	P JFET	2N2843		
2N2843	P JFET	2N2843	3-2	5-36
2N2844	P JFET	2N2844	3-2	5-37
2N3066	N JFET	2N4340		
2N3067	N JFET	2N4338		
2N3068	N JFET	2N4338		
2N3069	N JFET	2N4341		
2N3070	N JFET	2N4339		
2N3071	N JFET	2N4338		
2N3084	N JFET	2N3459		
2N3085	N JFET	2N3459		
2N3086	N JFET	2N3459		
2N3087	N JFET	2N3459		
2N3088	N JFET	2N3460		
2N3088A	N JFET	2N3460		
2N3089	N JFET	2N3460		
2N3089A	N JFET	2N3460		
2N3113	P JFET	2N2843		
2N3277	P JFET	2N2608		
2N3278	P JFET	2N2608		
2N3328	P JFET	2N3438		
2N3329	P JFET	2N3329	3-3	5-36
2N3330	P JFET	2N3330	3-3	5-36
2N3331	P JFET	2N3331	3-3	5-36
2N3332	P JFET	2N3332	3-3	5-36
2N3365	N JFET	2N4340		
2N3366	N JFET	2N4338		
2N3367	N JFET	2N4338		
2N3368	N JFET	2N3368	3-4	5-19
2N3369	N JFET	2N3369	3-4	5-19
2N3370	N JFET	2N3370	3-4	5-19
2N3376	P JFET	2N3329		
2N3378	P JFET	2N3330		
2N3380	P JFET	2N3331		
2N3382	P JFET	2N3382	3-5	5-38
2N3384	P JFET	2N3384	3-5	5-38
2N3386	P JFET	2N3386	3-5	5-38
2N3436	N JFET	2N3436	3-6	5-19
2N3437	N JFET	2N3437	3-6	5-19
2N3438	N JFET	2N3438	3-6	5-19
2N3452	N JFET	2N4340		
2N3453	N JFET	2N4338		
2N3454	N JFET	2N4338		
2N3455	N JFET	2N4340		
2N3456	N JFET	2N4338		
2N3457	N JFET	2N4338		
2N3458	N JFET	2N3458	3-7	5-19
2N3459	N JFET	2N3459	3-7	5-19
2N3460	N JFET	2N3460	3-7	5-19
2N3574	P JFET	2N2843		
2N3575	P JFET	2N2843		
2N3578	P JFET	2N2608		
2N3608	P MOS ENH	3N163		
2N3684	N JFET	2N3684	3-8	5-6
2N3685	N JFET	2N3685	3-8	5-6
2N3686	N JFET	2N3686	3-8	5-6
2N3687	N JFET	2N3687	3-8	5-6
2N3819	N JFET	2N3819	4-1	5-25
2N3820	P JFET	J270		
2N3821	N JFET	2N3821	3-9	5-25
2N3822	N JFET	2N3822	3-9	5-25
2N3823	N JFET	2N3823	3-10	5-25
2N3824	N JFET	2N3824	3-11	5-25

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
2N3909	P JFET	2N3909	3-12	5-36
2N3909A	P JFET	2N3909		
2N3921	D N JFET	2N3921	3-13	5-17
2N3922	D N JFET	2N3922	3-13	5-17
2N3954	D N JFET	2N3954	3-14	5-6
2N3954A	D N JFET	2N3954A	3-14	5-6
2N3955	D N JFET	2N3955	3-14	5-6
2N3955A	D N JFET	2N3955A	3-14	5-6
2N3956	D N JFET	2N3956	3-15	5-6
2N3957	D N JFET	2N3957	3-15	5-6
2N3958	D N JFET	2N3958	3-15	5-6
2N3966	N JFET	2N3966	3-16	5-8
2N3967	N JFET	2N4221		
2N3967A	N JFET	2N4221		
2N3968	N JFET	2N3685		
2N3968A	N JFET	2N3685		
2N3969	N JFET	2N3686		
2N3969A	N JFET	2N3686		
2N3970	N JFET	2N3970	3-17	5-3
2N3971	N JFET	2N3971	3-17	5-3
2N3972	N JFET	2N3972	3-17	5-3
2N3993	P JFET	2N3386		
2N3993A	P JFET	2N3386		
2N3994	P JFET	2N3382		
2N3994A	P JFET	2N3382		
2N4084	D N JFET	2N4084	3-13	5-17
2N4085	D N JFET	2N4085	3-13	5-17
2N4091	N JFET	2N4091	3-19	5-3
2N4091A	N JFET	2N4091		
2N4092	N JFET	2N4092	3-19	5-3
2N4092A	N JFET	2N4092		
2N4093	N JFET	2N4093	3-19	5-3
2N4093A	N JFET	2N4093		
2N4117	N JFET	2N4117	3-20	5-29
2N4117A	N JFET	2N4117A	3-20	5-29
2N4118	N JFET	2N4118	3-20	5-29
2N4118A	N JFET	2N4118A	3-20	5-29
2N4119	N JFET	2N4119	3-20	5-29
2N4119A	N JFET	2N4119A	3-20	5-29
2N4120	P MOS ENH	3N163		
2N4139	N JFET	2N3822		
2N4220	N JFET	2N4220	3-22	5-25
2N4220A	N JFET	2N4220A	3-22	5-25
2N4221	N JFET	2N4221	3-22	5-25
2N4221A	N JFET	2N4221A	3-22	5-25
2N4222	N JFET	2N4222	3-22	5-25
2N4222A	N JFET	2N4222A	3-22	5-25
2N4223	N JFET	2N4223	3-23	5-25
2N4224	N JFET	2N4224	3-23	5-25
2N4267	P MOS ENH	3N163		
2N4302	N JFET	PN4302-18		
2N4303	N JFET	PN4303-18		
2N4304	N JFET	PN4304-18		
2N4338	N JFET	2N4338	3-24	5-19
2N4339	N JFET	2N4339	3-24	5-19
2N4340	N JFET	2N4340	3-24	5-19
2N4341	N JFET	2N4341	3-24	5-19
2N4352	P MOS ENH	3N163		
2N4381	P JFET	2N2609		
2N4382	P JFET	2N5115		
2N4391	N JFET	2N4391	3-26	5-3
2N4392	N JFET	2N4392	3-26	5-3
2N4393	N JFET	2N4393	3-26	5-3
2N4416	N JFET	2N4416	3-27	5-8
2N4416A	N JFET	2N4416A	3-27	5-8
2N445	N JFET	2N5432		
2N446	N JFET	2N5433		
2N448	N JFET	2N5432		
2N448	N JFET	2N5433		
2N4856	N JFET	2N4856	3-28	5-3
2N4856A	N JFET	2N4856A	3-29	5-3
2N4856JAN	N JFET	2N4856JAN		5-3
2N4856JANTX	N JFET	2N4856JANTX		5-3
2N4856JANTXV	N JFET	2N4856JANTXV		5-3
2N4857	N JFET	2N4857	3-28	5-3
2N4857A	N JFET	2N4857A	3-29	5-3
2N4857JAN	N JFET	2N4857JAN		5-3
2N4857JANTX	N JFET	2N4857JANTX		5-3
2N4857JANTXV	N JFET	2N4857JANTXV		5-3
2N4858	N JFET	2N4858	3-28	5-3
2N4858A	N JFET	2N4858A	3-29	5-3
2N4858JAN	N JFET	2N4858JAN		5-3
2N4858JANTX	N JFET	2N4858JANTX		5-3
2N4858JANTXV	N JFET	2N4858JANTXV		5-3
2N4859	N JFET	2N4859	3-28	5-3
2N4859A	N JFET	2N4859A	3-29	5-3
2N4859JAN	N JFET	2N4859JAN		5-3
2N4859JANTX	N JFET	2N4859JANTX		5-3
2N4859JANTXV	N JFET	2N4859JANTXV		5-3
2N4860	N JFET	2N4860	3-28	5-3
2N4860A	N JFET	2N4860A	3-29	5-3
2N4860JAN	N JFET	2N4860JAN		5-3
2N4860JANTX	N JFET	2N4860JANTX		5-3
2N4860JANTXV	N JFET	2N4860JANTXV		5-3
2N4861	N JFET	2N4861	3-28	5-3
2N4861A	N JFET	2N4861A	3-29	5-3
2N4861JAN	N JFET	2N4861JAN		5-3
2N4861JANTX	N JFET	2N4861JANTX		5-3
2N4861JANTXV	N JFET	2N4861JANTXV		5-3
2N4867	N JFET	2N4867	3-30	5-27
2N4867A	N JFET	2N4867A	3-30	5-27
2N4868	N JFET	2N4868	3-30	5-27
2N4868A	N JFET	2N4868A	3-30	5-27
2N4869	N JFET	2N4869	3-30	5-27
2N4869A	N JFET	2N4869A	3-30	5-27
2N4977	N JFET	2N5432		
2N4978	N JFET	2N5433		
2N4979	N JFET	2N5434		
2N5018	P JFET	2N5018	3-31	5-39
2N5019	P JFET	2N5019	3-31	5-39

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
2N5020	P JFET	2N2843		
2N5021	P JFET	2N2608		
2N5033	P JFET	2N2608		
2N5045	D N JFET	2N5045	3-32	5-17
2N5046	D N JFET	2N5046	3-32	5-17
2N5047	D N JFET	2N5047	3-32	5-17
2N5103	N JFET	2N4416		
2N5104	N JFET	2N4416		
2N5105	N JFET	2N4416		
2N5114	P JFET	2N5114	3-33	5-39
2N5115	P JFET	2N5115	3-33	5-39
2N5116	P JFET	2N5116	3-33	5-39
2N5158	N JFET	2N5434		
2N5159	N JFET	2N5433		
2N5196	D N JFET	2N5196	3-34	5-15
2N5197	D N JFET	2N5197	3-34	5-15
2N5198	D N JFET	2N5198	3-34	5-15
2N5199	D N JFET	2N5199	3-34	5-15
2N5245	N JFET	KK4418		
2N5246	N JFET	J305-18		
2N5247	N JFE	J304-18		
2N5248	N JFET	2N5486		
2N5257	N JFET	2N5457		
2N5258	N JFET	2N5458		
2N5259	N JFET	2N5459		
2N5265	P JFET	2N2608		
2N5266	P JFET	2N2608		
2N5267	P JFET	2N2608		
2N5268	P JFET	2N2608		
2N5269	P JFET	2N3331		
2N5270	P JFET	2N3331		
2N5358	N JFET	2N3686		
2N5359	N JFET	2N3686		
2N5360	N JFET	2N3685		
2N5361	N JFET	2N3684		
2N5362	N JFET	2N3684		
2N5363	N JFET	2N4222A		
2N5364	N JFET	2N4224		
2N5391	N JFET	2N4867A		
2N5392	N JFET	2N4868A		
2N5393	N JFET	2N4869A		
2N5394	N JFET	2N4869A		
2N5395	N JFET	2N4869A		
2N5396	N JFET	2N4869A		
2N5397	N JFET	U310		
2N5398	N JFET	U312		
2N5432	N JFET	2N5432	3-35	5-10
2N5433	N JFET	2N5433	3-35	5-10
2N5434	N JFET	2N5434	3-35	5-10
2N5452	D N JFET	2N5452	3-36	5-6
2N5453	D N JFET	2N5453	3-36	5-6
2N5454	D N JFET	2N5454	3-36	5-6
2N5457	N JFET	2N5457	4-2	5-25
2N5458	N JFET	2N5458	4-2	5-25
2N5459	N JFET	2N5459	4-2	5-25
2N5484	N JFET	2N5484	4-3	5-8
2N5485	N JFET	2N5485	4-3	5-8
2N5486	N JFET	2N5486	4-3	5-8
2N5515	D N JFET	2N5515	3-37	5-27
2N5516	D N JFET	2N5516	3-37	5-27
2N5517	D N JFET	2N5517	3-37	5-27
2N5518	D N JFET	2N5518	3-37	5-27
2N5519	D N JFET	2N5519	3-37	5-27
2N5520	D N JFET	2N5520	3-37	5-27
2N5521	D N JFET	2N5521	3-37	5-27
2N5522	D N JFET	2N5522	3-37	5-27
2N5523	D N JFET	2N5523	3-37	5-27
2N5524	D N JFET	2N5524	3-37	5-27
2N5545	D N JFET	2N5545	3-38	5-15
2N5546	D N JFET	2N5546	3-38	5-15
2N5547	D N JFET	2N5547	3-38	5-15
2N5549	N JFET	2N4392		
2N5555	N JFET	2N5555	4-4	5-8
2N5556	N JFET	2N5556	3-39	5-25
2N5557	N JFET	2N5557	3-39	5-25
2N5558	N JFET	2N5558	3-39	5-25
2N5561	D N JFET	U401		
2N5562	D N JFET	U402		
2N5563	D N JFET	U404		
2N5564	D N JFET	2N5564	3-40	5-3
2N5565	D N JFET	2N5565	3-40	5-3
2N5566	D N JFET	2N5566	3-40	5-3
2N5592	N JFET	2N3822		
2N5593	N JFET	2N3822		
2N5594	N JFET	2N3822		
2N5638	N JFET	2N5638	4-5	5-3
2N5639	N JFET	2N5639	4-5	5-3
2N5640	N JFET	2N5640	4-5	5-3
2N5647	N JFET	2N4117A		
2N5648	N JFET	2N4117A		
2N5649	N JFET	2N4117A		
2N5653	N JFET	2N5653	4-6	5-3
2N5654	N JFET	2N5654	4-6	5-3
2N5668	N JFET	2N5668	4-7	5-8
2N5669	N JFET	2N5669	4-7	5-8
2N5670	N JFET	2N5670	4-7	5-8
2N5797	P JFET	2N2608		
2N5798	P JFET	2N2608		
2N5799	P JFET	2N2608		
2N5800	P JFET	2N2608		
2N5801	N JFET	2N4393		
2N5802	N JFET	2N4393		
2N5803	N JFET	2N4392		
2N5902	D N JFET	2N5902	3-41	5-29
2N5903	D N JFET	2N5903	3-41	5-29
2N5904	D N JFET	2N5904	3-41	5-29
2N5905	D N JFET	2N5905	3-41	5-29
2N5906	D N JFET	2N5906	3-41	5-29
2N5907	D N JFET	2N5907	3-41	5-29
2N5908	D N JFET	2N5908	3-41	5-29

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
2N5909	D N JFET	2N5909	3-41	5-29
2N5911	D N JFET	2N5911	3-43	5-34
2N5912	D N JFET	2N5912	3-43	5-34
2N5949	N JFET	K1837-18		
2N5950	N JFET	K1837-18		
2N5951	N JFET	K1837-18		
2N5952	N JFET	K305-18		
2N5953	N JFET	K305-18		
2N6451	N JFET	2N4393		
2N6452	N JFET	2N4393		
2N6453	N JFET	2N4393		
2N6454	N JFET	2N4393		
2N6483	D N JFET	U401		
2N6484	D N JFET	U402		
2N6585	D N JFET	U404		
2N6568	N JFET	U290		
2N6656	V MOS N ENH	2N6656		
2N6657	V MOS N ENH	2N6657		
2N6658	V MOS N ENH	2N6658		
2N6659	V MOS N ENH	2N6659		
2N6660	V MOS N ENH	2N6660		
2N6661	V MOS N ENH	2N6661		
3N145	P MOS ENH	3N163		
3N146	P MOS ENH	3N163		
3N155	P MOS ENH	3N163		
3N155A	P MOS ENH	3N163		
3N156	P MOS ENH	3N163		
3N156A	P MOS ENH	3N163		
3N157	P MOS ENH	3N163		
3N157A	P MOS ENH	3N163		
3N158	P MOS ENH	3N163		
3N158A	P MOS ENH	3N163		
3N163	P MOS ENH	3N163	3-44	5-1
3N164	P MOS ENH	3N164	3-44	5-1
3N174	P MOS ENH	3N163		
14T	N JFET	2N4224		
142T	N JFET	PN4392		
158T	N JFET	2N4302		
159T	N JFET	KK4416-18		
100S	N JFET	2N4304		
100U	N JFET	2N3684		
102M	N JFET	2N5486		
102S	N JFET	2N4302		
103M	N JFET	2N5457		
103S	N JFET	2N5459		
104M	N JFET	2N5458		
105M	N JFET	2N5459		
105U	N JFET	2N4222		
106M	N JFET	2N5485		
107M	N JFET	2N5486		
110U	N JFET	2N3685		
115U	N JFET	2N4340		
120U	N JFET	2N3686		
125U	N JFET	2N4339		
130U	N JFET	2N3687		
135U	N JFET	2N4339		
155U	N JFET	2N4416		
182S	N JFET	2N4391		
183S	N JFET	2N3823		
197S	N JFET	2N4338		
198S	N JFET	2N4340		
199S	N JFET	2N4341		
200S	N JFET	2N4392		
200U	N JFET	2N3824		
201S	N JFET	2N4391		
202S	N JFET	2N4392		
203S	N JFET	2N3821		
204S	N JFET	2N3821		
210U	N JFET	2N4416		
231S	D N JFET	2N3954		
232S	D N JFET	2N3955		
233S	D N JFET	2N3956		
234S	D N JFET	2N3957		
235S	D N JFET	2N3958		
241U	N JFET	2N4869		
250U	N JFET	2N4091		
251U	N JFET	2N4392		
703U	N JFET	2N4220		
704U	N JFET	2N4220		
705U	N JFET	2N4224		
707U	N JFET	2N4860		
714U	N JFET	2N3822		
734U	N JFET	2N4416		
734EU	N JFET	KK4416-18		
751U	N JFET	2N4340		
752U	N JFET	2N4340		
753U	N JFET	2N4341		
754U	N JFET	2N4340		
755U	N JFET	2N4341		
756U	N JFET	2N4340		
1277A	N JFET	2N3822		
1278A	N JFET	2N3821		
1279A	N JFET	2N3821		
1280A	N JFET	2N4224		
1281A	N JFET	2N3822		
1282A	N JFET	2N4341		
1283A	N JFET	2N4340		
1284A	N JFET	2N4222		
1285A	N JFET	2N3821		
1286A	N JFET	2N4220		
1325A	N JFET	2N4222		
1714A	N JFET	2N4340		
2000M	N JFET	2N3823		
2001M	N JFET	2N3823		
2078A	D N JFET	2N3955		
2079A	D N JFET	2N3955		
2080A	D N JFET	2N5546		
2081A	D N JFET	2N5546		
2093M	N JFET	2N3687		
2094M	N JFET	2N3686		

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
2095M	N JFET	2N3686		
2098A	D NJFET	2N5545		
2099A	D N JFET	2N5546		
2130U	D N JFET	2N5452		
2132U	D N JFET	2N3955		
2134U	D N JFET	2N3956		
2136U	D N JFET	2N3957		
2138U	D N JFET	2N3958		
2139U	D N JFET	2N3958		
2147U	D N JFET	2N3958		
2148U	D N JFET	2N3958		
2149U	D N JFET	2N3958		
A5T3821	N JFET	K305-18		
A5T3822	N JFET	K305-18		
A5T3823	N JFET	KK4416-18		
A5T3824	N JFET	J302-18		
A192	N JFET	2N4416		
AD830	D N JFET	U421		
AD831	D N JFET	U421		
AD832	D N JFET	U422		
AD833	D N JFET	U426		
AD833A	D N JFET	U423		
AD835	D N JFET	2N3921		
AD836	D N JFET	2N3921		
AD837	D N JFET	2N3922		
AD838	D N JFET	2N4085		
AD839	D N JFET	2N4085		
AD840	D N JFET	2N5196		
AD841	D N JFET	2N5197		
AD842	D N JFET	2N5199		
AD3954	D N JFET	2N3954		
AD3954A	D N JFET	2N3954A		
AD3955	D N JFET	2N3955		
AD3956	D N JFET	2N3956		
AD3957	D N JFET	2N3957		
AD3958	D N JFET	2N3958		
BC264	N JFET	2N4304		
BC264A	N JFET	2N4302		
BC264B	N JFET	2N4304		
BC264C	N JFET	2N4304		
BC264D	N JFET	KK4416-18		
BFR45	N JFET	2N4416		
BFS21	D N JFET	2N5199		
BFS21A	D N JFET	2N5199		
BFS67	N JFET	2N3821		
BFS67P	N JFET	2N4303		
BFS68	N JFET	2N3823		
BFS68P	N JFET	KK4416-18		
BFS70	N JFET	2N3821		
BFS71	N JFET	2N3822		
BFS72	N JFET	2N3823		
BFS73	N JFET	2N3821		
BFS74	N JFET	2N4856		
BFS75	N JFET	2N4857		
BFS76	N JFET	2N4858		
BFS77	N JFET	2N4859		
BFS78	N JFET	2N4860		
BFS79	N JFET	2N4861		
BFS80	N JFET	2N4416A		
BFW10	N JFET	2N3823		
BFW11	N JFET	2N3822		
BFW54	N JFET	2N3822		
BFW55	N JFET	2N3822		
BFW56	N JFET	2N4869		
BFW61	N JFET	2N4224		
BSV22	N JFET	2N4416		
BSV78	N JFET	2N4856A		
BSV80	N JFET	2N4858A		
C413N	N JFET	2N5434		
C673	N JFET	2N4341		
C674	N JFET	2N4341		
C680	N JFET	2N4338		
C680A	N JFET	2N4338		
C681	N JFET	2N4338		
C681A	N JFET	2N4338		
C682	N JFET	2N4339		
C682A	N JFET	2N4339		
C683	N JFET	2N4339		
C683A	N JFET	2N4339		
C684	N JFET	2N4220		
C684A	N JFET	2N4220		
C685	N JFET	2N4220		
C685A	N JFET	2N4220		
C6690	N JFET	2N3458		
C6691	N JFET	2N3458		
C6692	N JFET	2N3459		
CM600	N JFET	2N4092		
CM601	N JFET	2N4091		
CM602	N JFET	2N4091		
CM603	N JFET	2N4091		
CM640	N JFET	2N4093		
CM641	N JFET	2N4093		
CM642	N JFET	2N4093		
CM643	N JFET	2N4092		
CM644	N JFET	2N4092		
CM645	N JFET	2N4092		
CM646	N JFET	2N4092		
CM647	N JFET	2N4091		
CM650	N JFET	2N5432		
CM651	N JFET	2N5433		
CM652	N JFET	2N5432		
CM653	N JFET	2N5433		
CM697	N JFET	2N5434		
CM800	N JFET	2N5434		
CMX740	N JFET	U290		
CP640	N JFET	U296		
CP643	N JFET	2N5434		
CP650	N JFET	U322		
CP651	N JFET	U320		
CP652	N JFET	U322		
CP653	N JFET	U320		

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
CR022 Thru CR470 Referenced Under 1N Series				
DPAD1	D PAD N JFET	DPAD1	3-48	
DPAD2	D PAD N JFET	DPAD2	3-48	
DPAD5	D PAD N JFET	DPAD5	3-48	
DPAD10	D PAD N JFET	DPAD10	3-48	
DPAD20	D PAD N JFET	DPAD20	3-48	
DPAD50	D PAD N JFET	DPAD50	3-48	
DPAD100	D PAD N JFET	DPAD100	3-48	
DU4339	D N JFET	U235		
DU4340	D N JFET	U235		
E100	N JFET	J203-18		
E101	N JFET	J201-18		
E102	N JFET	J202-18		
E103	N JFET	J105-18		
E105	N JFET	J105-18		
E106	N JFET	J106-18		
E107	N JFET	J107-18		
E108	N JFET	J108-18		
E109	N JFET	J109-18		
E110	N JFET	J110-18		
E111	N JFET	J111-18		
E112	N JFET	J112-18		
E113	N JFET	J113-18		
E114	N JFET	K114-18		
E174	P JFET	J174-18		
E175	P JFET	J175-18		
E176	P JFET	J176-18		
E177	P JFET	J177-18		
E201	N JFET	J201-18		
E202	N JFET	J202-18		
E203	N JFET	J203-18		
E204	N JFET	J204-18		
E210	N JFET	K210-18		
E211	N JFET	K211-18		
E212	N JFET	K212-18		
E230	N JFET	J230-18		
E231	N JFET	J231-18		
E232	N JFET	J232-18		
E270	P JFET	J270-18		
E271	P JFET	J271-18		
E300	N JFET	K300-18		
E304	N JFET	K304-18		
E305	N JFET	K305-18		
E308	N JFET	K308-18		
E309	N JFET	K309-18		
E310	N JFET	K310-18		
E400	D N JFET	U410		
E401	D N JFET	U411		
E402	D N JFET	U410		
E410	D N JFET	U410		
E411	D N JFET	U411		
E412	D N JFET	U412		
E413	D N JFET	U410		
E414	D N JFET	U411		
E415	D N JFET	U412		
E420	D N JFET	U440		
E421	D N JFET	U441		
E430	D N JFET	U430		
E431	D N JFET	U431		
E500	CL N JFET	J500		
E501	CL N JFET	J501		
E502	CL N JFET	J502		
E503	CL N JFET	J503		
E504	CL N JFET	J504		
E505	CL N JFET	J505		
E506	CL N JFET	J506		
E507	CL N JFET	J507		
EPAD50	DD N JFET	JPAD50		
EPAD100	DD N JFET	JPAD100		
EPAD200	DD N JFET	JPAD200		
EPAD500	DD N JFET	JPAD500		
FE100	N JFET	2N3821		
FE100A	N JFET	2N3821		
FE102	N JFET	2N4119		
FE102A	N JFET	2N4119		
FE104	N JFET	2N4118		
FE104A	N JFET	2N4118		
FE200	N JFET	2N3821		
FE202	N JFET	2N3821		
FE204	N JFET	2N3821		
FE300	N JFET	2N3822		
FE302	N JFET	2N3821		
FE304	N JFET	2N3821		
FE0654A	N JFET	2N5486		
FE0654B	N JFET	2N5485		
FE3819	N JFET	2N3819		
FE5457	N JFET	2N5457		
FE5458	N JFET	2N5458		
FE5459	N JFET	2N5459		
FE5484	N JFET	2N5484		
FE5485	N JFET	2N5485		
FE5486	N JFET	2N5486		
FM3954	D N JFET	2N3954		
FM3954A	D N JFET	2N3954A		
FM3955	D N JFET	2N3955		
FM3955A	D N JFET	2N3955A		
FM3956	D N JFET	2N3956		
FM3957	D N JFET	2N3957		
FM3958	D N JFET	2N3958		
FT0654A	N JFET	2N5486		
FT0654B	N JFET	2N5486		
FT0654C	N JFET	2N4221		
FT0654D	N JFET	2N4221		
FT704	P MOS ENH	3N163		
GET5457	N JFET	2N5457		
GET5458	N JFET	2N5458		
GET5459	N JFET	2N5459		
HDIG1030	P MOS ENH	3N163		
ID100	D PAD N JFET	DPAD1		

1

Siliconix

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
ID101	D PAD N JFET	DPAD10		
IMF3954	D N JFET	2N3954		
IMF3954A	D N JFET	2N3954A		
IMF3955	D N JFET	2N3955		
IMF3955A	D N JFET	2N3955A		
IMF3956	D N JFET	2N3956		
IMF3957	D N JFET	2N3957		
IMF3958	D N JFET	2N3958		
IMF6485	D N JFET	U405		
IT100	P JFET	2N5116		
IT101	P JFET	2N5114		
IT108	N JFET	2N5486		
IT109	N JFET	U310		
IT1700	P MOS ENH	3N163		
IT1702	P MOSENH	3N163		
ITE500	CL N JFET	J500		
ITE501	CL N JFET	J501		
ITE502	CL N JFET	J502		
ITE503	CL N JFET	J503		
ITE504	CL N JFET	J504		
ITE505	CL N JFET	J505		
ITE506	CL N JFET	J506		
ITE507	CL N JFET	J507		
ITE3066	N JFET	J202-18		
ITE3067	N JFET	J201-18		
ITE3068	N JFET	J201-18		
ITE4117	N JFET	2N4117		
ITE4118	N JFET	2N4118		
ITE4119	N JFET	2N4119		
ITE4338	N JFET	J201-18		
ITE4339	N JFET	J201-18		
ITE4340	N JFET	J202-18		
ITE4341	N JFET	J203-18		
ITE4391	N JFET	PN4391-18		
ITE4392	N JFET	PN4392-18		
ITE4393	N JFET	PN4393-18		
ITE4416	N JFET	KK4416-18		
ITE4867	N JFET	J230-18		
ITE4868	N JFET	J231-18		
ITE4869	N JFET	J232-18		
J105	N JFET	J105	4-8	5-31
J105-18	N JFET	J105-18	4-8	5-31
J106	N JFET	J106	4-8	5-31
J106-18	N JFET	J106-18	4-8	5-31
J107	N JFET	J107	4-8	5-31
J107-18	N JFET	J107-18	4-8	5-31
J108	N JFET	J108	4-9	5-10
J108-18	N JFET	J108-18	4-9	5-10
J109	N JFET	J109	4-9	5-10
J109-18	N JFET	J109-18	4-9	5-10
J110	N JFET	J110	4-9	5-10
J110-18	N JFET	J110-18	4-9	5-10
J111	N JFET	J111	4-10	5-3
J111-18	N JFET	J111-18	4-10	5-3
J112	N JFET	J112	4-10	5-3
J112-18	N JFET	J112-18	4-10	5-3
J113	N JFET	J113	4-10	5-3
J113-18	N JFET	J113-18	4-10	5-3
J114	N JFET	J114	4-11	5-34
J174	P JFET	J174	4-12	5-39
J174-18	P JFET	J174-18	4-12	5-39
J175	P JFET	J175	4-12	5-39
J175-18	P JFET	J175-18	4-12	5-39
J176	P JFET	J176	4-12	5-39
J176-18	P JFET	J176-18	4-12	5-39
J177	P JFET	J177	4-12	5-39
J177-18	P JFET	J177-18	4-12	5-39
J201	N JFET		4-13	5-19
J201-18	N JFET		4-13	5-19
J202	N JFET		4-13	5-19
J202-18	N JFET		4-13	5-19
J203	N JFET		4-13	5-19
J203-18	N JFET		4-13	5-19
J204	N JFET	J204	4-14	5-19
J204-18	N JFET	J204-18	4-14	5-19
J210	N JFET	J210	4-15	5-34
J211	N JFET	J211	4-15	5-34
J212	N JFET	J212	4-15	5-34
J230	N JFET	J230	4-16	5-27
J230-18	N JFET	J230-18	4-16	5-27
J231	N JFET	J231	4-16	5-27
J231-18	N JFET	J231-18	4-16	5-27
J232	N JFET	J232	4-16	5-27
J232-18	N JFET	J232-18	4-16	5-27
J270	P JFET	J270	4-17	5-39
J270-18	P JFET	J270-18	4-17	5-39
J271	P JFET	J271	4-17	5-39
J271-18	P JFET	J271-18	4-17	5-39
J300	N JFET	J300	4-18	5-34
J304	N JFET	J304	4-19	5-8
J305	N JFET	J305	4-19	5-8
J308	N JFET	J308	4-20	5-32
J309	N JFET	J309	4-20	5-32
J310	N JFET	J310	4-20	5-32
J401	D N JFET	U401		
J402	D N JFET	U402		
J403	D N JFET	U403		
J404	D N JFET	U404		
J405	D N JFET	U405		
J406	D N JFET	U406		
J410	D N JFET	U410		
J411	D N JFET	U411		
J412	D N JFET	U412		
J500	CL N JFET	J500	4-21	5-5
J501	CL N JFET	J501	4-21	5-5
J502	CL N JFET	J502	4-21	5-5
J503	CL N JFET	J503	4-21	5-5
J504	CL N JFET	J504	4-21	5-5
J505	CL N JFET	J505	4-21	5-5
J506	CL N JFET	J506	4-22	5-5

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
J507	CL N JFET	J507	4-22	5-5
J508	CL N JFET	J508	4-22	5-5
J509	N JFET	J509	4-22	5-5
J510	N JFET	J510	4-22	5-5
J511	CL N JFET	J511	4-22	5-5
JPAD50	PAD N JFET	JPAD50	4-23	
JPAD100	PAD N JFET	JPAD100	4-23	
JPAD200	PAD NJFET	JPAD200	4-23	
JPAD500	PAD N JFET	JPAD500	4-23	
J1401	D N JFET	U401		
J1402	D N JFET	U402		
J1403	D N JFET	U403		
J1404	D N JFET	U404		
J1405	D N JFET	U405		
J1406	D N JFET	U406		
K114-18	N JFET	K114-18	4-24	5-34
K1837-18	N JFET	K1837-18	4-25	5-8
K210-18	N JFET	K210-18	4-26	5-34
K211-18	N JFET	K210-18	4-26	5-34
K212-18	N JFET	K210-18	4-26	5-34
K300-18	N JFET	K300-18	4-27	5-34
K304-18	N JFET	K304-18	4-28	5-8
K305-18	N JFET	K304-18	4-28	5-8
K308-18	N JFET	K308-18	4-29	5-32
K309-18	N JFET	K309-18	4-29	5-32
K310-18	N JFET	K310-8	4-29	5-32
KE3684	N JFET	2N3684		
KE3685	N JFET	2N3685		
KE3686	N JFET	2N3686		
KE3687	N JFET	2N3687		
KE3823	N JFET	J304-18		
KE3970	N JFET	PN4391-18		
KE3971	N JFET	PN4392-18		
KE3972	N JFET	PN4393-18		
KE4091	N JFET	PN4391-18		
KE4092	N JFET	PN4392-18		
KE4093	N JFET	PN4393-18		
KE4220	N JFET	2N5457		
KE4221	N JFET	2N5457		
KE4222	N JFET	2N5459		
KE4223	N JFET	J304-18		
KE4224	N JFET	J304-18		
KE4391	N JFET	PN4391-18		
KE4392	N JFET	PN4392-18		
KE4393	N JFET	PN4393-18		
KE4416	N JFET	KK4416-18		
KE4856	N JFET	PN4391-18		
KE4857	N JFET	PN4392-18		
KE4858	N JFET	PN4393-18		
KE4859	N JFET	PN4391-18		
KE4860	N JFET	PN4392-18		
KE4861	N JFET	PN4393-18		
KE5103	N JFET	K305-18		
KE5104	N JFET	K304-18		
KE5105	N JFET	K304-18		
KK4416-18	N JFET	KK4416-18	4-30	5-8
LDF603	N JFET	2N4221A		
LDF604	N JFET	2N4221A		
LDF605	N JFET	2N4221A		
M163	P MOS ENH	3N163		
M164	P MOS ENH	3N164		
MEM520	P MOS ENH	3N164		
MEM520C	P MOS ENH	3N164		
MEM561	P MOS ENH	3N163		
MEM561C	P MOS ENH	3N163		
MEM806	P MOS ENH	3N163		
MEM806A	P MOS ENH	3N163		
MFE823	P MOS ENH	MFE823	3-47	5-1
MFE2000	N JFET	2N4416		
MFE2001	N JFET	2N4416		
MFE2004	N JFET	2N4093		
MFE2005	N JFET	2N4092		
MFE2006	N JFET	2N4091		
MFE2007	N JFET	2N4860		
MFE2008	N JFET	2N4859		
MFE2009	N JFET	2N4859		
MFE2010	N JFET	2N5434		
MFE2011	N JFET	2N5433		
MFE2012	N JFET	2N5432		
MFE2093	N JFET	2N3687		
MFE2094	N JFET	2N3686		
MFE2095	N JFET	2N3685		
MFE4007	P JFET	2N2608		
MFE4008	P JFET	2N2608		
MFE4009	P JFET	2N3329		
MFE4010	P JFET	2N3330		
MFE4011	P JFET	2N3330		
MFE4012	P JFET	2N3331		
MK10	N JFET	2N4416		
MMF1	D N JFET	2N3921		
MMF2	D N JFET	2N3921		
MMF3	D N JFET	2N3921		
MMF4	D N JFET	2N3921		
MMF5	D N JFET	2N3921		
MMF6	D N JFET	2N3921		
MMT3823	N JFET	2N3823		
MPF102	N JFET	MPF102	4-31	5-8
MPF103	N JFET	2N5457		
MPF104	N JFET	2N5458		
MPF105	N JFET	2N5459		
MPF106	N JFET	2N5485		
MPF107	N JFET	2N5486		
MPF108	N JFET	MPF108	4-32	5-8
MPF109	N JFET	MPF109	4-33	5-25
MPF111	N JFET	MPF111	4-34	5-25
MPF112	N JFET	MPF112	4-35	5-8
MPF256	N JFET	J309		
MPF820	N JFET	U310		
MPF970	P JFET	J174		
MPF971	P JFET	J176		

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
MPF4391	N JFET	PN4391-18		
MPF4392	N JFET	PN4392-18		
MPF4393	N JFET	PN4393-18		
NF500	N JFET	2N4416		
NF501	N JFET	2N4416		
NF506	N JFET	2N4416		
NF510	N JFET	2N4393		
NF511	N JFET	2N4393		
NF520	N JFET	2N3684		
NF521	N JFET	2N3686		
NF522	N JFET	2N3684		
NF523	N JFET	2N3686		
NF530	N JFET	2N4341		
NF531	N JFET	2N4339		
NF532	N JFET	2N4341		
NF533	N JFET	2N4339		
NF580	N JFET	2N5432		
NF581	N JFET	2N5432		
NF582	N JFET	2N5433		
NF583	N JFET	2N5434		
NF584	N JFET	2N5433		
NF585	N JFET	2N4859		
NF4302	N JFET	2N4302		
NF4303	N JFET	2N4303		
NF4304	N JFET	2N4304		
NF4445	N JFET	2N5432		
NF4446	N JFET	2N5433		
NF4447	N JFET	2N5432		
NF4448	N JFET	2N5433		
NF5163	N JFET	2N5163		
NF5457	N JFET	2N5457		
NF5458	N JFET	2N5458		
NF5459	N JFET	2N5459		
NF5484	N JFET	2N5484		
NF5485	N JFET	2N5485		
NF5486	N JFET	2N5486		
NF5555	N JFET	2N5555		
NF5638	N JFET	2N5638		
NF5639	N JFET	2N5639		
NF5640	N JFET	2N5640		
NF5653	N JFET	2N5653		
NF5654	N JFET	2N5654		
PAD1	PAD N JFET	PAD1	3-49	
PAD2	PAD N JFET	PAD2	3-49	
PAD5	PAD N JFET	PAD5	3-49	
PAD10	PAD N JFET	PAD10	3-49	
PAD20	PAD N JFET	PAD20	3-49	
PAD50	PAD N JFET	PAD50	3-49	
PAD100	PAD N JFET	PAD100	3-49	
P1086	P JFET	P1086	4-36	5-39
P1086-18	P JFET	P1086-18	4-36	5-39
P1087	P JFET	P1087	4-36	5-39
P1087-18	P JFET	P1087-18	4-36	5-39
PN4091	N JFET	PN4091	4-37	5-3
PN4092	N JFET	PN4092	4-37	5-3
PN4093	N JFET	PN4093	4-37	5-3
PN4302	N JFET	PN4302	4-38	5-19
PN4302-18	N JFET	PN4302-18	4-38	5-19
PN4303	N JFET	PN4303	4-38	5-19
PN4303-18	N JFET	PN4303-18	4-38	5-19
PN4304	N JFET	PN4304	4-38	5-19
PN4304-18	N JFET	PN4304-18	4-38	5-19
PN4391	N JFET	PN4391	4-39	5-3
PN4391-18	N JFET	PN4391-18	4-39	5-3
PN4392	N JFET	PN4392	4-39	5-3
PN4392-18	N JFET	PN4392-18	4-39	5-3
PN4393	N JFET	PN4393	4-39	5-3
PN4393-18	N JFET	PN4393-18	4-39	5-3
PN4416	N JFET	PN4416	4-40	5-8
PN5163	N JFET	PN5163	4-41	
PF510	P JFET	2N5018		
PF511	P JFET	2N5014		
SU2078	D N JFET	U425		
SU2079	D N JFET	U425		
SU2098	D N JFET	2N5197		
SU2098A	D N JFET	2N5197		
SU2098B	D N JFET	2N5196		
SU2099	D N JFET	2N5197		
SU2099A	D N JFET	2N5197		
SU2365	D N JFET	U401		
SU2365A	D N JFET	U401		
SU2366	D N JFET	U402		
SU2366A	D N JFET	U402		
SU2367	D N JFET	U403		
SU2367A	D N JFET	U403		
SU2368	D N JFET	U404		
SU2368A	D N JFET	U404		
SU2369	D N JFET	U405		
SU2369A	D N JFET	U405		
SU2410	D N JFET	U424		
SU2411	D N JFET	U425		
SU2412	D N JFET	U426		
TD5902	D N JFET	2N5902		
TD5902	D N JFET	2N5902		
TD5902A	D N JFET	2N5902		
TD5903	D N JFET	2N5903		
TD5903A	D N JFET	2N5903		
TD5904	D N JFET	2N5904		
TD5904A	D N JFET	2N5904		
TD5905	D N JFET	2N5905		
TD5905A	D N JFET	2N5905		
TD5906	D N JFET	2N5906		
TD5906A	D N JFET	2N5906		
TD5907	D N JFET	2N5907		
TD5907A	D N JFET	2N5907		
TD5908	D N JFET	2N5908		
TD5908A	D N JFET	2N5908		
TD5909	D N JFET	2N5909		
TD5909A	D N JFET	2N5909		
TD5911	D N JFET	2N5911		

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
TD5911A	D N JFET	2N5911		
TD5912	D N JFET	2N5912		
TD5912A	D N JFET	2N5912		
TIS14	N JFET	2N4340		
TIS25	D N JFET	U401		
TIS26	D N JFET	U402		
TIS27	D N JFET	U404		
TIS41	N JFET	2N4859		
TIS58	N JFET	J305-18		
TIS59	D N JFET	U1837		
TIS73	N JFET	PN4391-18		
TIS74	N JFET	PN4392-18		
TIS75	N JFET	PN4393-18		
TIS88	N JFET	2N5486		
TIXS41	N JFET	2N4859		
TIXS42	N JFET	PN4393-18		
TN4117	N JFET	2N4117		
TN4117A	N JFET	2N4117A		
TN4118	N JFET	2N4118		
TN4118A	N JFET	2N4118A		
TN4119	N JFET	2N4119		
TN4119A	N JFET	2N4119A		
TN4338	N JFET	2N4338		
TN4339	N JFET	2N4339		
TN4340	N JFET	2N4340		
TN4341	N JFET	2N4341		
TP5114	P JFET	2N5114		
TP5115	P JFET	2N5115		
TP5116	P JFET	2N5116		
U110	P JFET	2N2608		
U112	P JFET	2N2608		
U133	P JFET	2N2608		
U146	P JFET	2N2608		
U147	P JFET	2N2608		
U148	P JFET	2N2608		
U149	P JFET	2N2609		
U168	P JFET	2N2609		
U182	N JFET	2N4857		
U183	N JFET	2N3824		
U197	N JFET	2N4339		
U198	N JFET	2N4340		
U199	N JFET	2N4341		
U200	N JFET	U200	3-50	5-3
U201	N JFET	U201	3-50	5-3
U202	N JFET	U202	3-50	5-3
U221	N JFET	2N4391		
U222	N JFET	2N4391		
U231	D N JFET	U231	3-51	5-15
U232	D N JFET	U232	3-51	5-15
U233	D N JFET	U233	3-51	5-15
U234	D N JFET	U234	3-51	5-15
U235	D N JFET	U235	3-51	5-15
U240	N JFET	2N5432		
U241	N JFET	2N5433		
U242	N JFET	2N5432		

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
U243	N JFET	2N5433		
U248	D N JFET	2N5902		
U248A	D N JFET	2N5906		
U249	D N JFET	2N5903		
U249A	D N JFET	2N5907		
U250	D N JFET	2N5904		
U250A	D N JFET	2N5908		
U251	D N JFET	2N5905		
U251A	D N JFET	2N5909		
U254	N JFET	2N4859		
U255	N JFET	2N4860		
U256	N JFET	2N4861		
U257	D N JFET	U257	3-52	5-34
U273	N JFET	2N4118A		
U273A	N JFET	2N4118A		
U274	N JFET	2N4119A		
U274A	N JFET	2N4119A		
U275	N JFET	2N4119A		
U275A	N JFET	2N4119A		
U280	D N JFET	U231		
U281	D N JFET	U231		
U282	D N JFET	U232		
U283	D N JFET	U232		
U284	D N JFET	U233		
U285	D N JFET	U234		
U290	N JFET	U290	3-53	5-31
U291	N JFET	U291	3-53	5-31
U295	N JFET	U295		
U296	N JFET	U296		
U300	P JFET	2N5114		
U301	P JFET	2N5115		
U304	P JFET	U304	3-54	5-39
U305	P JFET	U305	3-54	5-39
U306	P JFET	U306	3-54	5-39
U308	N JFET	U308	3-55	5-32
U309	N JFET	U309	3-55	5-32
U310	N JFET	U310	3-55	5-32
U311	N JFET	U311	3-57	5-32
U312	N JFET	U312	3-58	5-34
U320	N JFET	U320	3-59	5-10
U321	N JFET	U321	3-59	5-10
U322	N JFET	U322	3-59	5-10
U401	D N JFET	U401	3-61	5-17
U402	D N JFET	U402	3-61	5-17
U403	D N JFET	U403	3-61	5-17
U404	D N JFET	U404	3-61	5-17
U405	D N JFET	U405	3-61	5-17
U406	D N JFET	U406	3-61	5-17
U410	D N JFET	U410	3-63	5-21
U411	D N JFET	U411	3-63	5-21
U412	D N JFET	U412	3-63	5-21
U421	D N JFET	U421	3-64	5-23
U422	D N JFET	U422	3-64	5-23
U423	D N JFET	U423	3-64	5-23
U424	D N JFET	U424	3-64	5-23

FET Cross Reference *and* Index (cont'd.)

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
U425	D N JFET	U425	3-64	5-23
U426	D N JFET	U426	3-64	5-23
U430	D N JFET	U430	3-66	5-32
U431	D N JFET	U431	3-66	5-32
U440	D N JFET	U440	3-67	5-34
U441	D N JFET	U441	3-67	5-34
U508	N JFET	CR030		
U1177	N JFET	2N4220A		
U1178	N JFET	2N3821		
U1179	N JFET	2N3821		
U1180	N JFET	2N4221A		
U1181	N JFET	2N4220A		
U1182	N JFET	2N3821		
U1277	N JFET	2N3684		
U1278	N JFET	2N3685		
U1279	N JFET	2N3686		
U1280	N JFET	2N3684		
U1281	N JFET	2N3822		
U1282	N JFET	2N4341		
U1283	N JFET	2N4340		
U1284	N JFET	2N4341		
U1285	N JFET	2N4220		
U1288	N JFET	2N4341		
U1287	N JFET	2N4092		
U1321	N JFET	2N3966		
U1322	N JFET	2N4221A		
U1323	N JFET	2N4221A		
U1324	N JFET	2N4220A		
U1325	N JFET	2N4222		
U1420	N JFET	2N3821		
U1421	N JFET	2N3822		
U1422	N JFET	2N3822		
U1714	N JFET	2N4340		
U1837	N JFET	U1837	4-42	5-8
U1837E	N JFET	U1837		
U1897	N JFET	U1897	4-43	5-3
U1897-18	N JFET	U1897-18	4-43	5-3
U1897E	N JFET	U1897-18		
U1898	N JFET	U1898	4-43	5-3
U1898-18	N JFET	U1898-18	4-43	5-3
U1898E	N JFET	U1898-18		
U1899	N JFET	U1899	4-43	5-3
U1899-18	N JFET	U1899-18	4-43	5-3
U1899E	N JFT	U1899-18		
U1994	N JFET	U1994	4-44	5-8
U1994E	N JFET	U1994		
U2047E	N JFET	KK4416-18		
U3000	N JFET	2N4341		
U3001	N JFET	2N4339		
U3002	N JFET	2N4338		
U3010	N JFET	2N4341		
U3011	N JFET	2N4340		
U3012	N JFET	2N4338		
UC20	N JFET	2N3687		
UC40	P JFET	2N2608		
UC41	P JFET	2N2608		
UC100	N JFET	2N3684		
UC110	N JFET	2N3685		
UC115	N JFET	2N4340		
UC120	N JFET	2N3686		
UC130	N JFET	2N3687		
UC155	N JFET	2N4416		
UC200	N JFET	2N3824		
UC201	N JFET	2N3824		
UC210	N JFET	2N4416		
UC220	N JFET	2N3822		
UC240	N JFET	2N4869		
UC241	N JFET	2N4869		
UC250	N JFET	2N4091		
UC251	N JFET	2N4392		
UC300	P JFET	2N2608		
UC310	P JFET	2N2843		
UC320	P JFET	2N2843		
UC330	P JFET	2N2843		
UC340	P JFET	2N2843		
UC400	P JFET	2N3331		
UC401	P JFET	2N5116		
UC410	P JFET	2N3330		
UC420	P JFET	2N3329		
UC450	P JFET	2N5114		
UC451	P JFET	2N5116		
UC588	N JFET	2N4417		
UC703	N JFET	2N4220		
UC704	N JFET	2N4220		
UC705	N JFET	2N4224		
UC707	N JFET	2N4860		
UC714	N JFET	2N3822		
UC714E	N JFET	J203-18		
UC734	N JFET	2N4416		
UC734E	N JFET	KK4416-18		
UC751	N JFET	2N4340		
UC752	N JFET	2N4340		
UC753	N JFET	2N4341		
UC754	N JFET	2N4340		
UC755	N JFET	2N4341		
UC756	N JFET	2N4340		
UC805	P JFET	2N3331		
UC807	N JFET	2N4860		
UC814	P JFET	2N3331		
UC851	P JFET	2N2608		
UC853	P JFET	2N2608		
UC854	P JFET	2N2608		
UC855	P JFET	2N2609		
UC1700	P MOS ENH	3N163		
UC1764	P MOS ENH	3N163		
UC2130	D N JFET	2N5452		
UC2132	D N JFET	2N3955		
UC2134	D N JFET	2N3956		
UC2136	D N JFET	2N3957		
UC2138	D N JFET	2N3958		

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Date Sheet Page	Geometry Page
UC2139	D N JFET	2N3958		
UC2147	D N JFET	2N3958		
UC2148	D N JFET	2N3958		
UC2149	D N JFET	2N3958		
VCR2N	N JFET	VCR2N	3-68	5-3
VCR3P	P JFET	VCR3P	3-68	5-38
VCR4N	N JFET	VCR4N	3-68	5-19
VCR5P	P JFET	VCR5P	3-68	5-36
VCR6P	P JFET	2N5116		
VCR7N	N JFET	VCR7N	3-68	5-29
VMP1	VMOS N ENH	2N6657		
VMP2	VMOS N ENH	2N6660		
VMP4	VMOS N ENH	VMP4		
VMP11	VMOS N ENH	2N6656		
VMP12	VMOS N ENH	2N6658		
VMP21	VMOS N ENH	2N6659		
VMP22	VMOS N ENH	2N6661		
VN30AA	VMOS N ENH	VN30AA		
VN30AB	VMOS N ENH	VN30AB		
VN33AJ	VMOS N ENH	VN33AJ		
VN33AK	VMOS N ENH	VN33AK		
VN35AA	VMOS N ENH	VN35AA		
VN35AB	VMOS N ENH	VN35AB		
VN35AJ	VMOS N ENH	VN35AJ		
VN35AK	VMOS N ENH	VN35AK		
VN40AF	VMOS N ENH	VN40AF		
VN46AF	VMOS N ENH	VN46AF		
VN64GA	VMOS N ENH	VN64GA		
VN66AF	VMOS N ENH	VN64GF		
VN66AJ	VMOS N ENH	VN66AJ		
VN66AK	VMOS N ENH	VN66AK		
VN67AA	VMOS N ENH	VN67AA		
VN67AB	VMOS N ENH	VN67AB		
VN67AF	VMOS N ENH	VN67AF		
VN67AJ	VMOS N ENH	VN67AJ		
VN67AK	VMOS N ENH	VN67AK		
VN88AF	VMOS N ENH	VN88AF		
VN89AA	VMOS N ENH	VN89AA		
VN89AB	VMOS N ENH	VN89AB		
VN89AF	VMOS N ENH	VN89AF		
VN90AA	VMOS N ENH	VN90AA		
VN90AB	VMOS N ENH	VN90AB		
VN98AJ	VMOS N ENH	VN98AJ		
VN98AK	VMOS N ENH	VN98AK		
VN99AJ	VMOS N ENH	VN99AJ		
VN99AK	VMOS N ENH	VN99AK		
WK5457	N JFET	2N5457		
WK5458	N JFET	2N5458		
WK5459	N JFET	2N5459		

product information

Siliconix

Siliconix products are divided into three basic categories:

Standard Products, Modified Standard Products, Custom Products

- **Standard Products** — All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.
- **Examples of Modified Standard Products are:**

Electrical Specials — Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.

Mechanical Specials — Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.

High Reliability Specials — Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. These options include MIL-750B. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.

In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

- **Custom Products** — Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

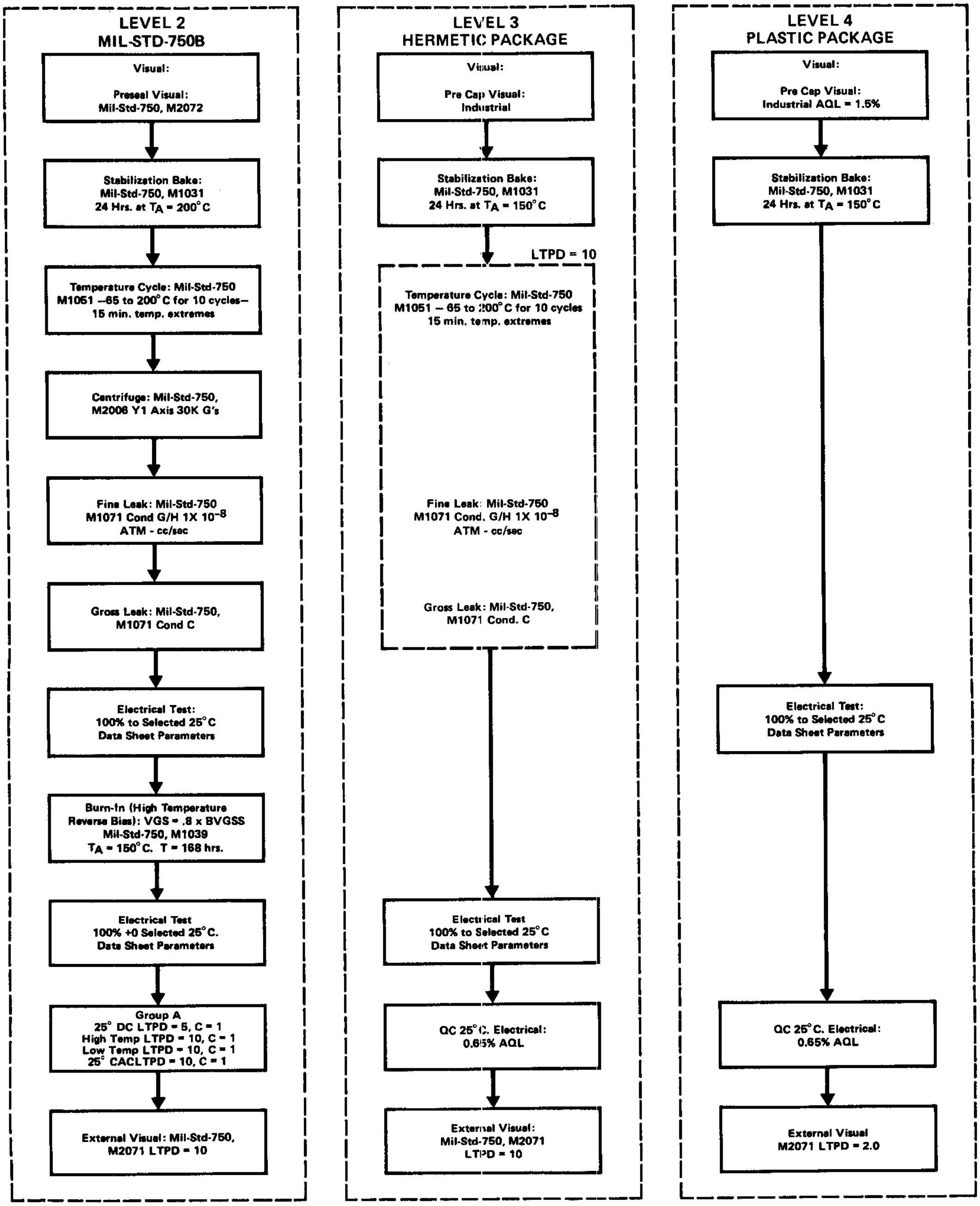
FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054,
Telephone: (408) 988-8000.

FETs/Part Number Prefixes and Suffixes

Prefix	XXX	XXXX
CR	Si Standard N-Channel Current Regulator	
DPAD	Si Standard Dual JFET Diode	
FN	Special N-Channel JFET	Special N-Channel JFET
J	Si Standard TO-92 Cased FET	Special TO-92 Cased FET
JPAD	Si Standard TO-92 Cased JFET Diode	
K	Si Standard TO-92 Cased FET	
KK	Si Standard TO-92 Cased FET	
M	Si Standard MOSFET	
MEM	Si Standard MOSFET	
MU	Special MOSFET	
PAD	Si Standard JFET Diode	
PF	Special P-Channel JFET	
PN		Si Standard TO-92 Cased FET
SU	Special P-Channel JFET	
U	Si Standard FET	Si Standard FET
VCR	Si Standard N- and P-Channel Voltage Controlled Resistors	
VMP	VMOS Power FET N-Channel	
VN		VMOS Power FET N-Channel
2N		JEDEC-Registered Device
3N	JEDEC-Registered Device	
Suffix		
-18	Std TO-92 Package with Center Lead Formed Toward Flat in TO-18 Pin Circle	

The above prefix list does not include some second source products supplied by Siliconix. Refer to FET Cross Reference and Index or current price list for availability of these devices.

process option flow chart



tips on selecting the right FET for your application

The "Product Specification," a short form version of technical data, will provide you direct reference to Siliconix part numbers and a condensed version of technical specifications

IF YOU ARE NOT FAMILIAR WITH THE FET PARAMETERS YOU NEED:

1. Turn to page 2-2 "How to Choose the Correct FET for Your Application." Using this guide, determine the important FET parameters.
2. Next, turn to page 2-4 "JFET Geometry Selector Guide." Using this guide, choose the appropriate geometry.
3. Once you have chosen a geometry, turn to the "Geometry Characteristics" section 5 of the catalog. Here you make the choice of a suitable part number.
4. Now that you have the part number, you will find complete electrical specifications of these products in the "Data Sheets" sections 3 and 4 of the catalog.

IF YOU ARE FAMILIAR WITH THE PARAMETERS YOU NEED:

1. Turn to the "Product Specifications" pages 2-6 through 2-16 to determine the proper part number(s).
2. Double-check your choices against the data sheets, and select the part most suited for your application.

how to choose the correct FET for your application

Siliconix

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters	
AMPLIFIER	Audio	Low noise ($\overline{e}_n$), g_{fs}/g_{os}	Voltage amplification factor μ $= g_{fs}/g_{os}$ $= \Delta V_{DS}/\Delta V_{GS}$ @ I_D = const	$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$ Switching Times	
	Buffer	Low I_G, high g_{fs}			
	Differential	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	High Input Impedance	Very low I_G (eg., MOSFET)			
	High Frequency	High g_{fs}/C_{iss} ratio, NF, RF parameters			
	FET Input Op Amp	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G			
	Low Distortion	High $V_{GS(off)}$ compared to signal amplitude			
	Low Supply Voltage	Low $V_{GS(off)}$			
	Low Noise	Low $\overline{e}_n$, $\overline{i}_n$, low 1/f noise, low NF			
	Preamplifier	Operate near I_{DZO}, high g_{fs}/I_D ratio			
	Video	High g_{fs}/C_{iss} ratio, NF			Noise, $\overline{e}_n$, NF while using high level signals
CONSTANT CURRENT SOURCE	Current Limiting	Low g_{oss}, low $V_{GS(off)}$, high BV_{GSS}		g_{fs}, $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters capacitance	RF parameters while operating below RF frequencies
	Reference Current Source				
	Biasing				
MIXERS	VHF	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss}		$R_{DS(on)}$ $V_{DS(on)}$ $I_{D(off)}$	Capacitance & switching times while operating in audio and lower frequencies
	UHF				
	Double Balanced	Matching characteristics			
OSCILLATORS	Class A	Good g_{fs} at operating frequency			
	Class C	Low C_{iss} for VHF operation			
SWITCHES	Analog Gates	Fast switching time	$R_{DS(on)}$ vs Capacitance	g_{fs} g_{os}	
	Choppers	$r_{DS}/I_{D(off)}$ switching efficiency			
	Commutators	Low C_{rss}			
	Digital	Fast switching time			
	Integrator Reset	Very low $R_{DS(on)}$, High I_{DSS}			
	Sample and Hold	Low C_{rss}			
VOLTAGE CONTROLLED RESISTORS	Gain Control	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs}, BV_{GSS}, I_{DSS}	
	Amplitude Stability				
	Attenuators				

JFET geometry selector guide

Once you have chosen the major FET parameters, you will find selecting the optimum JFET geometry is easy. If you are familiar with Field Effect Transistors, start your selection using the characteristic graphs on page 2-4. You will find the $V_{GS(off)}$ vs I_{DSS} graph the most meaningful, since it shows — in order of ascending active area — the complete line of Siliconix junction FETs.

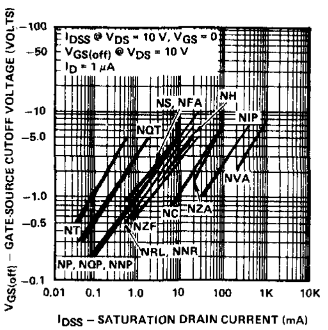
To give you an idea how this guide works, let's find the most suitable geometry for a 70 ohm ON-resistance analog switch which will be required to operate as close as 5 volts from the negative power supply. The power supply restraint requires a maximum $V_{GS(off)}$ of 5 volts. Examining the $R_{DS(on)}$ vs $V_{GS(off)}$ figure, you will find the NC, NIP, and NVA geometries meet the R_{on} and $V_{GS(off)}$ requirements. In order to minimize your cost, choose the geometry having the least chip area, that is the NC. You will find characteristic data and part numbers in the Geometry Characteristics section of the catalog. Below are the most important parameter inter-relationships expressed in analytical form.

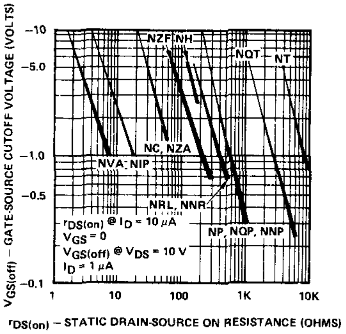
USEFUL JFET PARAMETER RELATIONSHIPS (APPROX.)

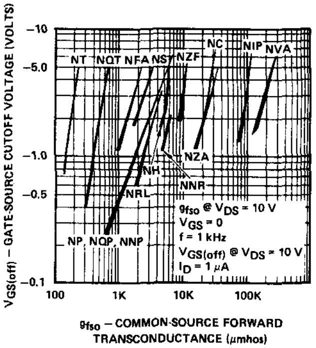
g_{fso}	$=$	$K \dfrac{I_{DSS}}{V_{GS(off)}}$	Forward transconductance as a function of I_{DSS} and $V_{GS(off)}$ at zero gate-source voltage ($K = 1.5$ to 2.5; typically $= 2$ for N-channel junction FET)
g_{fs}	$=$	$g_{fso} \left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)$	Variation of g_{fs} with gate bias
g_{fs}	$=$	$g_{fso} \sqrt{I_D / I_{DSS}}$	Variation of g_{fs} with drain current
$V_{GS(off)}$	$=$	$\dfrac{2\ I_{DSS}}{g_{fso}}$	Gate-Source cutoff voltage in terms of I_{DSS} and g_{fso}
V_{DS}	$\approx$	$V_{GS(off)} \left(\dfrac{I_D}{I_{DSS}}\right)^{1/2}$	Drain voltage at which drain current saturates
r_{DS}	$\simeq$	$\dfrac{1}{g_{fs}}$	Reciprocal relationship between drain-source resistance and forward transconductance. Accurate when $V_{DS} < V_{GS(off)}$ i.e. in the triode region
r_{DS}	$\simeq$	$\dfrac{[V_{GS(off)}]^2}{K I_{DSS}\ [V_{GS(off)} - V_{GS}]}$	$K = 1.5$ to 2.5 Variation of drain resistance in the triode region
I_D	$=$	$I_{DSS} \left(1 - \dfrac{V_{GS}}{V_{GS(off)}}\right)^2$	Variation of drain current with gate-source voltage. The square law transfer characteristic.

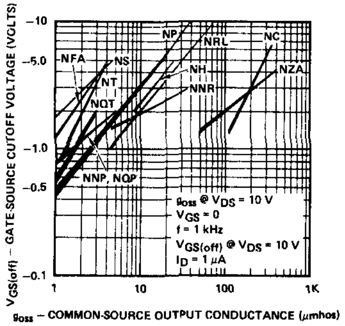
JFET geometry selector guide (cont'd)

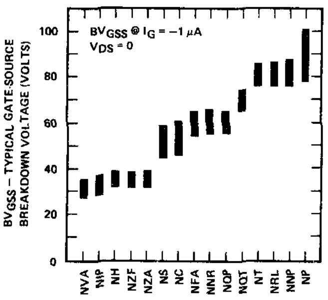
n-channel JFETs

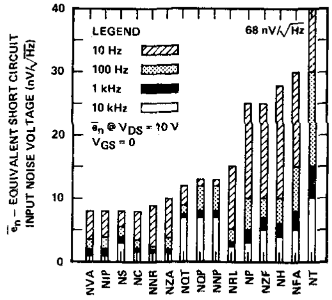


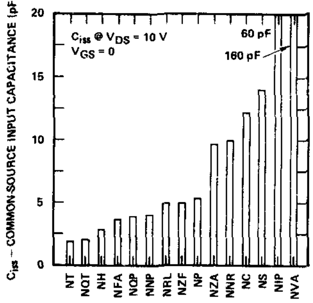


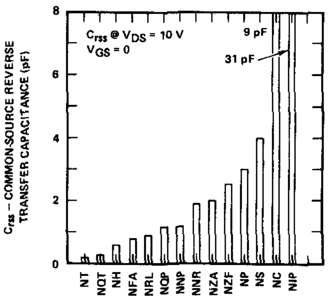






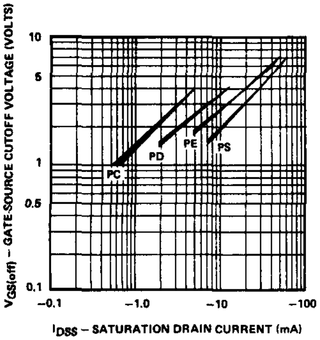


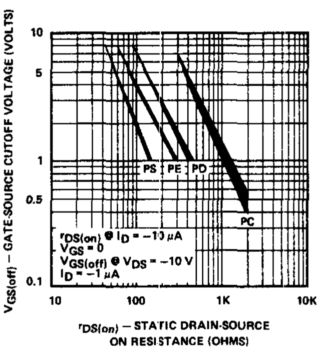


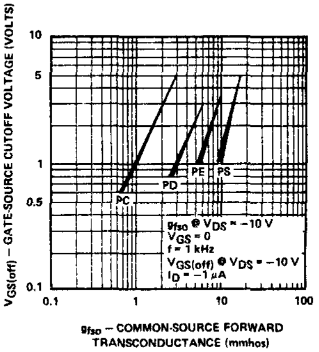


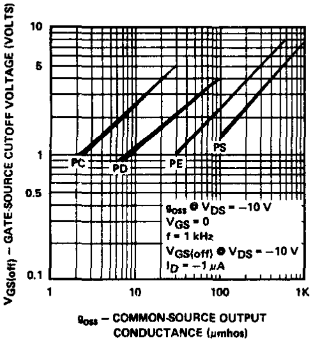
JFET geometry selector guide (cont'd)

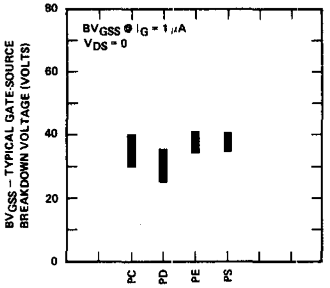
p-channel JFET

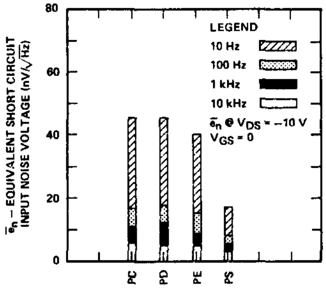


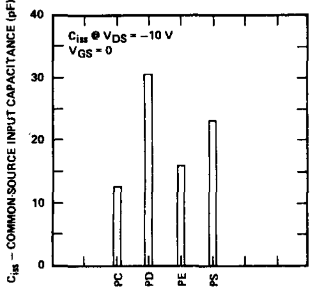


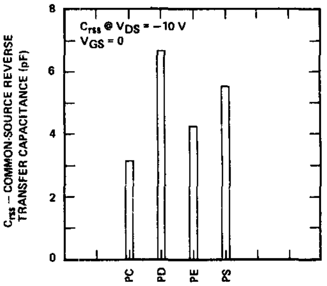












N & P-Channel Single JFETs

DEVICE	GEOMETRY (Section 5)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P	PART NUMBER
LOW LEAKAGE	NT	—	—	—	3	210	70	0.09	0.03	40	1.8	—	0.01	72	N	2N4117
	NT	—	—	—	3	210	70	0.09	0.03	40	1.8	—	0.001	72	N	2N4117A
	NT	—	—	—	3	250	80	0.24	0.08	40	3.0	—	0.01	72	N	2N4118
	NT	—	—	—	3	250	90	0.24	0.08	40	3.0	—	0.001	72	N	2N4118A
	NT	—	—	—	3	330	100	0.6	0.2	40	6.0	—	0.01	72	N	2N4119
	NT	—	—	—	3	330	100	0.6	0.2	40	6.0	—	0.001	72	N	2N4119A
LOW NOISE	NP	—	1M	4	18	6000	1500	4.0	0.8	50	3.4	—	0.25	18	N	2N3459
	NP	—	1M	4	18	4500	800	1.0	0.2	50	1.8	—	0.25	18	N	2N3460
	NRL	—	1M	2.5	6	4000	1000	3.0	0.5	30	4.0	—	0.1	72	N	2N4220A
	NRL	—	1M	2.5	6	5000	2000	6.0	2.0	30	6.0	—	0.1	72	N	2N4221A
	NRL	—	1M	2.5	6	6000	2500	15	5.0	30	8.0	—	0.1	72	N	2N4222A
	NP	—	1M	1.0	7	1800	600	0.6	0.2	50	1.0	—	0.1	18	N	2N4338
	NP	—	1M	1.0	7	2400	800	1.5	0.5	50	1.8	—	0.1	18	N	2N4339
	NP	—	1M	1.0	7	3000	1300	3.6	1.2	50	3.0	—	0.1	18	N	2N4340
	NP	—	1M	1.0	7	4000	2000	9.0	3.0	50	6.0	—	0.1	18	N	2N4341
	NS	—	—	20	25	2000	700	1.2	0.4	40	2.0	—	0.25	72	N	2N4867
	NS	—	—	10	25	2000	700	1.2	0.4	40	2.0	—	0.25	72	N	2N4867A
	NS	—	—	20	25	3000	1000	3.0	1.0	40	3.0	—	0.25	72	N	2N4868
	NS	—	—	10	25	3000	1000	3.0	1.0	40	3.0	—	0.25	72	N	2N4868A
	NS	—	—	20	25	4000	1300	7.5	2.5	40	5.0	—	0.25	72	N	2N4869
	NS	—	—	10	25	4000	1300	7.5	2.5	40	5.0	—	0.25	72	N	2N4869A
	NRL	—	—	35	6	6500	1500	2.5	0.5	30	4.0	—	0.1	72	N	2N5556
	NRL	—	—	35	6	6500	1500	5.0	2.0	30	5.0	—	0.1	72	N	2N5557
	NRL	—	—	35	6	6500	1500	10	4.0	30	6.0	—	0.1	72	N	2N5558
	NS	—	—	30	—	2500	1000	3.0	0.7	40	3.0	—	0.25	92	N	J230
	NS	—	—	30	—	2500	1000	3.0	0.7	40	3.0	—	0.25	92	N	J230-18
	NS	—	—	30	—	3000	1500	6.0	2.0	40	5.0	—	0.25	92	N	J231
	NS	—	—	30	—	3000	1500	6.0	2.0	40	5.0	—	0.25	92	N	J231-18
	NS	—	—	30	—	4000	2500	10	5.0	40	6.0	—	0.25	92	N	J232
	NS	—	—	30	—	4000	2500	10	5.0	40	6.0	—	0.25	92	N	J232-18
	PS	—	—	—	—	15000	6000	15	2.0	30	2.0	—	0.2	92	P	J270-18
RF AMP	NRL	—	—	—	8.0	6500	2000	20	2.0	25	8.0	—	2.0	92	N	2N3819
	NRL	—	1K	2.5	6	6500	3500	20	4.0	30	8.0	—	0.5	72	N	2N3823
	NRL	—	1K	5.0	6	7000	3000	18	3.0	30	8.0	—	0.25	72	N	2N4223
	NRL	—	—	—	6	7500	2000	20	2.0	30	8.0	—	0.5	72	N	2N4224
	NH	—	1K	2.0	4	7500	4500	15	5.0	30	6.0	—	0.1	72	N	2N4416
	NH	—	1K	2.0	4	7500	4500	15	5.0	35	6.0	—	0.1	72	N	2N4416A
	—	—	1K	3.0	6	10000	4500	25	4.0	30	8.0	—	0.25	72	N	2N5078

N & P-Channel Single JFETs

RF AMPLIFIERS

PART NUMBER	GEOMETRY (Section 5)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
2N5484	NH	—	1K	3.0	5	6000	3000	5.0	1.0	25	3.0	—	1.0	92	N
2N5485	NH	—	1K	2.0	5	7000	3500	10	4.0	25	4.0	—	1.0	92	N
2N5486	NH	—	1K	2.0	5	8000	4000	20	8.0	25	6.0	—	1.0	92	N
2N5668	NH	—	1K	2.5	7	6500	1500	5.0	1.0	25	4.0	—	2.0	92	N
2N5669	NH	—	1K	2.5	7	6500	2000	10	4.0	25	6.0	—	2.0	92	N
2N5670	NH	—	1K	2.5	7.0	7500	3000	20	8.0	25	8.0	—	2.0	92	N
J210	NZF	—	—	—	—	12000	4000	15	2.0	25	3.0	—	0.1	92	N
J211	NZF	—	—	—	—	12000	7000	20	7.0	25	4.5	—	0.1	92	N
J212	NZF	—	—	—	—	12000	7000	40	15	25	6.0	—	0.1	92	N
J270	PS	—	—	—	—	15000	6000	15	2.0	30	2.0	—	0.2	92	P
J271	PS	—	—	—	—	18000	8000	50	6.0	30	4.5	—	0.2	92	P
J300	NZF	—	—	—	5.5	9000	4500	30	6.0	25	6.0	—	0.5	92	N
J304	NH	—	—	—	—	7500	4500	15	5.0	30	6.0	—	0.1	92	N
J305	NH	—	—	—	—	—	3000	8.0	1.0	30	3.0	—	0.1	92	N
J308	NZA	—	—	—	7.5	20000	8000	60	12	25	6.5	—	1.0	92	N
J309	NZA	—	—	—	7.5	20000	10000	30	12	25	4.0	—	1.0	92	N
J310	NZA	—	—	—	7.5	18000	8000	60	24	25	6.5	—	1.0	92	N
K210-18	NZF	—	—	—	—	12000	4000	15	2.0	25	3.0	—	0.1	92	N
K211-18	NZF	—	—	—	—	12000	7000	20	7.0	25	4.5	—	0.1	92	N
K212-18	NZF	—	—	—	—	12000	7000	40	15	25	6.0	—	0.1	92	N
K300-18	NZF	—	—	—	5.5	9000	4500	30	6.0	25	6.0	—	0.5	92	N
K304-18	NH	—	—	—	—	7500	4500	15	5.0	30	6.0	—	0.1	92	N
K305-18	NH	—	—	—	—	—	3000	8.0	1.0	30	3.0	—	0.1	92	N
K308-18	NZA	—	—	—	7.5	20000	8000	60	12	25	6.5	—	1.0	92	N
K309-18	NZA	—	—	—	7.5	20000	10000	30	12	25	4.0	—	1.0	92	N
K310-18	NZA	—	—	—	7.5	18000	8000	60	24	25	6.5	—	1.0	92	N
K1837-18	NH	—	1K	3.0	6.0	10000	4500	25	4.0	30	8.0	—	0.25	92	N
KK4416-18	NH	—	1K	2.0	4.0	7500	4500	15	5.0	30	6.0	—	1.0	92	N
PN4416	NH	—	1K	2.0	4.0	7500	4500	15	5.0	30	6.0	—	1.0	92	N
MPF102	NH	—	—	—	7.0	7500	2000	20	2.0	25	7.5	—	2.0	92	N
MPF108	NH	—	1M	2.5	6.5	7500	2000	24	1.5	25	8.0	—	1.0	92	N
MPF112	NH	—	—	—	—	7500	1000	25	1.0	25	10	—	100	92	N
U308	NZA	—	—	—	7.5	20000	10000	60	12	25	6.0	—	0.15	52	N
U309	NZA	—	—	—	7.5	20000	10000	30	12	25	4.0	—	0.15	52	N
U310	NZA	—	—	—	7.5	18000	10000	60	24	25	6.0	—	0.15	52	N
U311	NZA	—	—	—	7.5	20000	10000	60	20	25	6.0	—	0.15	72	N
U312	NZF	—	—	—	5.0	10000	6000	30	10	25	6.0	—	0.1	52	N
U320	NIP	—	—	—	30	200000	75000	500	100	25	10	—	3.0	39	N
U321	NIP	—	—	—	30	200000	75000	250	80	25	4.0	—	3.0	39	N

2

Product Specifications (cont'd)

N & P-Channel Single JFETs

PART NUMBER	DEVICE	GEOMETRY (Section 5)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	*LEAKAGE (nA, MAX.) Chnl	*LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
U322	RF AMP	NIP	–	–	–	30	200000	75000	700	200	25	10	–	3.0	39	N
U1837		NH	–	1K	3.0	6.0	10000	4500	25	4.0	30	8.0	–	0.25	92	N
U1837-18		NH	–	1K	3.0	6.0	10000	4500	25	4.0	30	8.0	–	0.25	92	N
U1994		NH	–	–	–	4.0	7500	4500	15	5.0	30	6.0	–	0.1	92	N
2N3824	SWITCHES & CHOPPERS	NRL	250	–	–	6.0	–	–	–	–	50	8.0	0.1	0.1	72	N
2N3966		NH	220	–	–	6.0	–	–	–	2.0	30	6.0	1.0	0.1	72	N
2N3970		NC	30	–	–	25	–	–	150	50	40	10	0.25	0.25	18	N
2N3971		NC	60	–	–	25	–	–	75	25	40	5.0	0.25	0.25	18	N
2N3972		NC	100	–	–	25	–	–	30	5.0	40	3.0	0.25	0.25	18	N
2N4091		NC	30	–	–	16	–	–	–	30	40	10	0.2	0.2	18	N
2N4092		NC	50	–	–	16	–	–	–	15	40	7.0	0.2	0.2	18	N
2N4093		NC	80	–	–	16	–	–	–	8.0	40	5.0	0.2	0.2	18	N
2N4391		NC	30	–	–	14	–	–	150	50	40	10	0.1	0.1	18	N
2N4392		NC	60	–	–	14	–	–	75	25	40	5.0	0.1	0.1	18	N
2N4393		NC	100	–	–	14	–	–	30	5.0	40	3.0	0.1	0.1	18	N
2N4856		NC	25	–	–	18	–	–	–	50	40	10	0.25	0.25	18	N
2N4856A		NC	25	–	–	10	–	–	–	50	40	10	0.25	0.25	18	N
2N4857		NC	40	–	–	18	–	–	100	20	40	6.0	0.25	0.25	18	N
2N4857A		NC	40	–	–	10	–	–	100	20	40	6.0	0.25	0.25	18	N
2N4858		NC	60	–	–	18	–	–	80	8.0	40	4.0	0.25	0.25	18	N
2N4858A		NC	60	–	–	10	–	–	80	8.0	40	4.0	0.25	0.25	18	N
2N4859		NC	25	–	–	18	–	–	–	50	30	10	0.25	0.25	18	N
2N4859A		NC	25	–	–	10	–	–	–	50	30	10	0.25	0.25	18	N
2N4860		NC	40	–	–	18	–	–	100	20	30	6.0	0.25	0.25	18	N
2N4860A		NC	40	–	–	10	–	–	100	20	30	6.0	0.25	0.25	18	N
2N4861		NC	60	–	–	18	–	–	80	8.0	30	4.0	0.25	0.25	18	N
2N4861A		NC	60	–	–	10	–	–	80	8.0	30	4.0	0.25	0.25	18	N
2N5018		PS	75	–	–	45	–	–	–	10	30	10	10.0	2.0	18	P
2N5019		PS	150	–	–	45	–	–	–	5.0	30	5.0	10.0	2.0	18	P
2N5114		PS	75	–	–	25	–	–	90	30	30	10	0.5	0.5	18	P
2N5115		PS	100	–	–	25	–	–	60	15	30	6.0	0.5	0.5	18	P
2N5116		PS	150	–	–	25	–	–	25	5.0	30	4.0	0.5	0.5	18	P
2N5432		NIP	5.0	–	–	30	–	–	–	150	25	10	0.2	0.2	52	N
2N5433		NIP	7.0	–	–	30	–	–	–	100	25	9.0	0.2	0.2	52	N
2N5434		NIP	10	–	–	30	–	–	–	30	25	4.0	0.2	0.2	52	N
2N5555		NH	150	–	–	5.0	–	–	–	15	25	10	10.0	1.0	92	N
2N5638		NC	30	–	–	10	–	–	–	50	30	12	1.0	1.0	92	N
2N5639		NC	60	–	–	10	–	–	–	25	30	8.0	1.0	1.0	92	N

Product Specifications (cont'd)

Siliconix

N & P-Channel Single JFETs

2

DEVICE: SWITCHES & CHOPPERS

PART NUMBER	GEOMETRY (Section 5)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
2N5640	NC	100	—	—	10	—	—	—	5.0	30	6.0	1.0	1.0	92	N
2N5653	NC	50	—	—	10	—	—	—	40	30	12	1.0	1.0	92	N
2N5654	NC	100	—	—	10	—	—	—	15	30	8.0	1.0	1.0	92	N
J105	NVA	3.0	—	—	—	—	—	—	500	25	10.0	3.0	3.0	92	N
J105-18	NVA	3.0	—	—	—	—	—	—	500	25	10	3.0	3.0	92	N
J106	NVA	6.0	—	—	—	—	—	—	200	25	6.0	3.0	3.0	92	N
J106-18	NVA	6.0	—	—	—	—	—	—	200	25	6.0	3.0	3.0	92	N
J107	NVA	8.0	—	—	—	—	—	—	100	25	4.5	3.0	3.0	92	N
J107-18	NVA	8.0	—	—	—	—	—	—	100	25	4.5	3.0	3.0	92	N
J108	NIP	8.0	—	—	—	—	—	—	80	25	10	3.0	3.0	92	N
J108-18	NIP	8.0	—	—	—	—	—	—	80	25	10	3.0	3.0	92	N
J109	NIP	12	—	—	—	—	—	—	40	25	6.0	3.0	3.0	92	N
J109-18	NIP	12	—	—	—	—	—	—	40	25	6.0	3.0	3.0	92	N
J110	NIP	18	—	—	—	—	—	—	10	25	4.0	3.0	3.0	92	N
J110-18	NIP	18	—	—	—	—	—	—	10	25	4.0	3.0	3.0	92	N
J111	NC	30	—	—	—	—	—	—	20	35	10	1.0	1.0	92	N
J111-18	NC	30	—	—	—	—	—	—	20	35	10	1.0	1.0	92	N
J112	NC	50	—	—	—	—	—	—	5.0	35	5.0	1.0	1.0	92	N
J112-18	NC	50	—	—	—	—	—	—	5.0	35	5.0	1.0	1.0	92	N
J113	NC	100	—	—	—	—	—	—	2.0	35	3.0	1.0	1.0	92	N
J113-18	NC	100	—	—	—	—	—	—	2.0	35	3.0	1.0	1.0	92	N
J114	NIF	150	—	—	—	—	—	—	15	25	10	1.0	1.0	92	N
J174	PS	85	—	—	—	—	—	100	20	30	10	1.0	1.0	92	P
J174-18	PS	85	—	—	—	—	—	100	20	30	10	1.0	1.0	92	P
J175	PS	125	—	—	—	—	—	60	7.0	30	6.0	1.0	1.0	92	P
J175-18	PS	125	—	—	—	—	—	60	7.0	30	6.0	1.0	1.0	92	P
J176	PS	250	—	—	—	—	—	25	2.0	30	4.0	1.0	1.0	92	P
J176-18	PS	250	—	—	—	—	—	25	2.0	30	4.0	1.0	1.0	92	P
J177	PS	300	—	—	—	—	—	20	1.5	30	2.25	1.0	1.0	92	P
J177-18	PS	300	—	—	—	—	—	20	1.5	30	2.25	1.0	1.0	92	P
K114-18	NZF	150	—	—	—	—	—	—	15	25	10	1.0	1.0	92	N
PN4391	NC	30	—	—	14	—	—	150	50	40	10	1.0	1.0	92	N
PN4391-18	NC	30	—	—	14	—	—	150	50	40	10	1.0	1.0	92	N
PN4392	NC	60	—	—	14	—	—	75	25	40	5.0	1.0	1.0	92	N
PN4392-18	NC	60	—	—	14	—	—	75	25	40	5.0	1.0	1.0	92	N
PN4393	NC	100	—	—	14	—	—	30	5.0	40	3.0	1.0	1.0	92	N
PN4393-18	NC	100	—	—	14	—	—	30	5.0	40	3.0	1.0	1.0	92	N
P1086	PS	75	—	—	45	—	—	—	10	30	10	10.0	2.0	92	P
P1086-18	PS	75	—	—	45	—	—	—	10	30	10	10.0	2.0	92	P

Siliconix

N & P-Channel Single JFETs

PART NUMBER	DEVICE	GEOMETRY (Section 5)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate	PACKAGE (TO-)	N or P
P1087	SWITCHES & CHOPPERS	PS	150	—	—	45	—	—	—	5.0	30	5.0	10.0	2.0	92	P
P1087-18		PS	150	—	—	45	—	—	—	5.0	30	5.0	10.0	2.0	92	P
U200		NC	150	—	—	30	—	—	25	3.0	30	3.0	1.0	1.0	18	N
U201		NC	75	—	—	30	—	—	75	15	30	5.0	1.0	1.0	18	N
U202		NC	50	—	—	30	—	—	150	30	30	10	1.0	1.0	18	N
U290		NVA	2.5	—	—	60	—	—	—	500	30	10	1.0	1.0	52	N
U291		NVA	7.0	—	—	60	—	—	—	200	30	4.5	1.0	1.0	52	N
U304		PS	85	—	—	27	—	—	90	30	30	10	0.5	0.5	18	P
U305		PS	110	—	—	27	—	—	60	15	30	6.0	0.5	0.5	18	P
U306		PS	175	—	—	27	—	—	25	5.0	30	4.0	0.5	0.5	18	P
U1897		NC	30	—	—	16	—	—	—	30	40	10	0.2	0.4	92	N
U1897-18		NC	30	—	—	16	—	—	—	30	40	10	0.2	0.4	92	N
U1898		NC	50	—	—	16	—	—	—	15	40	7.0	0.2	0.4	92	N
U1898-18		NC	50	—	—	16	—	—	—	15	40	7.0	0.2	0.4	92	N
U1899		NC	80	—	—	16	—	—	—	8.0	40	5.0	0.2	0.4	92	N
U1899-18		NC	80	—	—	16	—	—	—	8.0	40	5.0	0.2	0.4	92	N
2N2608	GENERAL PURPOSE	PC	—	1M	3	17	—	1000	4.5	0.9	30	4.0	—	10	18	P
2N2609		PD	—	1M	3	30	—	2500	10.0	2.0	30	4.0	—	30	18	P
2N2843		PC	—	1M	3	17	—	540	1.0	0.2	30	1.7	—	10	18	P
2N2844		PD	—	1M	3	30	—	1400	2.2	0.44	30	1.7	—	30	18	P
2N3329		PC	—	1M	3	20	2000	1000	3.0	1.0	20	5.0	—	10	72	P
2N3330		PC	—	1M	3	20	3000	1500	6.0	2.0	20	6.0	—	10	72	P
2N3331		PC	—	1M	4	20	4000	2000	15	5.0	20	8.0	—	10	72	P
2N3332		PC	—	1M	1	20	2200	1000	6.0	1.0	20	6.0	—	10	72	P
2N3368		NP	—	—	—	20	4000	1000	12	2.0	40	11.5	—	5.0	18	N
2N3369		NP	—	—	—	20	2500	600	2.5	0.5	40	6.5	—	5.0	18	N
2N3370		NP	—	—	—	20	2500	300	0.6	0.1	40	3.2	—	5.0	18	N
2N3382		PE	—	—	—	—	12500	4500	30	3.0	30	5.0	—	15	72	P
2N3384		PE	—	—	—	—	12500	7500	30	15.0	30	5.0	—	15	72	P
2N3386		PE	—	—	—	—	15000	7500	50	15.0	30	9.5	—	15	72	P
2N3436		NP	—	1M	2	18	10000	2500	15	3.0	50	9.8	—	0.5	18	N
2N3437		NP	—	1M	2	18	6000	1500	4.0	0.8	50	4.8	—	0.5	18	N
2N3438		NP	—	1M	2	18	4500	800	1.0	0.2	50	2.3	—	0.5	18	N
2N3458		NP	—	1M	6	18	10000	2500	15	3.0	50	7.8	—	0.25	18	N
2N3684		NFA	—	10M	0.5	4	3000	2000	7.5	2.5	50	5.0	—	0.1	72	N
2N3685		NFA	—	10M	0.5	4	2500	1500	3.0	1.0	50	3.5	—	0.1	72	N
2N3686		NFA	—	10M	0.5	4	2000	1000	1.2	0.4	50	2.0	—	0.1	72	N
2N3687		NFA	—	10M	0.5	4	1500	500	0.5	0.1	50	1.2	—	0.1	72	N

N & P-Channel Single JFETs

DEVICE: GENERAL PURPOSE

PART NUMBER	N or P	PACKAGE (TO-)	GEOMETRY (Section 5)	RESISTANCE Chnl Ω, Max.	RESISTANCE Gate Ω	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	INPUT CAPACITANCE (pF, MAX.)	TRANS-CONDUCTANCE gfs (μmhos) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	BREAKDOWN VOLTAGE (V, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	LEAKAGE (nA, MAX.) Chnl	LEAKAGE (nA, MAX.) Gate
2N3821	N	72	NRL	-	-	200	6	4500	1500	2.5	0.5	50	4.0	-	0.1
2N3822	N	72	NRL	-	-	200	6	6500	3000	10	2.0	50	6.0	-	0.1
2N3909	P	72	PC	-	-	-	32	5000	1000	15	0.3	20	8.0	-	10
2N4220	N	72	NRL	-	-	-	6	4000	1000	3.0	0.5	30	4.0	-	0.1
2N4221	N	72	NRL	-	-	-	6	5000	2000	6.0	2.0	30	6.0	-	0.1
2N4222	N	72	NRL	-	-	-	6	6000	2500	15	5.0	30	8.0	-	0.1
2N5457	N	92	NRL	-	1M	3.0	7	5000	1000	5.0	1.0	25	6.0	-	1.0
2N5458	N	92	NRL	-	1M	3.0	7	5500	1500	9.0	2.0	25	7.0	-	1.0
2N5459	N	92	NRL	-	100M	3.0	7	6000	2000	16	4.0	25	8.0	-	1.0
J201	N	92	NP	-	-	-	5.0	-	500	1.0	0.2	40	1.5	-	0.1
J201-18	N	92	NP	-	-	-	5.0	-	500	1.00	0.2	40	1.5	-	0.1
J202	N	92	NP	-	-	-	5.0	-	1000	4.5	0.9	40	4.0	-	0.1
J202-18	N	92	NP	-	-	-	5.0	-	1000	4.5	0.9	40	4.0	-	0.1
J203	N	92	NP	-	-	-	5.0	-	1500	20	4.0	40	10	-	0.1
J203-18	N	92	NP	-	-	-	5.0	-	1500	20	4.0	40	10	-	0.1
J204	N	92	NP	-	-	-	5.0	-	-	-	-	25	2.0	-	0.1
J204-18	N	92	NP	-	-	-	5.0	-	-	-	-	25	2.0	-	0.1
J271-18	P	92	PS	-	-	-	-	18000	8000	50	6.0	30	4.5	-	0.2
PN4302	N	92	NP	-	1M	2.0	6	-	1000	5.0	0.5	30	4.0	-	1.0
PN4302-18	N	92	NP	-	1M	2.0	6.0	-	1000	5.0	0.5	30	4.0	-	1.0
PN4303	N	92	NP	-	1M	2.0	6	-	2000	10	4.0	30	6.0	-	1.0
PN4303-18	N	92	NP	-	1M	2.0	6.0	-	2000	10	4.0	30	6.0	-	1.0
PN4304	N	92	NP	-	1M	3.0	6	-	1000	15	0.5	30	10.0	-	1.0
PN4304-18	N	92	NP	-	1M	2.0	6.0	-	1000	15	0.5	30	10	-	1.0
PN5163	N	92	-	-	-	50.0	20	9000	2000	40.0	1.0	25	8.0	-	10
MPF109	N	92	NRL	-	1M	2.5	7.0	6000	800	24	0.5	25	8.0	-	1.0
MPF111	N	92	NRL	-	-	-	-	-	500	20	0.5	20	10	-	100

Product Specifications (cont'd)

Siliconix

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (μmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD		OUTPUT CONDUCTANCE gos (μmhos, MAX.)	GEOMETRY (Section 5)	DEVICE
			Gate			Min.	Max.	Min.	Max.			Static Match (mV, Max.)	Temp Tracking μV/°C			
2N5196	N	71	0.025	4.0	50	0.7	7.0	1000	–	6.0	20	5.0	5.0	50	NNP or NP-D	LOW LEAKAGE
2N5197	N	71	0.025	4.0	50	0.7	7.0	1000	–	6.0	20	5.0	10	50	NNP or NP-D	
2N5198	N	71	0.025	4.0	50	0.7	7.0	1000	–	6.0	20	10	20	50	NNP or NP-D	
2N5199	N	71	0.025	4.0	50	0.7	7.0	1000	–	6.0	20	15	40	50	NNP or NP-D	
2N5545	N	71	0.1	4.5	50	0.5	8.0	1500	–	6.0	200	5.0	10	25	NNP or NP-D	
2N5546	N	71	0.1	4.5	50	0.5	8.0	1500	–	6.0	200	10	20	25	NNP or NP-D	
2N5547	N	71	0.1	4.5	50	0.5	8.0	1500	–	6.0	200	15	40	25	NNP or NP-D	
2N5902	N	78	0.005	4.5	40	0.03	0.5	70	–	3.0	0.2	5.0	5.0	1.0	NT	
2N5903	N	78	0.005	4.5	40	0.03	0.5	70	–	3.0	0.2	5.0	10	1.0	NT	
2N5904	N	78	0.005	4.5	40	0.03	0.5	70	–	3.0	0.2	10	20	1.0	NT	
2N5905	N	78	0.005	4.5	40	0.03	0.5	70	–	3.0	0.2	15	40	1.0	NT	
2N5906	N	78	0.002	4.5	40	0.03	0.5	70	–	3.0	0.1	5.0	5.0	1.0	NT	
2N5907	N	78	0.002	4.5	40	0.03	0.5	70	–	3.0	0.1	5.0	10	1.0	NT	
2N5908	N	78	0.002	4.5	40	0.03	0.5	70	–	3.0	0.1	10	20	1.0	NT	
2N5909	N	78	0.002	4.5	40	0.03	0.5	70	–	3.0	0.1	15	20	1.0	NT	
U401	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	5.0	10	2.0	NNR	
U402	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	10	10	2.0	NNR	
U403	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	10	25	2.0	NNR	
U404	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	15	25	2.0	NNR	
U405	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	20	40	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	40	80	2.0	NNR	
U421	N	78	0.0002	2.0	40	0.06	1.0	300	–	3.0	10	10	10	0.5	NQT	
U422	N	78	0.0002	2.0	40	0.06	1.0	300	–	3.0	10	15	25	0.5	NQT	
U423	N	78	0.0002	2.0	40	0.06	1.0	300	–	3.0	10	25	40	0.5	NQT	
U424	N	78	0.001	3.0	40	0.06	1.8	300	–	3.0	10	10	10	1.0	NQT	
U425	N	78	0.001	3.0	40	0.06	1.8	300	–	3.0	10	15	25	1.0	NQT	
U426	N	78	0.001	3.0	40	0.06	1.8	300	–	3.0	10	25	40	1.0	NQT	
2N5515	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	30	5.0	5.0	1.0	NS	LOW NOISE
2N5516	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	30	5.0	10	1.0	NS	
2N5517	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	30	10	20	1.0	NS	
2N5518	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	30	15	40	1.0	NS	
2N5519	N	71	0.25	4.0	40	0.5	7.5	1000		25	30	15	80	1.0	NS	
2N5520	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	15	5.0	5.0	1.0	NS	
2N5521	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	15	5.0	10	1.0	NS	
2N5522	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	15	10	20	1.0	NS	
2N5523	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	15	15	40	1.0	NS	
2N5524	N	71	0.25	4.0	40	0.5	7.5	1000	–	25	15	15	80	1.0	NS	
U401	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	5.0	10	2.0	NNR	
U402	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	10	10	2.0	NNR	
U403	N	71	0.025	2.5	50	0.5	10	2000	–	8.0	20	10	25	2.0	NNR	

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (μmhos) Min.	TRANS-CONDUCTANCE gfs (μmhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD Static Match (mV, Max.)	THRESHOLD Temp Tracking μV/°C	OUTPUT CONDUCTANCE gos (μmhos, MAX.)	GEOMETRY (Section 5)	DEVICE
U404	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	15	25	2.0	NNR	LOW NOISE
U405	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	20	40	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000	—	8.0	20	40	80	2.0	NNR	
2N5564	N	71	0.1	3.0	40	5.0	30	7500	—	12	50	5.0	10	45	NC	RF AMPLIFIER
2N5565	N	71	0.1	3.0	40	5.0	30	7500	—	12	50	10	25	45	NC	
2N5566	N	71	0.1	3.0	40	5.0	30	7500	—	12	50	20	50	45	NC	
2N5911	N	78	0.1	5.0	25	7.0	40	5000	—	3.0	20	10	20	100	NZF	
2N5912	N	78	0.1	5.0	25	7.0	40	5000	—	3.0	20	15	40	100	NZF	
U257	N	78	0.1	5.0	25	5.0	40	5000	—	5.0	30	100	—	150	NZF	
U430	N	99	0.15	4.0	25	12	30	10000	—	7.5	12	—	—	150	NZA	
U431	N	99	0.15	6.0	25	24	60	10000	—	7.5	10	—	—	150	NZA	
U440	N	71	0.50	6.0	25	6.0	30	4500	—	—	—	10	—	200	NZF	
U441	N	71	0.50	6.0	25	6.0	30	4500	—	—	—	20	—	200	NZF	
2N3921	N	71	1.0	3.0	50	1.0	10	1500	—	18	2.0	5.0	10	35	NNR or NRL-D	GENERAL PURPOSE
2N3922	N	71	1.0	3.0	50	1.0	10	1500	—	18	2.0	5.0	25	35	NNR or NRL-D	
2N3954	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	5.0	10	35	NFA	
2N3954A	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	5.0	5.0	35	NFA	
2N3955	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	10	25	35	NFA	
2N3955A	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	10	15	35	NFA	
2N3956	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	15	50	35	NFA	
2N3957	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	20	75	35	NFA	
2N3958	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	0.5	25	100	35	NFA	
2N4084	N	71	1.0	3.0	50	1.0	10	1500	—	18	2	15	10	35	NNR or NRL-D	
2N4085	N	71	1.0	3.0	50	1.0	10	1500	—	18	2	15	25	35	NNR or NRL-D	
2N5045	N	71	0.25	4.5	50	0.5	8.0	1500	—	8.0	200	5.0	67	25	NNR or NRL-D	
2N5046	N	71	0.25	4.5	50	0.5	8.0	1500	—	8.0	200	10	133	25	NNR or NRL-D	
2N5047	N	71	0.25	4.5	50	0.5	8.0	1500	—	8.0	200	15	200	25	NNR or NRL-D	
2N5452	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	20	5.0	5.0	1.0	NFA	
2N5453	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	20	10	10	1.0	NFA	
2N5454	N	71	0.1	4.5	50	0.5	5.0	1000	—	4.0	20	15	25	1.0	NFA	
U231	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	5.0	10	35	NNP or NP-D	
U232	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	10	25	35	NNP or NP-D	
U233	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	15	50	35	NNP or NP-D	
U234	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	20	75	35	NNP or NP-D	
U235	N	71	0.1	4.5	50	0.5	5.0	1000	—	6.0	80	25	100	35	NNP or NP-D	
U410	N	71	0.2	3.5	40	0.5	6.0	1000	—	—	13	10	10	20	NQP	
U411	N	71	0.2	3.5	40	0.5	6.0	1000	—	—	13	20	25	20	NQP	
U412	N	71	0.2	3.5	40	0.5	6.0	1000	—	—	13	40	80	20	NQP	

Low Leakage Diodes

Part Number	Package (TO-)	Diode	Reverse Current (pA, Max.)	Breakdown Voltage (Volts)		Forward Voltage Drop (pF, Max.)	Capacitance
				Min.	Max.		
DPAD1	72	Dual	1	45	120	1.5	0.8
DPAD2	72	Dual	2	45	120	1.5	0.8
DPAD5	72	Dual	5	45	120	1.5	0.8
DPAD10	72	Dual	10	35	–	1.5	2.0
DPAD20	72	Dual	20	35	–	1.5	2.0
DPAD50	72	Dual	50	35	–	1.5	2.0
DPAD100	72	Dual	100	35	–	1.5	2.0
JPAD50	TO-92/TO-106	Single	20	35	–	1.5	2.0
JPAD100	TO-92/TO-106	Single	50	35	–	1.5	2.0
JPAD200	TO-92/TO-106	Single	100	35	–	1.5	2.0
JPAD500	TO-92/TO-106	Single	500	35	–	1.5	2.0
PAD1	18	Single	1	45	120	1.5	0.8
PAD2	18	Single	2	45	120	1.5	0.8
PAD5	18	Single	5	45	120	1.5	0.8
PAD10	18	Single	10	35	–	1.5	2.0
PAD20	18	Single	20	35	–	1.5	2.0
PAD50	18	Single	50	35	–	1.5	2.0
PAD100	18	Single	100	35	–	1.5	2.0

Voltage Controlled Resistors

Part Number	N or P	Package (TO-)	Breakdown Voltage (Volts, Min.)	Threshold Voltage (Volts)		Resistance (Channel Ω)		Geometry
				Min.	Max.	Min.	Max.	
VCR2N	N	18	15	3.5	7.0	20	60	NC
VCR3P	P	72	15	3.5	7.0	70	200	PE
VCR4N	N	18	15	3.5	7.0	200	600	NP
VCR5P	P	72	15	3.5	7.0	300	900	PC
VCR7N	N	72	15	2.5	5.0	4000	8000	NT

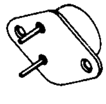
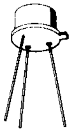
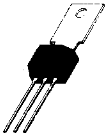
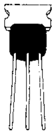
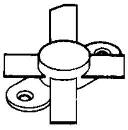
P-Channel MOSFETS

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω, Max.)	Leakage Channel On (mA)		Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
					Min.	Max.					
3N163	72	ENH	5.0	250	5.0	30	–	40	2.5	0.7	MRA
3N164	72	ENH	5.0	300	3.0	30	–	30	2.5	0.7	MRA
MFE823	18	ENH	6.0	–	3.0	–	20	25	6.0	1.5	MRA

Current Regulator Diodes

Part Number	Package (TO-)	Forward Current (mA)	Forward Current Tolerance (%)	Limiting Voltage (Volts, Max.)	Peak Operating Voltage (Volts, Max.)	Dynamic Impedance (MΩ, Max.)	Forward Capacitance (pF, typ)	Geometry
CR022	18	0.22	10	1.00	100	13	–	NKL
CR024	18	0.24	10	1.00	100	10	–	NKL
CR027	18	0.27	10	1.00	100	9.0	–	NKL
CR030	18	0.30	10	1.00	100	8.0	–	NKL
CR033	18	0.33	10	1.00	100	6.6	–	NKL
CR039	18	0.39	10	1.05	100	4.1	–	NKL
CR043	18	0.43	10	1.05	100	3.3	–	NKL
CR047	18	0.47	10	1.10	100	2.7	–	NKL
CR056	18	0.56	10	1.20	100	1.9	–	NKL
CR062	18	0.62	10	1.30	100	1.55	–	NKL
CR068	18	0.68	10	1.15	100	1.35	–	NKM
CR075	18	0.75	10	1.20	100	1.15	–	NKM
CR082	18	0.82	10	1.25	100	1.00	–	NKM
CR091	18	0.91	10	1.29	100	0.88	–	NKM
CR100	18	1.00	10	1.35	100	0.80	–	NKM
CR110	18	1.10	10	1.40	100	0.70	–	NKM
CR120	18	1.20	10	1.45	100	0.64	–	NKM
CR130	18	1.30	10	1.50	100	0.58	–	NKM
CR140	18	1.40	10	1.55	100	0.54	–	NKM
CR150	18	1.50	10	1.60	100	0.51	–	NKM
CR160	18	1.60	10	1.65	100	0.475	–	NKO
CR180	18	1.80	10	1.75	100	0.42	–	NKO
CR200	18	2.00	10	1.85	100	0.395	–	NKO
CR220	18	2.20	10	1.95	100	0.37	–	NKO
CR240	18	2.40	10	2.00	100	0.345	–	NKO
CR270	18	2.70	10	2.15	100	0.32	–	NKO
CR300	18	3.00	10	2.25	100	0.30	–	NKO
CR330	18	3.30	10	2.35	100	0.28	–	NKO
CR360	18	3.60	10	2.50	100	0.265	–	NKO
CR390	18	3.90	10	2.60	100	0.255	–	NKO
CR430	18	4.30	10	2.75	100	0.245	–	NKO
CR470	18	4.70	10	2.90	100	0.235	–	NKO
J500	92	0.24	20	1.20	50	5.0	2	NCL
J501	92	0.33	20	1.30	50	3.0	2	NCL
J502	92	0.43	20	1.50	50	2.0	2	NCL
J503	92	0.56	20	1.70	50	1.4	2	NCL
J504	92	0.75	20	1.90	50	1.0	2	NCL
J505	92	1.00	20	2.10	50	0.6	2	NCL
J506	92	1.40	20	2.50	50	0.4	2	NCL
J507	92	1.80	20	2.80	50	0.25	2	NCL
J508	92	2.40	20	3.10	50	0.25	2	NCL
J509	92	3.00	20	3.50	50	0.20	2	NCL
J510	92	3.60	20	3.90	50	0.20	2	NCL
J511	92	4.70	20	4.20	50	0.15	2	NCL

VMOS Power FETs

RDS(on)	BREAKDOWN VOLTAGE										PACKAGE
	35 V		40 V		60 V		80 V		90 V		
	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	
0.4						VN64GA					 TO-3
1.8	2N6656	VN33AJ									
2.5	VN35AA	VN35AJ									
3.0					2N6657	VN66AJ					
3.5					VN67AA	VN67AJ					
4.0									2N6658	VN98AJ	
4.5							VN89AA			VN99AJ	
5.0	VN30AA								VN90AA		
1.8	2N6659	VN33AK									 TO-39
2.5	VN35AB	VN35AK									
3.0					2N6660	VN66AK					
3.5					VN67AB	VN67AK					
4.0									2N6661	VN98AK	
4.5							VN89AB			VN99AK	
5.0	VN30AB								VN90AB		
3.0			VN46AF		VN66AF						 TO-202AA
3.5					VN67AF						
4.0							VN88AF				
4.5							VN89AF				
5.0			VN40AF								
5.0					VN10KM						 TO-237
3.0						VMP4					 380-SOE

Detailed Technical Specifications for the VMOS Power FETs listed above *are not* included in this data book. *Please* contact your nearest Siliconix Sales Office for a VMOS Design Catalog.

Die Process Information

Siliconix is a large volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

Physical Data

- Physical layout and dimensions are presented in the die topography section.
- Each die is passivated with approximately 8,000 angstroms of non-crystalline glass.
- All die are gold backed. Gold backing is approximately 1,500 angstroms thick.
- Die metallization is deposited aluminum approximately 12,000 angstroms thick.

Die Screening Criteria

Electrical Probe – Die are 100% probed in wafer form at 25°C to DC criteria.

Visual Criteria – Die are supplied with 100% visual sort to the criteria of MIL-Std-750 method 2072.

Packaging

Die are supplied in dust proof, anti-static waffle packs. (see illustration)

Assembly

- Chips supplied in waffle packs normally do not require cleaning. Wafers should be cleaned after sawing or scribing, and fracturing.
- Chips should be handled with a vacuum pick-up with protected tip or with tweezers gripping the chip on its sides.
- When handling MOSFET chips, particularly non-gate protected types, steps must be taken to prevent damage by static discharge. In some extreme cases, handling precautions may be necessary for junction FET chips.
- Chips can be die attached either eutectically or by conductive epoxy when lower temperatures are necessary. Gold silicon eutectic occurs at temperatures between 385°C and 425°C.
- Bonding of wires from chip pads to posts can be achieved by thermocompression gold wire or ultrasonic aluminum wire bonded.

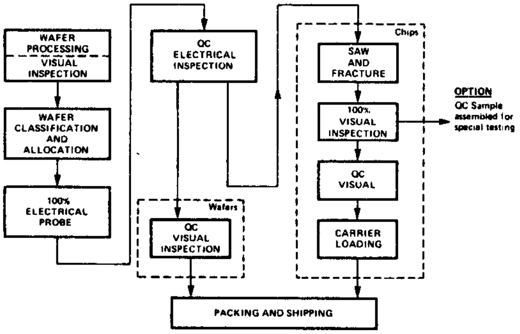
Options

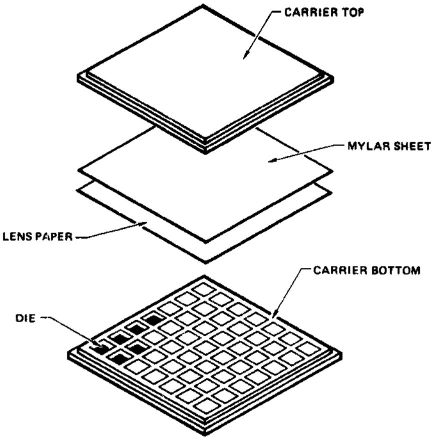
- **SEM** – Scanning electron microscope examination and control in accordance with MIL-Std-883 Method 2018 can be ordered on chips and wafers.
- **Wafer qualification to unprobed parameters** – sample testing of purchased chips to demonstrate capability to perform at data sheet temperature extremes by use of LTPD techniques can be provided.
- **Hot probe** – Siliconix has a chip processor/distributor with hot probe capability available.

Chip Packaging

Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.

Chip and Wafer Processing





NOTE: CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 1

pc board layout and construction for low leakage applications

In order to realize the full capability of these devices in circuits that are sensitive to very low currents, considerable care should be exercised in PC board layout and construction techniques. If proper care is not taken, board leakage currents can easily become much larger than the leakage currents of the devices themselves, especially under conditions of high temperature and humidity. Excessive leakage currents can be produced by poor quality boards, socket leakage, poor board layout, imperfectly cleaned boards, or improperly applied or cured protective coatings.

It is important to start with quality PC boards which have high resistivity and low susceptance to moisture. Boards of teflon or polycarbonate composition exhibit these attributes and are preferred. Glass-epoxy boards are less desirable because they will absorb moisture, and if used must be protected with a conformal coating.

The use of sockets should be avoided wherever possible since the pin-to-pin isolation is often not great enough to prevent small leakage currents from occurring. These currents can significantly degrade device performance in low leakage applications. If sockets cannot be avoided use the highest quality available, preferably teflon.

In laying out PC boards, care should be taken to keep pins and runs which are sensitive to very low currents away from pins and runs which will be at significantly higher or lower voltages. The most common leakage current problems occur between pins sensitive to low current levels and nearby pins at or near one of the supply voltages. Thus, if the isolation between critical pins and nearby high or low voltage pins is increased, leakage is minimized.

In order to reduce leakage currents, it is very important that all PC boards and experimental breadboards be thoroughly cleaned with a solvent after construction. A recommended procedure is to wash each board in an ultrasonic cleaning bath of alcohol, trichloroethylene, or some other commercial solvent, and to blow dry with compressed air. The purpose of this is to remove all skin oils (the greatest cause of leakage in improperly cleaned boards), solder fluxes, and other films and residues left over from the construction process which can cause gross leakage problems and erratic device behavior, especially at temperatures above 85°C.

For best results, the thoroughly cleaned boards should be protected against dirt, conductive films, and humidity by the application of a conformal coating. Urethane and Dow Corning's R-4-3117 Silicone are easy to use and offer sufficient protection under most operating conditions. Epoxy results in a more durable coating but care must be taken to insure that it is cured properly; an improperly cured layer of epoxy will make the high temperature leakage problem worse. Union Carbide's Parylene also results in a relatively durable coating.

The ultimate leakage protection method consists of printed circuit metalization guard rings driven from a low impedance buffer amplifier whose output is at the same potential as the pin being protected. This completely eliminates board surface leakage at critical pins by removing any difference in potential, but it is difficult to implement due to the extra buffer amplifier required and the tight PC board metalization spacings encountered.

p-channel JFETs designed for . . .

Siliconix

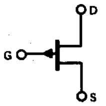
Performance Curves PC PD
See Section 5

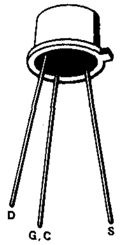
■ General Purpose Amplifiers

BENEFITS

- JAN Approved Version Available

TO-18
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3)	30 V
Gate Current, Forward Biased (Note 1)	50 mA
Total Device Dissipation (Derate 2 mW/°C)	300 mW
Storage Temperature Range	−65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N2608		2N2609		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		10		30	nA	V_{GS} = 30 V, V_{DS} = 0 V	
2					10		30	μA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	1	4	1	4	V	V_{DS} = -5 V, I_D = 1 μA	
5		I_{DSS}	Saturation Drain Current	-0.90	-4.50	-2	-10	mA	V_{DS} = -5 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		2500		μmho	V_{DS} = -5 V, V_{GS} = 0 V	f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		17		30	pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz
8		NF	Noise Figure		3		3	dB	V_{DS} = -5 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz

PC PD

*JEDEC Registered Data

NOTES:

1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

p-channel JFETs designed for . . .

■ Small-Signal Amplifiers

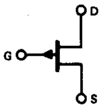
Siliconix

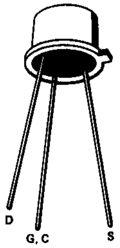
Performance Curves PC PD
See Section 5

BENEFITS

- Low Supply Voltage Operation
  $V_{GS(off)}$ Typically 1.2 V

TO-18
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3)	30 V
Gate Current, Forward Biased (Note 1)	50 mA
Total Device Dissipation (Derate 2mW/°C)	300 mW
Storage Temperature Range	-65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N2843		2N2844		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		10		30	nA	$V_{GS} = 30$ V, $V_{DS} = 0$	
2					10		30	μA	$V_{GS} = 5$ V, $V_{DS} = 0$, $T_A = 150°C$	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1$ μA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		1.7		1.7	V	$V_{DS} = -5$ V, $I_D = -1$ μA	
5		I_{DSS}	Saturation Drain Current	-200	-1000	-440	-2200	μA	$V_{DS} = -5$ V, $V_{GS} = 0$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	540		1400		μmho	$V_{DS} = -5$ V, $V_{GS} = 0$	f = 1 kHz
7		C_{iss}	Common-Source Capacitance		17		30	pF	$V_{DS} = -5$ V, $V_{GS} = 1$ V	f = 140 kHz
8		NF	Noise Figure		3		3	dB	$V_{DS} = -5$ V, $V_{GS} = 0$, $R_G = 1M\,\Omega$	f = 1 kHz
					PC		PD			

*JEDEC Registered Data

NOTES:

1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at $V_{GS} = 5$ V.
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

p-channel JFETs designed for . . .

Siliconix

2N3329 2N3330 2N3331 2N3332

Performance Curves PC
See Section 5

- **Small-Signal Amplifiers**
- **Analog Multipliers**
- **Modulators**

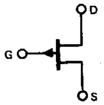
BENEFITS

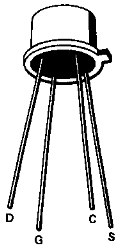
- Ease of Amplifier Design
  I_{DSS} & G_{fs} Closely Specified

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 1)	20 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	230°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3329		2N3330		2N3331		2N3332		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		0.01		0.01		0.01		0.01	μA	V_{GS} = 10 V, V_{DS} = 0	
2					10		10		10		10		V_{GS} = 10 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	20		20		20		20		V	I_G = 10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		5		6		8		6		V_{DS} = −15 V, I_D = −10 μA	
5		I_{DSS}	Saturation Drain Current	−1	−3	−2	−6	−5	−15	−1	−6	mA	V_{DS} = −10 V, V_{GS} = 0	
6		$r_{DS(on)}$	Drain-Source ON Resistance		1000		800		600			Ω	I_D = −100 μA, V_{GS} = 0	
7	DYNAMIC	g_{is}	Common-Source Input Conductance		0.2		0.2		0.2		0.2	μmho	V_{DS} = −10 V 2N3329: I_D = −1 mA 2N3330: I_D = −2 mA 2N3331: I_D = −5 mA 2N3332: I_D = −1 mA	f = 1 kHz
8		g_{rs}	Common-Source Reverse Transfer Conductance		0.1		0.1		0.1		0.1			
9		g_{os}	Common-Source Output Conductance		20		40		100		20			
10		g_{fs}	Common-Source Forward Transconductance	1000	2000	1500	3000	2000	4000	1000	2200			
11				900		1350		1800		900				f = 10MHz
12		C_{iss}	Common-Source Input Capacitance		20		20		20		20	pF	V_{DS} = −10 V, V_{GS} = 1 V	f = 1 MHz
13		NF	Noise Figure		3		3		4		1	dB	V_{DS} = −5 V, I_D = −1 mA R_{gen} = 1 MΩ	f = 1 kHz
14		NF	Noise Figure								5		V_{DS} = −5 V, I_D = −1 mA R_{gen} = 10 MΩ	f = 10 Hz

*JEDEC registered data

PC

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2.0 mW/°C

2N3368 2N3369 2N3370

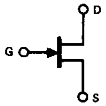
n-channel JFETs designed for . . .

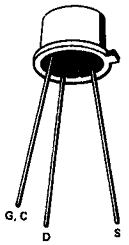
Siliconix

Performance Curves NP
See Section 5

■ Small-Signal Low Power Applications

TO-18
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−40 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +175°C
Maximum Operating Temperature	150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3368		2N3369		2N3370		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-5		-5	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1.5		-1.5		-1.5	μA		100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-11.5		-6.5		-3.2		V_{DS} = 20 V, I_D = 1 μA	
5		$I_{D(off)}$	Drain Cutoff Current		5 (-12.0)		5 (-7.0)		5 (-3.5)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
6		I_{DSS}	Saturation Drain Current	2.0	12.0	0.5	2.5	0.1	0.6	mA	V_{DS} = 30 V (Note 3), V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	4000	600	2500	300	2500	μmho	V_{DS} = 30 V (Note 3), V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		80		30		15		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		3		3		3	pF		
10		C_{iss}	Common-Source Input Capacitance		20		20		20		V_{DS} = 8 V, V_{GS} = 0	

*JEDEC registered data.

NP

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 150°C free-air temperature at rate of 2.1 mW/°C.
3. To minimize heating on high I_{DSS} units, this parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

p-channel JFETs designed for . . .

Siliconix

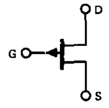
Performance Curves PE
See Section 5

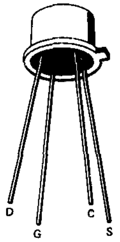
- **Analog Switches**
- **Choppers**
- **Commutators**
- **Amplifiers**

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 150\ \Omega$ (2N3386)

TO-72
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain Voltage (Note 1) . . . . 30 V
Gate-Source Voltage (Note 1) . . . . 30 V
Gate Current . . . . 50 mA
Storage Temperature Range . . . . -65 to +200°C
Total Dissipation at 25°C T_A (Note 2) . . . . 300 mW

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3382		2N3384		2N3386		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		15		15		15	nA	$V_{GS} = 30$ V $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		15		15		15	µA	$V_{GS} = 5$ V $V_{DS} = 0$	$T_A = 150°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A$ $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 3)	1.0	5.0	4.0	5.0	4.0	9.5		$V_{DS} = -5$ V $I_D = -1\ \mu A$	
5		I_{DSS}	Saturation Drain Current (Note 3)	-3.0	-30.0	-15.0	-30.0	-15.0	-50.0	mA	$V_{DS} = -10$ V $V_{GS} = 0$	
6		$I_{D(off)}$	Drain Cutoff Current		-2 (6)		-2 (6)		-2.5 (10)	nA (V)	$V_{DS} = -5$ V $V_{GS} = (\ \ )$	
7	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		300		180		150	Ω	$V_{GS} = 0$ $V_{DS} = 0$	f = 1 kHz
8		g_{fs}	Common-Source Forward Transconductance (Note 3)	4500	12,500	7500	12,500	7500	15,000	µmho	$V_{DS} = -10$ V $V_{GS} = 0$	
9		C_{sgs} + C_{dgs}	Source-Gate Capacitance Plus Drain-Gate Capacitance		6.0		6.0		6.0	pF	$V_{DS} = 0$ $V_{GS} = 10$ V	f = 140 kHz
10		C_{iss}	Common-Source Input Capacitance	16 Typ							$V_{DS} = -5$ V $V_{GS} = 1$ V	

PE

*JEDEC registered data.

NOTE:
1. Due to symmetrical geometry, units may be operated with source and drain leads interchanged.
2. Derate linearly to +175°C at 2 mW/°C
3. Pulsewidth = 2 ms, duty cycle ⩽ 3%.

n-channel JFETs designed for . . .

Siliconix

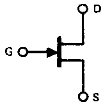
Performance Curves NP
See Section 5

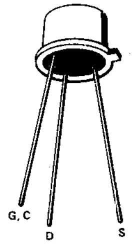
■ Small-Signal Amplifiers
■ Switches

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-18
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3436		2N3437		2N3438		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.5		-0.5		-0.5	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1.0		-1.0		-1.0	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	I_G = -1 µA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		1.0 (-10.0)		1.0 (-5.0)		1.0 (-2.5)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-9.8		-4.8		-2.3	V	V_{DS} = 20 V, I_D = 1 µA	
6		I_{DSS}	Saturation Drain Current	3.0	15.0	0.8	4.0	0.2	1.0	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2500	10,000	1500	6000	800	4500	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		35		20		5		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		6		6		6	pF		
10		C_{iss}	Common-Source Input Capacitance		18 (10)		18 (6)		18 (4)	pF (V)	V_{GS} = 0 V, V_{DS} = ( )	
11		NF	Noise Figure		2		2		2	dB	V_{DS} = 10 V, V_{GS} = 0 , R_{gen} = 1 meg, BW = 6 Hz	f = 1 kHz

*JEDEC Registered Data.

NP

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.

n-channel JFETs designed for . . .

Siliconix

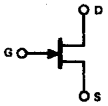
Performance Curves NP
See Section 5

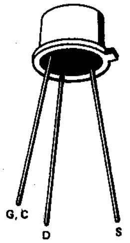
■ Small-Signal Low Noise Amplifiers

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-18
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3458		2N3459		2N3460		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.5		-0.5		-0.5	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	I_G = -1 µA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		1 (-8)		1 (-4)		1 (-2)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-7.8		-3.4		-1.8	V	V_{DS} = 20 V, I_D = 1 µA	
6		I_{DSS}	Drain Current at Zero Gate Voltage	3.0	15.0	0.8	4.0	0.2	1.0	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2500	10,000	1500	6000	800	4500	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		35		20		5		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		5		5		5	pF		
10		C_{iss}	Common-Source Input Capacitance		18 (10)		18 (6)		18 (4)	pF (V)	V_{GS} = 0 V, V_{DS} = ( ),	f = 1 MHz
11		NF	Noise Figure		6		4		4	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 6 Hz	f = 20 Hz

* JEDEC registered data.

NP

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.

Siliconix

n-channel JFETs designed for . . .

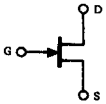
- **Low Noise Amplifiers**
- **Choppers**
- **Switches**

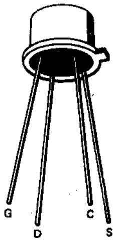
Performance Curves NFA
See Section 5

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-72
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 2) . . .	−50 V
Gate Current or Drain Current	50 mA
Total Device Dissipation (Derate 2 mW/°C to 175°C)	350 mW
Storage Temperature Range	−65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3684		2N3685		2N3686		2N3687		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−0.1		−0.1		−0.1		−0.1	nA	$V_{GS} = -30$ V, $V_{DS} = 0$	
2					−0.5		−0.5		−0.5		−0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		V	$I_G = -1$ μA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−2	−5	−1	−3.5	−0.6	−2	−0.3	−1.2		$V_{DS} = 20$ V, $I_D = 1$ nA	
5		I_{DSS}	Saturation Drain Current	2.5	7.5	1	3	0.4	1.2	0.1	0.5	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
6		$r_{DS(on)}$	Drain-Source ON Resistance (Note 1)		600		800		1200		2400	ohm	$V_{DS} = 0$ V, $V_{GS} = 0$	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	3000	1500	2500	1000	2000	500	1500	μmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		50		25		10		5			
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF		
10		C_{iss}	Common-Source Input Capacitance		4		4		4		4			
11		$\bar{e}_n$	Equivalent Short Circuit Input Spot Noise Voltage		0.15		0.15		0.15		0.15	$\frac{\mu V}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 20 Hz
12		NF	Noise Figure		0.5		0.5		0.5		0.5	dB	$V_{DS} = 10$ V, $V_{GS} = 0$ $R_{gen} = 10$ meg, BW = 6 Hz	f = 100 Hz

*JEDEC registered data

NFA

NOTES:
1. Not JEDEC registered data
2. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

Siliconix

n-channel JFETs designed for . . .

- **Small-Signal Amplifiers**
- **Oscillators**

Performance Curves NRL
See Section 5

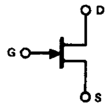
BENEFITS

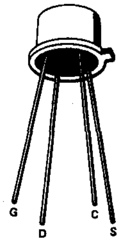
- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	–50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	–65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3821 Min	2N3821 Max	2N3822 Min	2N3822 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1		-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate-Source Voltage	-0.5	-2				V_{DS} = 15 V, I_D = 50 μA	
						-1	-4		V_{DS} = 15 V, I_D = 200 μA	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	2.5	2	10	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1500	4500	3000	6500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	1500		3000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3			
12		NF	Noise Figure		5		5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
13		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

*JEDEC Registered Data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFET designed for . . .

Siliconix

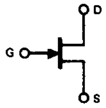
Performance Curves NRL
See Section 5

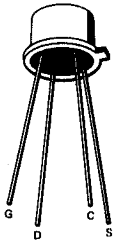
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

BENEFITS

- Low Noise
  NF < 2.5 dB @ 100 MHz

TO-72
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-30 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" From Case for 10 Sec)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-8		V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate-Source Voltage	-1.0	-7.5		V_{DS} = 15 V, I_D = 400 μA	
6		I_{DSS}	Saturation Drain Current	4	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 3)	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3,500	6,500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz (Note 3)
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	3,200				f = 200 MHz
9		g_{os}	Common-Source Output Conductance		35			f = 1 kHz (Note 3)
10		g_{iss}	Common-Source Input Conductance		800			f = 200 MHz
11		g_{oss}	Common-Source Output Conductance		200			
12		C_{iss}	Common-Source Input Capacitance		6	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		NF	Noise Figure		2.5	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 kΩ	f = 100 MHz

NRL

*JEDEC Registered Data

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFET designed for . . .

Siliconix

Performance Curves NRL
See Section 5

- **High Speed Commutators**
- **Choppers**

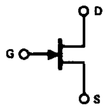
BENEFITS

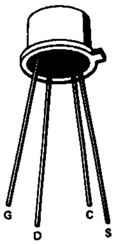
- Low Insertion Loss
  $r_{ds(on)} < 250\ \Omega$
- High Off-Isolation
  $I_{D(off)} < 0.1$ nA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		0.1	nA	V_{DS} = 15 V, V_{GS} = -8 V	
					0.1	μA		150°C
5	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		250	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
6		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
7		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF	V_{GS} = -8 V, V_{DS} = 0	

*JEDEC registered data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

p-channel JFET designed for . . .

Siliconix

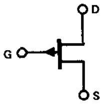
Performance Curves PC
See Section 5

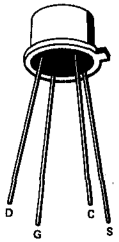
■ General Purpose Amplifiers

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	20 V
Drain-Source Voltage	-20 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature 1/16" From Case For 10 Sec	300°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3909 Min	2N3909 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		10	nA	$V_{GS} = 10$ V, $V_{DS} = 0$	
2					1	µA		T = 100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	20		V	$I_G = 10\,\mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		8.0		$V_{DS} = -10$ V, $I_D = -10\,\mu A$	
5		V_{GS}	Gate-Source Voltage	0.3	7.9		$V_{DS} = -10$ V, $I_D = -30\,\mu A$	
6		I_{DSS}	Saturation Drain Current	-0.3	-15	mA	$V_{DS} = -10$ V, $V_{GS} = 0$	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000	5,000	µmho		f = 1 kHz
8		g_{os}	Common-Source Output Conductance		100			
9		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	900				f = 10 MHz
10		C_{iss}	Common-Source Input Capacitance		32	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		16			

*JEDEC registered data

PC

Notes

1 Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2 Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

Siliconix

monolithic dual n-channel JFETs *designed for . . .*

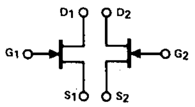
- **Differential Amplifiers**

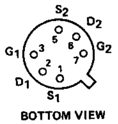
Performance Curves NNR
See Section 5

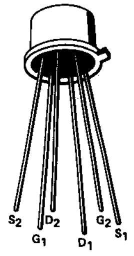
BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N3921)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 7







*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-50 V
Gate Current	50 mA
Total Device Dissipation (Derate 1.7 mW/°C to 200°C)	300 mW
Storage Temperature Range	-65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1	μA		100°C
3		BV_{DGO}	Drain-Gate Breakdown Voltage	50		V	I_D = 1 μA, I_S = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-2.7		V_{DS} = 10 V, I_D = 100 μA	
6		I_G	Gate Operating Current		-250	pA	V_{DG} = 10 V, I_D = 700 μA	
7					-25	nA		100°C
8		I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10 V, V_{GS} = 0	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35			
11		C_{iss}	Common-Source Input Capacitance		18	pF		
12		C_{rss}	Common-Source Reverse Transfer Capacitance		6			
13		g_{fs}	Common-Source Forward Transconductance	1500		μmho	V_{DG} = 10 V, I_D = 700 μA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		20			
15		NF	Spot Noise Figure		2	dB	V_{DS} = 10 V, V_{GS} 0	f = 1 kHz, R_G = 1 meg

		Characteristic		2N3921		2N3922		2N4084		2N4085		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCH	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		15		15	mV	V_{DG} = 10 V, I_D = 700 μA	
17		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		10		25		10		25	μV/°C		T_A = 0°C T_B = 100°C
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data.

NOTES:

1. Pulse test duration = 2 ms.
2. Measured at end points; T_A and T_B.
3. Assumes smaller value in numerator.

NNR
NRL-D

matched dual n-channel JFETs designed for . . .

Siliconix

Performance Curves NFA
See Section 5

- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

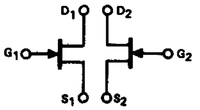
BENEFITS

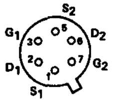
- High Accuracy & Stability
  Offset Less Than 5 mV (2N3954, 54A)
  Drift Less Than 5 µV/°C (2N3954A)
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

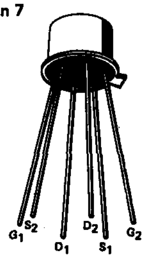
Any Case-To-Lead Voltage		±100 V
Gate-Drain or Gate-Source Voltage		-50 V
Gate-To-Gate Voltage		±100 V
Gate Current		50 mA
Total Device Dissipation 85°C	(Each Side)	250 mW
Case Temperature	(Both Sides)	500 mW
Power Derating	(Each Side)	2.86 mW/°C
	(Both Sides)	4.3 mW/°C
Storage Temperature Range		-65 to +125°C
Lead Temperature (1/16" from case for 10 seconds)		300°C

TO-71
See Section 7





BOTTOM VIEW



(ALTERNATE)

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3954		2N3954A		2N3955		2N3955A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100		-100	pA	V_{GS} = -30 V,	
2					-500		-500		-500		-500	nA	V_{DS} = 0	T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	V_{DS} = 0, I_G = -1 µA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		V_{DS} = 0, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		-4.2		V_{DS} = 20 V	I_D = 50 µA
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0			I_D = 200 µA
8		I_G	Gate Operating Current		-50		-50		-50		-50	pA	V_{DS} = 20 V,	
9					-250		-250		-250		-250	nA	I_D = 200 µA	T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common Source Spot Noise Figure		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\|I_{G1}-I_{G2}\|$	Differential Gate Current		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 µA,	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V V_{GS} = 0	
20		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0	mV	V_{DS} = 20 V, I_D = 200 µA	
21		$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2			T = 25°C to -55°C
22					1.0		0.5		2.5		1.5			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NFA

matched dual n-channel JFETs designed for . . .

Siliconix

Performance Curves NFA
See Section 5

■ Low and Medium Frequency Differential Amplifiers

■ High Input Impedance Amplifiers

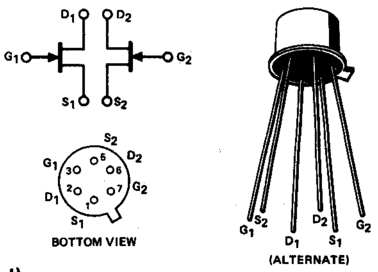
BENEFITS

- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage . . . . ±100 V
Gate-Drain or Gate-Source Voltage . . . . -50 V
Gate-To-Gate Voltage . . . . ±100 V
Gate Current . . . . 50 mA
Total Device Dissipation 85°C (Each Side). . . . . 250 mW
Case Temperature (Both Sides) . . . . 500 mW
Power Derating (Each Side) . . . . 2.86 mW/°C
(Both Sides) . . . . 4.3 mW/°C
Storage Temperature Range. . . . . -65 to +250°C
Lead Temperature (1/16" from case for 10 seconds). . . 300°C

TO-71
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3956		2N3957		2N3958		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500		-500		-500	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		V_{DS} = 0 V, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		V_{DS} = 20 V, I_D = 50 μA	
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0		V_{DS} = 20 V, I_D = 200 μA	
8		I_G	Gate Operating Current		-50		-50		-50	pA	V_{DS} = 20 V, I_D = 200 μA	
9					-250		-250		-250	nA		T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	$\lvert y_{fs} \rvert$	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\lvert I_{G1}-I_{G2} \rvert$	Differential Gate Reverse Current		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	–	V_{DS} = 20 V, V_{GS} = 0	
20		$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta \lvert V_{GS1}-V_{GS2} \rvert$	Gate-Source Voltage Differential Change With Temperature		4.0		6.0		8.0			T = 25°C to -55°C
22					5.0		7.5		10.0			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	–		f = 1 kHz

*JEDEC registered data

NOTE:

1. Assumes smaller value in numerator.

NFA

n-channel JFET designed for . . .

Siliconix

Performance Curves NH
See Section 5

- **Analog Switches**
- **Choppers**
- **Commutators**

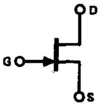
BENEFITS

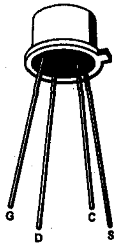
- Low Insertion Loss, No Offset Voltage
  $R_{DS(on)} < 220\ \Omega$
- Short Switching Aperture Times
  $C_{rss} < 1.5$ pF
  $t_{(on)} + t_{(off)} < 50$ ns Typical

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−30 V
Gate Current	10 mA
Total Device Dissipation (25°C Free-Air Temperature)	300 mW
Power Derating	1.7 mW/°C
Storage Temperature Range	−55 to +200°C
Operating Temperature Range	−55 to +175°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-72
See Section 7





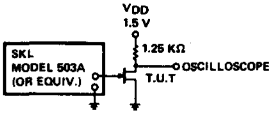
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-0.1	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4		-6.0	V	$V_{DS} = 10$ V, $I_D = 10$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30				$I_G = -1\ \mu A$, $V_{DS} = 0$	
4		I_{DSS}	Saturation Drain Current (Note 1)	2.0			mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current			1.0	nA	$V_{DS} = 10$ V, $V_{GS} = -7$ V	
6						2.0	μA		$T_A = 150°C$
7		$r_{DS(on)}$	Static Drain-Source ON Resistance			220	Ω	$V_{DS} = \leq 0.1$ V, $V_{GS} = 0$	
8		$V_{DS(on)}$	Drain-Source ON Voltage			0.25	V	$I_D = 1$ mA, $V_{GS} = 0$	
9		I_{DGO}	Drain Reverse Current			0.1	nA	$V_{DG} = 20$ V, $I_S = 0$	
10						0.2	μA		$T_A = 150°C$
11	DYN	$r_{ds(on)}$	Drain-Source ON Resistance			220	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
12		C_{iss}	Common-Source Input Capacitance		3.1	6.0	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	1.5		$V_{DS} = 0$, $V_{GS} = -7$ V	
14	SWITCH	$t_{d(on)}$	Turn ON Delay Time		3.0	20	ns	$V_{DD} = 1.5$ V $I_{D(on)} = 1.0$ mA $V_{GS(on)} = 0$ $V_{GS(off)} = -6$ V $R_L = 1.25$k Ω	See Circuit Below
15		t_r	Rise Time		10.0	100			
16		t_{off}	Turn OFF Time		30.0	100			
17		$t_{d(off)}$	Turn OFF Delay Time (Note 2)		10.0				
18		t_f	Fall Time (Note 2)		20.0				

*JEDEC registered parameters unless otherwise noted (apply to min/max only).

NOTES:

1. Pulse test duration ≤ 2 ms.
2. Non-JEDEC registered parameters: $t_{d(off)} + t_f = t_{off}$.



NH

INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 ns
PULSE DUTY CYCLE 50%
INPUT RESISTANCE 50 Ω

SAMPLING SCOPE
RISE TIME < 10 ns
INPUT RESISTANCE > 5 MΩ @ < 10 pF

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Amplifiers**

Performance Curves NC
See Section 5

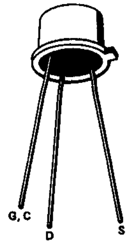
BENEFITS

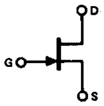
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (2N3970)
- Good Off-Isolation
  $I_{D(off)} < 250$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . –40 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Note 1) . . . . 1.8 W
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature
(1/16″ from case for 60 seconds) . . . . .300°C

TO-18
See Section 7



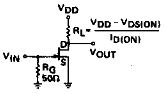


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3970		2N3971		2N3972		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate Reverse Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A,\ V_{DS} = 0$	
2		I_{DGO}	Drain Reverse Current		250		250		250	pA	$V_{DG} = 20\ V,\ I_S = 0$	
3					500		500		500	nA		150°C
4		$I_{D(off)}$	Drain Cutoff Current		250		250		250	pA	$V_{DS} = 20\ V,\ V_{GS} = -12\ V$	
5					500		500		500	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20\ V,\ I_D = 1\ nA$	
7		I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ⩽ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20\ V,\ V_{GS} = 0$	
8		$V_{DS(on)}$	Drain-Source ON Voltage						2	V	$V_{GS} = 0$	$I_D = 5\ mA$
9							1.5					$I_D = 10\ mA$
10					1							$I_D = 20\ mA$
11		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0,\ I_D = 1\ mA$	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0,\ I_D = 0$	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20\ V,\ V_{GS} = 0$	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		6		6		6		$V_{DS} = 0,\ V_{GS} = -12\ V$	
15	SW	$t_{d(on)}$	Turn–On Delay Time		10		15		40	ns	$V_{DD} = 10\ V,\ V_{GS(on)} = 0$ $I_{D(on)}$ R_L $V_{GS(off)}$ 2N3970 20 mA 450 Ω -10 V 2N3971 10 mA 850 Ω - 5 V 2N3972 5 mA 1.6KΩ - 3 V	
16		t_r	Rise Time		10		15		40			
17		t_{off}	Turn–Off Time		30		60		100			

*JEDEC registered data.

NOTE:
1. Derate linearly at the rate of 10 mW/°C.

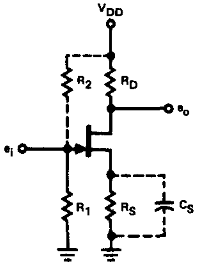


NC

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

APPLICATIONS



Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

V_{DD} (V)	R_S (Ω)	R_1 (MΩ)	R_2 (MΩ)	C_S (μF)	I_{DD} (mA)	R_D (Ω)	e_o Max (V)	A_V
2N3970								
30	560	1	∞	100	11	1K	3	9
	2.7K	3.3	10	100	6	1K	2.5	8
V_{DD} = 15 V_{SS} = -15	3K	1	Source Follower		7	0	8.5	0.96
	7.5K	1			6	0	8.5	0.96
V_{DD} = 15 V_{SS} = -15	7.5K	1	Source Follower		6	0	15	0.97
2N3971								
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97
2N3972								
10	220	1	∞	0	5	1.2K	1.5	3.5
20	220	1	∞	0	5	2.2K	3.5	7
30	1K	1	12	100	4	3.9K	5	38
	1K	1	12	100	4	5.6K	3.5	40-55
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		2.5	0	13	0.98
	7.5K	1			1.5	0	13	0.98

n-channel JFETs designed for . . .

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

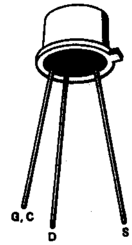
BENEFITS

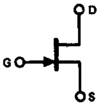
- Low Insertion Loss
  High Accuracy in Test Systems
  $R_{ON} < 30\ \Omega$ (2N4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (2N4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-55 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

TO-18
See Section 7





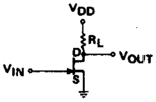
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4091		2N4092		2N4093		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V	
5									400	nA			150°C
6							200			pA		$V_{GS} = -8$ V	
7							400			nA			150°C
8					200					pA		$V_{GS} = -12$ V	
9					400					nA			150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20$ V, $I_D = 1$ nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	$V_{GS} = 0$	$I_D = 2.5$ mA	
13							0.2					$I_D = 4$ mA	
14					0.2							$I_D = 6.6$ mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
16	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		$V_{DS} = 0$, $V_{GS} = -20$ V		
19	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	$V_{DD} = 3$ V, $V_{GS(on)} = 0$ $I_{D(on)}$ $V_{GS(off)}$ R_L 2N4091 6.6 mA -12 V 425 Ω 2N4092 4 -8 700 2N4093 2.5 -6 1120		
20		t_r	Rise Time		10		20		40				
21		t_{off}	Turn-OFF Time		40		60		80				

*JEDEC registered data.

NOTE:

1. Pulsewidth = 300 μs, duty cycle ≤ 3%.



NC

INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 μs
PULSE DUTY CYCLE ≤ 10%
PULSE GENERATOR IMPEDANCE 50Ω

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

2N4117 2N4117A 2N4118 2N4118A 2N4119 2N4119A

n-channel JFETs designed for . . .

Siliconix

Performance Curves NT
See Section 5

■ Ultra-High Input Impedance Amplifiers

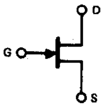
Electrometers
pH Meters
Smoke Detectors

BENEFITS

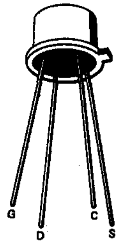
- Low Power
  $I_{DSS} < 90\ \mu A$ (2N4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (2N4117A Series)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-40 V
Gate-Current	50 mA
Total Device Dissipation (Derate 2 mW/°C to 175°C)	300 mW
Storage Temperature Range	-65 to +175°C
Lead Temperature (1/16" from case for 10 seconds)	255°C



TO-72
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4117 2N4117A		2N4118 2N4118A		2N4119 2N4119A		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current 2N4117 Series Only		-10		-10		-10	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2					-25		-25		-25	nA		150°C
3		I_{GSS}	Gate Reverse Current 2N4117A Series Only		-1		-1		-1	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4					-2.5		-2.5		-2.5	nA		150°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6		$V_{DS} = 10$ V, $I_D = 1$ nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	0.03	0.09	0.08	0.24	0.20	0.60	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70	210	80	250	100	330	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		3		5		10			
10		C_{iss}	Common-Source Input Capacitance		3		3		3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5			

*JEDEC registered data.

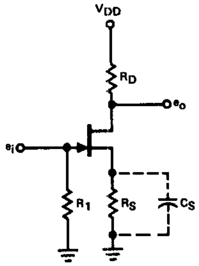
NT

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

Siliconix

APPLICATIONS



Amplifier Design Chart

V_{DD} (V)	R_S (kΩ)	C_S	I_{DD} (µA)	R_D (kΩ)	e_o Max (pK V)	A_V
2N4117						
10	10		45	120	1	5.7
20	10		45	270	1.5	12
				360	1	15
30	10		45	420	4	17
				620	1	22
V_{DD} = +15 V_{SS} = −15	510	Source Follower	35	0	8	0.97
2N4118						
10	8.2		120	36	0.6	2.2
				50	0.2	3.5
20	8.2		120	120	1	7.5
30	8.2		120	180	2	10
V_{DD} = +15 V_{SS} = −15	510	Source Follower	35	0	8	0.97
2N4119						
20	56	5 µF* at 5 V	70	150	1	10
30	56		70	240	3	17
				330	1	17-23
20	6.8		300	27	1	1.8
30	6.8		300	68	2	4.5
V_{DD} = +15 V_{SS} = −15	510	Source Follower	40	0	10	0.97

*AC Amplifier

Siliconix

n-channel JFETs designed for . . .

Performance Curves NRL
See Section 5

- **Small-Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

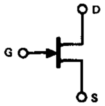
BENEFITS

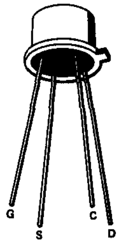
- High Gain
- Low Receiver Noise Figure

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-30 V
Gate Current	10 mA
Drain Current	15 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N4220, 2N4220A		2N4221, 2N4221A		2N4222, 2N4222A		Units	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					-0.1		-0.1		-0.1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	$I_G = -10$ µA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8		$V_{DS} = 15$ V, $I_D = 0.1$ nA	
5		V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-6	V	$V_{DS} = 15$ V, $I_D = (\ \ )$	
				(50)	(50)	(200)	(200)	(500)	(500)	(µA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000	µmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20		40			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			
12		NF	Noise Figure, Only 2N4220A, 2N4221A, 2N4222A		2.5		2.5		2.5	dB	$V_{DS} = 15$ V, $V_{GS} = 0$ $R_{gen} = 1$ meg	f = 100 Hz

*JEDEC registered data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

n-channel JFETs designed for . . .

Siliconix

Performance Curves NRL
See Section 5

■ VHF Amplifiers

■ Mixers

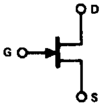
BENEFITS

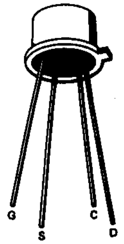
- Low Noise
  NF = 3 dB Typical @ 200 MHz
- Easy Tuning
  $C_{rss} < 2$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . -30 V
Gate Current . . . . 10 mA
Drain Current . . . . 20 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . 300 mW
Storage Temperature Range . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . 300°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4223		2N4224		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.25		-0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	V_{DS} = 15 V, I_D = ( )	
				(0.25)	(0.25)	(0.5)	(0.5)	(nA)		
5		V_{GS}	Gate-Source Voltage	-1.0	-7.0	-1.0	-7.5	V		
				(0.3)	(0.3)	(0.2)	(0.2)	(mA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYN	g_{fs}	Common-Source Forward Transconductance (Note 3)	3000	7000	2000	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
10	HIGH FREQ	$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	2700		1700		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
11		g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
12		g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
13		G_{ps}	Small Signal Power Gain	10				dB		
14		NF	Noise Figure		5				V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 K	

*JEDEC registered data.

NRL

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

Siliconix

n-channel JFETs designed for . . .

- **Small-Signal Amplifiers**
- **Choppers**
- **Voltage-Controlled Resistors**

Performance Curves NP
See Section 5

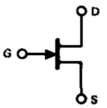
BENEFITS

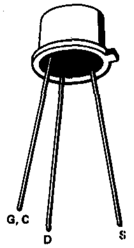
- Low Noise
  - NF < 1 dB at 1 kHz
- Operation from Low Power Supply Voltages
  - $V_{GS(off)} < 1$ V (2N4338)
- Simple Biasing Design with Tightly Specified Parameter Tolerances
  - 3:1 I_{DSS}, V_P, g_{fs} Ranges
- High Off-Isolation as a Switch
  - $I_{D(off)} < 50$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-50 V
Gate Current	50 mA
Total Device Dissipation (Note 2)	300 mW
Storage Temperature Range	-65 to +200°C
Maximum Operating Temperature	175°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		2N4338		2N4339		2N4340		2N4341		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1		-0.1		-0.1		-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 15 V, I_D = 0.1 μA	
5		$I_{D(off)}$	Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	V_{DS} = 15 V V_{GS} = ( )	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		5		15		30		60			
9		$r_{ds(on)}$	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, V_{GS} = 0	
10		C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
12		NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

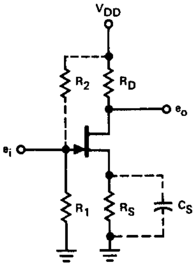
*JEDEC registered data

NP

NOTES:

1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 125 msec (I_{DSS}) and 625 msec (g_{fs}) after d-c power is applied. (Not a JEDEC condition.)

APPLICATIONS



Amplifier Design Chart

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4338								
15	1500	1M	∞	0	0.25	36	2.5	9-12
				30		36	1.5	16-24
						47	2.0	20-30
	5100	1M	∞	0	0.12	82	3.0	10-10.5
				25		82	1.5	24-37
	36K	1M	2M	30	0.15	27	1.0	13-18.5
30	1500	1M	∞	0	0.25	82	4.0	21.5-27
				30		82	2.5	32-49
						100	3.0	43-64
	5100	1M	∞	0	0.12	150	4.5	14.5-16
				25		150	2.5	38-54
						200	1.5	40-50
	36K	1M	5M	30	0.15	82	5.0	37-52
45	1500	1M	∞	0	0.25	120	6.5	27-33
				30		120	4.0	45-68
	5100	1M	∞	0	0.12	270	10	28-31
				25		270	5.0	76-105
	36K	1M	8.2M	0	0.15	120	14	2.8
				30		120	7.0	54-76
V_{DD} = +15 V_{SS} = −15	100K	1M	∞	0	0.15	0	9.0	0.98
2N4339								
15	1800	1M	∞	0	0.42	20	3.0	7-7.5
				40		20	2.0	17-22
						27	2.0	23-27
	9100	1M	6.8M	35	0.32	18	2.0	17-19
						30	2.5	26-28
	27K	1M	3M	25	0.2	22	1.0	16-18
						43	2.0	28-30
30	1800	1M	∞	0	0.42	47	6.5	15-17
				40		47	4.0	38-47
						51	4.5	40-50
	9100	1M	13M	0	0.32	43	8.0	4.5
				35		43	5.0	40-43
						68	4.5	53-60
	27K	1M	7.5M	25	0.2	68	4.0	49-52
						100	7.0	66-70
45	1800	1M	∞	0	0.42	75	7.5	23-25
				40		75	5.0	58-70
						100	7.0	73-77
	9100	1M	22M	0	0.32	68	7.0	7.0
				25		68	6.5	59-64
						120	7.0	80-85
	27K	1M	12M	0	0.2	100	12	3.3
				25		100	5.0	65-68
						180	8.0	100-115
V_{DD} = +15 V_{SS} = −15	75K	1M	∞	0	0.22	0	10	0.98

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (μF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4340								
15	680	1M	∞	0	1.5	5.1	3.0	3.5-4
				65		5.1	1.5	7-8.5
						6.8	2.0	9-10.5
	1200	1M	∞	0	1.1	7.5	2.5	3.5-4
				60		7.5	2.0	9-11
						10	2.0	11-13
	3900	1M	∞	0	0.4	18	4.0	3.5-4
				40		18	1.5	15-18
						22	1.0	19-22
30	680	1M	∞	0	1.5	12	6.0	9.5-10
				65		12	3.0	17-22
						18	1.0	24-26
	1200	1M	∞	0	1.1	18	6.0	9-9.5
				60		18	4.0	21-26
						24	2.0	29
	3900	1M	∞	0	0.4	39	7.0	7.5-8
				40		39	7.0	30-36
						62	0.5	34-45
	20K	1M	6.8M	35	0.35	30	3.0	25-27
						56	6.5	40
45	680	1M	∞	0	1.5	20	10.5	14-15.5
				65		20	8.0	27-32
						27	4.0	35
	1200	1M	∞	0	1.1	27	12.5	16-18
				60		27	5.0	30-37
						39	2.0	39-42
	3900	1M	∞	0	0.4	68	12	12-13
				40		68	7.0	52-61
						91	3.0	56-63
	20K	2M	3M	55	1.0	10	5.0	15
						20	4.0	27-28
V_{DD} = +15 V_{SS} = −15	22K	1M	∞	0	0.75	0	12	0.96
2N4341								
15	1000	1M	∞	70	2.7	2	1.0	3-3.5
						2.7	2.0	4-4.5
	1200	1.2M	7.5M	80	3.5	1.2	2.0	2.5
						2.2	3.0	3-4.5
	2000	1M	∞	65	1.8	3	2.0	4-4.5
						4.7	1.5	6-6.5
30	1000	1M	∞	0	2.7	6.2	7.0	4.0
				70		6.2	3.5	10
						9.1	1.5	11-13
	1200	1.1M	15M	80	3.5	3.9	4.0	7.5-8
	2000	1M	∞	0	1.8	9.1	6.0	3.0
				65		9.1	4.0	12
						15	1.0	13-19
	15K	1M	3.3M	50	0.7	18	3.0	16-21
45	1000	1M	∞	0	2.7	10	8.5	6.3
				70		10	6.0	16
	1200	1M	22M	80	3.5	6.8	7.0	13
	2000	1M	∞	0	1.8	15	8.5	5.5
				65		15	5.0	20-21
	15K	1M	5.6M	50	0.7	30	9.0	28-35
V_{DD} = +15 V_{SS} = −15	10K	1M	∞	0	1.9	0	13.5	0.94

n-channel JFETs designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Siliconix

Performance Curves NC
See Section 5

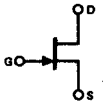
BENEFITS

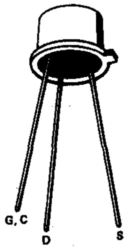
- Low Insertion Loss, High Accuracy in Test Systems $r_{ON} < 30\ \Omega$ (2N4391)
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . –40 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . 1.8 W
Storage Temperature Range . . . . –65 to +200°C
Lead Temperature
(1/16″ from case for 60 seconds) . . . . 300°C

TO-18
See Section 7

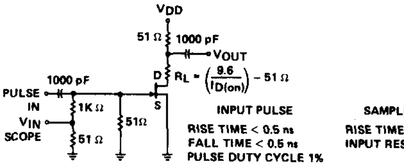




*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4391 Min	2N4391 Max	2N4392 Min	2N4392 Max	2N4393 Min	2N4393 Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	$V_{GS} = -20$ V, $V_{DS} = 0$		
2					-200		-200		-200	nA			150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
4		$I_{D(off)}$	Drain Cutoff Current						100	pA	$V_{DS} = 20$ V	$V_{GS} = -5$ V	
5									200	nA			150°C
6							100			pA		$V_{GS} = -7$ V	
7							200			nA			150°C
8					100					pA		$V_{GS} = -12$ V	
9					200					nA			150°C
10		$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	$I_G = 1$ mA, $V_{DS} = 0$		
11		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		$V_{DS} = 20$ V, $I_D = 1$ nA		
12		I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
13		$V_{DS(on)}$	Drain Source ON Voltage						0.4	V	$V_{GS} = 0$	$I_D = 3$ mA	
14							0.4					$I_D = 6$ mA	
15					0.4							$I_D = 12$ mA	
16		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
17	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
18		C_{iss}	Common-Source Input Capacitance		14		14		14	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
19		C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		$V_{DS} = 0$	$V_{GS} = -5$ V	
20							3.5					$V_{GS} = -7$ V	
21					3.5							$V_{GS} = -12$ V	
22	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		15	ns	$V_{DD} = 10$ V, $V_{GS(on)} = 0$		
23		t_r	Rise Time		5		5		5				
24		$t_{d(off)}$	Turn-OFF Delay Time		20		35		50				
25		t_f	Fall Time		15		20		30				

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4391	12 mA	-12 V	800 Ω
2N4392	6	-7	1.6K Ω
2N4393	3	-5	3.2K Ω



INPUT PULSE
RISE TIME < 0.5 ns
FALL TIME < 0.5 ns
PULSE DUTY CYCLE 1%

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 50 Ω

NC

*JEDEC registered data.

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

n-channel JFETs designed for . . .

- **VHF Amplifiers**
- **Mixers**

Siliconix

Performance Curves NH
See Section 5

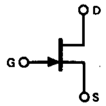
BENEFITS

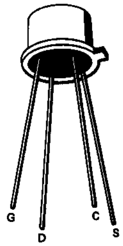
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage, 2N4416 . . . . -30 V
Gate-Drain or Gate-Source Voltage, 2N4416A . . . . . . -35 V
Gate Current . . . . 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . 300°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -20 V, V_{DS} = 0 V	
2					-0.1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 µA, V_{DS} = 0 V	2N4416
				-35				2N4416A
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416
				-2.5	-6			2N4416A
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	µmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50	µmho		
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4	pF		
10		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz		400 MHz		Unit	Test Conditions
				Min	Max	Min	Max		
11	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		100		1000	µmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000	µmho	
13		g_{oss}	Common-Source Output Conductance		75		100	µmho	
14		b_{oss}	Common-Source Output Susceptance		1000		4000	µmho	
15		g_{fs}	Common-Source Forward Transconductance			4000		µmho	
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

*JEDEC Registered data

NH

NOTES:
1. Pulse test duration = 300 µs.

n-channel JFETs designed for . . .

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

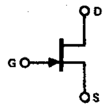
BENEFITS

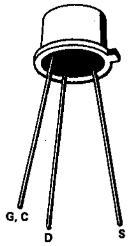
- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856, 59)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- High Speed
  $t_{ON} < 9$ ns
- Fully Qualified
  JAN, JANTX and JANTXV Available

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage, 2N4856-58	-40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859-61	-30 V
Gate Current	50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 7



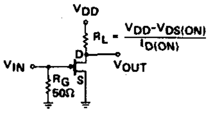


*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic		2N4856 2N4859		2N4857 2N4860		2N4858 2N4861		Unit	Test Conditions	
					Min	Max	Min	Max	Min	Max			
1		BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2				2N4859-61	−30		−30		−30				
3	S T A T I C	I_{GSS}	Gate Reverse Current	2N4856-58		−250		−250		−250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4						−500		−500		−500	nA		150°C
5				2N4859-61		−250		−250		−250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6						−500		−500		−500	nA		150°C
7		$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8						500		500		500	nA		150°C
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0.8	−4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ \ )$	
12	D Y N	$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8			
15	S W I T C H I N G	$t_{d(on)}$	Turn-ON Delay Time			6 (20) [−10]		6 (10) [−6]		10 (5) [−4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ \ )$, $V_{GS(off)} = [\ ]$	$R_L =$ 464 Ω, 2N4856, 59 953 Ω, 2N4857, 60 1910 Ω, 2N4858, 61
16		t_r	Rise Time			3 (20) [−10]		4 (10) [−6]		10 (5) [−4]	ns (mA) [V]		
17		t_{off}	Turn-OFF Time			25 (20) [−10]		50 (10) [−6]		100 (5) [−4]	ns (mA) [V]		

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.



NC

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

n-channel JFETs designed for . . .

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

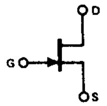
BENEFITS

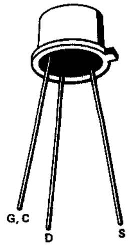
- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856A, 59A)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF
- High Speed
  $t_{ON} < 8$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage, 2N4856A-58A	−40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859A-61A	−30 V
Gate Current	50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-18
See Section 7





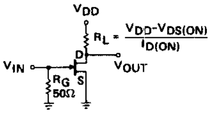
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			2N4856A 2N4859A		2N4857A 2N4860A		2N4858A 2N4861A		Unit	Test Conditions	
					Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	2N4856A-58A	−40		−40		−40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2				2N4859A-61A	−30		−30		−30				
3		I_{GSS}	Gate Reverse Current	2N4856A-58A		−250		−250		−250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4						−500		−500		−500	nA		150°C
5				2N4859A-61A		−250		−250		−250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6						−500		−500		−500	nA		150°C
7		$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8						500		500		500	nA		150°C
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4	−10	−2	−6	−0.8	−4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ \ )$	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance			10		10		10	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance			4		3.5		3.5			
15	SWITCHING	$t_{d(on)}$	Turn-ON Delay Time			5 (20) [−10]		6 (10) [−6]		8 (5) [−4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ \ )$, $V_{GS(off)} = [\ ]$	$R_L = \begin{cases} 464\ \Omega, \text{2N4856A, 59A} \\ 953\ \Omega, \text{2N4857A, 60A} \\ 1910\ \Omega, \text{2N4858A, 61A} \end{cases}$
16		t_r	Rise Time			3 (20) [−10]		4 (10) [−6]		8 (5) [−4]	ns (mA) [V]		
17		t_{off}	Turn-OFF Time			20 (20) [−10]		40 (10) [−6]		80 (5) [−4]	ns (mA) [V]		

NC

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 μs, duty cycle ⩽ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

n-channel JFETs designed for . . .

Siliconix

Performance Curves NS
See Section 5

■ Audio and Sub-Audio Amplifiers

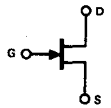
BENEFITS

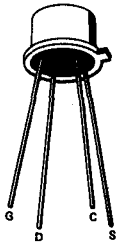
- Ultra Low Noise
  $\overline{e}_n$ = 8 nV/$\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e}_n$ = 2 nV/$\sqrt{Hz}$ Typical at 1 kHz

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . -40 V
Gate Current or Drain Current . . . . 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C) . . . . 300 mW
Storage Temperature Range . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . 300°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N4867 2N4867A		2N4868 2N4868A		2N4869 2N4869A		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0		
2					-0.25		-0.25		-0.25	μA		150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5		V_{DS} = 20 V, I_D = 1 μA		
5		I_{DSS}	Saturation Drain Current (Note 2)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	700	2000	1000	3000	1300	4000	μmho	V_{DS} = 20 V, V_{GS} = 0		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1.5		4		10				
8		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF			f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		25		25		25				
10		$\overline{e}_n$	Short Circuit Equivalent Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	2N4867 Series	f = 10 Hz
11					10		10		10			2N4867A Series	
12					10		10		10			2N4867 Series	f = 1 kHz
13					5		5		5			2N4867A Series	
14		NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0 R_{gen} = 20 K, 2N4867 Series 5 K, 2N4867A Series		f = 1 kHz

*JEDEC registered data.

NS

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms.

p-channel JFETs designed for . . .

Siliconix

Performance Curves PS
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**

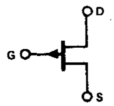
BENEFITS

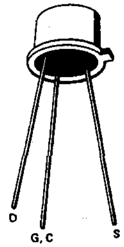
- Low Insertion Loss
  $R_{DS(on)} < 75\ \Omega$ (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

TO-18
See Section 7





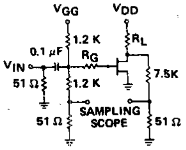
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5018		2N5019		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A, V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15\ V, V_{DS} = 0$	
3		$I_{D(off)}$	Drain Cutoff Current		−10		−10		$V_{DS} = -15\ V, V_{GS} = 12\ V$ (2N5018)	
4					−10		−10	μA	$V_{GS} = 7\ V$ (2N5019)	150°C
5		I_{DGO}	Drain Reverse Current		−2		−2	nA	$V_{DG} = -15\ V, I_S = 0$	
6					−3		−3	μA		150°C
7		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15\ V, I_D = -1\ \mu A$	
8		I_{DSS}	Saturation Drain Current	−10		−5		mA	$V_{DS} = -20\ V, V_{GS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		−0.5		−0.5	V	$V_{GS} = 0, I_D = -6$ mA (2N5018), $I_D = -3$ mA (2N5019)	
10	DYN	$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1\ mA, V_{GS} = 0$	
11		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0, V_{GS} = 0$	f = 1 kHz
12		C_{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15\ V, V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0, V_{GS} = 12\ V$ (2N5018), $V_{GS} = 7\ V$ (2N5019)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6\ V, V_{GS(on)} = 0$ $V_{GS(off)}$ $I_{D(on)}$ R_L 2N5018 12 V −6 mA 910 Ω 2N5019 7 V −3 mA 1.8K Ω	
15		t_r	Rise Time		20		75			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		25			
17		t_f	Fall Time		50		100			

*JEDEC registered data.

NOTE:

1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



PS

INPUT PULSE

RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 100 ns
REPETITION RATE 1 MHz

SAMPLING SCOPE

RISE TIME 0.4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1.5 pF

Siliconix

monolithic dual n-channel JFETs designed for . . .

- **High Gain Differential Amplifiers**

Performance Curves NNR
See Section 5

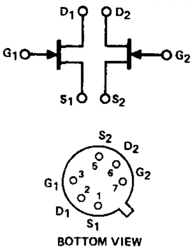
BENEFITS

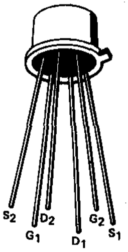
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5045)
- Low Drift
  5 mV Drift Maximum (2N5045)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-50 V
Forward Gate Current	30 mA
Total Dissipation (25°C Free Air Temp.)	400 mW
Power Derating (to 175°C)	2.67 mW/°C
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic (Note 1)		2N5045		2N5046		2N5047		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	μA	V_{GS} = -50 V, V_{DS} = 0 V	
2					-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0 V	
3					-250		-250		-250			T = 150°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5	-0.5	-4.5	-0.5	-4.5	V	V_{DS} = 15 V, I_D = 0.5 nA	
5		I_{DSS}	Drain Saturation Current	0.5	8.0	0.5	8.0	0.5	8.0	mA		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1.5	6.0	1.5	6.0	1.5	6.0	mmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		$\lvert y_{fs} \rvert$	Common-Source Forward Admittance	1.5		1.5		1.5				f = 100 MHz
8		g_{os}	Common-Source Output Conductance		25		25		25	μmho		f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0	pF		f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
11		NF	Spot Noise Figure		5.0		5.0			dB		f = 10 Hz, R_G = 1 MΩ
12		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200			$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
13	MATCHING	$\lvert I_{GSS1}-I_{GSS2} \rvert$	Differential Gate Current		10		10		10	nA	V_{GS} = -15 V, V_{DS} = 0 V	T_A = 100°C
14		I_{DSS1}/I_{DSS2}	Drain Current Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{GS} = 0 V, V_{DS} = 15 V	
15		$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DS} = 15 V	I_D = 50 μA
16					5		10		15			I_D = 200 μA
17		$\lvert \Delta \lvert V_{GS1}-V_{GS2} \rvert$	Gate-Source Voltage Differential Drift (Note 3)		5		10		15		V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C	T_B = -25°C
18					5		10		15			T_B = 100°C
19		$\lvert g_{fs1}/g_{fs2}$	Transconductance Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{DS} = 15 V, I_D = 200 μA	f = 1 kHz
20		$\lvert g_{os1}-g_{os2} \rvert$	Diff. Output Conductance		1.0		2.0		3.0	μmho		

*JEDEC registered data.

NNR
NRL-D

NOTES:
1. Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements..
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

p-channel JFETs designed for . . .

Siliconix

Performance Curves PS
See Section 5

■ Analog Switches
■ Commutators
■ Choppers
■ Integrator Reset Switch

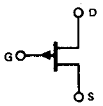
BENEFITS

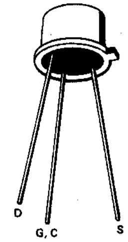
- Simplifies Series-Shunt Switching when Combined with 2N4393, its N-Channel Complement
- Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	.50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-18
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5114 Min	2N5114 Max	2N5115 Min	2N5115 Max	2N5116 Min	2N5116 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20$ V, $V_{DS} = 0$	
3					1.0		1.0		1.0	μA		150°C
4		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (2N5114) $V_{GS} = 7$ V (2N5115), $V_{GS} = 5$ V (2N5116)	
5					-1.0		-1.0		-1.0	μA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	$V_{DS} = -15$ V, $I_D = -1$ nA	
7		I_{DSS}	Saturation Drain Current (Note 2),	-30	-90	-15	-60	-5	-25	mA	$V_{GS} = 0$, $V_{DS} = -18$ V (2N5114) $V_{DS} = -15$ V (2N5115, 2N5116)	
8		$V_{GS(f)}$	Forward Gate-Source Voltage		-1		-1		-1	V	$I_G = -1$ mA, $V_{DS} = 0$	
9		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		$V_{GS} = 0$, $I_D = -15$ mA (2N5114) $I_D = -7$ mA (2N5115), $I_D = -3$ mA (2N5116)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = -1$ mA	
11	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		75		100		150	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
12		C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = -15$, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		$V_{DS} = 0$, $V_{GS} = 12$ V (2N5114) $V_{GS} = 7$ V (2N5115), $V_{GS} = 5$ V (2N5116)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		6		10		12	ns		
15		t_r	Rise Time		10		20		30			
16		$t_{d(off)}$	Turn-OFF Delay Time		6		8		10			
17		t_f	Fall Time		15		30		50			

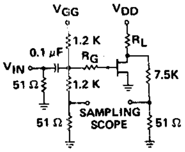
	2N5114	2N5115	2N5116
V_{DD}	-10 V	-6 V	-6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15 mA	-7 mA	-3 mA

*JEDEC registered data.

NOTES:

1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse Test PW 300 μs, duty cycle ≤ 3%.

PS



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 100 ns
REPETITION RATE 1 MHz

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 MΩ
INPUT CAPACITANCE 1.5 pF

monolithic dual n-channel JFETs designed for . . .

- ■ **Differential Amplifiers**
- ■ **FET Input Op Amps**

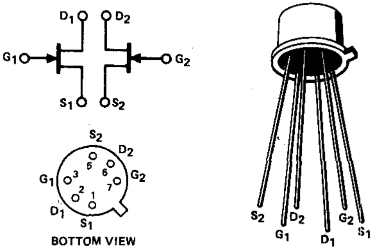
Siliconix

Performance Curves NNP
See Section 5

BENEFITS

- Minimum System Error and Calibration
  5 mV Maximum Offset (2N5196, 97)
- Low Drift
  5 $\mu V/^\circ C$ Maximum (2N5196)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -50 V
Gate Current . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.56 mW/°C) . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 4.3 mW/°C) . . . . 500 mW
Storage Temperature Range . . . . -65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-25	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-50	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-3.8		V_{DG} = 20 V, I_D = 200 μA	
6		I_G	Gate Operating Current		-15	pA		
					-15	nA		125°C
7		I_{DSS}	Saturation Drain Current	0.7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	700	1600		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
15		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

		Characteristic		2N5196		2N5197		2N5198		2N5199		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
19		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
20		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	$\mu V/^\circ C$		T_A = 25°C T_B = 125°C
21					5		10		20		40			T_A = -55°C T_B = 25°C
22		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	μmho		f = 1 kHz

*JEDEC registered data.

NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

NNP
NP-D

n-channel JFETs designed for . . .

Siliconix

Performance Curves NIP
See Section 5

- **Low ON Resistance Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Capacitors**
- **Low Noise Audio Amplifiers**

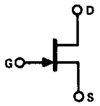
BENEFITS

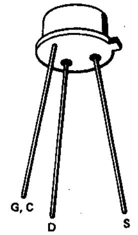
- Low Insertion Loss
  $R_{DS(on)} < 5\ \Omega$ (2N5432)
- Small Error in Measurement Systems
  $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{d(on)} < 4$ ns
- Low Noise Audio-Frequency Amplification
  $e_n < 2\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 1 kHz Typical

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . −25 V
Gate Current . . . . 100 mA
Drain Current . . . . 400 mA
Total Device Dissipation at 25°C
  Free-Air Temperature (Note 1) . . . . 300 mW
Storage Temperature Range . . . . −65 to +150°C
Lead Temperature
  (1/16" from case for 10 seconds) . . . . .300°C

TO-52
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

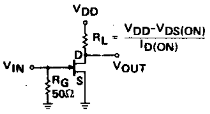
		Characteristic		2N5432		2N5433		2N5434		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-200		-200		-200	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-200		-200		-200	nA		150°C
3		BV_{GSS}	Gate Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 5 V, V_{GS} = -10 V	
5					200		200		200	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V_{DS} = 5 V, I_D = 3 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	150		100		30		mA	V_{DS} = 15 V, V_{GS} = 0	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	V_{GS} = 0, I_D = 10 mA	
9		$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		30		30		30	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
13	SW	$t_{d(on)}$	Turn-ON Delay Time		4		4		4	ns	V_{DD} = 1.5 V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -12 V, $I_{D(on)}$ = 10 mA	R_L = 145 Ω (2N5432) 143 Ω (2N5433) 140 Ω (2N5434)
14		t_r	Rise Time		1		1		1			
15		$t_{d(off)}$	Turn-OFF Delay Time		6		6		6			
16		t_f	Fall Time		30		30		30			

*JEDEC registered data.

NIP

NOTES:

1. Derate linearly at the rate of 2.3 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.



$R_L = \dfrac{V_{DD} - V_{DS(ON)}}{I_{D(ON)}}$

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

matched dual n-channel JFETs designed for . . .

Siliconix

Performance Curves NFA
See Section 5

■ Low and Medium Frequency Differential Amplifiers

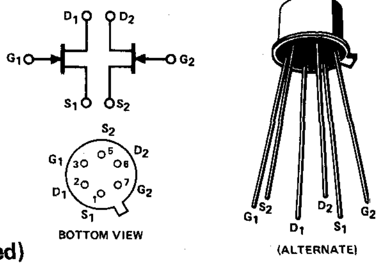
*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead-To-Case Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +250°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5452)
- Simplifies Amplifier Design
  Output Conductance Less that
  1 µmho

TO-71
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5452		2N5453		2N5454		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0 V	
2					-200		-200		-200	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 µA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2		V_{DS} = 20 V, I_D = 50 µA	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2		V_{DS} = 0 V, I_G = 1 mA	
7		I_{DSS}	Drain Saturation Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	µmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
9				1000		1000		1000				f = 100 MHz
10		g_{os}	Common-Source Output Conductance		3.0		3.0		3.0			f = 1 kHz
11					1.0		1.0		1.0		V_{DS} = 20 V, I_D = 200 µA	
12		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
14		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0 V	
15		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
16		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
17	MATCHING	I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 µA	
19		$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to -55°C
20					0.5		1.0		2.5			T = 25°C to +125°C
21		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz
22		$\|g_{os1}-g_{os2}\|$	Differential Output Conductance		0.25		0.25		0.25	|µmhos|		

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

matched dual n-channel JFETs designed for . . .

■ Differential Amplifiers

Siliconix

Performance Curves NS
See Section 5

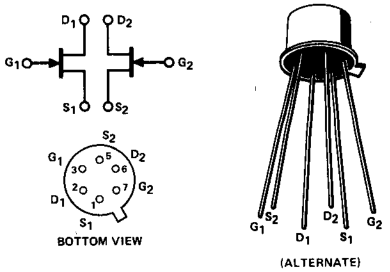
BENEFITS

- Ultra-Low Noise
  $\overline{e}_n$ = 8 nV/$\sqrt{\text{Hz}}$ at 10 Hz (Typical)
  $\overline{e}_n$ = 2 nV/$\sqrt{\text{Hz}}$ at 1 kHz (Typical)
- Minimum System Error and Calibration
  5 mV Offset Maximum
  CMRR > 100 dB

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -40 V
Gate Current . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.0 mW/°C) . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 3.0 mW/°C) . . . . 375 mW
Storage Temperature Range . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 30 seconds) . . . . 300°C

TO-71
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic					Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-250	pA	V_{GS} = -30 V, V_{DS} = 0	
2						-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage		-0.2	-3.8		V_{DG} = 20 V, I_D = 200 μA	
6		I_G	Gate Operating Current			-100	pA		
						-100	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)		0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)		1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)		500	1000		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance			10		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance			1		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance			25	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance			5			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage	2N5515-19		30	$\frac{nV}{\sqrt{Hz}}$	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
				2N5520-24		15			
				2N5515-24		10			f = 1 kHz

Characteristic				2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	–	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV	V_{DG} = 20 V, I_D = 200 μA	
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		5		10		20		40		80	μV/°C		T_A = 25°C T_B = 125°C
					5		10		20		40		80			T_A = -55°C T_B = 25°C
19		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho		f = 1 kHz
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	–		
21		CMRR	Common Mode Rejection Ratio (Note 4)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA	

*JEDEC registered data.

NOTES:

1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.
4. CMRR = $20\log_{10}\left(\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right)$, ΔV_{DD} = 10 V.

NS

monolithic dual n-channel JFETs designed for . . .

■ General Purpose Differential Amplifiers

Siliconix

Performance Curves NNP
See Section 5

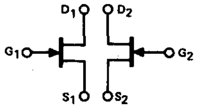
BENEFITS

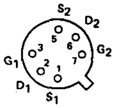
- High Input Impedance
  $I_G < 50$ pA
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5545)

*ABSOLUTE MAXIMUM RATINGS (25°C)

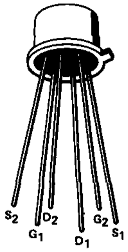
Gate-Drain or Gate-Source Voltage	−50 V
Gate Current	30 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 1.67 mW/°C)	250 mW
Total Device Dissipation, T_A = 25°C (Derate 2.67 mW/°C)	400 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16″ from case for 30 seconds)	300°C

TO-71
See Section 7





BOTTOM VIEW



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0		
2					-150	nA			T_A = 150°
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 15 V, I_D = 0.5 nA		
5		I_G	Gate Operating Current		-50	pA	V_{DG} = 15 V, I_D = 200 μA		
6		I_{DSS}	Saturation Drain Current	0.5	8	mA	V_{DS} = 15 V, V_{GS} = 0		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0		f = 1 kHz
8		g_{os}	Common-Source Output Conductance		25				
9		C_{iss}	Common-Source Input Capacitance		6	pF			f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		2				
11		NF	Spot Noise Figure		3.5	dB	V_{DG} = 15 V, I_D = 200 μA	2N5545	f = 10 Hz, R_G = 1 MΩ
					5			2N5546	
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		180	$\frac{nV}{\sqrt{Hz}}$		2N5545	f = 10 Hz
					200			2N5546	

		Characteristic		2N5545		2N5546		2N5547		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
13	MATCHING	$\|I_{G1}-I_{G2}\|$	Differential Gate Current		5		5		5	nA	V_{DG} = 15 V, I_D = 200 μA	T_A = 125°C
14		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.90	1	0.90	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 15 V	I_D = 50 μA
					5		10		15			I_D = 200 μA
16		$\frac{\Delta\|V_{GS1}-V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		10		20		40	μV/°C	V_{DG} = 15 V, I_D = 200 μA	T_A = 25°C T_B = 125°C
					10		20		40			T_A = -55°C T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.95	1	0.90	1	–		f = 1 kHz
18		$\|g_{os1}-g_{os2}\|$	Differential Output Conductance		1		2		3	μmho		

*JEDEC registered data.

NOTES:

1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

NNP
NP-D

n-channel JFETs designed for . . .

Siliconix

Performance Curves NRL
See Section 5

■ General Purpose Amplifiers

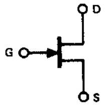
BENEFITS

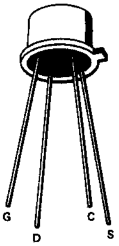
- Low Noise
- Low Output Conductance

*ABSOLUTE MAXIMUM RATINGS (at 25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	-30 V
Gate Current	10 mA
Total Device Dissipation (25°C Free Air Temperature)	300 mW
Power Derating (to +175°C)	2.0 mW/°C
Storage Temperature Range	-65 to +200°C
Operating Temperature Range	-65 to +175°C
Lead Temperature (1/16" from case for 10 seconds)	240°C

TO-72
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5556		2N5557		2N5558		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0 V	
2					-100		-100		-100			T = 150°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.2	-4.0	-0.8	5.0	-1.5	-6.0	V	V_{DS} = 15 V, I_D = 1 nA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30			I_G = -10 μA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	2.5	2.0	5.0	4.0	10.0	mA	V_{DG} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6500	1500	6500	1500	6500	μmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		20		20		20			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		$\overline{e}_n$	Common-Source Equivalent Short Circuit Input Noise Voltage		35		35		35	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
11					20		20		20			f = 100 Hz
12		NF	Noise Figure		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 V, BW = 1.0 Hz	f = 10 Hz
13					1		1		1			f = 100 Hz

*JEDEC registered data

NRL

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Pulse test duration ⩽ 2 ms.

Siliconix

matched dual n-channel JFETs designed for . . .

Performance Curves NC
See Section 5

- **Wideband Differential Amplifiers**
- **Commutators**

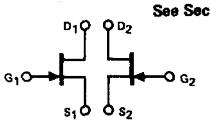
BENEFITS

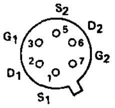
- High Gain
  7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

*ABSOLUTE MAXIMUM RATINGS (25°C)

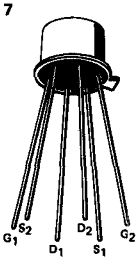
Gate-Gate Voltage .... ±80 V
Gate-Drain or Gate-Source Voltage .... -40 V
Gate Current .... 50 mA
Device Dissipation (Each Side), T_A = 25°C
  (Derate 2.2 mW/°C) .... 325 mW
Total Device Dissipation, T_A = 25°C
  (Derate 3.3 mW/°C) .... 650 mW
Storage Temperature Range.............. -65 to +200°C
Lead Temperature
  (1/16" from case for 10 seconds) ....300°C

TO-71
See Section 7





BOTTOM VIEW



(ALTERNATE)

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		1.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	30	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
				7000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance		45			f = 1 kHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		12			
12		NF	Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
13		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristics		2N5564		2N5565		2N5566		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
14	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
16		$\frac{\Delta\|V_{GS1}-V_{GS2}\|}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		10		25		50	μV/°C		T_A = 25°C T_B = 125°C
					10		25		50			T_A = -55°C T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	–		f = 1 kHz

*JEDEC registered data.

NC

NOTES:
1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B.

matched dual n-channel JFETs designed for . . .

Siliconix

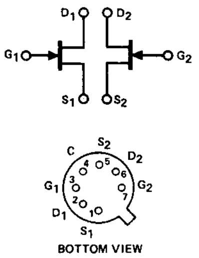
- **Differential Amplifiers**
- **High Input Impedance Amplifiers**

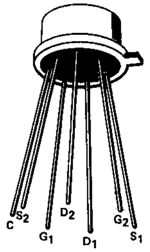
Performance Curves NT
See Section 5

BENEFITS

- Matching Characteristics Specified
- High Input Impedance
  I_G = 1 pA Max (2N5906–9)

TO-78
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage . . . . ±80 V
Gate-Drain or Gate-Source Voltage . . . . –40 V
Gate Current . . . . 10 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 3 mW/°C) . . . . 367 mW
Total Device Dissipation, T_A = 25°C
(Derate 4 mW/°C) . . . . 500 mW
Storage Temperature Range . . . . –65 to +150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5902-5		2N5906-9		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-2	pA	V_{GS} = –20 V, V_{DS} = 0	
2					-10		-5	nA		125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage		-4		-4		V_{DG} = 10 V, I_D = 30 μA	
6		I_G	Gate Operating Current		-3		-1	pA		
7					-3		-1	nA		125°C
8	DYNAMIC	I_{DSS}	Saturation Drain Current	30	500	30	500	μA	V_{DS} = 10 V, V_{GS} = 0	
9		g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho		f = 1 kHz
10		g_{os}	Common-Source Output Conductance		5		5			
11		C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
13		g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		1		1			
15		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	
16		NF	Spot Noise Figure		3		1	dB		f = 100 Hz, R_G = 10 M

		Characteristic		2N5902, 6		2N5903, 7		2N5904, 8		2N5905, 9		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max			
17	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	V_{DG} = 10 V, I_D = 30 μA, T_A = 125°C	2N5902-5
18					0.2		0.2		0.2		0.2			2N5906-9
19		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
21		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
22		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		5		10		20		40	μV/°C		T_A = 25°C T_B = 125°C
23					5		10		20		40			T_A = –55°C T_B = 25°C
24		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

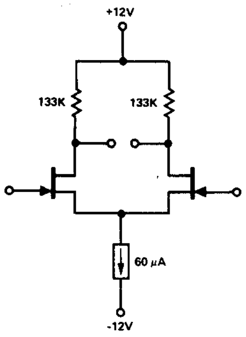
*JEDEC registered data.

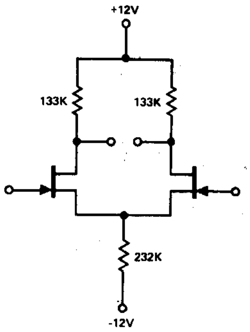
NOTES:

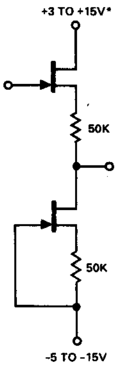
1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

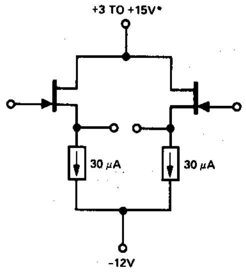
NT

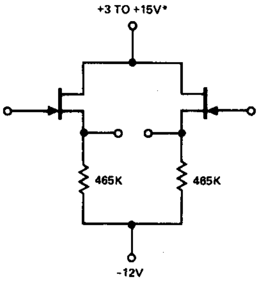
APPLICATIONS

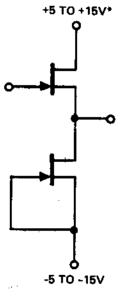












*Use lower voltages for minimum I_G

matched dual n-channel JFETs designed for . . .

■ Wideband Differential Amplifiers

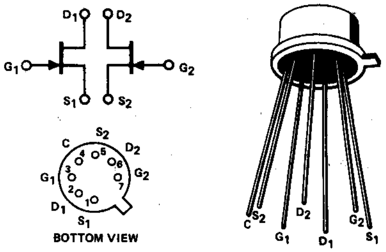
Siliconix

Performance Curves NZF
See Section 5

BENEFITS

- High Gain through 100 MHz
  $g_{fs} > 5000\ \mu mho$
- Matching Characteristics Specified

TO-78
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation, (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					-250	nA		$T_A = 150°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		$V_{DS} = 10$ V, $I_D = 1$ nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4		$V_{DG} = 10$ V, $I_D = 5$ mA	
6		I_G	Gate Operating Current		-100	pA		
					-100	nA		$T_A = 125°C$
7		I_{DSS}	Saturation Drain Current (Note 1)	7	40	mA	$V_{DS} = 10$ V, $V_{GS} = 0$ V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	µmho	$V_{DG} = 10$ V, $I_D = 5$ mA	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
10		g_{os}	Common-Source Output Conductance		100			f = 1 kHz
11		g_{os}	Common-Source Output Conductance		150			f = 100 MHz
12		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
15		NF	Spot Noise Figure		1	dB		f = 10 kHz $R_G = 100K$

			Characteristic	2N5911		2N5912		Unit	Test Conditions	
				Min	Max	Min	Max			
16	MATCHING	$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		20		20	nA	$V_{DG} = 10$ V, $I_D = 5$ mA	$T_A = 125°C$
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	—	$V_{DS} = 10$ V, $V_{GS} = 0$	
18		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		10		15	mV	$V_{DG} = 10$ V, $I_D = 5$ mA	
19		$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		20		40	µV/°C		$T_A = 25°C$ $T_B = 125°C$
20					20		40			$T_A = -55°C$ $T_B = 25°C$
21		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.95	1	0.95	1	—		f = 1 kHz

*JEDEC registered data.

NZF

NOTES:

1. Pulsewidth ≤ 300 µs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

Siliconix

enhancement-type p-channel MOSFETs designed for . . .

Performance Curves MRA
See Section 5

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **Smoke Detectors**
  - **pH Meters**
- **Digital Switching Interfaces**
- **Analog Switching**

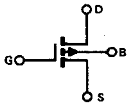
BENEFITS

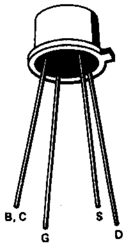
- Rugged MOS Gate Minimizes Handling Problems
  ±150 V Transient Capability
- Low Gate-Leakage
  Typically 0.02 pA
- High Off-Isolation as a Switch
  $I_{DSS} < 200$ pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source or Gate-Source Voltage 3N163	-40 V
Drain-Source or Gate-Source Voltage 3N164	-30 V
Transient Gate-Source Voltage (Note 1)	±150 V
Drain Current	-50 mA
Storage Temperature	-65 to +200°C
Operating Junction Temperature	-55 to +150°C
Total Device Dissipation (Derate 3.0 mW/°C to 150°C)	375 mW
Lead Temperature 1/16" From Case For 10 Seconds	265°C

TO-72
See Section 7





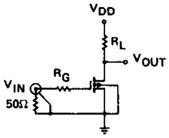
*ELECTRICAL CHARACTERISTICS (25°C and $V_{BS} = 0$ unless otherwise noted)

		Characteristic		3N163 Min	3N163 Max	3N164 Min	3N164 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Body Leakage Current		-10			pA	$V_{GS} = -40$ V, $V_{DS} = 0$	
2					-25					$T_A = 125°C$
3							-10		$V_{GS} = -30$ V, $V_{DS} = 0$	
4							-25			$T_A = 125°C$
5		BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	$I_D = -10\,\mu A$, $V_{GS} = 0$	
6		BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30			$I_S = -10\,\mu A$, $V_{GD} = V_{BD} = 0$	
7		V_{GS}	Gate Source Voltage	-3	-6.5	-2.5	-6.5		$V_{DS} = -15$ V, $I_D = -0.5$ mA	
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2	-5	-2	-5		$V_{DS} = V_{GS}$, $I_D = -10\,\mu A$	
9		I_{DSS}	Drain Cutoff Current		-200		-400	pA	$V_{DS} = -15$ V, $V_{GS} = 0$	
10		I_{SDS}	Source Cutoff Current		-400		-800		$V_{SD} = -20$ V, $V_{GD} = 0$, $V_{DB} = 0$	
11		$I_{D(on)}$	ON Drain Current	-5	-30	-3	-30	mA	$V_{DS} = -15$ V, $V_{GS} = -10$ V	
12		$r_{DS(on)}$	Drain-Source ON Resistance		250		300	Ω	$V_{GS} = -20$ V, $I_D = -100\,\mu A$	
13	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2,000	4,000	1,000	4,000	μmho	$V_{DS} = -15$ V, $I_D = -10$ mA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		250		250			
15		C_{iss}	Common-Source Input Capacitance		2.5		2.5	pF	$V_{DS} = -15$ V, $I_D = -10$ mA	f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		0.7		0.7			
17		C_{oss}	Common-Source Output Capacitance		3		3			
18	SW	$t_{d(on)}$	Turn-ON Delay Time		12		12	ns	$V_{DD} = -15$ V	
19		t_r	Rise Time		24		24		$I_{D(on)} = -10$ mA	
20		t_{off}	Turn-OFF Time		50		50		$R_G = R_L = 1.5\,k\Omega$	

*JEDEC registered data

NOTE:

1. Transient gate-source voltage JEDEC registered as ±125 V.



INPUT PULSE
RISE TIME ⩽ 2 ns
PULSE WIDTH ⩾ 200 ns

SAMPLING SCOPE
$t_r \leqslant 0.2$ ns
$C_{IN} \leqslant 2$ pF
$R_{IN} \geqslant 10\,M\Omega$

MRA

current regulator diodes designed for . . .

Siliconix

Performance Curves
NKL NKM NKO See Section 5

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

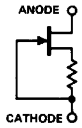
BENEFITS

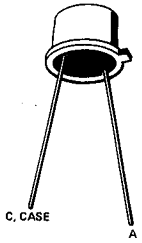
- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
  - Temperature Coefficient Better Than 1500 ppm/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
  - No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	100 V
Forward Current	20 mA
Reverse Current	50 mA
Thermal Resistance θ_{JC}	100°C/W
Power Dissipation at $T_C = 25°C$	1.25 W
Operating Junction Temperature	-55 to +150°C
Storage Temperature	-55 to +200°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

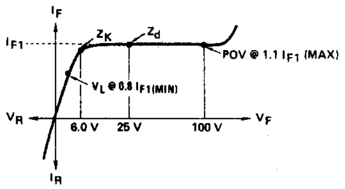
Symbol	I_{F1}			Z_d		Z_k		V_L		POV	θ_1			GEOM
Parameter	Regulator Current			Dynamic Impedance		Knee Impedance		Limiting Voltage		Peak Operating Voltage	Temperature Coefficient			
Test Conditions	$V_F = 25$ V (Note 1)			$V_F = 25$ V (Note 2)		$V_F = 6$ V		$I_F = 0.8\ I_{F1(Min)}$ (Note 3)		$I_F = 1.1\ I_{F1(Max)}$ (Note 4)	$V_F = 25$ V $-55°C < T_A < 25°C$	$V_F = 25$ V $0°C < T_A < 50°C$	$V_F = 25$ V $25°C < T_A < 125°C$	
Units	(mA)			MΩ		MΩ		Volts		Min Volts	Typ ppm/°C	Typ ppm/°C	Typ ppm/°C	
	Nom	Min	Max	Min	Typ	Min	Typ	Max	Typ					
CR022	0.22	0.198	0.242	13.0	16.0	2.75	3.5	1.0	0.40	100	+1350	+1050	+750	NKL
CR024	0.24	0.216	0.264	10.0	14.0	2.35	3.0	1.0	0.45	100	+1200	+900	+600	
CR027	0.27	0.243	0.297	9.0	13.0	1.95	2.8	1.0	0.50	100	+1000	+700	+400	
CR030	0.30	0.270	0.330	8.0	12.0	1.60	2.5	1.0	0.55	100	+800	+500	+200	
CR033	0.33	0.297	0.363	6.6	11.0	1.35	2.2	1.0	0.60	100	+600	+300	-50	
CR039	0.39	0.351	0.429	4.10	9.5	1.00	1.90	1.05	0.70	100	+300	+50	-300	
CR043	0.43	0.387	0.473	3.30	8.6	0.87	1.65	1.05	0.78	100	+150	-150	-450	
CR047	0.47	0.423	0.517	2.70	8.0	0.75	1.50	1.10	0.85	100	-50	-300	-600	
CR056	0.56	0.504	0.616	1.90	6.5	0.56	1.25	1.20	0.98	100	-300	-600	-900	
CR062	0.62	0.558	0.682	1.55	6.2	0.47	1.15	1.30	1.10	100	-500	-800	-1100	
CR068	0.68	0.612	0.748	1.35	8.5	0.400	1.70	1.15	0.70	100	+850	+400	-50	NKM
CR075	0.75	0.675	0.825	1.15	7.2	0.335	1.50	1.20	0.75	100	+650	+200	-250	
CR082	0.82	0.738	0.902	1.00	6.0	0.290	1.30	1.25	0.80	100	+450	+50	-450	
CR091	0.91	0.819	1.001	0.88	5.2	0.240	1.10	1.29	0.85	100	+300	-150	-600	
CR100	1.00	0.900	1.100	0.80	4.4	0.205	0.95	1.35	0.95	100	+150	-300	-750	
CR110	1.10	0.990	1.210	0.70	3.8	0.180	0.80	1.40	1.05	100	+50	-450	-900	
CR120	1.20	1.08	1.32	0.64	3.3	0.155	0.71	1.45	1.15	100	-150	-600	-1050	
CR130	1.30	1.17	1.43	0.58	3.2	0.135	0.60	1.50	1.25	100	-300	-750	-1200	
CR140	1.40	1.26	1.54	0.54	2.5	0.115	0.52	1.55	1.30	100	-400	-850	-1300	
CR150	1.50	1.35	1.65	0.51	2.2	0.105	0.46	1.60	1.35	100	-500	-950	-1400	
CR160	1.60	1.44	1.76	0.475	1.00	0.092	0.35	1.65	0.50	100	+650	+350	+50	NKO
CR180	1.80	1.62	1.98	0.420	0.95	0.074	0.30	1.75	0.55	100	+500	+200	-100	
CR200	2.00	1.80	2.20	0.395	0.88	0.061	0.25	1.85	0.60	100	+350	+50	-250	
CR220	2.20	1.98	2.42	0.370	0.80	0.052	0.22	1.95	0.65	100	+200	-100	-350	
CR240	2.40	2.16	2.64	0.345	0.75	0.044	0.20	2.00	0.70	100	+50	-200	-450	
CR270	2.70	2.43	2.97	0.320	0.68	0.035	0.18	2.15	0.75	100	-100	-300	-550	
CR300	3.00	2.70	3.30	0.300	0.60	0.029	0.14	2.25	0.85	100	-250	-450	-700	
CR330	3.30	2.97	3.63	0.280	0.56	0.024	0.13	2.35	0.90	100	-400	-600	-800	
CR360	3.60	3.24	3.96	0.265	0.52	0.020	0.11	2.50	0.95	100	-560	-750	-900	
CR390	3.90	3.51	4.29	0.255	0.48	0.017	0.10	2.60	1.00	100	-700	-850	-1000	
CR430	4.30	3.87	4.73	0.245	0.45	0.014	0.09	2.75	1.10	100	-850	-950	-1100	
CR470	4.70	4.23	5.17	0.235	0.40	0.012	0.08	2.90	1.40	100	-1000	-1100	-1200	

NOTES:

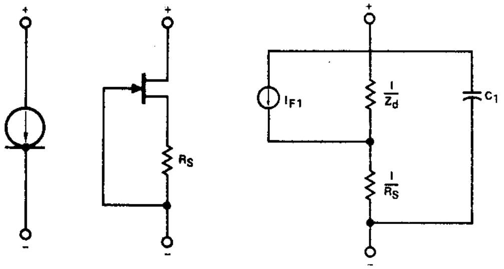
1. Pulse test — steady state currents may vary.
2. Pulse test — steady state impedances may vary.
3. Min V_F required to insure $I_F > 0.8\ I_{F1(min)}$.
4. Max V_F where $I_F < 1.1\ I_{F1(max)}$ is guaranteed.

NKL, NKM, NKO

Current-Limiter Diode V-I Characteristic



EQUIVALENT CIRCUIT



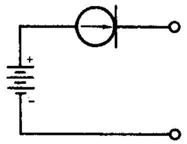
SYMBOLS AND DEFINITIONS

A	Anode (Drain)
C	Cathode (Source and Gate Shorted)
I_F	Forward Current (Anode Positive)
I_{F1}	Current at a specified Test Voltage, V_F
POV	Peak Operating Voltage
θ_I	Current Temperature Coefficient
θ_{JC}	Thermal Resistance Junction to Case
θ_{JA}	Thermal Resistance Junction to Ambient
Z_K	Knee AC Impedance at specified V_F. Z_K should be as high as possible and is specified as a minimum.
Z_d	Dynamic Impedance at specified V_F. Z_d is specified as a minimum.

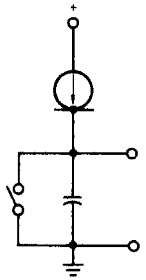
APPLICATIONS

The current-limiter diode is the electrical dual of the Zener diode.

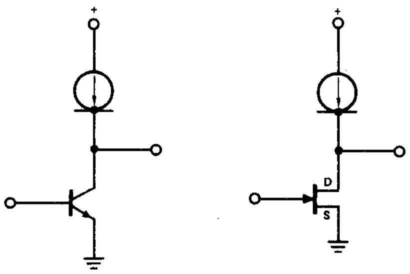
Constant-Current Supply
or Current-Limiting Element



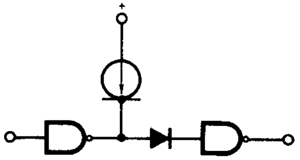
Constant-Current
Timing Circuits



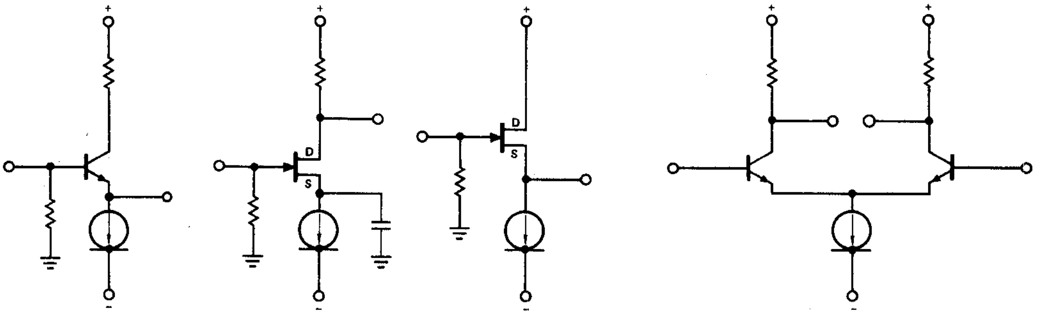
Collector or Drain
Hi-Z Load Resistors



Logic Circuit Pull-Up
Current Source



Emitter or Source Biasing



Siliconix

enhancement-type p-channel MOSFET designed for . . .

Performance Curves MRA
See Section 5

■ High-Input Impedance Amplifiers

Smoke Detectors
Electrometers
pH Meters

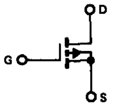
BENEFITS

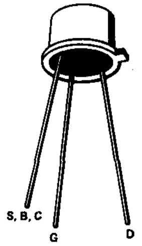
- High Input Impedance
  I_{GSS} = 30 Femto Amp Typical
- High Gain
  g_{fs} = 1000 μmho Minimum

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Gate-Source Voltage	±10 V
Drain Current	30 mA
Total Device Dissipation at (Or Below) T_A = 25°C (Derate 3 mW/°C to +150°C)	375 mW
Operating Junction Temperature	−55 to +150°C
Storage Temperature	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	265°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C)

			Characteristic	Min	Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate-Source Leakage Current		−1.0	pA	V_{GS} = −10 V, V_{DS} = 0
2		BV_{DSS}	Drain-Source Breakdown Voltage	−25		V	I_D = −10 μA, V_{GS} = 0
3		V_{GS}	Gate-Source Voltage	−2.0	−6.0	V	V_{DS} = −10 V, I_D = −10 μA
4		I_{DSS}	Drain Cutoff Current		−20	nA	V_{DS} = −10 V, V_{GS} = 0
5		$I_{D(on)}$	ON Drain Current	−3.0		mA	V_{DS} = −10 V, V_{GS} = −10 V
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		μmhos	V_{DS} = −10 V, I_D = −2 mA, f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		6.0	pF	V_{DS} = −10 V, V_{GS} = −10 V, f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		

MRA

dual pico ampere diodes

Siliconix

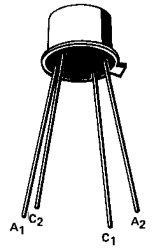
designed for . . .

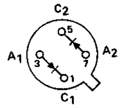
- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS

- Very High Off-Isolation
  1 pA Max (DPAD1)
- High Isolation Between Diodes
  20 Femto Amp Typical (DPAD1)
- Matched Capacitances
- Compact Packaging

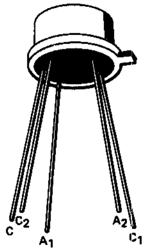
TO-71
(Pins 2 and 6 Removed)
See Section 7

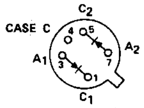




BOTTOM VIEW
(ALTERNATE)

TO-78
(DPAD1 Only)
See Section 7





BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (25°C)

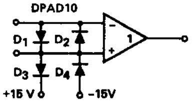
Forward Gate Current, Each Side	50 mA
Total Device Dissipation @ T_A = 25°C Derate 4.0 mW/°C to 125°C	400 mW
Storage Temperature Range	−55 to +125°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

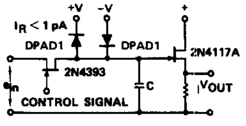
		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION	
1	STATIC	I_R	Reverse Current			-1	pA	V_R = −20 V	DPAD1
2						-2			DPAD2
3						-5			DPAD5
4						-10			DPAD10
5						-20			DPAD20
6						-50			DPAD50
7						-100			DPAD100
8		B_{VR}	Reverse Breakdown Voltage	-45		-120	V	I_R = −1 μA	DPAD1, 2, 5
9				-35					DPAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		I_F = 1 mA	DPAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R	Capacitance			0.8	pF	V_R = −5 V, f = 1 MHz	DPAD1, 2, 5
12						2.0			DPAD10, 20, 50, 100
13	MAT	$\lvert C_{R1}-C_{R2}\rvert$	Differential Capacitance		0.1	0.2	pF	$V_{R1} = V_{R2}$ = −5 V, f = 1 MHz	DPAD1, 2, 5, 10, 20, 50, 100

APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by DPADS D_1 and D_2 Common mode input voltage limited by DPADS D_3 and D_4 to ±15 V.



Typical sample and hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the FET switch gate.



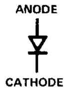
low-leakage pico-amp diodes *designed for . . .*

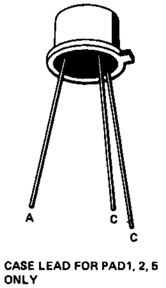
- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS

- Very High Off-Isolation
  1 pA Max (PAD1)

TO-18
See Section 7





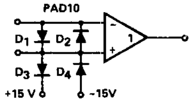
CASE LEAD FOR PAD1, 2, 5 ONLY

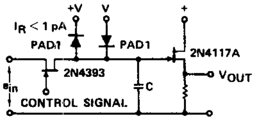
ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current	50 mA
Total Device Dissipation	300 mW
Storage Temperature Range	-55°C to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_R	Reverse Current			-1	pA	V_R = -20 V	PAD1
2						-2			2
3						-5			5
4						-10			PAD10
5						-20			20
6						-50			50
7						-100			PAD100
8		BV_R	Breakdown Voltage (Reverse)	-45		-120	V	I_R = -1 μA	PAD1, 2, 5
9				-35					PAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		I_F = 5 mA	PAD1, 2, 5, 10, 20, 50, 100
11	DYN	$\|C_R\|$	Capacitance			0.8	pF	V_R = -5 V, f = 1 MHz	PAD1, 2, 5
12						2			PAD10, 20, 50, 100





APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by PADS D_1 and D_2 Common mode input voltage limited by PADS D_3 and D_4 to ±15 V.

Typical sample and hold circuit with clipping. PAD diodes reduce offset voltages fed capacitively from the FET switch gate.

n-channel JFETs designed for . . .

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NC
See Section 5

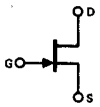
BENEFITS

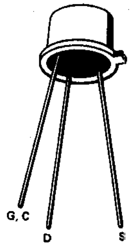
- Low Insertion Loss
  $R_{DS(on)} < 50\ \Omega$ (U202)
- Good Off-Isolation
  $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-30 V
Gate Current	50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C)	1.8 W
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U200		U201		U202		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2					-1		-1		-1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		$V_{DS} = 20$ V, $I_D = 10$ nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	$V_{DS} = 10$ V, $V_{GS} = -12$ V	
					1		1		1	µA		150°C
6		I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
7	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		8		8		8		$V_{DS} = 0$, $V_{GS} = -12$ V	

NOTE:

1. Pulse test required, pulsewidth = 300 µsec, duty cycle ⩽ 3%.

NC

Siliconix

monolithic dual n-channel JFETs *designed for . . .*

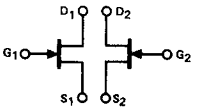
■ Differential Amplifiers

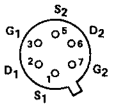
Performance Curves NNP
See Section 5

BENEFITS

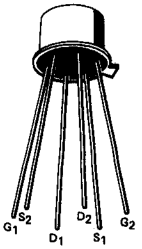
- Good Matching Characteristics

TO-71
See Section 7





BOTTOM VIEW



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-50 V
Gate Current	50 mA
Total Device Dissipation at 25°C (Derate 1.7 mW/°C to 200°C)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	$V_{GS} = -30\ V, V_{DS} = 0$	
2					-500	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	$I_G = -1\ \mu A, V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		$V_{DS} = 20\ V, I_D = 1\ nA$	
5		V_{GS}	Gate-Source Voltage	-0.3	-4.0		$V_{DG} = 20\ V, I_D = 200\ \mu A$	
6		I_G	Gate Operating Current		-50	pA		
					-250	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	5.0	mA	$V_{DS} = 20\ V, V_{GS} = 0$	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	3000	μmho	$V_{DS} = 20\ V, V_{GS} = 0$	f = 1 kHz
				1000				f = 100 MHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		$V_{DG} = 20\ V, I_D = 200\ \mu A$	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35		$V_{DS} = 20\ V, V_{GS} = 0$	
11		g_{os}	Common-Source Output Conductance		10		$V_{DG} = 20\ V, I_D = 200\ \mu A$	
12		C_{iss}	Common-Source Input Capacitance		6	pF	$V_{DS} = 20\ V, V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

		Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current	10	10	10	10	10	nA	$V_{DG} = 20\ V, I_D = 200\ \mu A$	125°C
16		$\frac{(I_{DSS1} - I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	$V_{DS} = 20\ V, V_{GS} = 0$	
17		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage	5	10	15	20	25	mV	$V_{DG} = 20\ V, I_D = 200\ \mu A$	
18		$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	μV/°C		$T_A = 25°C$ $T_B = 125°C$
19				10	25	50	75	100			$T_A = -55°C$ $T_B = 25°C$
20		$\frac{(g_{fs1} - g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 1)	3	5	5	10	15	%		f = 1 kHz
21		$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance	5	5	5	5	5	μmho		

NOTES:

1. Pulse test required, pulsewidth = 300 μs, duty cycle ⩽ 3%.
2. Measured at end points, T_A and T_B.

NNP
NP-D

matched dual n-channel JFET designed for . . .

- **Wideband Differential Amplifiers**

Performance Curves NZF
See Section 5

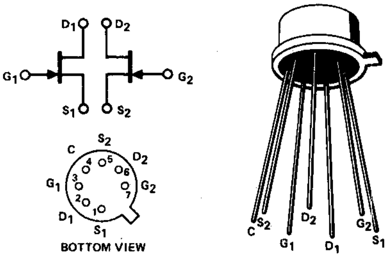
BENEFITS

- High Gain through 100 MHz
  g_{fs} = 5000 µmho Minimum
- Matching Characteristics Specified

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C (Derate 3.85 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C (Derate 7.7 mW/°C)	500 mW
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-78
See Section 7



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	µmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{fs}	Common-Source Forward Transconductance	5000	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
8		g_{os}	Common-Source Output Conductance		150		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		150		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
10		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
13	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
14		$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
15		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.85	1			f = 1 kHz
16		$\lvert g_{os1}-g_{os2} \rvert$	Differential Output Conductance		20	µmho		

NOTES:
1. Pulse test required, pulse width = 300 µs, duty cycle ≤ 30%.
2. Assumes smaller value in numerator.

NZF

n-channel JFETs designed for . . .

Siliconix

U290 U291

- **Analog Switches**
- **Commutators**
- **Choppers**

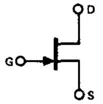
Performance Curves NVA
See Section 5

BENEFITS

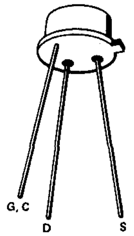
- Ultra-Low Insertion Loss
  $R_{DS(on)} < 2.5\ \Omega$ (U290)
- High Off-Isolation
  $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	-30 V
Gate Current	100 mA
Drain Current	1.5 A
Total Device Dissipation at 25°C Free-Air Temperature (Note 1)	500 mW
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



TO-52
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U290 Min	U290 Max	U291 Min	U291 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					-1		-1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-1.5	-4.5		$V_{DS} = 15$ V, $I_D = 3$ nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6					1		1	µA		150°C
7		$V_{DS(on)}$	Drain-Source ON Voltage		25		70	mV	$V_{GS} = 0$, $I_D = 10$ mA	
8		I_{DSS}	Saturation Drain Current (Note 2)	500		200		mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance	1.0	2.5	2	7	Ω	$V_{GS} = 0$ V, $I_D = 10$ mA	
10	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance	1.0	2.5	2	7	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
11		C_{SGO}	Source-Gate OFF Capacitance		30		30	pF	$V_{SG} = 15$ V, $I_D = 0$	f = 1 MHz
12		C_{DGO}	Drain-Gate OFF Capacitance		30		30		$V_{DG} = 15$ V, $I_S = 0$	
13		$C_{SG}+C_{DG}$	Source Gate Plus Drain Gate On Capacitance		160		160		$V_{DS} = 0$, $V_{GS} = 0$	
14	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = 1.5$ V, $I_{D(on)} = 30$ mA, $R_L = 50\ \Omega$, $V_{GS(on)} = 0$ V, $V_{GS(off)} = -12$ V (U290) $V_{GS(off)} = -7$ V (U291)	
15		t_r	Rise Time		20		20			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		15			
17		t_f	Fall Time		20		20			

NOTES:

NVA

1. Derate linearly at the rate of 4.0 mW/°C.
2. Pulse test required pulsewidth 300 µs, duty cycle ≤ 3%.

p-channel JFETs designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves PS
See Section 5

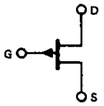
BENEFITS

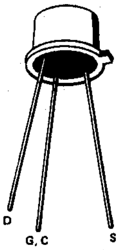
- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (U304)
- High Off-Isolation
  $I_{D(off)} < 500$ pA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	50 mA
Total Device Dissipation, Free-Air (Derate 2.8 mW/°C)	350 mW
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 60 seconds)	300°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		500		500		500	pA	$V_{GS} = 20$ V, $V_{DS} = 0$	
2					1.0		1.0		1.0	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	$I_G = 1\ \mu$A, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4		$V_{DS} = -15$ V, $I_D = -1\ \mu$A	
5		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		$V_{GS} = 0$, $I_D = -15$ mA (U304), $I_D = -7$ mA (U305), $I_D = -3$ mA (U306)	
6		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	$V_{DS} = -15$ V, $V_{GS} = 0$	
7		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	$V_{DS} = -15$ V, $V_{GS} = 12$ V (U304), $V_{GS} = 7$ V (U305), $V_{GS} = 5$ V (U306)	
8					-1.0		-1.0		-1.0	μA		150°C
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	$V_{GS} = 0$ V, $I_D = -1$ mA	
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	$V_{GS} = 0$ V, $I_D = 0$	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		27		27		27	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		$V_{DS} = 0$, $V_{GS} = 12$ V (U304) $V_{GS} = 7$ V (U305), $V_{GS} = 5$ V (U306)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		20		25		25	ns		
14		t_r	Rise Time		15		25		35			
15		$t_{d(off)}$	Turn-OFF Delay Time		10		15		20			
16		t_f	Fall Time		25		40		60			

	U304	U305	U306
V_{DD}	-10 V	-6 V	-6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15 mA	-7 mA	-3 mA

PS

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

n-channel JFETs designed for . . .

Siliconix

- **VHF Amplifiers**
- **Front End High Sensitivity Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA
See Section 5

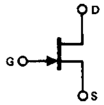
BENEFITS

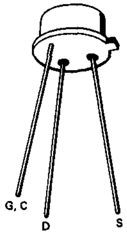
- Industry Standard
- High Power Gain
  16 dB at 105 MHz, Common-Gate
  11 dB at 450 MHz, Common-Gate
- Low Noise
  2.7 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- 75 Ω Input Match Common Gate

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -25 V
Gate Current . . . . 20 mA
Total Power Dissipation at T_A = 25°C . . . . 500 mW
Power Derating to 150°C . . . . 4.0 mW/°C
Storage Temperature Range. . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . 300°C

TO-52
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U308			U309			U310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current			–150			–150			–150	pA	V_{GS} = –15 V, V_{GS} = 0	
2						–150			–150			–150	nA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0		–6.0	–1.0		–4.0	–2.5		–6.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
7	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance			200			200			200	μmho		
9		C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = –10 V, V_{DS} = 10 V	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
11		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fg}	Common-Gate Forward Transconductance		15			15			15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
13					14			14			14				f = 450 MHz
14		g_{og}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 105 MHz
15					0.32			0.32			0.32				f = 450 MHz
16		G_{pg}	Common-Gate Power Gain (Note 2)	14	16		14	16		14	16		dB		f = 105 MHz
17				10	11		10	11		10	11				f = 450 MHz
18		NF	Noise Figure		1.5	2.0		1.5	2.0		1.5	2.0			f = 105 MHz
19					2.7	3.5		2.7	3.5		2.7	3.5			f = 450 MHz

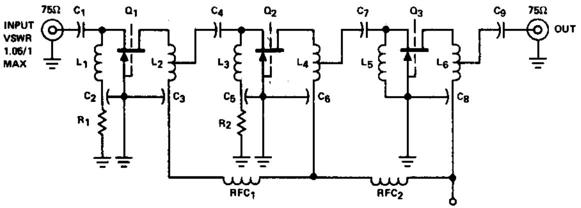
NOTES:

1. Pulse test duration = 2 ms.
2. Gain (G_{pg}) measured at optimum input noise match.

NZA

APPLICATIONS

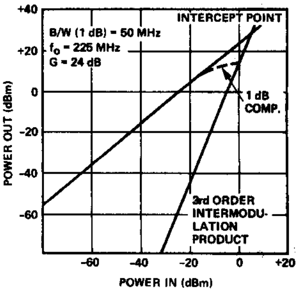
200-250 MHz Wideband Amplifer (1 dB Ripple) 3-Stage Amplifier Circuit



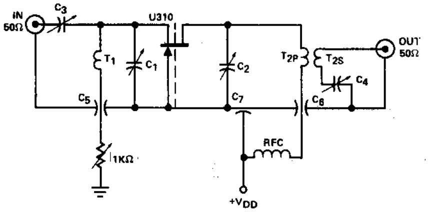
C_1, C_4, C_7, C_9 = 68 pF
C_2, C_5 = 500 pF
C_3, C_6, C_8 = 1,000 pF
Q_1, Q_2, Q_3 = Siliconix U310

L_1, L_3, L_5 = 120 nHy
L_2, L_4, L_6 = 222 nHy
RFC_1, RFC_2 = 2.2 μHy
R_1, R_2 = 51 Ω

2 Tone Intercept & Compression Point Measurement



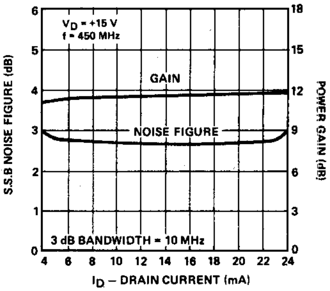
450 MHz Common Gate Amplifier



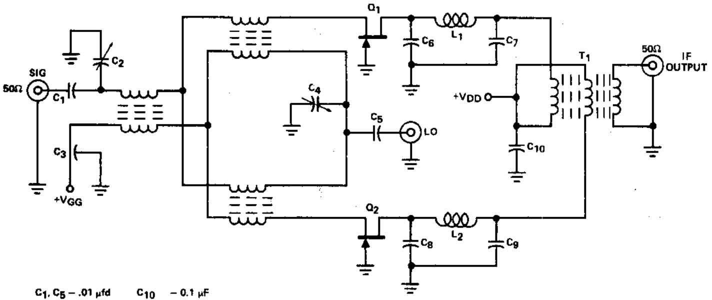
C_1, C_2 – 0.8–10 pF JFD model MVM 010W
C_3, C_4 – 8–35 pF Erie series 539-002D
C_5, C_6 – 5000 pF Erie (2443-000)
C_7 – 1000 pF ALLEN-BRADLEY type FA5C

RFC – .33 μH MILLER type (9230-30)
T_1 – one turn, #16 copper wire, ¼" I.D. (Air Core)
T_{2P} – one turn, #16 copper wire, ¼" I.D. (Air Core)
T_{2S} – one turn, #16 copper wire, ¼" I.D. (Air Core)

Noise Figure vs. Power Gain



Prototype Active Balanced Mixer*



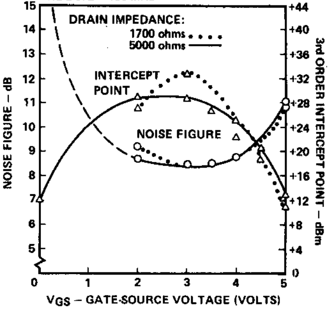
C_1, C_5 – .01 μfd
C_2, C_4 – 1-10 pF
C_3 – 1000 pF
C_6, C_8 – 30 pF
C_7, C_9 – 68 pF

C_{10} – 0.1 μF
L_1, L_2 – 1.3 μhy
Q_1, Q_2 – U310
T_1 – RELCOM BT-9

*Reference Siliconix Application Note AN71-2.

Comparison of Mixer IM Characteristics

SOURCE INJECTED MIXER (L.O. & SIGNAL)
FREQ LO = 120 MHz; POWER LO: +17 dBm
FREQ SIG = 150 MHz



n-channel JFET designed for . . .

Siliconix

- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA
See Section 5

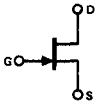
BENEFITS

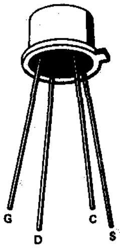
- High Power Gain
  16 dB Typ @ 105 MHz, Common-Gate
  11 dB Typ @ 450 MHz, Common-Gate
- Low Noise Figure
  1.5 dB Typ @ 105 MHz
  2.7 dB Typ @ 450 MHz
- Wide Dynamic Range—Greater than 100 dB

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	10 mA
Total Device Dissipation (Derate 1.7 mW/°C)	300 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-150	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					-150	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	$I_G = -1$ μA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6		$V_{DS} = 10$ V, $I_D = 1$ nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	20	60	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		1	V	$I_G = 1$ mA, $V_{DS} = 0$	
7	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10,000	20,000	μmho	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance		200			
9		C_{gd}	Gate-Drain Capacitance		2.5	pF	$V_{DG} = 10$ V, $I_D = 5$ mA	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance		5.0			

NZA

NOTE:
1. Pulse test duration = 2 ms.

n-channel JFET designed for . . .

- **VHF/UHF Common-Gate Amplifiers**
- **Mixers**

Siliconix

Performance Curves NZF
See Section 5

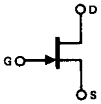
BENEFITS

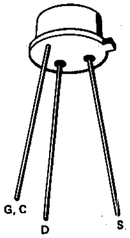
- High Power Gain
  10 dB Typical at 450 MHz, Common Gate
- Low Noise
  NF = 3.5 dB Typical at 450 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -25 V
Gate Current . . . . 10 mA
Total Power Dissipation at or below 25°C
  Free-Air Temperature . . . . 500 mW
Power Derating . . . . 4.0 mW/°C
Operating Temperature Range . . . . -65 to +150°C
Storage Temperature Range . . . . -65 to +150°C
Lead Temperature
  (1/16" from case for 10 seconds) . . . . .300°C

TO-52
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-0.1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6	V	V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	10	30	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	6000	10,000	μmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
7		g_{og}	Common-Gate Output Conductance		200	μmho		
8		C_{gd}	Gate-Drain Capacitance		1.2	pF	V_{DG} = 10 V, I_D = 10 mA	f = 1 MHz
9		C_{gs}	Gate-Source Capacitance		3.8	pF		

NOTE:
1. Pulse test duration = 2 ms.

NZF

n-channel JFETs designed for . . .

■ VHF Buffer Amplifiers
■ IF Amplifiers

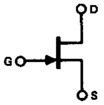
Siliconix

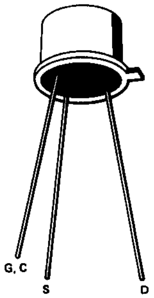
Performance Curves NIP
See Section 5

BENEFITS

- High Gain
  g_{fs} = 120,000 μmho Typical
- Wide Dynamic Range
- Low Intermodulation Distortion

TO-39
See Section 7





ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	100 mA
Total Device Dissipation (25°C Case Temperature)	3 W
Power Derating (to 150°C)	24 mW/°C
Storage Temperature Range	−55 to +150°C
Operating Temperature Range	−55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

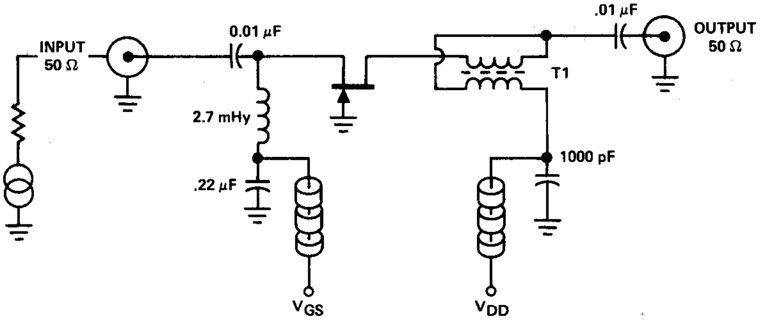
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U320			U321			U322			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{GS} = −15 V, V_{DS} = 0 V	
2						-0.5			-0.5			-0.5	μA		T = 100°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2		-10	-1		-4	-3		-10	V	V_{DS} = 5 V, I_D = 1 mA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				I_G = −1 μA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	100		500	80		250	200		700	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1			1			1	V	I_G = 1 mA, V_{DS} = 0 V	
7		$r_{DS(on)}$	Drain-Source ON Resistance			10			11			8	Ω	V_{GS} = 0 V, I_D = 10 mA	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	75	120	200	75	120	200	75	130	200	mmhos	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance			30			30			30	pF	V_{GS} = −10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance			15			15			15			
11		C_{gs}	Gate-Source Capacitance		12			12			12			V_{GS} = −10 V, I_D = 0	
12		C_{gd}	Gate-Drain Capacitance		12			12			12			V_{GD} = −10 V, I_S = 0	
13		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		2			2			2		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 5 V, I_D = 10 mA	f = 1 kHz
14	HIGH FREQ	g_{fg}	Common Gate Forward Transconductance		55			55			55		mmho	V_{DG} = 20 V, I_D = 25 mA	f = 50 MHz
15		g_{ig}	Commen-Gate Input Conductance		56			56			56				
16		g_{og}	Common-Gate Output Conductance		0.5			0.5			0.5				
17		G_{PS}	Power Gain (Note 3)		9			9			9		dB		
18		F_t	Gain-Bandwidth (Note 4)		400			400			400		MHz	V_{DS} = 15 V, V_{GS} = 0 V	
19		NF	Noise Figure (Note 3)		2.5			2.5			2.5		dB	V_{DG} = 20 V, I_D = 25 mA	f = 30 MHz

NOTES:

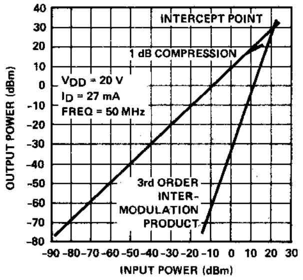
NIP

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.
3. Noise figure (SSB) and power gain measured in circuit shown in Figure 1.
4. Computed as g_{fs}/C_{rss}.



T1–6 TURNS #22 AWG TWISTED PAIR WIRE ON 0.375 INCH DIAMETER INDIANA GENERAL F625-9Q2 TOROID CORE.

50 MHz Power Gain and Noise Figure Test Circuit for U320, U321 and U322
Figure 1



Gain – Intermodulation Characteristics
Figure 2

monolithic dual n-channel JFETs *designed for . . .*

- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Siliconix

Performance Curves NNR See Section 5

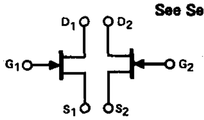
BENEFITS

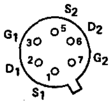
- Minimum System Error and Calibration
  - 5 mV Offset Maximum (U401)
  - 95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature
  - 10 µV/°C Maximum (U401, 02)
- Operates from Low Power Supply Voltages
  - $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  - Output Conductance < 2 µmho
- Low Noise
  - $\overline{e}_n = 6\ nV/\sqrt{Hz}$ at 10 Hz Typical

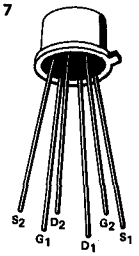
ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side)	
@ T_A = 85°C derate 2.6 mW/°C	300 mW
Total Device Dissipation	
@ T_A = 85°C (derate 5 mW/°C)	500 mW
Storage Temperature Range	–65 to 200°C

TO-71
See Section 7







ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

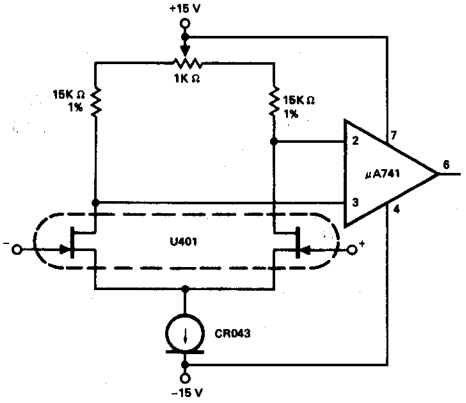
		Characteristic		U401 Min	U401 Max	U402 Min	U402 Max	U403 Min	U403 Max	U404 Min	U404 Max	U405 Min	U405 Max	U406 Min	U406 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–50		–50		–50		–50		–50		–50		V	V_{DS} = 0, I_G = –1 µA	
2		I_{GSS}	Gate Reverse Current (Note 1)		–25		–25		–25		–25		–25		–25	pA	V_{DS} = 0, V_{GS} = –30 V	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–.5	–2.5	–.5	–2.5	–.5	–2.5	–.5	–2.5	–.5	–2.5	–.5	–2.5	V	V_{DS} = 15 V, I_D = 1 nA	
4		$V_{GS(on)}$	Gate-Source Voltage (on)		–2.3		–2.3		–2.3		–2.3		–2.3		–2.3		V_{DG} = 15 V, I_D = 200 µA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6		I_G	Gate Current (Note 1)		–15		–15		–15		–15		–15		–15	pA	V_{DG} = 15 V, I_D = 200 µA	
7					–10		–10		–10		–10		–10		–10	nA		T_A = 125°C
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 µA	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	µmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
11		g_{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600		V_{DG} = 15 V, I_D = 200 µA	f = 1 kHz
12		g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
13		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
15		$\overline{e}_N$	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 µA	
17		$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 µA	
18		$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4).		10		10		25		25		40		80	µV/°C	V_{DG} = 10 V, I_D = 200 µA	T_A = –55°C, T_B = +25°C T_C = +125°C

NOTES:
1. Approximately doubles for every 10°C increase in T_A. 2. Pulse test duration = 300 µs; duty cycle ≤ 3%. 3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.
4. Measured at end points, T_A, T_B and T_C.

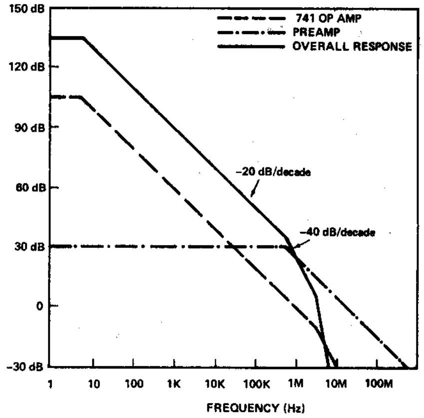
NNR
NRL-D

APPLICATIONS

General Purpose FET Input Op Amp



Open Loop Gain and Frequency Response of Op Amp



Typical Specs for General Purpose FET Input Op Amp*

Common Mode Range	+6.7 to -8.8 Volts
Worst Case Drift Referred to the Input	≈ 12 µV/°C
Broad Band Noise Referred to the Input (0.1 to 1 kHz)	≈ 188 nV/Rms
Gain and Bandwidth	(see graph)

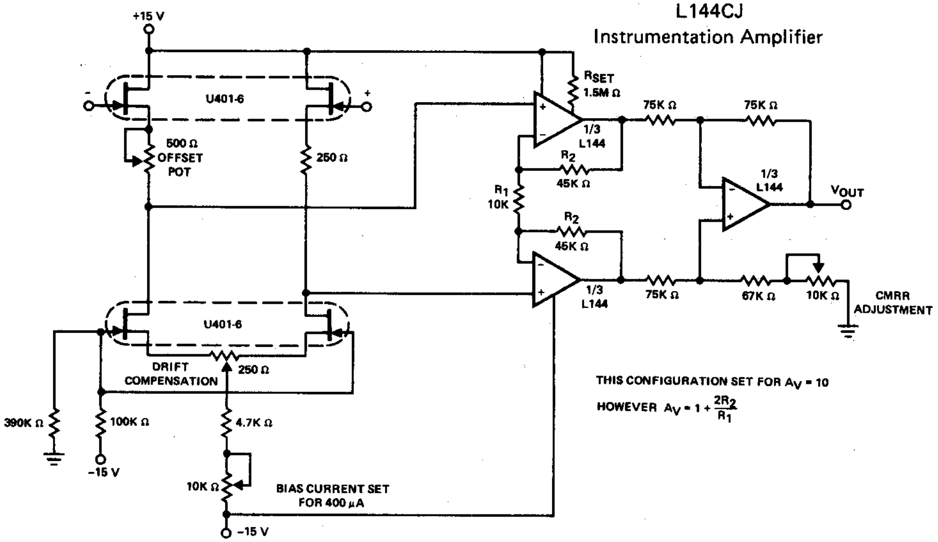
*These specs depend upon the specifications of the Operational amplifier IC used.

For futher design information, write for:

DESIGNING FET-INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included. (16 pages).

FET Input Instrumentation Amplifier



THIS CONFIGURATION SET FOR $A_V = 10$

HOWEVER $A_V = 1 + \frac{2R_2}{R_1}$

monolithic dual n-channel JFETs designed for . . .

Siliconix

- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NQP See Section 5

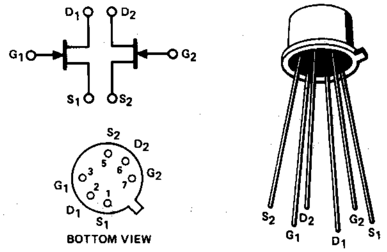
BENEFITS

- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (U410)
  70 dB Minimum CMRR (U410)
- Low Drift with Temperature
  10 µV/°C Maximum (U410)
- Simplifies Amplifier Design
  Low Output Conductance

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	50 mA
Total Package Dissipation (25°C Free-Air)	375 mW
Power Derating	3.0 mW/°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (1/16″ from case for 10 seconds)	300°C

TO-71
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U410			U411			U412			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			−200			−200			−200	pA	$V_{DS} = 0, V_{GS} = -30$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0		−3.5	−1.0		−3.5	−1.0		−3.5	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	−40			−40			−40				$V_{DS} = 0$ V, $I_G = -1$ µA	
4		I_{DSS}	Saturation Drain Current (Note 2)	0.5		5.0	0.5		5.0	0.5		5.0	mA	$V_{DS} = 20$ V, $V_{GS} = 0$ V	
5		I_G	Gate Current (Note 1)			−200			−200			−200	pA	$V_{DG} = 20$ V, $I_D = 200$ µA	
6		V_{GS}	Gate-Source Voltage	−0.2		−3.0	−0.2		−3.0	−0.2		−3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	µmho	$V_{DS} = 20$ V, $V_{GS} = 0$ V	f = 1 kHz
8				600		1,200	600		1,200	600		1,200		$V_{DG} = 20$ V, $I_D = 200$ µA	
9		g_{os}	Common-Source Output Conductance			20			20			20		$V_{DS} = 20$ V, $V_{GS} = 0$ V	
10						5			5			5		$V_{DG} = 20$ V, $I_D = 200$ µA	
11		C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	$V_{DS} = 20$ V, $V_{GS} = 0$ V	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2				
13		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			50			50			50	$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 20$ V, $I_D = 200$ µA	f = 100 H
14	MATCHING	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage			10			20			40	mV	$V_{DG} = 20$ V, $I_D = 200$ µA	
15		$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	µV/°C	$V_{DG} = 20$ V, $I_D = 200$ µA $T_A = 25$°C to $T_B = 85$°C	
16		CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	$V_{DD} = 10$ V to $V_{DD} = 20$ V $I_D = 200$ µA	

NOTES:

NQP

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 µsec; duty cycle ⩽ 3%.
3. Measured at end points, T_A and T_B.
4. $\text{CMRR} = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta \lvert V_{GS1} - V_{GS2} \rvert}\right], \Delta V_{DD} = 10\text{ V}.$

monolithic dual n-channel JFETs designed for . . .

- **Very High Input Impedance Differential Amplifiers**
  Electrometers
- **Impedance Converters**

Performance Curves NQT
See Section 5

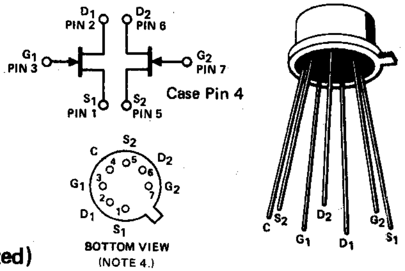
BENEFITS

- High Input Impedance
  I_G = 0.1 pA Maximum (U421-3)
- High Gain g_{fs} = 140 µmho Minimum @ I_D = 30 µA (U421-3)
- Low Power Supply Operation
  $V_{GS(off)}$ = 2 V Maximum (U421-3)
- Minimum System Error and Calibration
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

ABSOLUTE MAXIMUM RATINGS (25° C)

Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25° C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25° C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	−65 to +150° C

TO-78
See Section 7



ELECTRICAL CHARACTERISTICS (25° C unless otherwise noted)

		Characteristic		U421-3 Min	U421-3 Typ	U421-3 Max	U424-6 Min	U424-6 Typ	U424-6 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	I_G = −1 µA, V_{DS} = 0	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40				I_G = −1 µA, I_D = 0, I_S = 0	
3		I_{GSS}	Gate Reverse Current (Note 1)			0.2			1.0	pA	T = +25°C	V_{GS} = −20 V, V_{DS} = 0
						0.5			1.0	nA	T = +125°C	
4		I_G	Gate Operating Current (Note 1)			0.1			0.5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 µA
						−100			−500		T = +125°C	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4		−2.0	−0.4		−3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6		V_{GS}	Gate-Source Voltage			−1.8			−2.9		V_{DG} = 10 V, I_D = 30 µA	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	µA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1000	µ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3.0			5.0			
10		C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
12		g_{fs}	Common-Source Forward Transconductance	140		250	135		300	µ℧	V_{DG} = 10 V, I_D = 30 µA	f = 1 kHz
13		g_{os}	Common-Source Output Conductance			0.5			1.0			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	$nV/\sqrt{Hz}$		f = 10 Hz
					10			10	50			f = 1 kHz
15		NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10M Ω

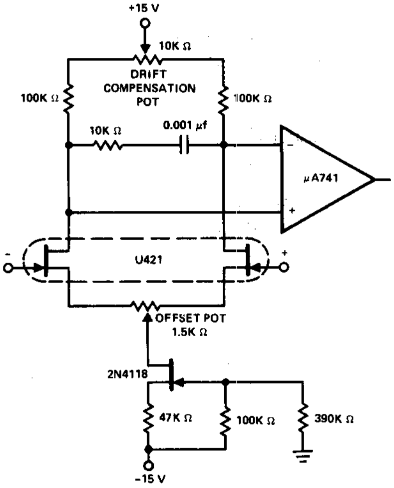
		Characteristic		U421, 4 Min	U421, 4 Typ	U421, 4 Max	U422, 5 Min	U422, 5 Typ	U422, 5 Max	U423,6 Min	U423,6 Typ	U423,6 Max	Unit	Test Conditions
16	MATCH	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage			10			15			25	mV	V_{DG} = 10 V, I_D = 30 µA
17		$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	µV/°C	V_{DG} = 10 V, I_D = 30 µA, T_A = −55°C, T_B = 25°C, T_C = 125°C
18		CMRR	Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	I_D = 30 µA, V_{DG} = 10 to 20 V

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta \lvert V_{GS1} - V_{GS2} \rvert}\right]$ ΔV_{DD} = 10 V.
4. Case lead not connected.

NQT

APPLICATIONS

Very Low Leakage FET Input Op Amps



I_G = 0.1 pA at V_{cm} = 0
Offset = Can be nulled to 0 volts
Drift = Can be nulled to 2 μV/°C
Slew Rate = 0.5 V/μs

NOTE: Pin 4 (case) is isolated from the substrate and should be left floating.

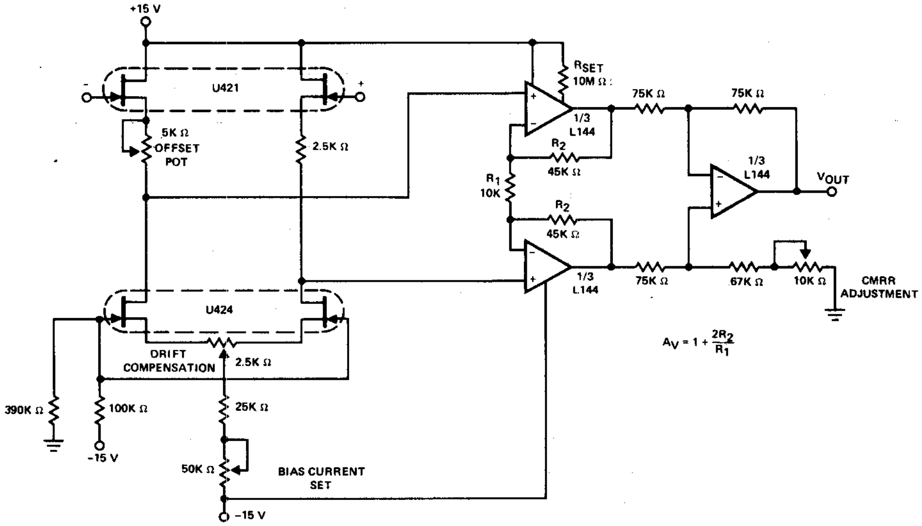
For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

Electrometer Amplifier

L144CJ
Instrumentation Amplifier



Voltage Gain = 10
Input Current = 0.1 pA
Compensated Drift = 3 μV/°C
Nulled Offset = 0 mV
CMRR = 80 dB typical
Power Consumption = Approx. 30 Volt x 120 μA = 3.6 mW

matched dual n-channel JFETs designed for . . .

Siliconix

- **Balanced Mixers**
- **Differential Amplifiers**

Performance Curves NZA
See Section 5

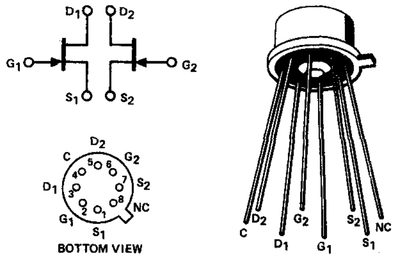
BENEFITS

- Low Noise Figure
- Low IMD
  30 dBm Intercept Point

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -25 V
Gate Current . . . . 10 mA
Total Continuous Power Dissipation at
(or Below) 25°C Free Air Temperature
Derate 4 mW/°C to 150°C. . . . . 500 mW
Continuous Device Dissipation (Each Side) at
(or Below) 25°C Free Air Temperature
Derate 2.4 mW/°C to 150°C . . . . 300 mW
Storage Temperature Range. . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . 300°C

TO-99
See Section 7



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		U430 Min	U430 Typ	U430 Max	U431 Min	U431 Typ	U431 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-150			-150	pA	V_{GS} = -15 V, V_{DS} = 0 V	
2						-150			-150	nA		T = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			V	I_G = -1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-4.0	-2.0		-6.0		V_{DS} = 10 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0		V_{DS} = 0 V, I_G = 10 mA	
6		I_{DSS}	Saturation Drain Current (Note 4)	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0 V	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10		20	10		20	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			200			200	μmho		
9		C_{gs}	Gate-Source Capacitance			5.0			5.0	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{gd}	Drain Gate Capacitance			2.5			2.5			
11		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fs}	Common-Source Forward Transconductance		12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
13		g_{os}	Common-Source Output Conductance		0.15			0.15				
14		g_{ig}	Power-Match Source Admittance		12			12				
15		G_c	Conversion Gain (See Note 1)		3.0			3.0		dB	V_{DS} = 20 V, V_{GS} = 1/2 $V_{GS(off)}$	
16		IMD	Intercept Point (See Notes 1 and 2)		+30			+30		dBm		
17	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 3)	0.9		1.0	0.9		1.0		V_{DS} = 10 V	V_G = 0 V
18		$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	Gate-Source Cutoff Voltage Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 1 nA
19		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 10 mA

NOTES:
1. VHF single-balanced mixer drain load impedance 2k Ω.
2. 2-tone 3rd-order IMD.
3. Assumes smaller value in numerator.
4. Pulse test pulsewidth = 300 μs, duty cycle ≤ 3%.

NZA

matched dual n-channel JFETs *designed for . . .*

- **VHF/UHF Amplifiers**

Performance Curves NZF
See Section 5

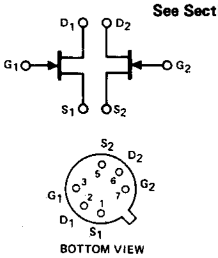
BENEFITS

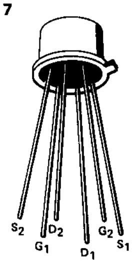
- High Gain
  g_{fs} = 4500 μmho Minimum
- Dual Version of J300 with Matched Gate-to-Source Voltage

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage	±50 V
Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Total Package Dissipation (25°C Free-Air Temperature)	350 mW
Power Derating	2.8 mW/°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U440			U441			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500			-500	pA	V_{DS} = 0, V_{GS} = -15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	-1		-6	V	V_{DS} = 10 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)			-500			-500	pA	V_{DG} = 10 V, I_D = 5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			200			
8		C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8			0.8				
10	MAT	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20	mV	V_{DG} = 10 V, I_D = 5 mA	

NZF

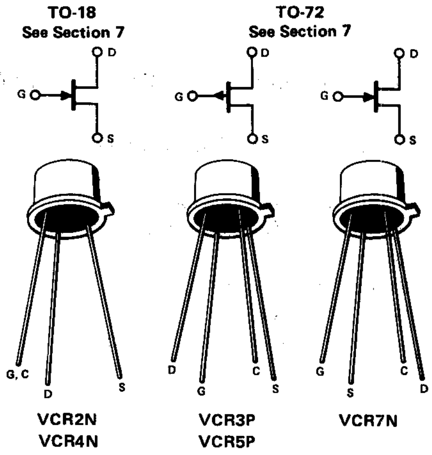
NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.

voltage-controlled resistor FETs designed for . . .

Siliconix

Performance Curves NC NP NT PC PE See Section 5

- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**



ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . 15 V
Gate Current . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . 300 mW
Storage Temperature Range . . . . –55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

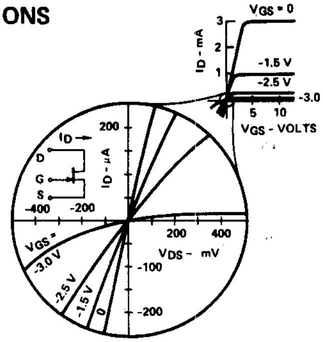
N-Channel VCR FETs

		Characteristic		VCR2N		VCR4N		VCR7N		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 µA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5		I_D = 1 µA, V_{DS} = 10 V	
4		$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		7.5		3		1.5		V_{GS} = -10 V, I_D = 0	
				NC		NP		NT				

P-Channel VCR FETs

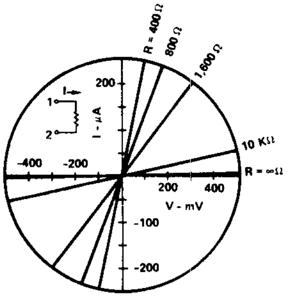
				VCR3P		VCR5P				
1	STATIC	I_{GSS}	Gate Reverse Current		20		10	nA	V_{GS} = 15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	15		15		V	I_G = 1 µA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7	3.5	7		I_D = -1 µA, V_{DS} = -10 V	
4		$r_{ds(on)}$	Drain-Source ON Resistance	70	200	300	900	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		6		3	pF	V_{GD} = 10 V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		6		3		V_{GS} = 10 V, I_D = 0	
				PE		PC				

APPLICATIONS



N-CHANNEL FET

N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 1



FOUR FIXED RESISTORS

V-I Characteristic of Four Fixed Resistors
Figure 2

The VCR FET has an a-c drain–source resistance, evaluated around $V_{DS} = 0$, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{ds} occurs when $V_{GS} = 0$ and, as V_{GS} approaches the pinch-off voltage, r_{ds} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and V_{GS} = constant, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain–source voltage is a low-level a–c signal with no d-c component. Thus the FET operating point will swing symmetrically around $V_{DS} = 0$. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate–channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds}, it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where $V_{GS(off)}$ is defined as that value of V_{GS} at $I_D/I_{DSS} = 0.001$. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 $V_{GS(off)}$ because as V_{GS} approaches $V_{GS(off)}$, r_{DS} increases very rapidly so that r_{ds} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at $V_{DS} = V_{GS} = 0$) varies as an inverse function of $V_{GS(off)}$. In Fig. 5 r_{ds} has a typical 0.7%/°C temperature coefficient for P-channels which decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical 0.3%/°C t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does $V_{GS(off)}$, from device to device.*

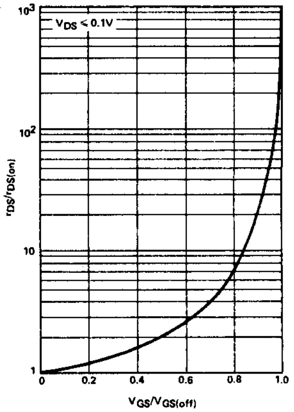


Fig. 3

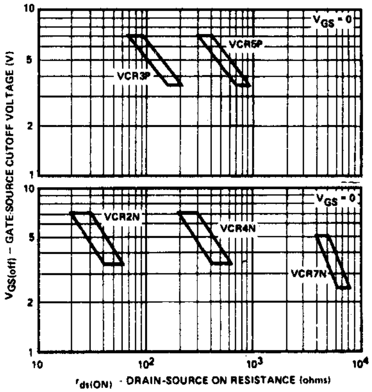


Fig. 4

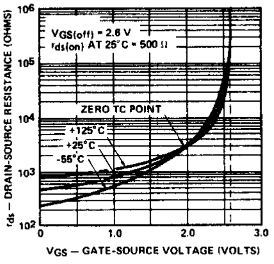


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

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* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

n-channel JFET designed for . . .

Siliconix

- **General Purpose Amplifiers**
- **Analog Switching**

Performance Curves NRL
See Section 5

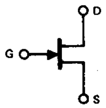
BENEFITS

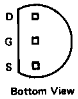
- Low Cost
- Specified at 100 MHz
- Automatic Insertion Package

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Drain-Source Voltage	25 V
Reverse Gate-Source Voltage	−25 V
Gate Current	10 mA
Continuous Device Dissipation at (or Below) 25°C Free Air Temperature (Note 1)	200 mW
Storage Temperature Range	−55°C to +150°C
Lead Temperature (1/16″ from Case for 10 seconds)	260°C

TO-92
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				Min	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		−2	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3					−2	μA		$T_A = 100°C$
4		I_{DSS}	Saturation Drain Current	2	20	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 2)	
5		V_{GS}	Gate-Source Voltage	−0.5	−7.5	V	$V_{DS} = 15$ V, $I_D = 200\ \mu A$	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−8	V	$V_{DS} = 15$ V, $I_D = 2$ nA	
7	DYNAMIC	$\|y_{fs}\|$	Common-Source Forward Transfer Admittance	2000	6500	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 2)	f = 1 kHz
8		$\|y_{os}\|$	Common Source Output Admittance		50	μmho		
9		C_{iss}	Common Source Input Capacitance		8	pF	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 MHz
10		C_{rss}	Common Source Reverse Transfer Capacitance		4	pF		
11		$\|y_{fs}\|$	Common Source Forward Transfer Admittance	1600		μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 100 MHz

*JEDEC registered data

NRL

NOTES:

1. Derate linearly to 125°C (free air temperature at a rate of 2 mW/°C).
2. Pulse tested pulse width = 100 ms, duty cycle ≤ 10%.

Siliconix

n-channel JFETs designed for . . .

Performance Curves NRL
See Section 5

■ General Purpose Amplifiers
■ Switches

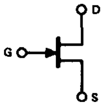
BENEFITS

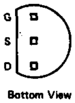
- Low Cost
- Automated Insertion Package

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage . . . . 25 V
Drain-Gate Voltage . . . . 25 V
Source-Gate Voltage . . . . 25 V
Total Device Dissipation at 25°C . . . . 310 mW
Derate above 25°C . . . . 2.82 mW/°C
Operating Junction Temperature . . . . 135°C
Storage Temperature Range . . . . -65 to +150°C

TO-92
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5457			2N5458			2N5459			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-.01	-1.0		-.01	-1.0		-.01	-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
2						-200			-200			-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25	-60		-25	-60		-25	-60		V	I_G = -10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-6.0	-1.0		-7.0	-2.0		-8.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0		5.0	2.0		9.0	4.0		16	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		5,000	1,500		5,500	2,000		6,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		10	50		15	50		20	50			
8		C_{iss}	Common-Source Input Capacitance		4.5	7.0		4.5	7.0		4.5	7.0	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0		1.0	3.0		1.0	3.0			
10		NF	Noise Figure		.04	3.0		.04	3.0		.04	3.0	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 MΩ, NBW =1 Hz	f = 1 kHz

*JEDEC registered data

NOTE:

1. Pulse test pulsewidth = 2 ms.

NRL

Siliconix

n-channel JFETs designed for . . .

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**
- **Analog Switches**

Performance Curves NH
See Section 5

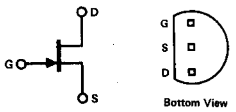
BENEFITS

- Low Cost
- Completely Specified for 400 MHz Operation
- Low Error Analog Switch
  Very Little Charge Coupling
  $C_{rss} < 1.0$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source Gate Voltage	25 V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	360 mW
Derate above 25°C	3.27 mW/°C
Operating Junction Temperature Range	−65 to +135°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (1/16″ from case for 10 seconds)	240°C

TO-92
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5484		2N5485		2N5486		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-200		-200		-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3,000	6,000	3,500	7,000	4,000	8,000	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		60		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	2,500								f = 100 MHz
9						3,000		3,500				f = 400 MHz
10		$Re(y_{os})$	Common-Source Output Conductance		75							f = 100 MHz
11							100		100			f = 400 MHz
12		$Re(y_{is})$	Common-Source Input Conductance		100							f = 100 MHz
13							1,000		1,000			f = 400 MHz
14		C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
16		C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
17		NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz
18					3.0						V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ	f = 100 MHz
19							2.0		2.0		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	
20							4.0		4.0			f = 400 MHz
21		G_{ps}	Common-Source Power Gain	16	25						V_{DS} = 15 V, I_D = 1 mA	f = 100 MHz
22						18	30	18	30		V_{DS} = 15 V, I_D = 4 mA	
23						10	20	10	20			f = 400 MHz

* JEDEC registered data

NH

NOTE:

1 Pulse Test PW 300 µs, duty cycle ≤ 3%

n-channel JFET designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves NH
See Section 5

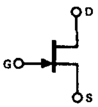
BENEFITS

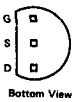
- Low Cost
- Automatic Insertion Package
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
- Low Charge Coupling from Driver to Load
  C_{rss} = 0.8 pF Typically

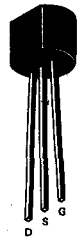
*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 10 mA
Total Device Dissipation at (or Below) T_A = 25°C . . 360 mW
(Derate 3.28 mW/°C to 135°C)
Operating Temperature Range . . . . –55 to +135°C
Storage Temperature Range . . . . –65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . 240°C

TO-92
See Section 7







*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–0.2	μA		T_A = 100°C
3		I_{DGO}	Drain Leakage Current		1.0	nA	V_{DG} = 15 V, I_S = 0	
4					0.2	μA		T_A = 100°C
5		$I_{D(off)}$	Drain Cutoff Current		10	nA	V_{DS} = 12 V, V_{GS} = –10 V	
6					2.0	μA		T_A = 100°C
7		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0	
8		$V_{GS(f)}$	Gate-Source Forward Voltage		1.0		I_G = 1 mA, V_{DS} = 0	
9		$V_{DS(on)}$	Drain-Source ON Voltage		1.5		I_D = 7 mA, V_{GS} = 0	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		150	Ω	I_D = 0.1 mA, V_{GS} = 0	
11		I_{DSS}	Saturation Drain Current	15		mA	V_{DS} = 15 V, V_{GS} = 0	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		150	Ω	I_D = 0, V_{GS} = 0	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance		5.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		V_{DS} = 0, V_{GS} = –10 V	
15	SWITCH	$t_{d(on)}$	Turn ON Delay Time		5	ns	V_{DD} = 10 V, $I_{D(on)}$ = 7 mA, R_L = 1.21K Ω $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 V	
16		t_r	Rise Time		5			
17		$t_{d(off)}$	Turn OFF Delay Time		15			
18		t_f	Fall Time		10			

*JEDEC registered data

NH

n-channel JFETs designed for . . .

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**

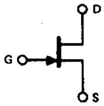
BENEFITS

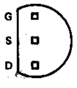
- Low Cost
- Industry Standard Package
- Automatic Insertion Package
- Fast Switching
  $t_{rise} < 5$ ns (2N5638)
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (2N5638)
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at T_{LEAD} = 25°C	625 mW
Derate above 25°C	5.68 mW/°C
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-92
See Section 7





Bottom View

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5638 Min	2N5638 Max	2N5639 Min	2N5639 Max	2N5640 Min	2N5640 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
3					-1.0		-1.0		-1.0	μA		T_A = +100°C
4		$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	V_{DS} = 15 V, V_{GS} = -12 V (2N5638) V_{GS} = -8 V (2N5639), V_{GS} = -6 V (2N5640)	
5					1.0		1.0		1.0	μA		T_A = +100°C
6		I_{DSS}	Saturation Drain Current	50		25		5.0		mA	V_{DS} = 20 V, V_{GS} = 0 (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	V_{GS} = 0, I_D = 12 mA (2N5638), I_D = 6 mA (2N5639), I_D = 3 mA (2N5640)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	I_D = 1 mA, V_{GS} = 0	
9	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		V_{GS} = 0, I_D = 0	f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		10		10		10	pF	V_{GS} = -12 V, V_{DS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
12	SW	$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	nsec	V_{DD} = 10 V $I_{D(on)}$ = 12 mA (2N5638) R_L = 800 Ω (2N5638) $V_{GS(on)}$ = 0 $I_{D(on)}$ = 6, mA (2N5639) R_L = 1.6k Ω (2N5639) $V_{GS(off)}$ = -10 V $I_{D(on)}$ = 3 mA (2N5640) R_L = 3.2k Ω (2N5640)	
13		t_r	Rise Time		5.0		8.0		10			
14		$t_{d(off)}$	Turn-OFF Delay Time		5.0		10		15			
15		t_f	Fall Time		10		20		30			

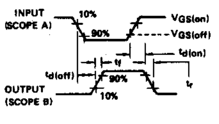
* JEDEC registered data

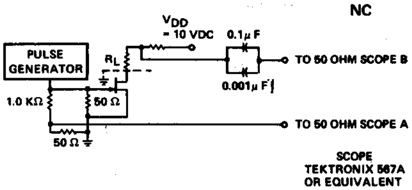
NOTE:

1 Pulse test PW ⩽ 300 μsec, duty cycle ⩽ 3.0%

NC

$R_L = \frac{V_{DD}}{I_D} - (r_{DS(on)} + 50)$





SCOPE
TEKTRONIX 567A
OR EQUIVALENT

n-channel JFETs designed for . . .

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**

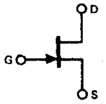
BENEFITS

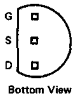
- Low Cost
- Automatic Insertion Package
- High Speed
  $t_{ON} + t_{OFF} = 24$ ns Max (2N5653)
- Low Insertion Loss
  $R_{DS(on)} = 50\ \Omega$ Max (2N5653)

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	30 V
Drain-Gate Voltage	30 V
Source-Gate Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at (or Below) $T_A = 25°C$ (Derate 2.82 mW/°C to 135°C)	360 mW
Operating Junction Temperature Range	−65 to +135°C
Storage Temperature Range	−65 to +150°C

TO-92
See Section 7





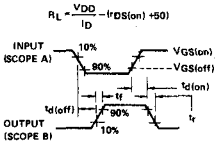
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

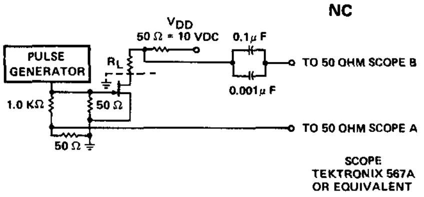
			Characteristic	2N5653		2N5654		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		−1.0		−1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3					−1.0		−1.0	μA		$T_A = +100°C$
4		$I_{D(off)}$	Drain Cutoff Current		1.0		1.0	nA	$V_{DS} = 15$ V, $V_{GS} = -12$ V (2N5653)	
5					1.0		1.0	μA	$V_{GS} = -8$ V (2N5654)	$T_A = +100°C$
6		I_{DSS}	Saturation Drain Current	40		15		mA	$V_{DS} = 20$ V, $V_{GS} = 0$ (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.75		0.75	V	$V_{GS} = 0$, $I_D = 10$ mA (2N5653), $I_D = 5$ mA (2N5654)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		50		100	Ω	$I_D = 1$ mA, $V_{GS} = 0$	
9	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		50		100		$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		10		10	pF	$V_{GS} = -12$ V, $V_{DS} = 0$	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5			
12	SW	$t_{d(on)}$	Turn-ON Delay Time		4.0		6.0	nsec	$V_{DD} = 10$ V, $I_{D(on)} = 10$ mA (2N5653)	
13		t_r	Rise Time		5.0		8.0		$V_{GS(on)} = 0$, $I_{D(on)} = 5$ mA (2N5654)	
14		$t_{d(off)}$	Turn-OFF Delay Time		5.0		10		$V_{GS(off)} = -12$ V, $R_L = 925\ \Omega$ (2N5653)	
15		t_f	Fall Time		10		20		$R_L = 1.85K\ \Omega$ (2N5654)	

*JEDEC registered data

NOTE:
1. Pulse test PW ≤ 300 μs, duty cycle ≤ 3%.

NC





2N5668 2N5669 2N5670

n-channel JFETs designed for . . .

Siliconix

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Performance Curves NH
See Section 5

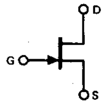
BENEFITS

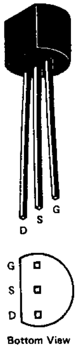
- Low Cost
- Automatic Insertion Package
- Specified for 100 MHz Operation

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

TO-92
See Section 7





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	2N5668		2N5669		2N5670		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		−2.0		−2.0		−2.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					−2.0		−2.0		−2.0	μA		$T_A = +100°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		−25		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.2	4.0	1.0	6.0	2.0	8.0		$V_{DS} = 15$ V, $I_D = 10$ nA	
5		I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6500	2000	6500	3000	7500	μmhos	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		20		50		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1000		1600		2500				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		50		100		150			
10		$Re(y_{is})$	Common-Source Input Conductance		800		800		800			
11		C_{iss}	Common-Source Input Capacitance		7.0		7.0		7.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0			
13		C_{oss}	Common-Source Output Capacitance		4.0		4.0		4.0			
14		NF	Noise Figure		2.5		2.5		2.5	dB	$V_{DS} = 15$ V, $V_{GS} = 0$, $R_G = 1K\ \Omega$	f = 100 MHz
15		G_{ps}	Common-Source Power Gain	16		16		16			$V_{DS} = 15$ V, $V_{GS} = 0$	

*JEDEC registered data

NH

NOTE:

1. Pulse test PW = 300 μs, duty cycle ≤ 3%.

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

**Performance Curves NVA
See Section 5**

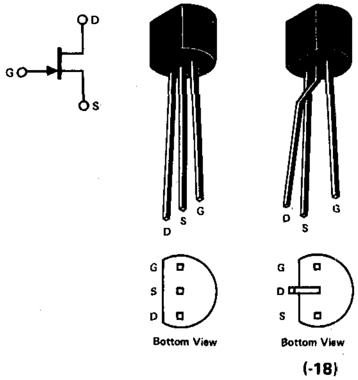
BENEFITS

- Very Low Insertion Loss
  $R_{DS(on)} < 3\ \Omega$ (J105)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

**TO-92
See Section 7**



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J105			J106			J107			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	$V_{DS} = 0\ V, V_{GS} = -15\ V$	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	$V_{DS} = 5\ V, I_D = 1\ \mu A$	
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25				$V_{DS} = 0\ V, I_G = -1\ \mu A$	
4		I_{DSS}	Drain Saturation Current (Note 2)	500			200			100			mA	$V_{DS} = 15\ V, V_{GS} = 0\ V$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5\ V, V_{GS} = -10\ V$	
6		$r_{DS(on)}$	Drain Source ON Resistance			3			6			8	Ω	$V_{DS} \leqslant 0.1\ V, V_{GS} = 0\ V$	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	$V_{DS} = 0\ V, V_{GS} = -10\ V$	f = 1 MHz
8		$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35			
9		$C_{dg(on)} + C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160		$V_{DS} = V_{GS} = 0\ V$	
10		$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions J105 J106 J107 V_{DD} 1.5 V 1.5 V 1.5 V $V_{GS(off)}$ -12 V -7 V -5 V R_L 50 Ω 50 Ω 50 Ω	
11		t_r	Rise Time		20			20			20				
12		$t_{d(off)}$	Turn Off Delay Time		15			15			15				
13		t_f	Fall Time		20			20			20				

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ⩽ 3%.

NVA

n-channel JFETs designed for . . .

Siliconix

Performance Curves NIP
See Section 5

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Low Noise Audio Amplifiers**

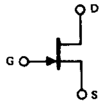
BENEFITS

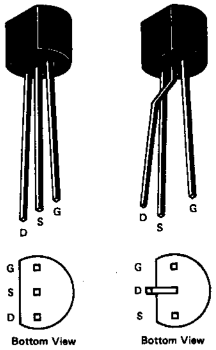
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $R_{DS(on)} < 8\ \Omega$ (J108)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{D(on)} + t_r = 5$ ns Typical
- Low Noise
  $\overline{e}_n = 6\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 Hz, Typ (J110)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−25V
Gate Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

TO-92
See Section 7





(-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J108			J109			J110			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			−3			−3			−3	nA	$V_{DS} = 0\ V, V_{GS} = -15\ V$	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−3		−10	−2		−6	−0.5		−4	V	$V_{DS} = 5\ V, I_D = 1\ \mu A$	
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25				$V_{DS} = 0\ V, I_G = -1\ \mu A$	
4		I_{DSS}	Drain Saturation Current (Note 2)	80			40			10			mA	$V_{DS} = 15\ V, V_{GS} = 0\ V$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	$V_{DS} = 5\ V, V_{GS} = -10\ V$	
6		$r_{DS(on)}$	Drain-Source ON Resistance			8			12			18	Ω	$V_{DS} \leqslant 0.1\ V, V_{GS} = 0\ V$	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			15			15			15	pF	$V_{DS} = 0\ V, V_{GS} = -10\ V$	f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance			15			15			15			
9		$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85		$V_{DS} = V_{GS} = 0$	
10		$t_{d(on)}$	Turn ON Delay Time		4			4			4		ns	Switching Time Test Conditions J108 / J109 / J110 V_{DD}: 1.5 V / 1.5 V / 1.5 V $V_{GS(off)}$: −12 V / −7 V / −5 V R_L: 150 Ω / 150 Ω / 150 Ω	
11		t_r	Rise Time		1			1			1				
12		$t_{d(off)}$	Turn OFF Delay Time		6			6			6				
13		t_f	Fall Time		30			30			30				

NIP

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle ⩽ 3%.

n-channel FETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NC
See Section 5

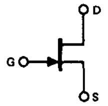
BENEFITS

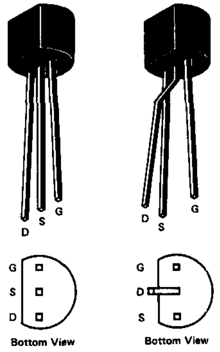
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (J111)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{D(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 5$ pF
  $C_{gs(off)} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –35V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . .300°C

TO-92
See Section 7





(-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J111			J112			J113			UNIT	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–1			–1			–1	nA	$V_{DS} = 0$ V, $V_{GS} = -15$ V	
2		$V_{GS(off)}$	Gate Source Cutoff Voltage	–3		–10	–1		–5	–0.5		–3	V	$V_{DS} = 5$ V, $I_D = 1\ \mu A$	
3		BV_{GSS}	Gate Source Breakdown Voltage	35			35			–35				$V_{DS} = 0$ V, $I_G = -1\ \mu A$	
4		I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	$V_{DS} = 15$ V, $V_{GS} = 0$ V	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			–1			–1			–1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6		$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	$V_{DS} = 0.1$ V, $V_{GS} = 0$ V	
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V	f = 1 MHz
8		$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5			
9		$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28		$V_{DS} = V_{GS} = 0$	
10		$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions J111 / J112 / J113 V_{DD}: 10 V / 10 V / 10 V $V_{GS(off)}$: –12 V / –7 V / –5 V R_L: 800 Ω / 1,600 Ω / 3,200 Ω	
11		t_r	Rise Time		6			6			6				
12		$t_{d(off)}$	Turn Off Delay Time		20			20			20				
13		t_f	Fall Time		15			15			15				

NC

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 μs; duty cycle ≤ 3%.

n-channel JFET designed for . . .

Siliconix

Performance Curves NZF
See Section 5

- **Analog Switches**
- **Choppers**
- **Commutators**

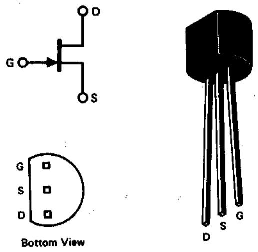
BENEFITS

- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Very Fast Switching
  - $t_{D(on)} + t_r = 6$ ns Typical
- Short Sample and Hold Aperture Time
  - $C_{gd(off)} < 2$ pF
  - $C_{gs(off)} < 2$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . −25V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J114 Min	J114 Typ	J114 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-1	nA	$V_{DS} = 0$, $V_{GS} = -15$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	V	$V_{DS} = 5$ V, $I_D = 1\ \mu A$	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25				$V_{DS} = 0$, $I_G = -1\ \mu A$	
4		I_{DSS}	Saturation Drain Current (Note 2)	15			mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
6		$r_{DS(on)}$	Drain-Source ON Resistance			150	Ω	$V_{DS} \leqslant 0.1$ V, $V_{GS} = 0$	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			2	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance			2			
9		$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			8		$V_{DS} = V_{GS} = 0$	
10		$t_{d(on)}$	Turn On Delay Time		3		ns	Switching Time Test Conditions $V_{DD} = 10$ V, $V_{GS(off)} = -12$ V $R_L = 1$ KΩ, $V_{GS(on)} = 0$	
11		t_r	Rise Time		3				
12		$t_{d(off)}$	Turn Off Delay Time		12				
13		t_f	Fall Time		8				

NZF

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ⩽ 3%.

p-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 5

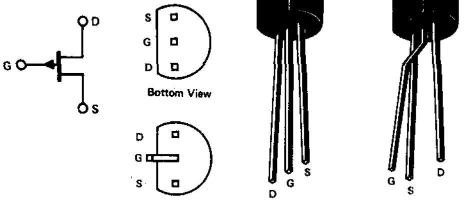
BENEFITS

- Low Cost
- Simplifies Series-Shunt Switching when when Combined with J113, its N-Chan-Channel Complement
- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)} < 5.5$ pF
  $C_{dg(off)} < 5.5$ pF
- Fast Switching
  $t_{d(on)} + t_r = 7$ ns Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics		J174			J175			J176			J177			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15 V, I_D = -10 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30				V_{DS} = 0, I_G = 1 μA	
4		I_{DSS}	Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	V_{DS} = -15 V, V_{GS} = 0	
5		$I_{D(off)}$	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V_{DS} = -15 V, V_{GS} = 10 V	
6		$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = -0.1 V	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V	f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5				
9		$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance		32			32			32			32			V_{DS} = V_{GS} = 0	
10		$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions	
11		t_r	Rise Time		5			10			20			25				
12		$t_{d(off)}$	Turn Off Delay Time		5			10			15			20				
13		t_f	Fall Time		10			20			20			25				

Switching Time Test Conditions

	J174	J175	J176	J177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ
$V_{GS(on)}$	0 V	0 V	0 V	0 V

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A. **PS**
3. Pulse test duration = 300 μs; duty cycle ≤ 3%.

Siliconix

n-channel JFETs *designed for . . .*

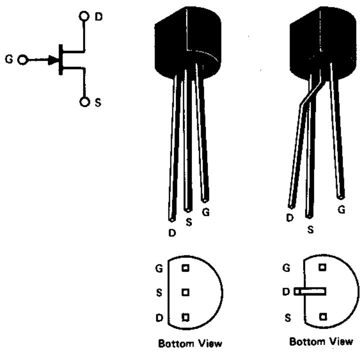
■ General Purpose Amplifiers

Performance Curves NP
See Section 5

BENEFITS

- High Input Impedance
  I_G = 35 pA Typical
- Good for Low Power Supply Operation
  $V_{GS(off)} < 1.5$ V (J201)

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . -40 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . —55 to 135°C
Storage Temperature Range. . . . . —55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				J201			J202			J203			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	V	V_{DS} = 20 V, I_D = 10 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20	mA	V_{DS} = 20 V, V_{GS} = 0	
5		I_G	Gate Current (Note 2)		-35			-35			-35		pA	V_{DG} = 20 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	500			1,000			1,500			μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1			3.5			10				
8		C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1				
10		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		5			5			5		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES:

NP

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFETs designed for . . .

Siliconix

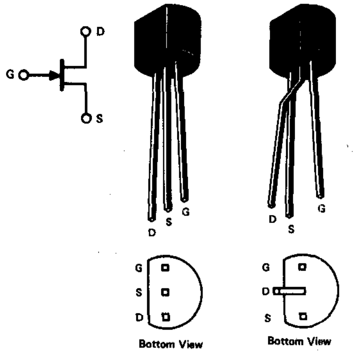
Performance Curves NP
See Section 5

- **General Purpose Switching**

BENEFITS

- Very Low Leakage

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . −25V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				J204			Unit	Test Conditions	
				Min	Typ	Max			
1	S T A T I C	I_{GSS}	Gate Reverse Current (Note 2)			-100	pA	$V_{DS} = 0$, $V_{GS} = -20$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-2.0	V	$V_{DS} = 20$ V, $I_D = 10$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25				$V_{DS} = 0$, $I_G = -1$ μA	
4		I_{DSS}	Saturation Drain Current (Note 3)		1.2		mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
5		I_G	Gate Current (Note 2)		-35		pA	$V_{DG} = 20$ V, $I_D = 200$ μA	
6	D Y N A M I C	g_{fs}	Common Source Forward Transconductance (Note 3)		1500		μmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		2.5				
8		C_{iss}	Common-Source Input Capacitance		4		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1				
10		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz

NOTES:

NP

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

Siliconix

n-channel JFETs designed for . . .

■ General Purpose Amplifiers

Performance Curves NZF
See Section 5

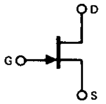
BENEFITS

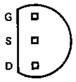
- High Gain
  G_{FS} = 7000 μmho Minimum (J211, J212)
- High Input Impedance
  I_{GSS} = 100 pA Maximum
  C_{iss} = 5 pF Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

TO-92
See Section 7





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	J210			J211			J212			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100			-100	pA	$V_{DS} = 0$, $V_{GS} = -15$ V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2.5		-4.5	-4		-6	V	$V_{DS} = 15$ V, $I_D = 1$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				$V_{DS} = 0$, $I_G = -1$ μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5		I_G	Gate Current (Note 1)		-10			-10			-10		pA	$V_{DG} = 10$ V, $I_D = 1$ mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,000		12,000	7,000		12,000	7,000		12,000	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			150			200			200			
8		C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1				
10		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NZF

n-channel JFETs designed for . . .

- **Audio and Sub-Audio Amplifiers**

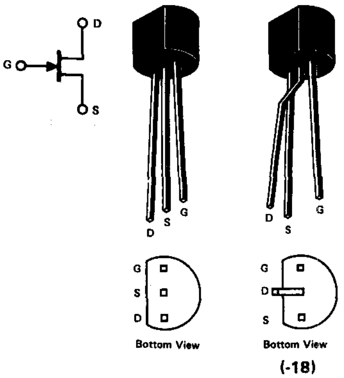
Siliconix

Performance Curves NS
See Section 5

BENEFITS

- Ultra Low Noise
  $\overline{e}_n$ = 8 nV/$\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e}_n$ = 2 nV/$\sqrt{Hz}$ Typical at 1 kHz

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . –40V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J230			J231			J232			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-250			-250			-250	pA	V_{DS} = 0, V_{GS} = -30 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2		-5	-4		-6	V	V_{DS} = 20 V, I_D = 1 µA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40				V_{DS} = 0, I_G = -1 µA	
4		I_{DSS}	Saturation Drain Current (Note 3)	0.7		3	2		6	5		10	mA	V_{DS} = 20 V, V_{GS} = 0	
5		I_G	Gate Current (Note 2)		-10			-10			-10		pA	V_{DG} = 10 V, I_D = 0.5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1,000		2,500	1,500		3,000	2,500		4,000	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			2			4			6			
8		C_{iss}	Common-Source Input Capacitance		12			12			12		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		2			2			2				
10		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		8	30		8	30		8	30	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 10 Hz
11					2			2			2				f = 1 kHz

NOTES:

NS

1. Geometry is symmetrical. Unit may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

p-channel JFETs designed for . . .

Siliconix

■ General Purpose Amplifiers

**Performance Curves PS
See Section 5**

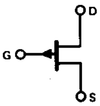
BENEFITS

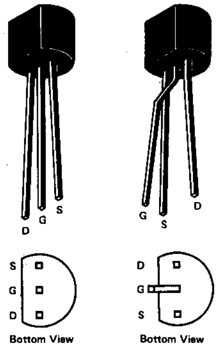
- Low Cost
- Automatic Insertion Package
- High Gain Amplifiers
  g_{fs} = 14,000 µmho Typical (J271)
- Low Noise
  $\overline{e_n}$ = 6 nV/$\sqrt{\text{Hz}}$ at 1 kHz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate Source Voltage (Note 1) . . . . 30 V
Gate Current . . . . –50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 7





(-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	J270 Min	J270 Typ	J270 Max	J271 Min	J271 Typ	J271 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			200			200	pA	V_{DS} = 0, V_{GS} = 20 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.5		2.0	1.5		4.5	V	V_{DS} = -15 V, I_D = -1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30			30				V_{DS} = 0, I_G = 1 µA	
4		I_{DSS}	Saturation Drain Current (Note 3)	-2		-15	-6		-50	mA	V_{DS} = -15 V, V_{GS} = 0	
5		I_G	Gate Current (Note 2)		15			60		pA	V_{DG} = -15 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	µmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			500			
8		C_{iss}	Common-Source Input Capacitance		32			32		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		4			4				
10		e_n	Equivalent Short-Circuit Input Noise Voltage		6			6		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = -10 V, I_D = $I_{DSS(min)}$	f = 1 kHz

PS

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFETs designed for . . .

Siliconix

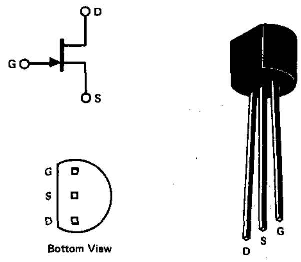
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZF
See Section 5

BENEFITS

- High Power Gain
  20–23 dB Typical at 100 MHz, Common-Source
  17.5–20.5 dB Typical at 100 MHz, Common-Gate
- Low Noise Figure
  1.3 dB Typical at 100 MHz
- High Dynamic Range
  Greater than 100 dB

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.5	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–0.1	µA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 1)	–1.5	–7.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1, 2)	4	45	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	9000	µmho	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	
7		g_{os}	Common-Source Output Conductance		200			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.7	pF	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	
9		C_{iss}	Common-Source Input Capacitance		5.5			

NOTES:
1. I_{DSS} and $V_{GSS(off)}$ are selected into 5 ranges and labeled according to above table.
2. Pulse test PW ≤ 300 µs, duty cycle ≤ 3%.

NZF

n-channel JFETs *designed for . . .*

Siliconix

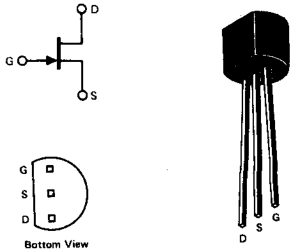
■ VHF/UHF Amplifiers
■ Oscillators
■ Mixers

Performance Curves NH
See Section 5

BENEFITS

- Characterized for Operation at 100 and 400 MHz
- Low Noise
  NF = 1.7 dB Typical at 100 MHz

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . -30 V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
  (Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
  (1/16" from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				J304			J305			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100	pA	$V_{DS} = 0, V_{GS} = -20$ V	
2		$V_{GS(off)}$	Gate Source Cutoff Voltage	-2		-6	-0.5		-3	V	$V_{DS} = 15$ V, $I_D = 1$ nA	
3		BV_{GSS}	Gate Source Breakdown Voltage	-30			-30				$V_{DS} = 0, I_G = -1\ \mu A$	
4		I_{DSS}	Saturation Drain Current (Note 2)	5		15	1		8	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
6		g_{os}	Common-Source Output Transconductance			50			50			
7		C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.85			0.85				
9		C_{oss}	Common-Source Output Capacitance		1.0			1.0				
10	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance					3,000		μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 100 MHz
11					4,200							f = 400 MHz
12		g_{oss}	Common-Source Output Conductance		60			60				f = 100 MHz
13					80							f = 400 MHz
14		b_{oss}	Common-Source Output Susceptance		800			800				f = 100 MHz
15					3,600							f = 400 MHz
16		g_{iss}	Common-Source Input Conductance		80			80				f = 100 MHz
17					800							f = 400 MHz
18		b_{iss}	Common-Source Input Susceptance		2,000			2,000				f = 100 MHz
19					7,500							f = 400 MHz
20		G_{ps}	Common-Source Power Gain		20					dB	$V_{DS} = 15$ V, $I_D = 5$ mA	f = 100 MHz
21					11							f = 400 MHz
22		NF	Noise Figure (Single Sideband)		1.7						$V_{DS} = 15$ V, $I_D = 5$ mA, $R_G = 1\ K\Omega$	f = 100 MHz
23					3.8							f = 400 MHz

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NH

n-channel JFETs designed for . . .

Siliconix

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA See Section 5

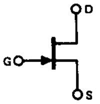
BENEFITS

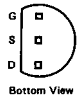
- Industry Standard Part
  In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- Easily Matches to 75 Ω Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

TO-92
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J308			J309			J310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1		BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25			V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2	STATIC	I_{GSS}	Gate Reverse Current			−1.0			−1.0			−1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3						−1.0			−1.0			−1.0	µA		T = +125°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0		−6.5	−1.0		−4.0	−2.0		−6.5	V	$V_{DS} = 10$ V, $I_D = 1$ nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	$V_{DS} = 0$, $I_G = 1$ mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	µmhos	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			200			200			200			
9		g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000				
10		g_{og}	Common-Gate Output Conductance		150			100			150				
11		C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
12		C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0			
13		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 100 Hz
14	HI FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 105 MHz
15		$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14				
16		$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4				
17		$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15				
18		G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		
19		NF	Noise Figure		1.5			1.5			1.5				
20		G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				f = 450 MHz
21		NF	Noise Figure		2.7			2.7			2.7				

NOTE:
1. Pulse test PW 300 µs, duty cycle ≤ 3%.

NZA

n-channel JFETs current regulator diodes

Siliconix

designed for . . .

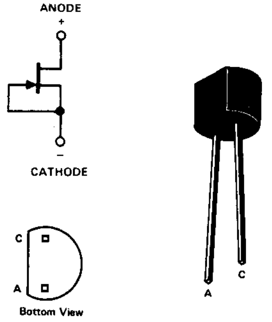
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

**Performance Curves NCL
See Section 5**

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Good Operating Current Tolerance ±20%

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . 50 V
Forward Current . . . . 20 mA
Reverse Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

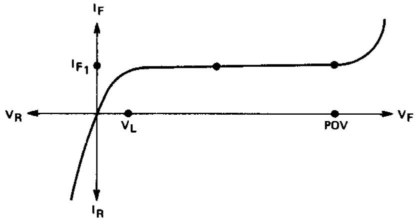
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			J500	J501	J502	J503	J504	J505	Unit	Test Conditions
1		I_{FI}	Forward Current (Note 1)	Min	0.192	0.264	0.344	0.448	0.600	0.800	mA	$V_F = 25$ V
2	STATIC			Nominal	0.240	0.330	0.430	0.560	0.750	1.000		
3				Max	0.288	0.396	0.516	0.672	0.900	1.200		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	$I_F = 1.1\ I_{FI}$ (Max)
5		V_L	Limiting Voltage (Note 3)	Max	1.2	1.3	1.5	1.7	1.9	2.1		$I_F = 0.9\ I_{FI}$ (Min)
6				Typ	0.8	0.9	1.1	1.2	1.4	1.5		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	5.0	3.0	2.0	1.4	1.0	0.6	MΩ	$V_F = 25$ V, f = 1 kHz
8				Typ	8.0	6.0	4.4	3.4	2.5	1.9		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	pF	$V_F = 25$ V, f = 1 MHz

NOTES:
1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$.

NCL

Current-Limiter Diode
V-I Characteristic



Siliconix

n-channel JFETs current regulator diodes designed for . . .

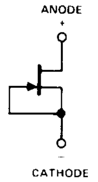
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

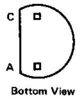
Performance Curves NCL See Section 5

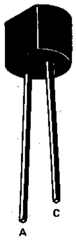
BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Good Operating Current Tolerance ±20%

TO-92
See Section 7







ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage	50 V
Forward Current	20 mA
Reverse Current	50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

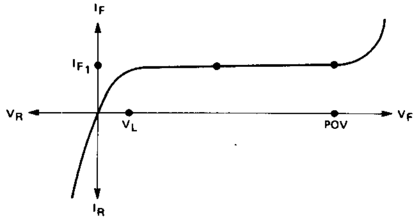
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			J506	J507	J508	J509	J510	J511	Unit	Test Conditions
1	STATIC	I_{FI}	Forward Current (Note 1)	Min	1.120	1.440	1.9	2.4	2.9	3.8	mA	$V_F = 25$ V
2				Nominal	1.400	1.800	2.4	3.0	3.6	4.7		
3				Max	1.680	2.160	2.9	3.6	4.3	5.6		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	$I_F = 1.1\ I_{FI}$ (Max)
5		V_L	Limiting Voltage (Note 3)	Max	2.5	2.8	3.1	3.5	3.9	4.2		$I_F = 0.9\ I_{FI}$ (Min)
6				Typ	1.8	2.0	2.2	2.5	2.8	3.0		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	0.4	0.25	0.25	0.20	0.20	0.15	MΩ	$V_F = 25$ V, f = 1 kHz
8				Typ	1.4	1.0	0.70	0.60	0.50	0.30		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	pF	$V_F = 25$ V, f = 1 MHz

NOTES:
1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$.

NCL

Current-Limiter Diode
V-I Characteristic



Siliconix

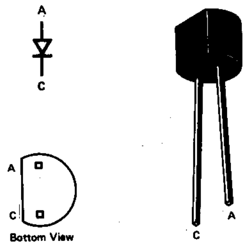
low-leakage pico-amp diodes designed for . . .

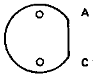
- **High Impedance Diode Switching**
- **High Dynamic Range Log Amps**
- **High Isolation Protection Circuits**

BENEFITS

- Low Cost

TO-92
See Section 7





Bottom View
(TO-106)

Also Available As EPAD50, 100, 200, 500 (TO-106)

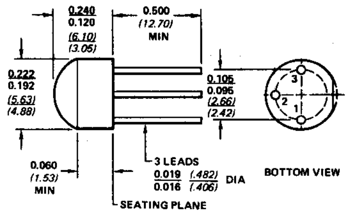
ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current . . . . 10 mA
Total Device Dissipation . . . . 360 mW
Storage Temperature Range. . . . . –65°C to +135°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic			Min	Typ	Max	Unit	Test Conditions
1	S T A T I C	I_R	Reverse Current (Note 1)	JPAD50			–50	pA	$V_R = -20$ V
2				JPAD100			–100		
3				JPAD200			–200		
4				JPAD500			–500		
5		BV_R	Breakdown Voltage (Reverse)		–35	–80		V	$I_R = -1\ \mu A$
6		V_F	Forward Voltage Drop			0.8	1.5	V	$I_F = 5$ mA
7	D Y N	C_{R}	Capacitance			1.5	2.0	pF	$V_R = -5$ V, f = 1 MHz

NOTE:
1. The JPAD type number denotes its maximum reverse current value in pico amps. Devices with I_R values intermediate to those shown are also available on request.



TO-106

n-channel JFET designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves NZF
See Section 5

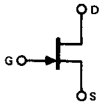
BENEFITS

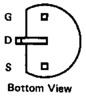
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Very Fast Switching
  - $t_{D(on)} + t_r = 6$ ns Typical
- Short Sample and Hold Aperture Time
  - $C_{gd(off)} < 2$ pF
  - $C_{gs(off)} < 2$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25 V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . .360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . .300°C

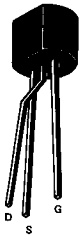
TO-92 Lead-form
See Section 7





Bottom View

(-18)



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		K114			Unit	Test Conditions
				Min	Typ	Max		
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-1	nA	$V_{DS} = 0$, $V_{GS} = -15$ V
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	V	$V_{DS} = 5$ V, $I_D = 1$ μA
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25				$V_{DS} = 0$, $I_G = -1$ μA
4		I_{DSS}	Saturation Drain Current (Note 2)	15			mA	$V_{DS} = 15$ V, $V_{GS} = 0$
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V
6		$r_{DS(on)}$	Drain-Source ON Resistance			150	Ω	$V_{DS} \leq 0.1$ V, $V_{GS} = 0$
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			2	pF	$V_{DS} = 0$, $V_{GS} = -10$ V, f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance			2		
9		$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			8		$V_{DS} = V_{GS} = 0$
10		$t_{d(on)}$	Turn On Delay Time		3		ns	Switching Time Test Conditions $V_{DD} = 10$ V, $V_{GS(off)} = -12$ V $R_L = 1$ KΩ, $V_{GS(on)} = 0$
11		t_r	Rise Time		3			
12		$t_{d(off)}$	Turn Off Delay Time		12			
13		t_f	Fall Time		8			

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μs; duty cycle ≤ 3%.

NZF

n-channel JFET
designed for . . .

Siliconix

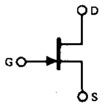
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

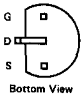
Performance Curves NH
See Section 5

BENEFITS

- Specified for 200 MHz Operation

TO-92
See Section 7





(-18)

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−250	pA	V_{GS} = −20 V, V_{DS} = 0	
2					−15	nA		T_A = +85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = −1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−8.0		V_{DS} = 15 V, I_D = 1 μA	
5		I_{DSS}	Saturation Drain Current	4.0	25	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6		$r_{DS(on)}$	Drain-Source ON Resistance		300	Ω	I_D = 1 mA, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500	10,000	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$Re(y_{fs})$	Common-Source Forward Transconductance	4,000				f = 200 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		150			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.0			
13		NF	Noise Figure		3.0	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 200 MHz
14					5.0		V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω, BW = 5 Hz	f = 10 Hz
15		G_{PS}	Common-Source Power Gain	15			V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz

NOTE:
1. Pulse test PW = 300 μs; duty cycle ⩽ 3%.

NH

n-channel JFETs designed for . . .

Siliconix

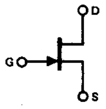
Performance Curves NZF
See Section 5

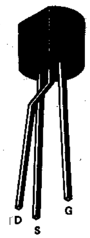
■ General Purpose Amplifiers

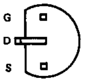
BENEFITS

- High Gain
  G_{FS} = 7000 μmho Minimum
  (K211-18, K212-18)
- High Input Impedance
  I_{GSS} = 100 pA Maximum
  C_{iss} = 5 pF Typical

TO-92 Lead-form
See Section 7







Bottom View
(-18)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . −25V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
  (Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . −55 to 135°C
Storage Temperature Range. . . . . −55 to 150°C
Lead Temperature Range
  (1/16" from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J210			J211			J212			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2.5		-4.5	-4		-6	V	V_{DS} = 15 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS} = 0, I_G = -1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	V_{DS} = 15 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)		-10			-10			-10		pA	V_{DG} = 10 V, I_D = 1 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,000		12,000	7,000		12,000	7,000		12,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			150			200			200			
8		C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1				
10		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NZF

n-channel JFET *designed for . . .*

Siliconix

Performance Curves NZF
See Section 5

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

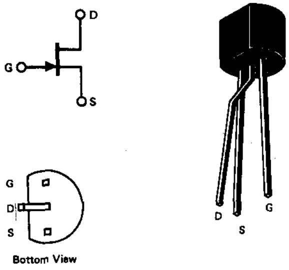
BENEFITS

- High Power Gain
  22 dB Typical at 100 MHz
  Common-Source
  17 dB Typical at 100 MHz
  Common-Gate
- Low Noise
  NF = 2 dB Typical at 100 MHz
- High Dynamic Range Greater than 100 dB

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –25V
Gate Current (FWD) . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92 Lead-form
See Section 7



Bottom View
(-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	V	$V_{DS} = 10$ V, $I_D = 1$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25				$V_{DS} = 0$, $I_G = -1$ μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	6		30	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1	V	$I_G = 1$ mA, $V_{DS} = 0$	
6	DYN	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		9,000	μmho	$V_{DG} = 10$ V, $I_D = 5$ mA	f = 1 kHz
7		g_{os}	Common-Source Output Transconductance			200			
8		C_{iss}	Common-Source Input Capacitance		4	5.5	pF	$V_{DG} = 10$ V, $I_D = 5$ mA	f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1	1.7			
10		C_{oss}	Common-Source Output Capacitance		1.5				
11	HI FREQ	$\lvert y_{fs} \rvert$	Common-Source Forward Transcadmittance		6,200		μmho	$V_{DG} = 15$ V, $I_D = 5$ mA	f = 100 MHz
12					6,000				f = 450 MHz
13		$\lvert y_{fg} \rvert$	Common-Gate Forward Transcadmittance		6,000				f = 100 MHz
14					5,500				f = 450 MHz
15		G_{fg}	Common-Gate Power Gain		17		dB		f = 100 MHz (Note 3)
16		NF	Noise Figure (Single Sideband)		2				

NOTES:

1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.
3. Typical values for performance at 100 MHz in a common-gate circuit operating 3 dB bandwidth is 2 MHz.

NZF

n-channel JFETs designed for . . .

Siliconix

Performance Curves NH
See Section 5

■ VHF/UHF Amplifiers
■ Oscillators
■ Mixers

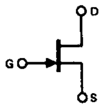
BENEFITS

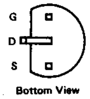
- Characterized for Operation at 100 and 400 MHz
- Low Noise
  NF = 1.7 dB Typical at 100 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –30V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92 Lead-form
See Section 7





(-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		K304-18			K305-18			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100	pA	$V_{DS} = 0$, $V_{GS} = -20$ V	
2		$V_{GS(off)}$	Gate Source Cutoff Voltage	-2		-6	-0.5		-3	V	$V_{DS} = 15$ V, $I_D = 1$ nA	
3		BV_{GSS}	Gate Source Breakdown Voltage	-30			-30				$V_{DS} = 0$, $I_G = -1$ μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	5		15	1		8	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
6		g_{os}	Common-Source Output Transconductance			50			50			
7		C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.85			0.85				
9		C_{oss}	Common-Source Output Capacitance		1.0			1.0				
10	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance					3,000		μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 100 MHz
11					4,200							f = 400 MHz
12		g_{oss}	Common-Source Output Conductance		60			60				f = 100 MHz
13					80							f = 400 MHz
14		b_{oss}	Common-Source Output Susceptance		800			800				f = 100 MHz
15					3,600							f = 400 MHz
16		g_{iss}	Common-Source Input Conductance		80			80				f = 100 MHz
17					800							f = 400 MHz
18		b_{iss}	Common-Source Input Susceptance		2,000			2,000				f = 100 MHz
19					7,500							f = 400 MHz
20		G_{ps}	Common-Source Power Gain		20					dB	$V_{DS} = 15$ V, $I_D = 5$ mA	f = 100 MHz
21					11							f = 400 MHz
22		NF	Noise Figure (Single Sideband)		1.7						$V_{DS} = 15$ V, $I_D = 5$ mA, $R_G = 1$ KΩ	f = 100 MHz
23					3.8							f = 400 MHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NH

n-channel JFETs designed for . . .

Siliconix

- ■ **VHF/UHF Amplifiers**
- ■ **Oscillators**
- ■ **Mixers**

Performance Curves NZA
See Section 5

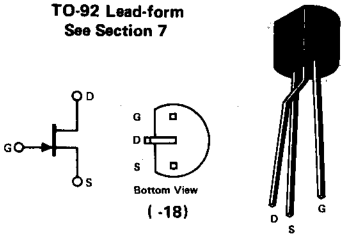
BENEFITS

- Industry Standard Part
  In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- Easily Matches to 75 Ω Input

* ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . .25 V
Source-Gate Voltage . . . . .25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . .300°C

TO-92 Lead-form
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		K308			K309			K310			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current			–1.0			–1.0			–1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
3						–1.0			–1.0			–1.0	μA		T = +125°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0		–6.5	–1.0		–4.0	–2.0		–6.5	V	$V_{DS} = 10$ V, $I_D = 1$ nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	$V_{DS} = 10$ V, $V_{GS} = 0$	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	$V_{DS} = 0$, $I_G = 1$ mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	μmhos	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			200			200			200			
9		g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000				
10		g_{og}	Common-Gate Output Conductance		150			100			150				
11		C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
12		C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0			
13		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 100 Hz
14	HI FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	$V_{DS} = 10$ V, $I_D = 10$ mA	f = 105 MHz
15		$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14				
16		$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4				
17		$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15				
18		G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		
19		NF	Noise Figure		1.5			1.5			1.5				
20		G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				f = 450 MHz
21		NF	Noise Figure		2.7			2.7			2.7				

NOTE:
1. Pulse test PW 300 μs, duty cycle ≤ 3%.

NZA

Siliconix

n-channel JFET designed for . . .

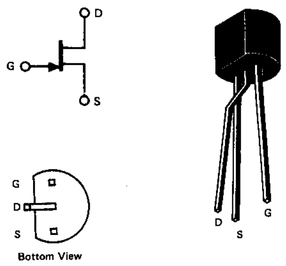
■ VHF Amplifiers
■ Mixers

Performance Curves NH
See Section 5

BENEFITS

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Bandwidth
- Low Cost

TO-92 Lead-form
See Section 7



Bottom View
(-18)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –30V
Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STA	I_{GSS}	Gate Reverse Current		–1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2		BV_{GSS}	Gate-Source Breakdown Voltage	–30		V	$I_G = -1$ µA, $V_{DS} = 0$	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–6		$V_{DS} = 15$ V, $I_D = 1$ nA	
4		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
5	DYN	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	7500	µmho		f = 1 kHz
6		g_{os}	Common-Source Output Conductance		50			
7		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	pF		f = 1 MHz
8		C_{iss}	Common-Source Input Capacitance		4			
9		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz		400 MHz		Unit	Test Conditions	
				Min	Max	Min	Max			
10	HI FREQ	g_{iss}	Common-Source Input Conductance		100		1000	µmho	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		b_{iss}	Common-Source Input Susceptance		2500		10,000			
12		g_{oss}	Common-Source Output Conductance		75		100			
13		b_{oss}	Common-Source Output Susceptance		1000		4000			
14		g_{fs}	Common-Source Forward Transconductance (Note 1)			4000				
15		G_{ps}	Common-Source Power Gain	18		10		dB	$V_{DS} = 15$ V, $I_D = 5$ mA	
16		NF	Noise Figure		2		4			$R_G = 1K\ \Omega$

NOTE:
1. Pulse test duration = 300 µs.

NH

n-channel JFET designed for . . .

Siliconix

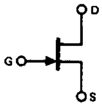
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

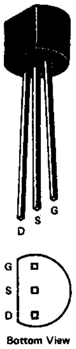
Performance Curves NH
See Section 5

BENEFITS

- Low Cost
- Automatic Insertion Package

TO-92
See Section 7





ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Drain-Source Voltage	25 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	−55 to 135°C
Storage Temperature Range	−55 to 150°C
Lead Temperature Range (1/16″ from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−2.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					−2.0	µA		$T_A = +100°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	$I_G = -10$ µA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−8.0		$V_{DS} = 15$ V, $I_D = 2$ nA	
5		I_{DSS}	Saturation Drain Current	2.0	20	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 1)	
6		V_{GS}	Gate-Source Voltage	−0.5	−7.5	V	$V_{DS} = 15$ V, $I_D = 200$ µA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		7.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0			

NOTE:

1. Pulse test PW = 300 µs; duty cycle < 3%.

NH

n-channel JFET designed for . . .

Siliconix

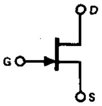
Performance Curves NH
See Section 5

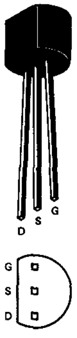
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

BENEFITS

- Low Cost
- Automatic Insertion Package

TO-92
See Section 7





ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . 25 V
Source-Gate Voltage . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . −55 to 135°C
Storage Temperature Range. . . . . −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Characteristic				Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2					−1.0	µA		$T_A = +100°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	$I_G = -10$ µA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−8.0		$V_{DS} = 15$ V, $I_D = 10$ µA	
5		I_{DSS}	Saturation Drain Current	1.5	24	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.5	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.5			
13		NF	Noise Figure		2.5	dB	$V_{DS} = 15$ V, $V_{GS} = 0$, $R_G = 1M\ \Omega$	f = 1 kHz
14					3.0		$V_{DS} = 15$ V, $V_{GS} = 0$, $R_G = 1K\ \Omega$	f = 100 MHz

NOTE:
1. Pulse test, pulse width = 300 µs, duty cycle ≤ 3%.

NH

n-channel JFET designed for . . .

■ General Purpose Amplifiers

■ Analog Switches

Siliconix

Performance Curves NRL
See Section 5

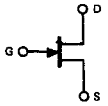
BENEFITS

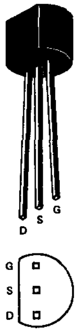
- Low Cost
- Automatic Insertion Package

TO-92
See Section 7

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . .25 V
Source-Gate Voltage . . . . .25 V
Drain-Source Voltage. . . . . .25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . .−55 to 135°C
Storage Temperature Range. . . . .−55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . .300°C





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.01	−1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
2		BV_{GSS}	Gate-Source Breakdown Voltage	−25	−60		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.2		−8.0		$V_{DS} = 15$ V, $I_D = 10\ \mu A$	
4		I_{DSS}	Saturation Drain Current	0.5		24	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	800		6000	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
6		g_{os}	Common-Source Output Conductance		10	75			
7		C_{iss}	Common-Source Input Capacitance		4.5	7.0	pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0			
9		NF	Noise Figure		0.04	2.5	dB	$V_{DS} = 15$ V, $V_{GS} = 0$, $R_G = 1\text{M}\ \Omega$	f = 1 kHz

NOTE:
1. Pulse test PW ≤ 630 ms, duty cycle ≤ 10%.

NRL

n-channel JFET designed for . . .

Siliconix

Performance Curves NRL
See Section 5

- **General Purpose Amplifiers**
- **Analog Switches**

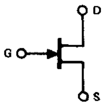
BENEFITS

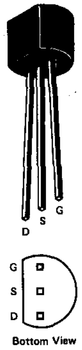
- Low Cost
- Automatic Insertion Package

TO-92
See Section 7

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	20V
Source-Gate Voltage	20V
Drain-Source Voltage	20V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	–55 to 135°C
Storage Temperature Range	–55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate-Reverse Current		–.01	–100	nA	V_{GS} = –10 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	–20			V	I_G = –10 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–10.0		V_{DS} = 10 V, I_D = 1 μA	
4		I_{DSS}	Saturation Drain Current	0.5		20	mA	V_{DS} = 10 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	500			μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Conductance		10				
7		C_{iss}	Common-Source Input Capacitance		4.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0				

NRL

NOTE:
1. Pulse test PW ≤ 630 msec, duty cycle ≤ 10%.

Siliconix

n-channel JFET designed for . . .

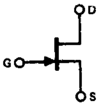
Performance Curves NH
See Section 5

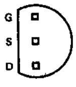
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

BENEFITS

- Low Cost
- Automatic Insertion Package

TO-92
See Section 7





Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . .25 V
Source-Gate Voltage . . . . .25 V
Drain-Source Voltage. . . . . .25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . .360 mW
Operating Temperature Range. . . . .–55 to 135°C
Storage Temperature Range. . . . .–55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . .300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.01	–100	nA	V_{GS} = –10 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	–25			V	I_G = –10 µA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–10.0		V_{DS} = 10 V, I_D = 1 µA	
4		I_{DSS}	Saturation Drain Current	1		25	mA	V_{DS} = 10 V, V_{GS} = 0, (Note 1)	
5		g_{fs}	Common-Source Forward Transconductance	1000		7500	µmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6	DYN	$Re(y_{fs})$	Common-Source Forward Transconductance	800					f = 100 MHz
7		C_{iss}	Common-Source Input Capacitance		3.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.85				

NH

NOTE:
1. Pulse test PW = 300 µs, duty cycle ≤ 3%.

P1086 P1087
P1086-18 P1087-18

p-channel JFETs designed for . . .

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 5

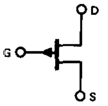
BENEFITS

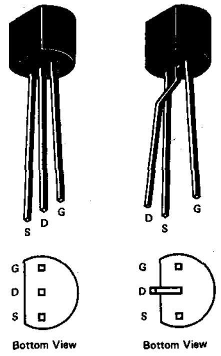
- Low Insertion Loss
  $R_{DS(on)} = 75\,\Omega$ Maximum (P1086E)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 7





(-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	P1086		P1087		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
2		I_{GSS}	Gate Reverse Current		2		2	nA	$V_{GS} = 15$ V, $V_{DS} = 0$	
3		$I_{D(off)}$	Drain Cutoff Current		–10		–10		$V_{DS} = -15$ V, $V_{GS} = 12$ V (P1086E) $V_{GS} = 7$ V (P1087E)	
4					–0.5		–0.5	µA		$T_A = 85°C$
5		I_{DGO}	Drain Reverse Current		2		2	nA	$V_{DG} = -15$ V, $I_S = 0$	
					0.1		0.1	µA		$T_A = 85°C$
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	$V_{DS} = -15$ V, $I_D = -1\ \mu A$	
7		I_{DSS}	Saturation Drain Current	–10		–5		mA	$V_{DS} = -20$ V, $V_{GS} = 0$	
8		$V_{DS(on)}$	Drain-Source ON Voltage		–0.5		–0.5	V	$V_{GS} = 0$, $I_D = -6$ mA (P1086E), $I_D = -3$ mA (P1087E)	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	$I_D = -1$ mA, $V_{GS} = 0$	
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	$I_D = 0$, $V_{GS} = 0$	f = 1 kHz
11		C_{iss}	Common-Source Input Capacitance		45		45	pF	$V_{DS} = -15$ V, $V_{GS} = 0$	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		$V_{DS} = 0$, $V_{GS} = 12$ V (P1086E) $V_{GS} = 7$ V (P1087E)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	$V_{DD} = -6$ V, $V_{GS(on)} = 0$	
14		t_r	Rise Time		20		75		$V_{GS(off)}$ $I_{D(on)}$ R_L	
15		$t_{d(off)}$	Turn-OFF Delay Time		15		25		P1086E 12 V –6 mA 910 Ω	
16		t_f	Fall Time		50		100		P1087E 7 V –3 mA 1.8K Ω	

NOTE:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

PS

n-channel JFETs designed for . . .

Siliconix

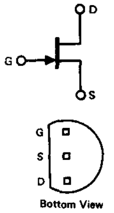
- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC
See Section 5

BENEFITS

- Low Insertion Loss
  High Accuracy in Test Systems
  $R_{ON} < 30\ \Omega$ (PN4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (PN4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

TO-92
See Section 7



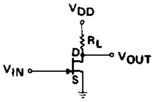
ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage .... -40 V
Gate Current .... 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) .... 360 mW
Operating Temperature Range .... −55 to 135°C
Storage Temperature Range .... −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) .... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4091		PN4092		PN4093		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$		
2		I_{DGO}	*Drain Reverse Current*		200		200		200	pA	$V_{GS} = -20$ V, $I_S = 0$		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20$ V	$V_{GS} = -6$ V	
5									400	nA			150°C
6							200			pA		$V_{GS} = -8$ V	
7							400			nA			150°C
8					200					pA		$V_{GS} = -12$ V	
9					400					nA			150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	$V_{DS} = 20$ V, $I_D = 1$ nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	$V_{DS} = 20$ V, $V_{GS} = 0$		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	$V_{GS} = 0$	$I_D = 2.5$ mA	
13							0.2					$I_D = 4$ mA	
14					0.2							$I_D = 6.6$ mA	
15		$r_{DS(on)}$	*Static Drain-Source ON Resistance*		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
16	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	$V_{DS} = 20$ V, $V_{GS} = 0$		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		$V_{DS} = 0$, $V_{GS} = -20$ V		
19	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	$V_{DD} = 3$ V, $V_{GS(on)} = 0$ $I_{D(on)}$ $V_{GS(off)}$ R_L PN4091 6.6 mA -12 V 425 Ω PN4092 4 -8 700 PN4093 2.5 -6 1120		
20		t_r	Rise Time		10		20		40				
21		t_{off}	Turn-OFF Time		40		60		80				

NOTE:
1. Pulsewidth = 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 μs
PULSE DUTY CYCLE ≤ 10%
PULSE GENERATOR IMPEDANCE 50Ω

NC

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

n-channel JFETs designed for . . .

Siliconix

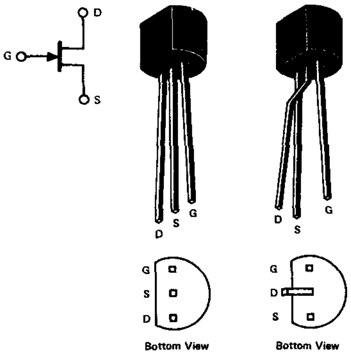
■ General Purpose Amplifiers

**Performance Curves NP
See Section 5**

BENEFITS

- Low Cost
- High Input Impedance
  I_G = 35 pA Typically
- Low Noise
  $\overline{e}_n = 5\ nV/\sqrt{Hz}$ Typically @ 1 kHz

**TO-92
See Section 7**



Bottom View

Bottom View
(-18)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) .... −30V
Gate Current .... 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C)...................... 360 mW
Operating Temperature Range............. −55 to 135°C
Storage Temperature Range............... −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) .... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4302 Min	PN4302 Max	PN4303 Min	PN4303 Max	PN4304 Min	PN4304 Max	Unit	Test Conditons	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		1		−1		−1	nA	$V_{GS} = -10$ V, $V_{DS} = 0$	
2					0.1		−0.1		−0.1	μA		$T_A = 85°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		−30		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4.0		−6.0		−10		$V_{DS} = 20$ V, $I_D = 10$ nA	
5		I_{DSS}	Saturation Drain Current (Note 3)	0.5	5.0	4.0	10	0.5	15	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000		2000		1000		μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		50		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		C_{DG}	Drain-Gate Capacitance		2		2		2		$V_{DG} = 10$ V, $I_S = 0$	f = 140 kHz
11		NF	Noise Figure		2.0		2.0		3.0	dB	$V_{DS} = 10$ V, $V_{GS} = 0$	f = 1 kHz, $R_{gen} = 1.0M\ \Omega$
12		$\|y_{fs}\|$	Common-Source Short Circuit Forward Transadmittance (Note 3)	700		1400		700		μmho	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 10 MHz

NP

NOTES:

1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

n-channel JFETs designed for . . .

Siliconix

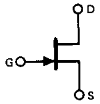
- **Analog Switches**
- **Commutators**
- **Choppers**

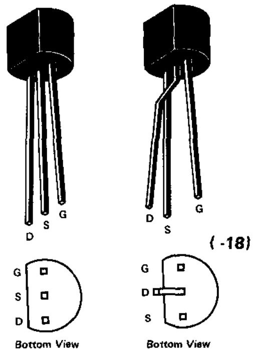
Performance Curves NC
See Section 5

BENEFITS

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Low Cost

TO-92
See Section 7





ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . –40 V
Forward Gate Current . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C *unless otherwise noted*)

		Characteristic		PN4391		PN4392		PN4393		Unit	Test Conditions		
				Min	Max	Min	Max	Min	Max				
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0		–1.0		–1.0	nA	V_{GS} = –20 V, V_{DS} = 0		
2					–200		–200		–200				100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 μA, V_{DS} = 0		
4		$I_{D(off)}$	Drain Cutoff Current						1.0	nA	V_{DS} = 20 V	V_{GS} = –5 V	
5									200				100°C
6							1.0					V_{GS} = –7 V	
7							200						100°C
8					1.0							V_{GS} = –12 V	
9					200								100°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–4	–10	–2	–5	–0.5	–3	V	V_{DS} = 20 V, I_D = 1 nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
13							0.4					I_D = 6 mA	
14					0.4							I_D = 12 mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
16		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, V_{DS} = 0		f = 1 kHz
17	DYN	C_{iss}	Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = –5 V	
19							3.5					V_{GS} = –7V	
20					3.5							V_{GS} = –12 V	
21		$t_{d(on)}$	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0 $I_{D(on)}$ $V_{GS(off)}$ R_L PN4391 12 mA –12 V 800 Ω PN4392 6 –7 1.6K PN4393 3 –5 3.2K		
22	SW	t_r	Rise Time		5		5		5				
23		$t_{d(off)}$	Turn-OFF Delay Time		20		35		50				
24		t_f	Fall Time		15		20		30				

NC

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%.

PN4416

n-channel JFETs designed for . . .

Siliconix

Performance Curves NH
See Section 5

- **VHF Amplifiers**
- **Mixers**

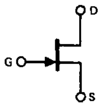
BENEFITS

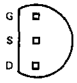
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –30V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . –55 to 135°C
Storage Temperature Range . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 7





Bottom View

			Characteristic	Min	Max	Unit	Test Conditions	
1 2	S T A T I C	I_{GSS}	Gate Reverse Current		1.0	nA	V_{GS} = –15 V, V_{DS} = 0 V	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6		V_{DS} = 15 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	D Y N A M I C	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4			
10		C_{oss}	Common-Source Output Capacitance		2			

			Characteristic	100 MHz		400 MHz		Unit	Test Conditions
				Min	Max	Min	Max		
11	H I G H F R E Q U E N C Y	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000		
13		g_{oss}	Common-Source Output Conductance		75		100		
14		b_{oss}	Common-Source Output Susceptance		1000		4000		
15		g_{fs}	Common-Source Forward Transconductance			4000			
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4		V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

NH

NOTES:
1. Pulse test duration = 300 μs.

n-channel JFET designed for . . .

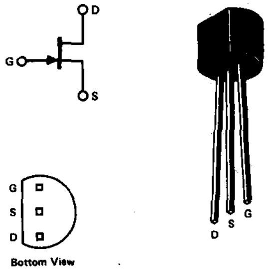
Siliconix

■ Low and Medium Frequency Amplifiers

BENEFITS

- Low Cost

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . −25V
Gate Current (FWD) . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . −55 to 135°C
Storage Temperature Range. . . . . −55 to 150°C
Lead Temperature Range
(1/16″ from case for 10 seconds) . . . . .300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		−10	nA	$V_{GS} = -15$ V, $V_{DS} = 0$		
2					−0.6	μA			$T_A = 85°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	$I_G = -10$ μA, $V_{DS} = 0$		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4	−8.0		$V_{DS} = 15$ V, $I_D = 1$ μA		
5		V_{GS}	Gate-Source Voltage		−7.5		$V_{DS} = 15$ V, $I_D = 100$ μA		
6		I_{DSS}	Saturation Drain Current	1.0	40	mA	$V_{DS} = 15$ V, $V_{GS} = 0$		
7	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		500	Ω	$V_{GS} = 0$, $I_D = 0$		f = 1 kHz
8		g_{fs}	Common-Source Forward Transconductance	2000	9000	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$		
9		g_{os}	Common-Source Output Conductance		200				
10		g_{fs}	Common-Source Forward Transconductance	1800					f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		20	pF			
12		C_{rss}	Common-Source Reverse Transfer Capacitance		5.0				
13		NF	Common-Source Spot Noise Figure		3.0	dB	$V_{DS} = 15$ V, $I_D = 1$ mA	$R_G = 150k\ \Omega$	f = 1 kHz NBW = 150 Hz
14		$\overline{e}_N$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$			

**JEDEC registered data*

n-channel JFET designed for . . .

Siliconix

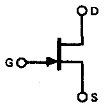
Performance Curves NH
See Section 5

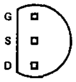
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

BENEFITS

- Specified for 200 MHz Operation

TO-92
See Section 7





Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	30V
Source-Gate Voltage	30V
Drain-Source Voltage	30V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C)	360 mW
Operating Temperature Range	–55 to 135°C
Storage Temperature Range	–55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2					–15	nA		$T_A = +85$°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		V	$I_G = -1$ µA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5	–8.0		$V_{DS} = 15$ V, $I_D = 1$ µA	
5		I_{DSS}	Saturation Drain Current	4.0	25	mA	$V_{DS} = 15$ V, $V_{GS} = 0$ (Note 1)	
6		$r_{DS(on)}$	Drain-Source ON Resistance		300	Ω	$I_D = 1$ mA, $V_{GS} = 0$	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500	10,000	µmhos	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
8		$Re(y_{fs})$	Common-Source Forward Transconductance	4,000				f = 200 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		150			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.0			
13		NF	Noise Figure		3.0	dB	$V_{DS} = 15$ V, $V_{GS} = 0$, $R_G = 1$K Ω	f = 200 MHz
14					5.0		$V_{DS} = 15$ V, $V_{GS} = 0$, $R_G = 1$M Ω, BW = 5 Hz	f = 10 Hz
15		G_{PS}	Common-Source Power Gain	15			$V_{DS} = 15$ V, $V_{GS} = 0$	f = 200 MHz

NOTE:
1. Pulse test PW = 300 µs; duty cycle ≤ 3%.

NH

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

**Performance Curves NC
See Section 5**

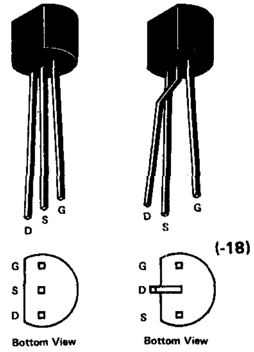
BENEFITS

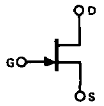
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (U1897E)
- No Error or Offset Voltage Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . −40V
Gate Current . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . 360 mW
Operating Temperature Range . . . . −55 to 135°C
Storage Temperature Range . . . . −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

**TO-92
See Section 7**





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U1897		U1898		U1899		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = -1\ \mu A, V_{DS} = 0$	
2		BV_{DGO}	Drain-Gate Breakdown Voltage	40		40		40			$I_G = -1\ \mu A, I_S = 0$	
3		BV_{SGO}	Source-Gate Breakdown Voltage	40		40		40			$I_G = -1\ \mu A, I_D = 0$	
4		I_{GSS}	Gate Reverse Current		−400		−400		−400	pA	$V_{GS} = -20\ V, V_{DS} = 0$	
5		I_{DGO}	Drain-Gate Leakage Current		200		200		200		$V_{DG} = 20\ V, I_S = 0$	
6		I_{SGO}	Source-Gate Leakage Current		200		200		200		$V_{SG} = 20\ V, I_D = 0$	
7		$I_{D(off)}$	Drain Cutoff Current		200		200		200		$V_{DS} = 20\ V, V_{GS} = -12\ V$ (U1897E) $V_{GS} = -8\ V$ (U1898E) $V_{GS} = -6\ V$ (U1899E)	
8					10		10		10	nA		$T_A = 85°C$
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−5.0	−10	−2.0	−7.0	−1.0	−5.0	V	$V_{DS} = 20\ V, I_D = 1\ nA$	
10		I_{DSS}	Saturation Drain Current (*Note 1*)	30		15		8.0		mA	$V_{DS} = 20\ V, V_{GS} = 0$	
11		$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	$V_{GS} = 0, I_D = 6.6\ mA$ (U1897E) $I_D = 4.0\ mA$ (U1898E), $I_D = 2.5\ mA$ (U1899E)	
12		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$I_D = 1\ mA, V_{GS} = 0$	
13	DYNAMIC	C_{DG}	Drain-Gate Capacitance		5		5		5	pF	$V_{DG} = 20\ V, I_S = 0$	f = 1 MHz
14		C_{SG}	Source-Gate Capacitance		5		5		5		$V_{SG} = 20\ V, I_D = 0$	
15		C_{iss}	Common-Source Input Capacitance		16		16		16		$V_{DS} = 20\ V, V_{GS} = 0$	
16		C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5			
17		$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions	
18		t_r	Rise Time		10		20		40			
19		t_{off}	Turn-OFF Time		40		60		80			

Switching Time Test Conditions

	U1897E	U1898E	U1899E
V_{DD}	3 V	3 V	3 V
$V_{GS(on)}$	0	0	0
$V_{GS(off)}$	−12 V	−8 V	−6 V
R_L	430 Ω	700 Ω	1100 Ω
$I_{D(on)}$	6.6 mA	4 mA	2.5 mA

NOTE:

1. Pulse test pulsewidth = 300 μs; duty cycle ≤ 3%.

NC

n-channel silicon JFET designed for . . .

Siliconix

- **VHF Amplifiers**
- **Mixers**

Performance Curves NH
See Section 5

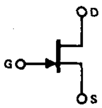
BENEFITS

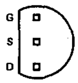
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wideband
  High G_{fs}/C_{iss} Ratio
- Specified for Operation at 400 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . –30V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . 300°C

TO-92
See Section 7





Bottom View

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

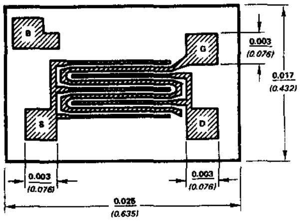
			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–100	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2					–10	nA		$T_A = 100°C$
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		V	$I_G = -1$ μA, $V_{DS} = 0$	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–6	V	$V_{DS} = 15$ V, $I_D = 1$ nA	
5		V_{GS}	Gate-Source Voltage	–1.0	–5.5	V	$V_{DS} = 15$ V, $I_D = 500$ μA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	7500	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		50	μmho		
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1	pF		f = 1 MHz
10		C_{iss}	Common-Source Input Capacitance		4	pF		
11		C_{oss}	Common-Source Output Capacitance		2			

			Characteristic	100 MHz		400 MHz		Unit	Test Conditions
				Min	Max	Min	Max		
12	HI FREQ	g_{iss}	Common-Source Input Conductance		100		1000	μmho	$V_{DS} = 15$ V, $V_{GS} = 0$
13		b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
14		g_{oss}	Common-Source Output Conductance		75		100	μmho	
15		b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
16		g_{fs}	Common-Source Forward Transconductance (Note 1)			4000		μmho	
17		G_{ps}	Common-Source Power Gain	18		10		dB	$V_{DS} = 15$ V, $I_D = 5$ mA
18		NF	Noise Figure		2		4	dB	$V_{DS} = 15$ V, $I_D = 5$ mA, $R_G = 1K\ \Omega$

NOTE:
1. Pulse test duration = 300 μs.

NH

BODY ALSO BACKSIDE CONTACT



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

enhancement-type p-channel MOSFET

designed for . . .

Siliconix

- **Analog and Digital Switching**
- **General Purpose Amplifiers**
- **Smoke Detectors**

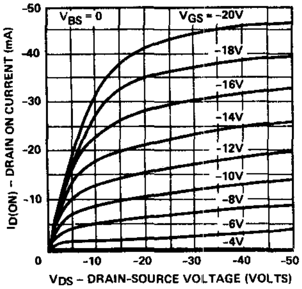
BENEFITS:

- **High Gate Transient Voltage Breakdown Eliminates Need for Gate *Protective Diode***
- **Ultra-High Input Impedance**
- **Low Leakage**
- **Normally OFF**

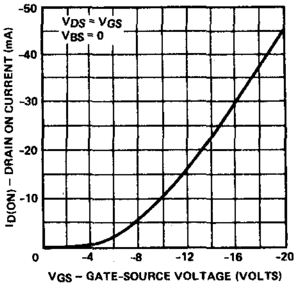
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	MFE823
Single	TO-72	3N163-64
Single	Chip	3N163-64CHP, MFE823CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

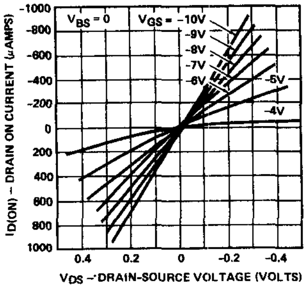
Output Characteristics



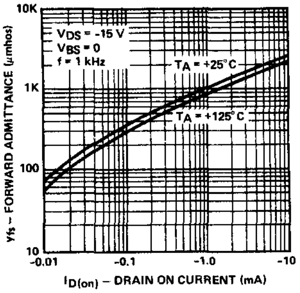
Transfer Characteristic



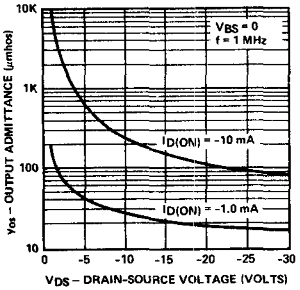
Low-Level Output Characteristics



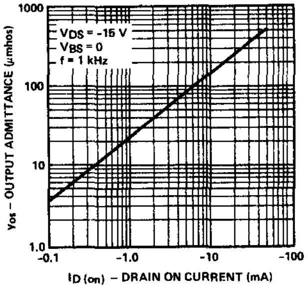
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage

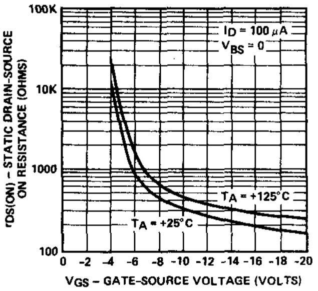


Common-Source, Short-Circuit, Output Admittance vs Drain Current

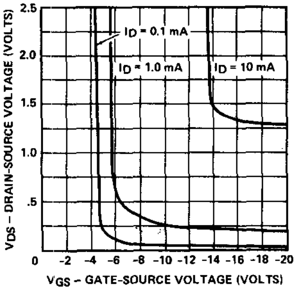


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

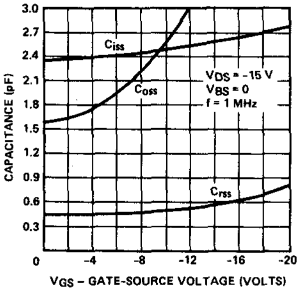
Drain-Source ON Resistance vs Gate-Source Voltage



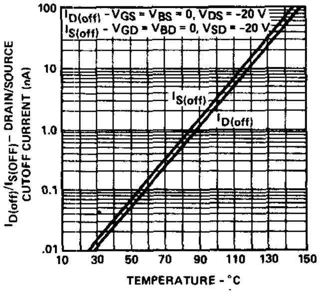
Low-Level ON Drain-Source Voltage vs Gate-Source Voltage

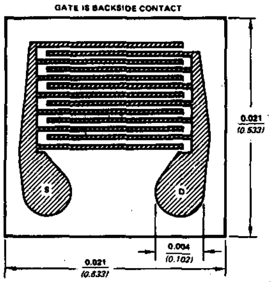


Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFETs designed for . . .

- Analog Switches
- Commutators
- Choppers
- *Integrator Reset Switch*

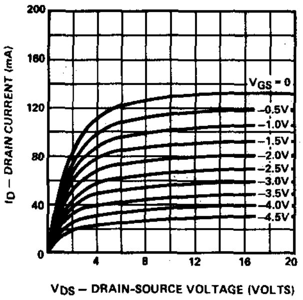
Siliconix

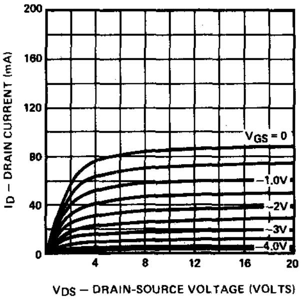
BENEFITS:

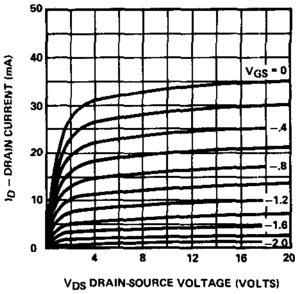
- *No Offset or Error Voltages Generated* by Closed Switch. Purely Resistive. High Isolation Resistance From Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

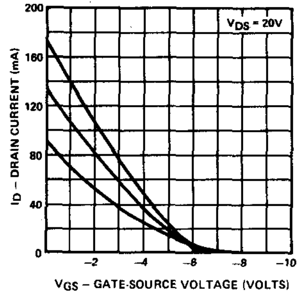
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N3970-72, 2N4091-93, 2N4391-93 2N4856-61, 2N4856A-61A, U200-02, UCR2N
Dual	TO-71	2N5564-66
Single	TO-92	2N5638-40, 2N5653-54, J111-13, PN4091-93, PN4302-04, PN4391-93, U1897-99
	To-92 Lead-form	J111-18 - J113-18, PN4302-18 - PN4304-18, PN4391-18 - PN4393-18, U1897-18 - U1899-18
Single	Chip	All of above single devices
Dual	Chip	2N5566 CHP

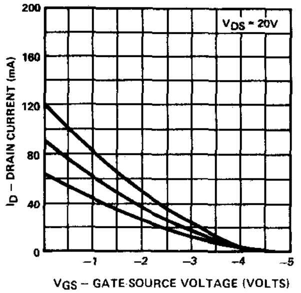
PERFORMANCE CURVES (25°C *unless otherwise* noted)

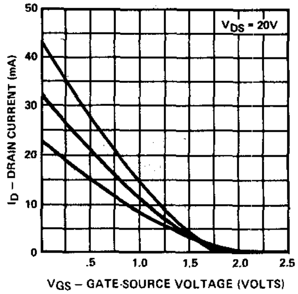

Output Characteristic

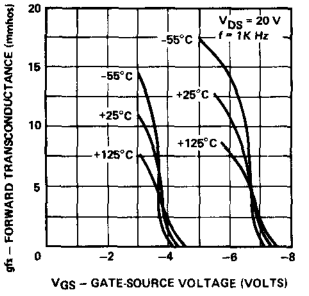

Output Characteristic

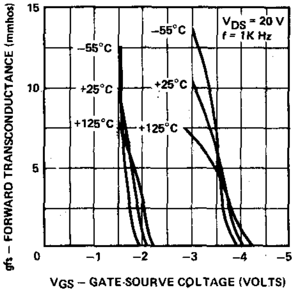

Output Characteristic

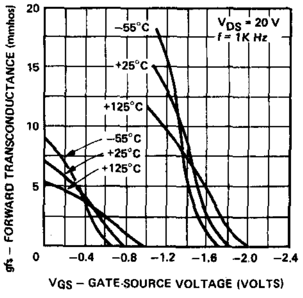

Transfer Characteristics


Transfer Characteristics


Transfer Characteristics

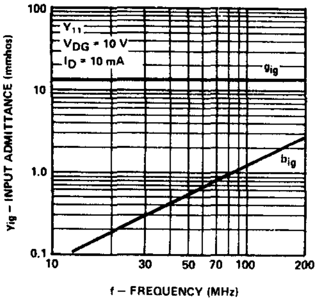

Transconductance Characteristics


Transconductance Characteristics

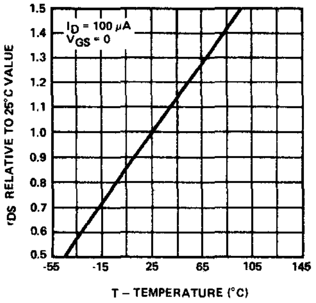

Transconductance Characteristics

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

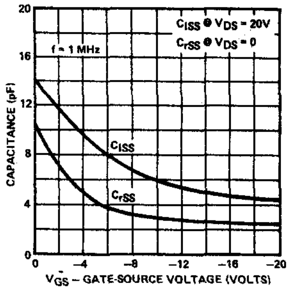
Common-Gate Input Admittance vs Frequency



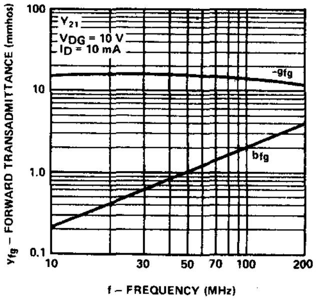
ON Resistance vs Ambient Temperature



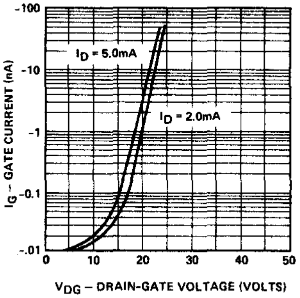
Common-Source Capacitances vs Gate-Source Voltage



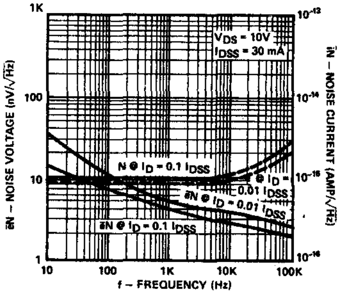
Common-Gate Forward Transadmittance vs Frequency



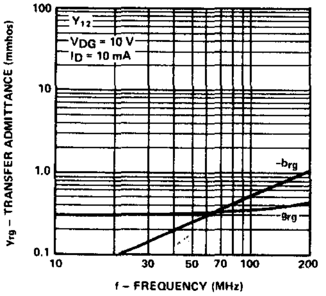
Gate Operating Current vs Drain-Gate Voltage



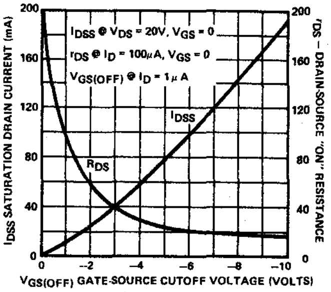
Equivalent Input Noise Voltage and Noise Current vs Frequency



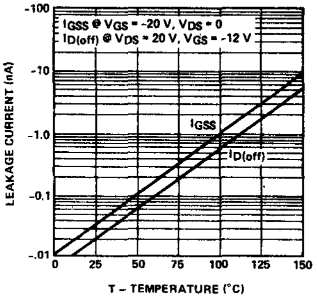
Common-Gate Reverse Transfer Admittance vs Frequency



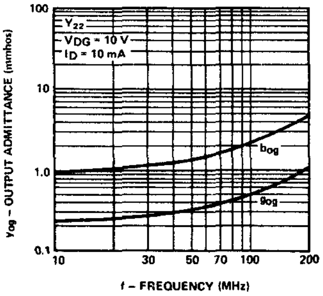
Drain Current & ON Resistance vs Gate-Source Cutoff Voltage



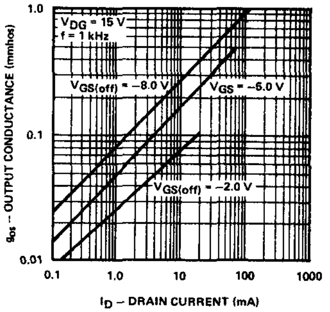
Leakage Current vs Ambient Temperature



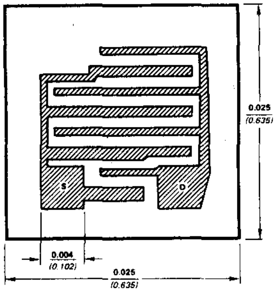
Common-Gate Output Admittance vs Frequency



Common-Source Output Conductance vs Drain Current



GATE IS BACKSIDE CONTACT.
SOURCE AND GATE ARE COMMON.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET current regulator diode
designed for . . .

Siliconix

- Current Regulation
- Current Limiting
- Biasing

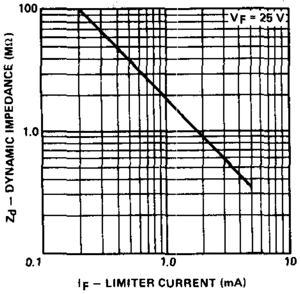
BENEFITS:

- Simple Two Lead Current Source
- Simplifies Floating Current Sources
  No Power Supplies Required
- Low Cost

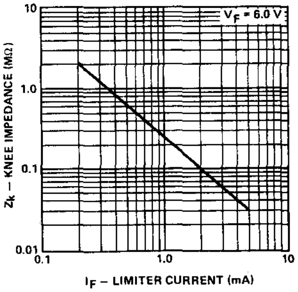
TYPE	PACKAGE	*PRINCIPAL DEVICES*
Single	TO-92	J500-505, J506-511
Single	Chip	J500CHP-505CHP, J506CHP-511CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

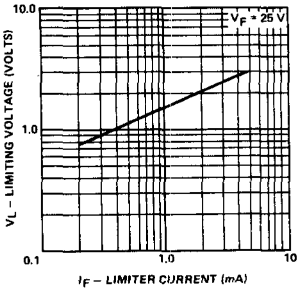
Dynamic Impedance vs
Limiter Current



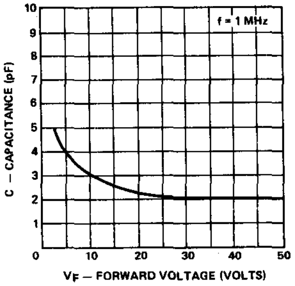
Knee Impedance vs Limiter Current



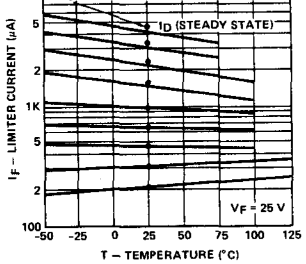
Limiting Voltage at 0.9 I_D vs
Limiter Current

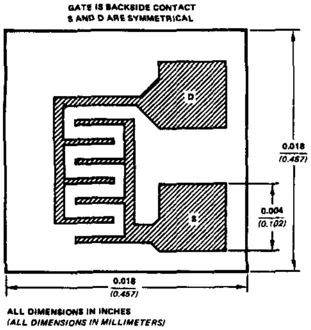


Capacitance vs Forward Voltage



Typical Variation of I_D with Temperature
Steady State and Pulsed Value





n-channel JFET

designed for . . .

Siliconix

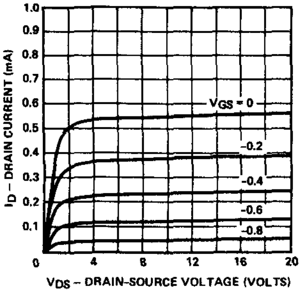
- **Low and Medium Frequency Single and Differential Amplifiers**
- **High Input Impedance Amplifiers**

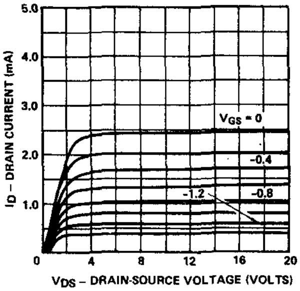
BENEFITS:

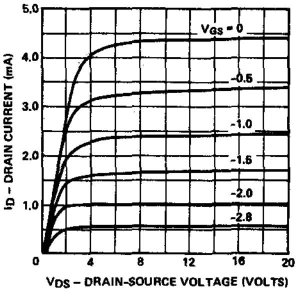
- **Wide Dynamic Range**
  I_G Specified @ V_{DG} = 20 V
- **Low Capacitance $C_{iss} < 4$ pF**
- **Low Output Conductance**

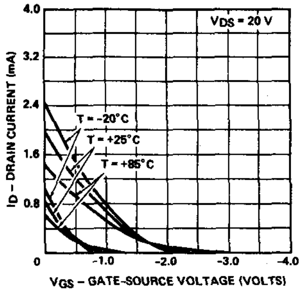
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N3954, 2N3954A, 2N3955, 2N3955A, 2N3956-8, 2N5452-54
Single	TO-72	2N3684-7
Dual	Chip	2N3955CHP, 2N3956CHP-8CHP, 2N5454CHP
Single	Chip	2N3684CHP-7CHP

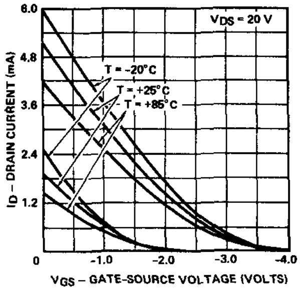
PERFORMANCE CURVES (25°C unless otherwise noted)

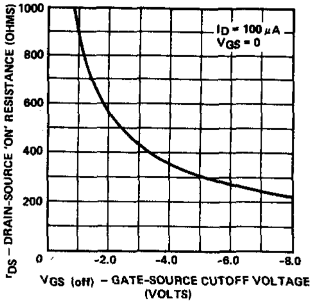

Output Characteristic

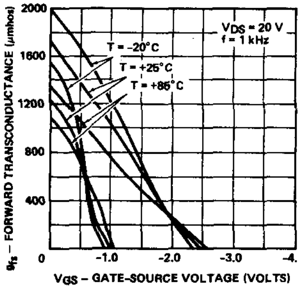

Output Characteristic

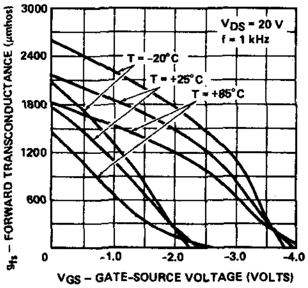

Output Characteristic

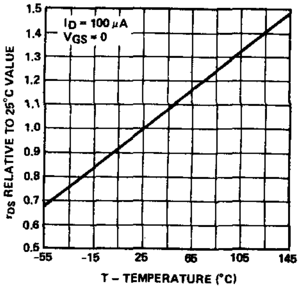

Transfer Characteristics


Transfer Characteristics


Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage

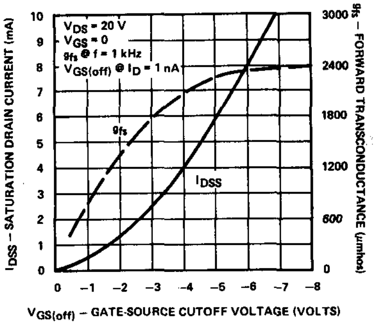

Transconductance Characteristics


Transconductance Characteristics

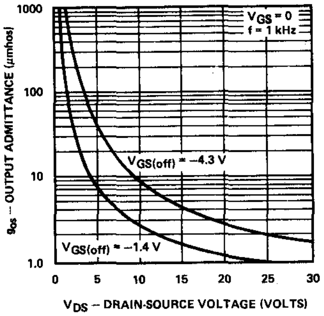

'ON' Resistance vs Ambient Temperature

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

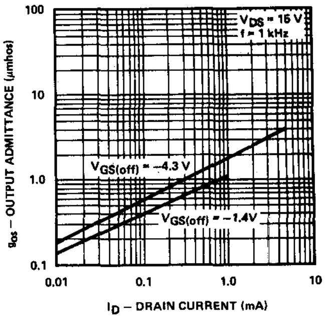
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



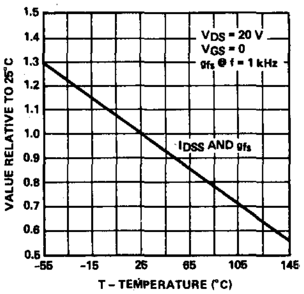
Common-Source Output Conductance vs Drain-Source Voltage



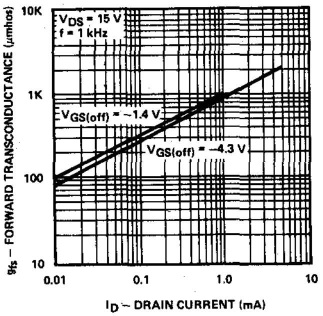
Common-Source Output Conductance vs Drain Current



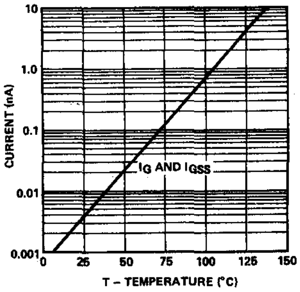
Drain Current and Transconductance vs Ambient Temperature



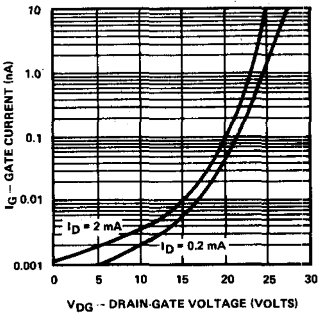
Common-Source Forward Transconductance vs Drain Current



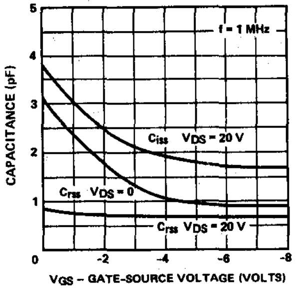
Leakage Currents vs Ambient Temperature



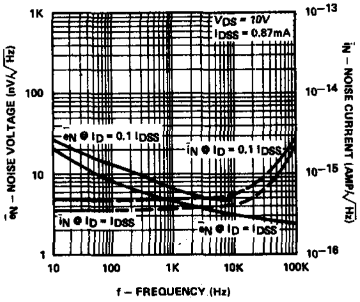
Gate Operating Current vs Drain-Gate Voltage

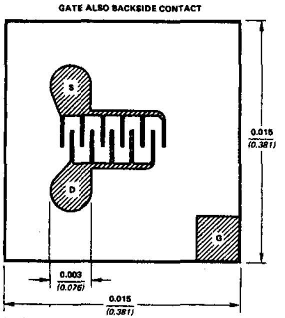


Common-Source Input Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**
- **Low Input Capacitance High Speed Switch**

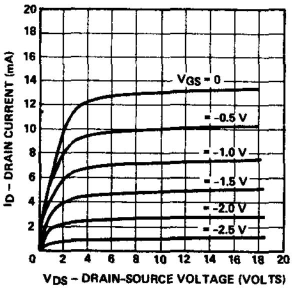
BENEFITS:

- **Low Noise**
  NF = 3 dB Typical @ 400 MHz
- **Wideband**
  High g_{fs}/C_{iss} Ratio

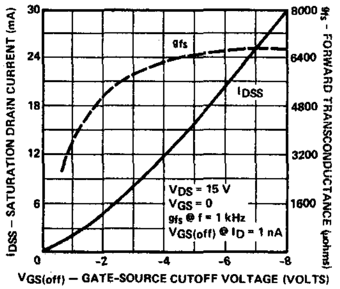
TYPE	**PACKAGE**	**PRINCIPAL DEVICES**
Single	TO-72	2N3966, 2N4416-16A
Single	TO-92	2N5484-6, 2N5555, 2N5668-70, MPF102, MPF108, MPF112, PN4416, J304-5, U1837, U1994
Single	TO-92 Lead-form	KK4416-18, K304-18, KK305-18, K1837-18
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

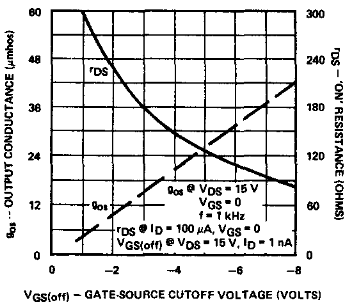
Output Characteristic



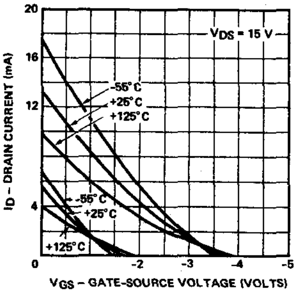
Drain Current & Transconductance vs Gate-Source Voltage



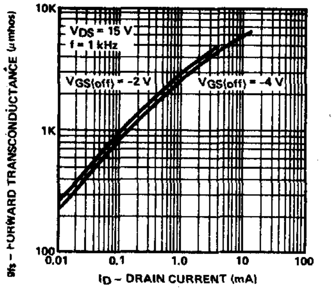
'ON' Resistance & Output Conductance vs Gate-Source Cutoff Voltage



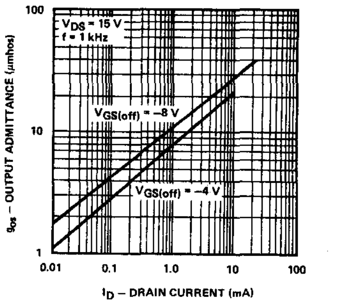
Transfer Characteristics



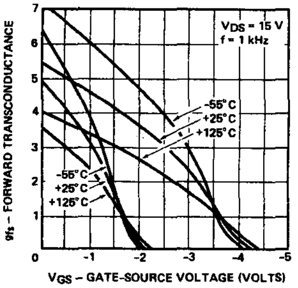
Common-Source Forward Transconductance vs Drain Current



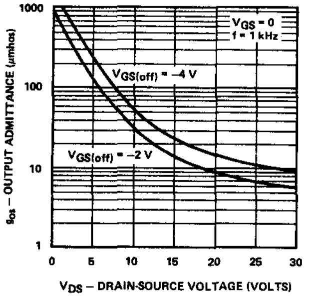
Common-Source Output Conductance vs Drain Current



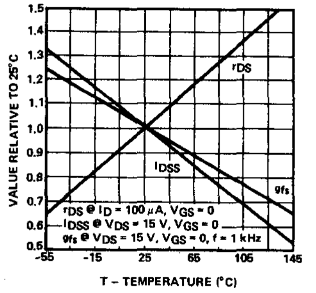
Transconductance Characteristics



Common-Source Output Conductance vs Drain-Source Voltage

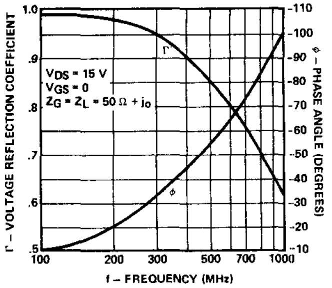


Drain Current, Transconductance and 'ON' Resistance vs Ambient Temperature

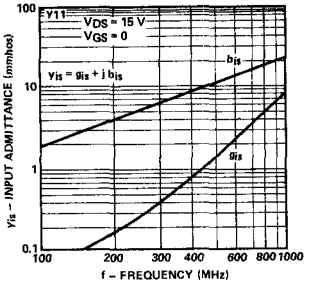


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

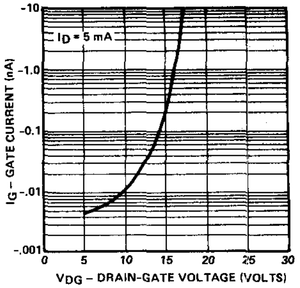
S Parameters S_{11} Common-Source vs Frequency



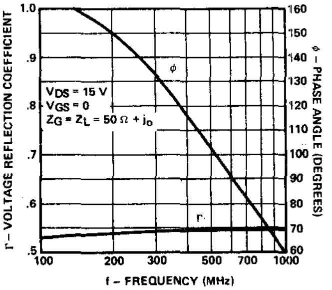
Common-Source Input Admittance vs Frequency



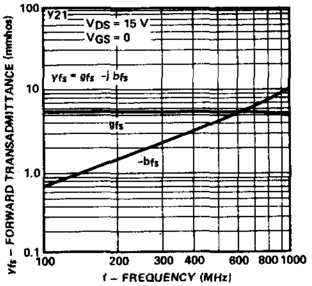
Gate Operating Current vs Drain-Gate Voltage



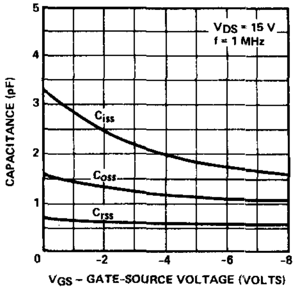
S Parameters S_{21} Common-Source vs Frequency



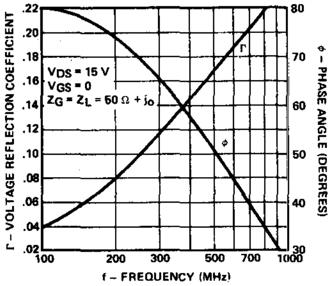
Common-Source Forward Transadmittance vs Frequency



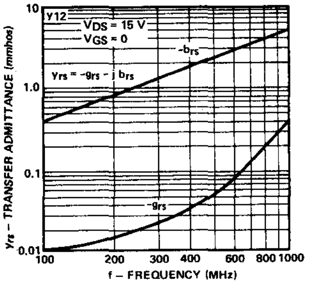
Common-Source Capacitances vs Gate-Source Voltage



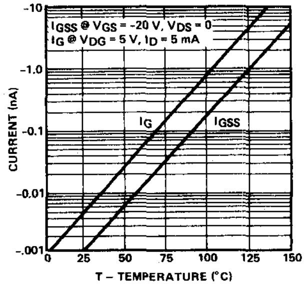
S Parameters S_{12} Common-Source vs Frequency



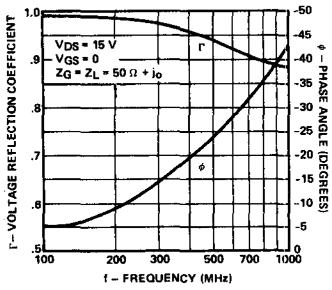
Common-Source Reverse Transfer Admittance vs Frequency



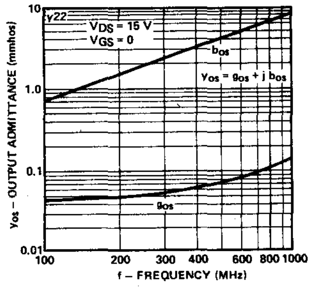
Gate Current vs Ambient Temperature



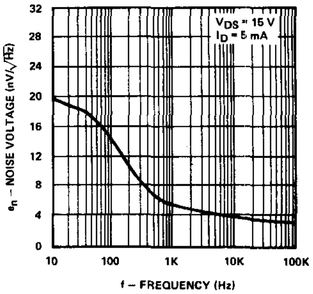
S Parameters S_{22} Common-Source vs Frequency

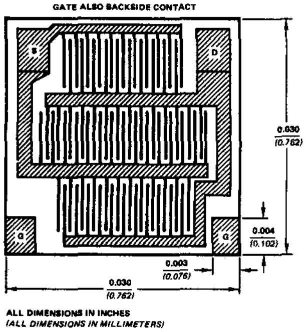


Common-Source Output Admittance vs Frequency



Equivalent Input Noise Voltage vs Frequency





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

Siliconix

n-channel JFET
designed for . . .

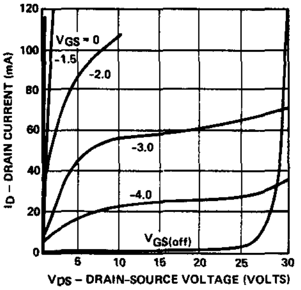
- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

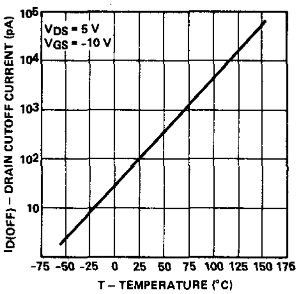
BENEFITS:

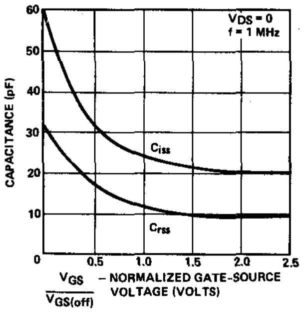
- Low Insertion Loss
- Small Error in Measurement Systems $V_{DS(on)} < 50$ mV (2N5432)
- High Off-Isolation $I_{D(off)} < 200$ pA
- High Speed $t_{d(on)} < 4$ ns
- Low Noise Audio-Freq Amplification $e_N < 2\ nV/\sqrt{Hz}$ at 1 kHz

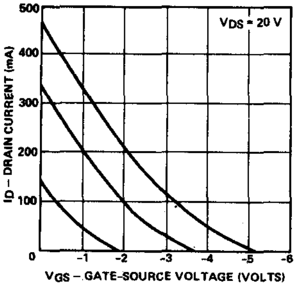
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-39	U320-2
Single	TO-52	2N5432-34
Single	TO-92	J108-10
Single	TO-92 Lead-form	J108-18 -110-18
Single	Chip	All of the above devices

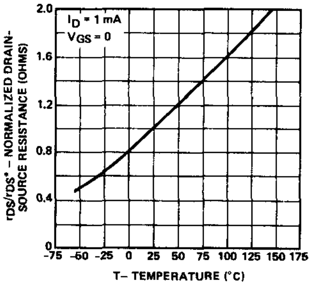
PERFORMANCE CURVES (25°C unless otherwise noted)

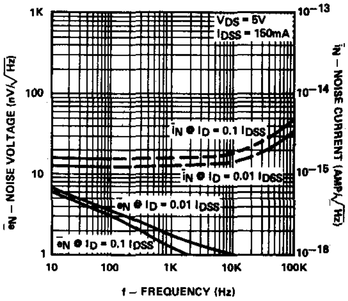

Output Characteristic

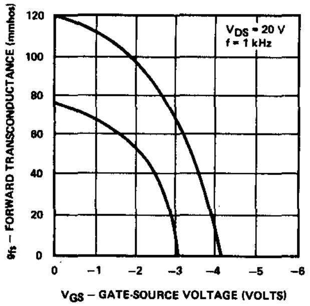

Drain Cutoff Current vs Ambient Temperature

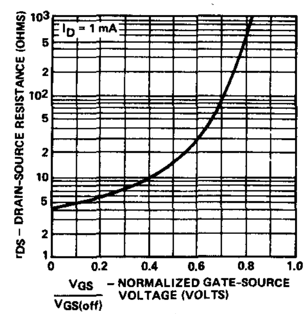

Common-Source Capacitance vs Normalized Gate-Source Voltage

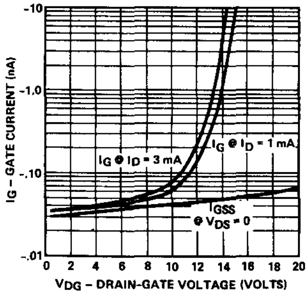

Transfer Characteristics


ON Resistance vs Ambient Temperature


Equivalent Input Noise Voltage and Noise Current vs Frequency

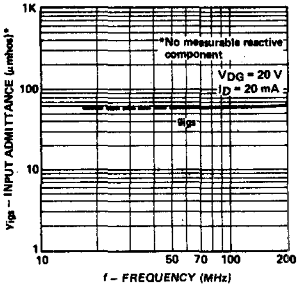

Forward Transconductance vs Drain Current


Resistance vs Normalized Gate-Source Voltage

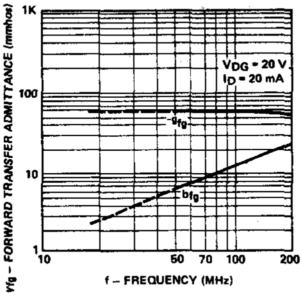

Gate Currents vs Drain-Gate Voltage

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

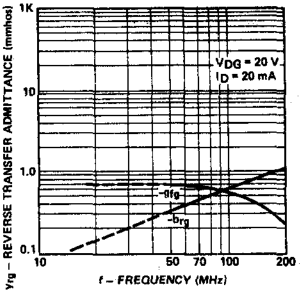
Input Admittance Common Gate vs Frequency



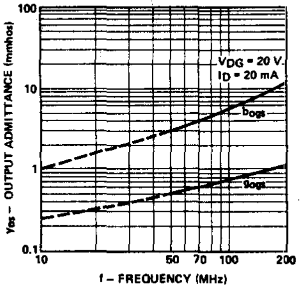
Forward Transfer Admittance Common Gate vs Frequency



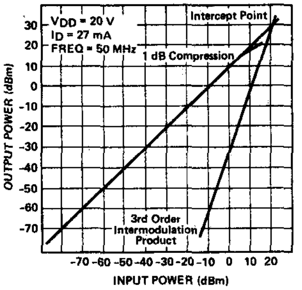
Reverse Transfer Admittance Common Gate vs Frequency



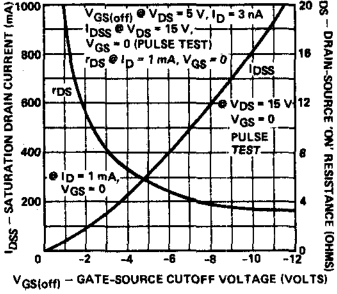
Output Admittance Common Gate vs Frequency

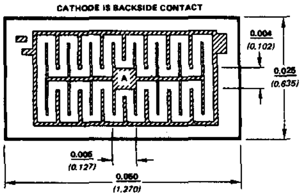


Gain – Intermodulation Characteristics



Drain Current & 'ON' Resistance vs Gate-Source Voltage





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET current regulator diode

designed for . . .

Siliconix

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

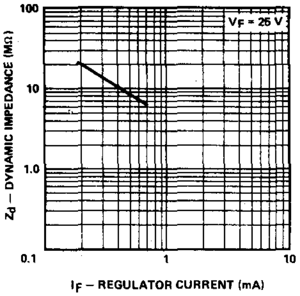
BENEFITS:

- **Simple Two Lead Current Source**
- **Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices**
- **TO-18 Package for Improved Current Control**
- **Simplifies Floating Current Sources No Power Supplies Required**

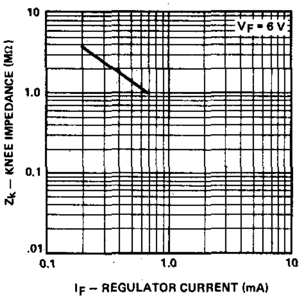
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR022 Thru CR062, U508
Single	Chip	CR022CHP Thru CRO62CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

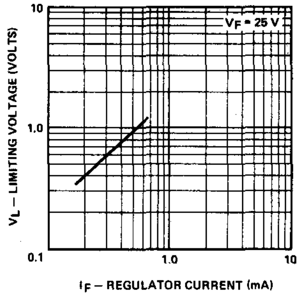
Dynamic Impedance vs Regulator Current



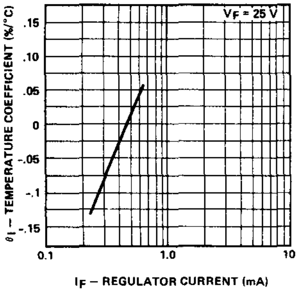
Knee Impedance vs Regulator Current



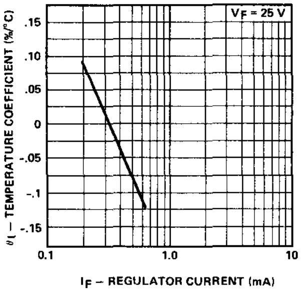
Limiting Voltage @ 0.8 I_F vs Regulator Current



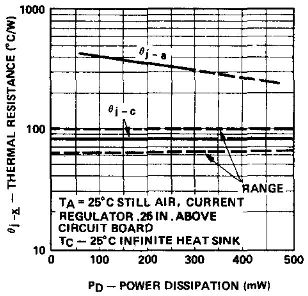
Temperature Coefficient -55°C ⩽ T_j ⩽ 25°C vs Regulator Current



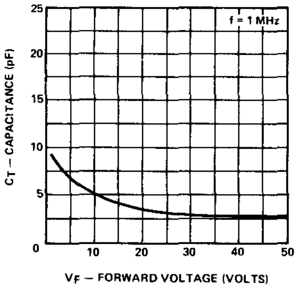
Temperature Coefficient 25°C ⩽ T_j ⩽ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation

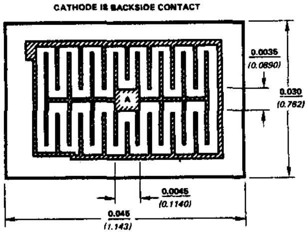


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a} P_D = T_{case} + \theta_{j\text{-}c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET current regulator diode

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- Current Limiting
- Biasing
- Low Voltage References

Siliconix

BENEFITS:

- Simple Two Lead Current Source
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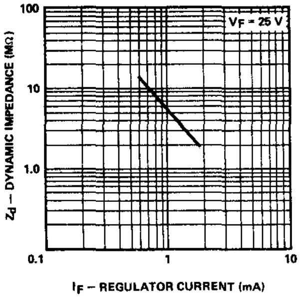
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

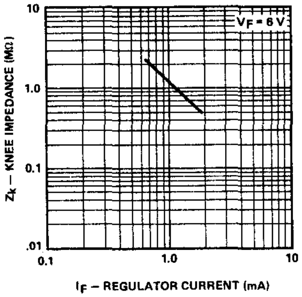
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR068 Thru CR150
Single	Chip	CR068CHP Thru CR150CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

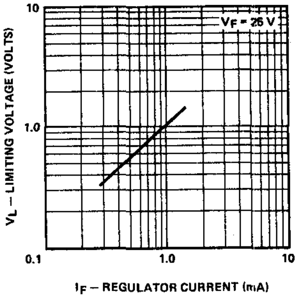
Dynamic Impedance vs Regulator Current



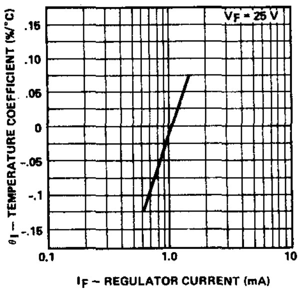
Knee Impedance vs Regulator Current



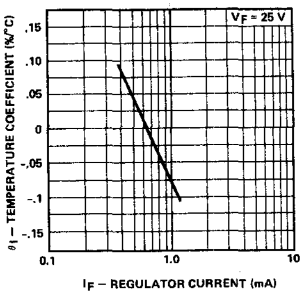
Limiting Voltage @ 0.8 I_F vs Regulator Current



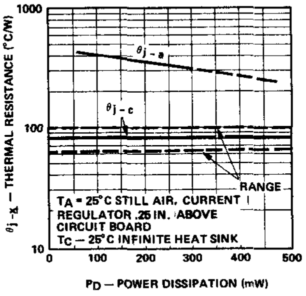
Temperature Coefficient $-55°C \leq T_j \leq 25°C$ vs Regulator Current



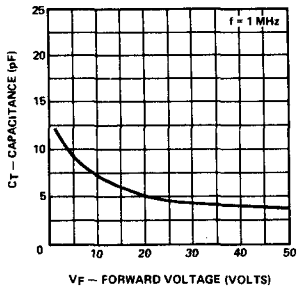
Temperature Coefficient $25°C \leq T_j \leq 125°C$ vs Regulator Current



Thermal Resistance vs Power Dissipation

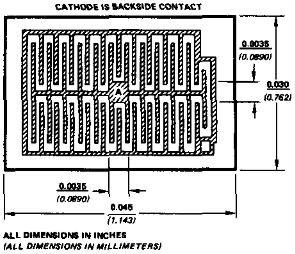


Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the *temperature coefficient of I_F and T_j is the junction temperature.*

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a} P_D = T_{case} + \theta_{j\text{-}c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Siliconix

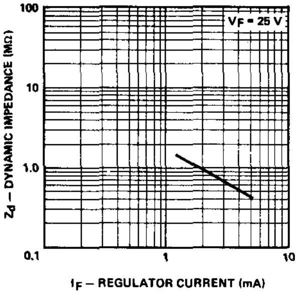
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

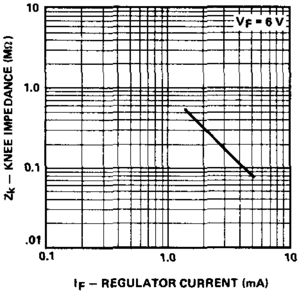
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR160 Thru CR470
Single	Chip	CR160CHP Thru CR470CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

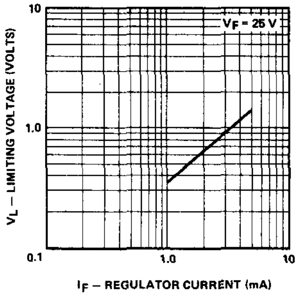
Dynamic Impedance vs Regulator Current



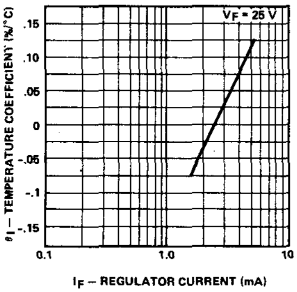
Knee Impedance vs Regulator Current



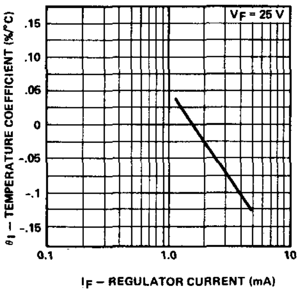
Limiting Voltage @ 0.8 I_F vs Regulator Current



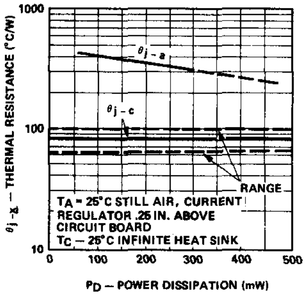
Temperature Coefficient -55°C ≤ T_j ≤ 25°C vs Regulator Current



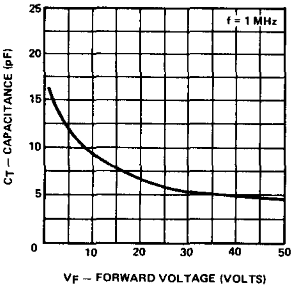
Temperature Coefficient 25°C ≤ T_j ≤ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation

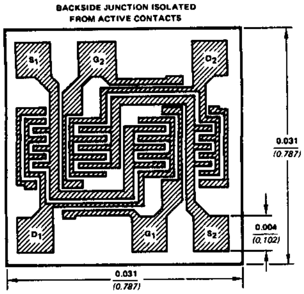


Capacitance vs Forward Voltage



NOTE: **I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.**

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a} P_D = T_{case} + \theta_{j\text{-}c} P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

monolithic dual n-channel JFET *designed for . . .*

Siliconix

- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

BENEFITS:

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5196)
- Low Drift With Temperature
  5 μV/°C Maximum (2N5196)

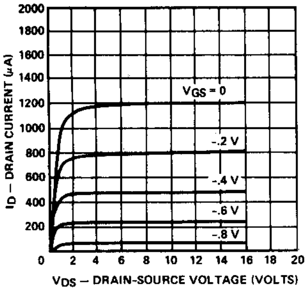
TYPE	PACKAGE
Dual	TO-71
Dual	Chip

PRINCIPAL DEVICES

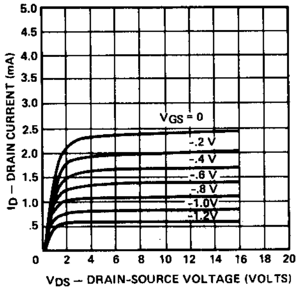
2N5196-9, 2N5545-47, U231-35
2N5199CHP, U232CHP-35CHP
2N5547CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

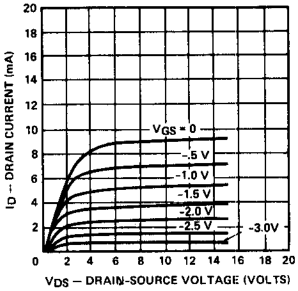
Output Characteristics
Low $V_{GS(off)}$ Unit



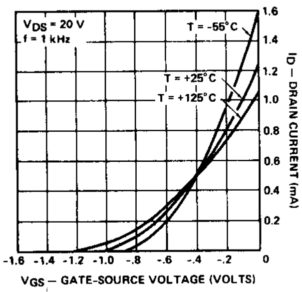
Output Characteristics
Medium $V_{GS(off)}$ Unit



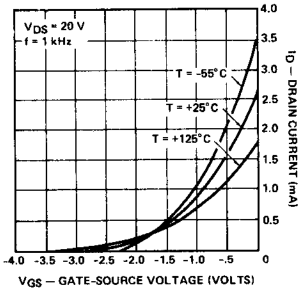
Output Characteristics
High $V_{GS(off)}$ Unit



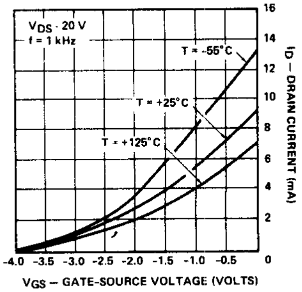
Transfer Characteristics
Low $V_{GS(off)}$



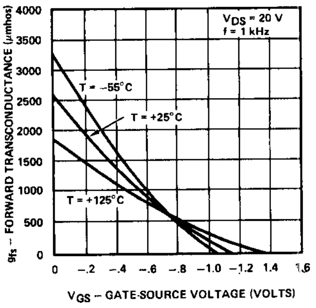
Transfer Characteristics
Medium $V_{GS(off)}$



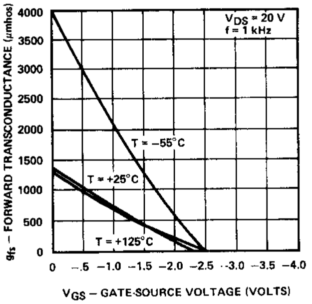
Transfer Characteristics
High $V_{GS(off)}$



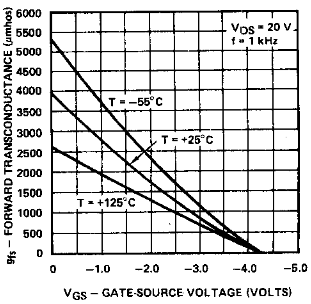
Transconductance Characteristics
Low $V_{GS(off)}$



Transconductance Characteristics
Medium $V_{GS(off)}$



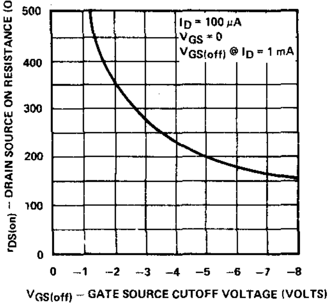
Transconductance Characteristics
High $V_{GS(off)}$



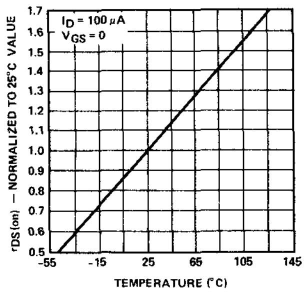
5

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

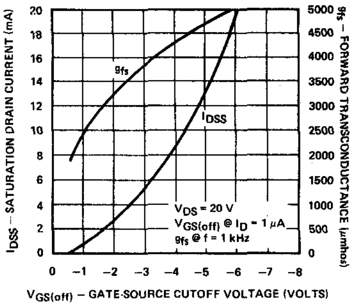
Static Drain-Source ON Resistance vs Gate-Source Cutoff Voltage



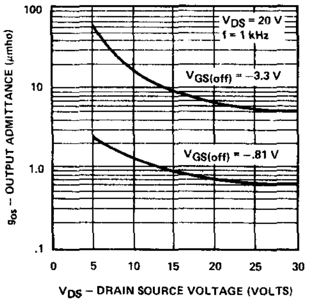
Normalized ON Resistance vs Ambient Temperature



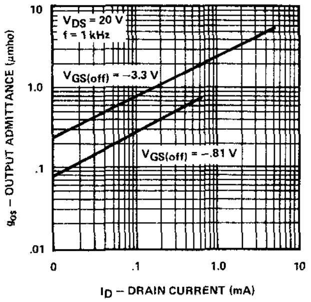
I_{DSS} and g_{fs} vs Gate-Source Cutoff Voltage



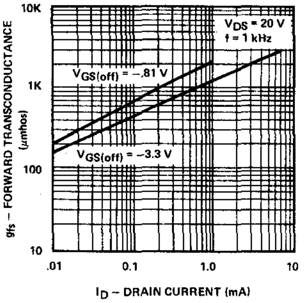
Common-Source Output Conductance vs Drain-Source Voltage



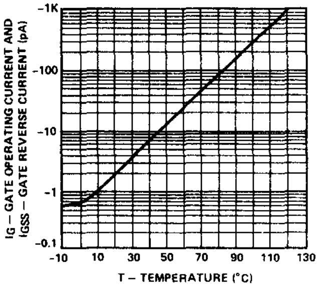
Common-Source Output Conductance vs Drain Current



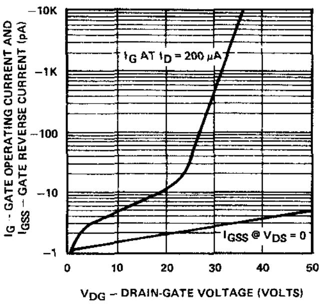
Common Source Forward Transconductance vs Drain Current



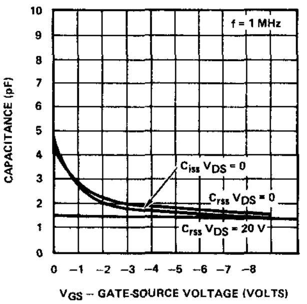
Gate Leakage Currents vs Ambient Temperature



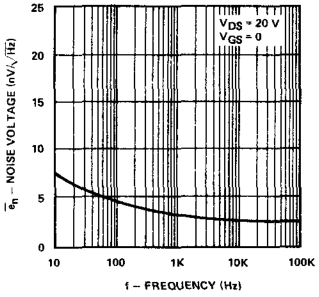
Gate Leakage Currents vs Drain-Gate Voltage

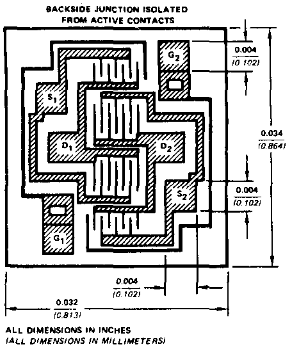


Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage vs Frequency





monolithic dual n-channel JFET designed for . . .

Siliconix

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- *Precision Instrumentation Amplifiers*
- Comparators

BENEFITS:

- **Minimum System Error and Calibration**
  5 mV Offset Maximum (J401)
  95 dB Minimum CMRR
- **Low Drift With Temperature**
  10 μV/°C (J401)
- **Simplifies Amplifier Design**
  Output Conductance < 2 μmho
- **Low Noise**
  $\bar{e}_n$ = 6 nV/$\sqrt{Hz}$ at 10 Hz Typical

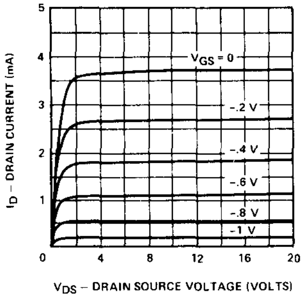
TYPE	PACKAGE
Dual	TO-71
Dual	Chip

PRINCIPAL DEVICES

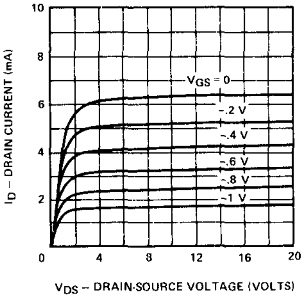
2N3921-2, 2N4084-5, 2N5045-7, U401-6
2N4085CHP, 2N5046CHP-47CHP,
U403CHP-06CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

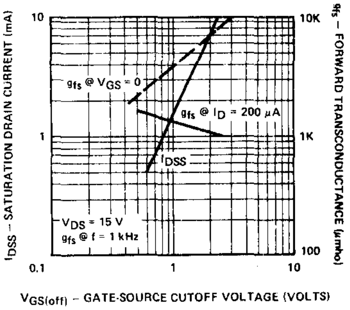
Output Characteristics
Low $V_{GS(off)}$ Unit (−1.5 V)



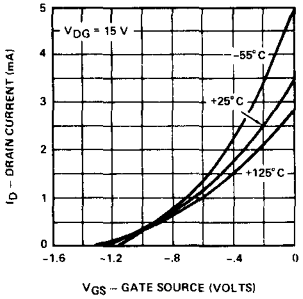
Output Characteristics
Medium $V_{GS(off)}$ Unit (−2.2 V)



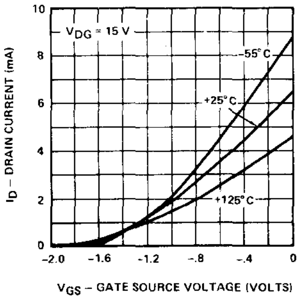
Drain Current and Transconductance vs
Gate-Source Cutoff Voltage



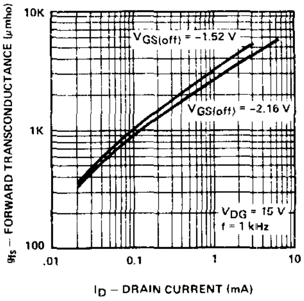
Transfer Characteristics
Low $V_{GS(off)}$ Unit (−1.5 V)



Transfer Characteristics
Medium $V_{GS(off)}$ Unit (−2.2 V)

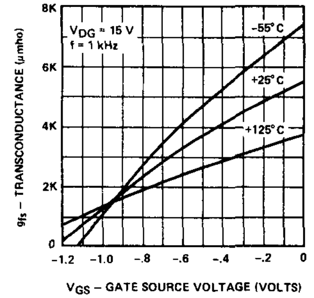


Forward Transconductance
vs Drain Current

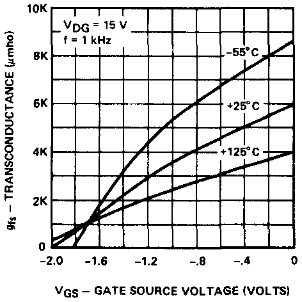


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

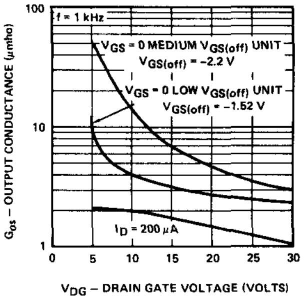
Transconductance vs Gate Source Voltage Low $V_{GS(off)}$ Unit (−1.5 V)



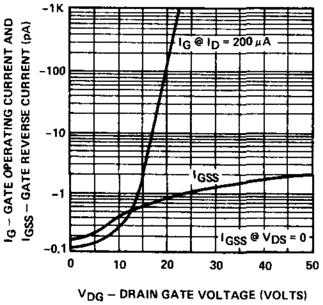
Transconductance vs Gate Source Voltage Medium $V_{GS(off)}$ Unit (−2.2 V)



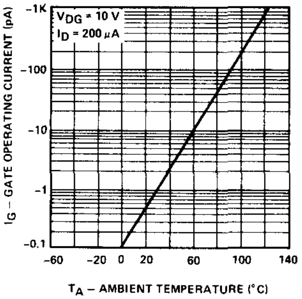
Output Conductance vs Drain Gate Voltage



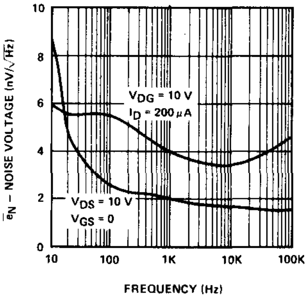
Gate Operating Current vs Drain Gate Voltage



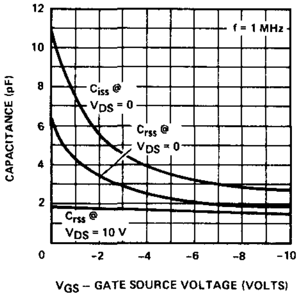
Gate Operating Current vs Ambient Temperature



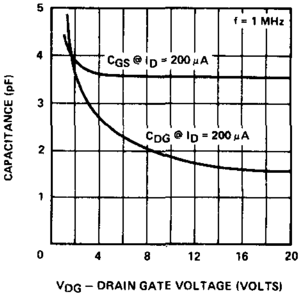
Equivalent Short Circuit Input Noise vs Frequency

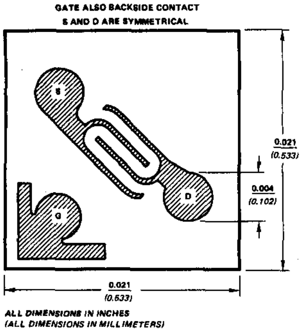


Capacitance vs Gate Source Voltage



Capacitance vs Drain to Gate Voltage





Siliconix

n-channel JFET designed for . . .

- Small Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

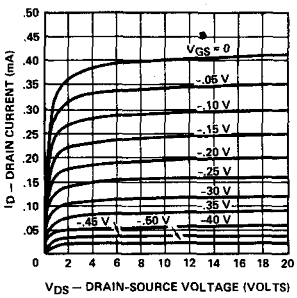
BENEFITS:

- Low Noise NF < 1 dB at 1 kHz
- Operation From Low Power Supply Voltages, $V_{GS(off)} < 1$ V (2N4338)
- High Off-Isolation As a Switch $I_{D(off)} < 50$ pA
- High Input Impedance

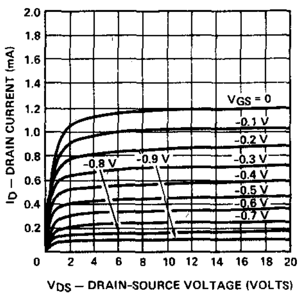
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N3368-70, 2N3436-8, 2N3458-60, 2N4338-41, VCR4N
Dual	TO-71	2N5196-9, U231-5, 2N5545-47
Single	TO-92	J201-203, J204, PN4302-04
Single	TO-92 Lead-form	J201-18 - 203-18, J204-18,
		All of the above
Single	Chip	PN4302-18 - 4304-18

PERFORMANCE CURVES (25°C unless otherwise noted)

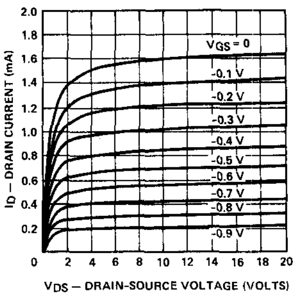
Output Characteristic



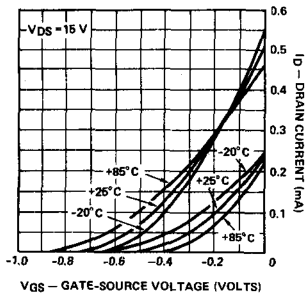
Output Characteristic



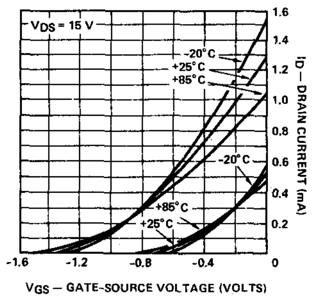
Output Characteristic



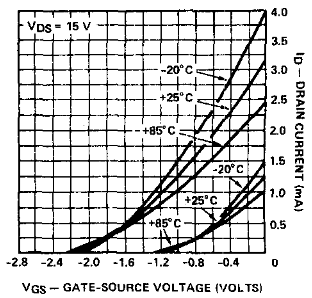
Transfer Characteristics



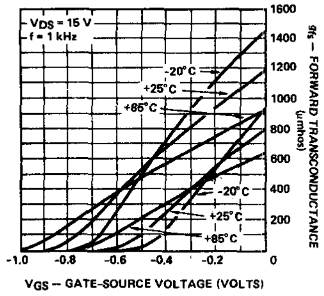
Transfer Characteristics



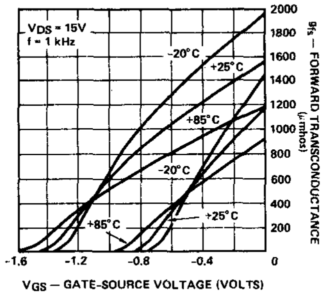
Transfer Characteristics



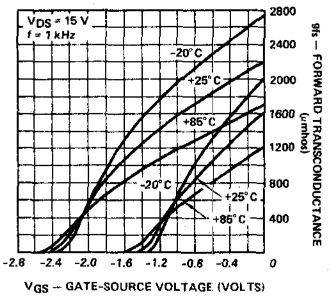
Transconductance Characteristics



Transconductance Characteristics

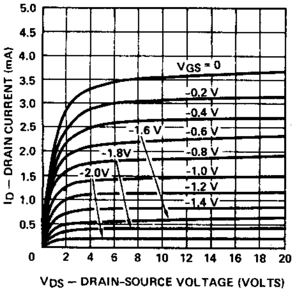


Transconductance Characteristics

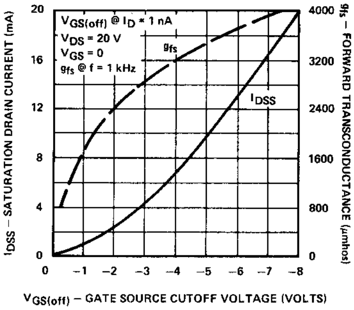


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

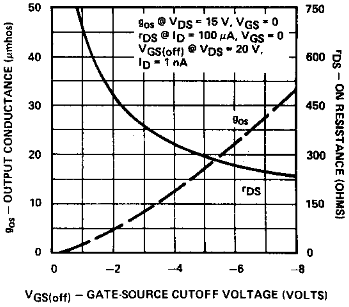
Output Characteristic



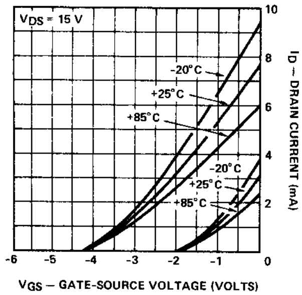
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



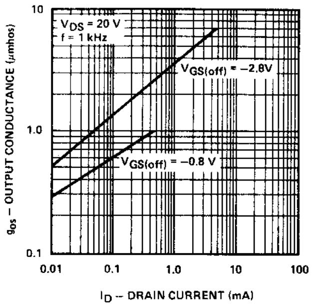
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



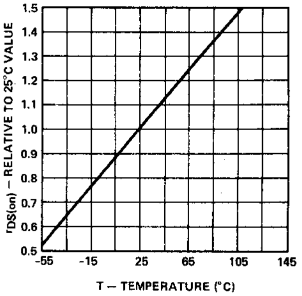
Transfer Characteristics



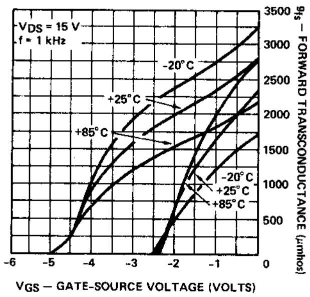
Common-Source Output Conductance vs Drain Current



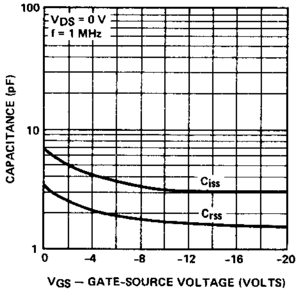
ON Resistance vs Ambient Temperature



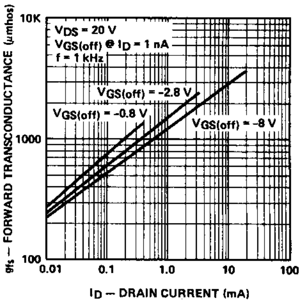
Transconductance Characteristics



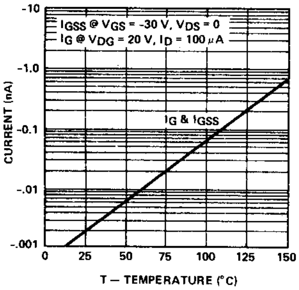
Common-Source Capacitances vs Gate-Source Voltage



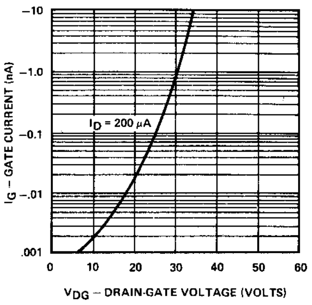
Common-Source Forward Transconductance vs Drain Current



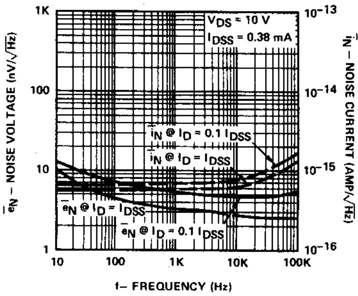
Gate Currents vs Ambient Temperature

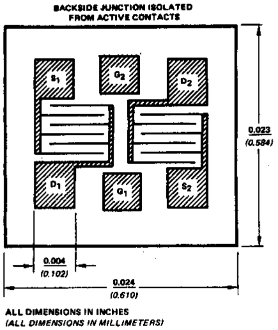


Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency





monolithic dual n-channel JFET designed for . . .

Siliconix

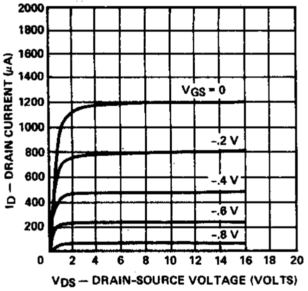
- General Purpose Differential Amplifiers

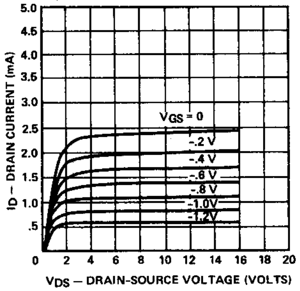
BENEFITS:

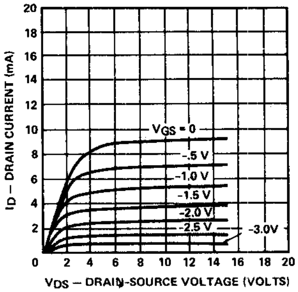
- Low Cost
- High Input Impedance

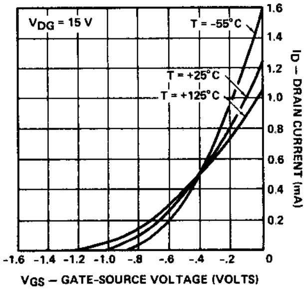
TYPE	**PACKAGE**	**PRINCIPAL DEVICES**
Dual	TO-71	U410-12
Dual	Chip	U411CHP, U412CHP

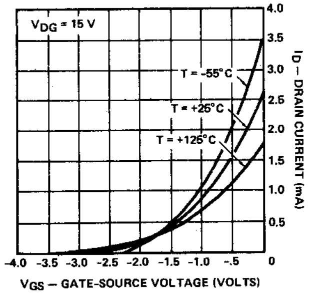
PERFORMANCE CURVES (25°C unless otherwise noted)

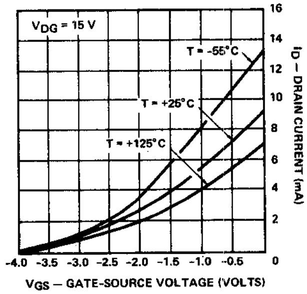

Output Characteristics Low $V_{GS(off)}$ Unit

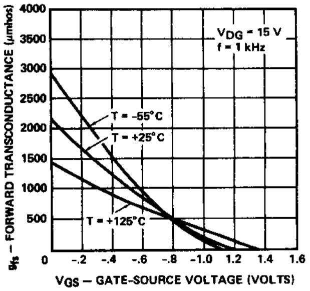

Output Characteristics Medium $V_{GS(off)}$ Unit

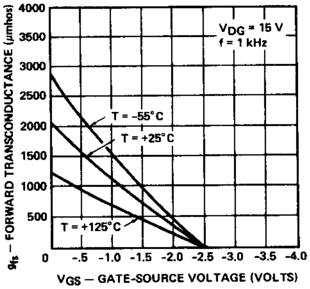

Output Characteristics High $V_{GS(off)}$ Unit

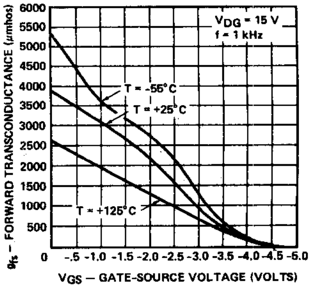

Transfer Characteristics Low $V_{GS(off)}$


Transfer Characteristics Medium $V_{GS(off)}$


Transfer Characteristics High $V_{GS(off)}$

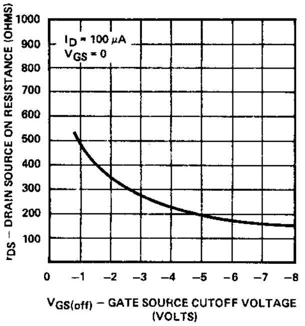

Transconductance Characteristics Low $V_{GS(off)}$


Transconductance Characteristics Medium $V_{GS(off)}$

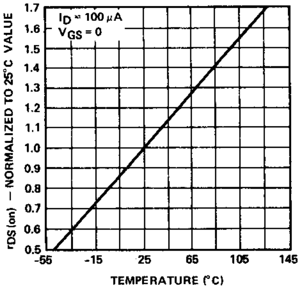

Transconductance Characteristics High $V_{GS(off)}$

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

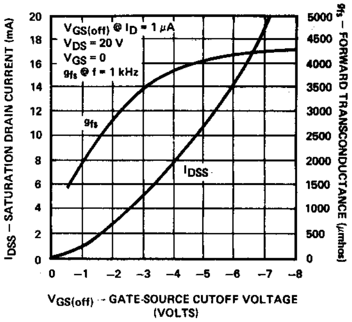
Static Drain-Source ON Resistance vs Gate-Source Cutoff Voltage



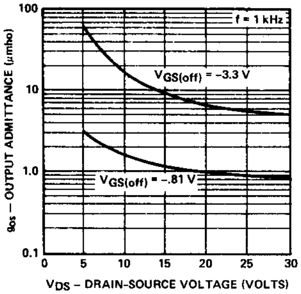
Normalized ON Resistance vs Ambient Temperature



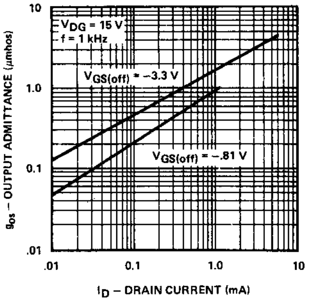
I_{DSS} and g_{fs} vs Gate-Source Cutoff Voltage



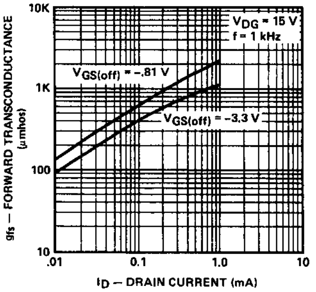
Common Source Output Admittance vs Drain-Source Voltage



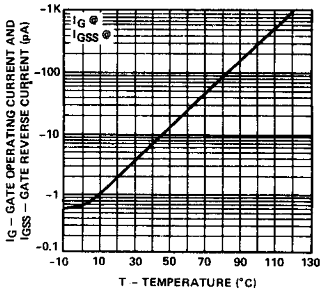
Common-Source Output Conductance vs Drain Current



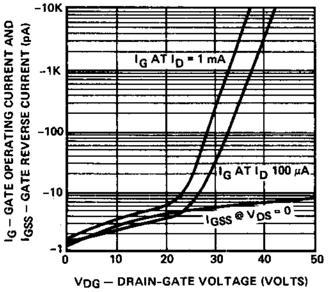
Common Source Forward Transconductance vs Drain Current



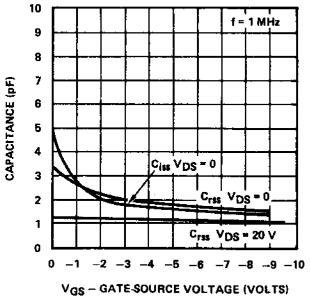
Leakage Current vs Ambient Temperature



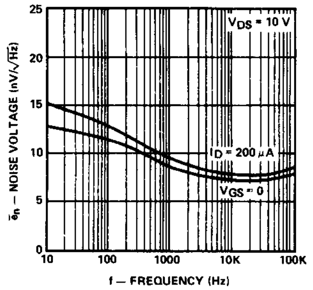
Gate Operating Current vs Drain-Gate Voltage

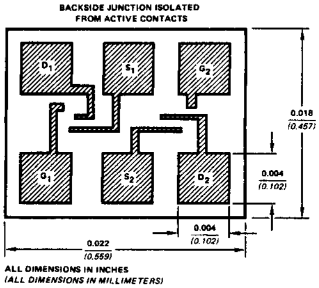


Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage vs Frequency





monolithic dual n-channel JFETs *designed for . . .*

Siliconix

- **Low Leakage FET Input Op Amps**
- **pH Meters**
- **Electrometers**

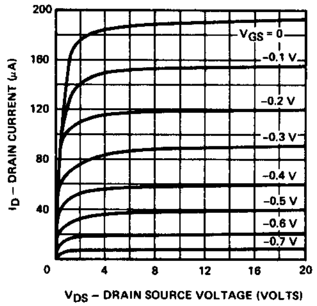
BENEFITS:

- **Ultra-High Input Impedance**
- **Good Voltage Gain**
- **Low Noise**

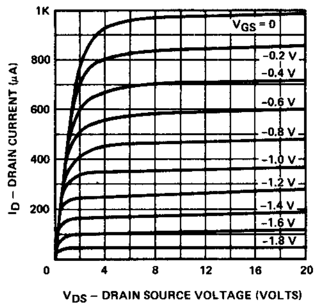
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-78	U421-6
Dual	Chip	U422CHP, U423CHP, U425CHP, U426CHP

PERFORMANCE CURVES (25° C unless otherwise noted)

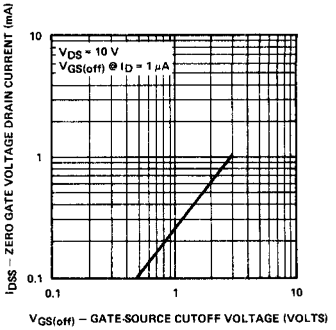
Output Characteristics
Low $V_{GS(off)}$ Unit (1.0 V)



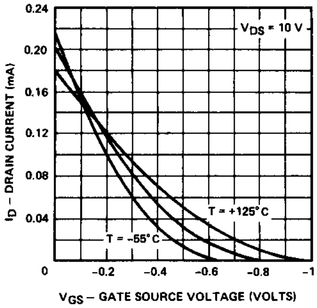
Output Characteristics
High $V_{GS(off)}$ Unit (2.5 V)



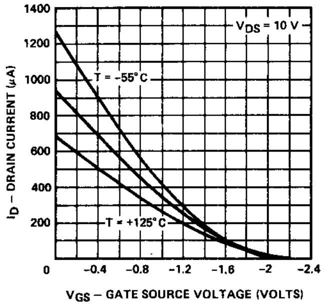
I_{DSS} vs Gate Source Cutoff Voltage



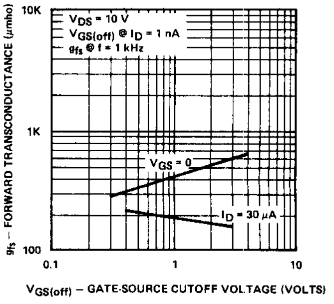
Transfer Characteristics
Low $V_{GS(off)}$ Unit (1.0 V)



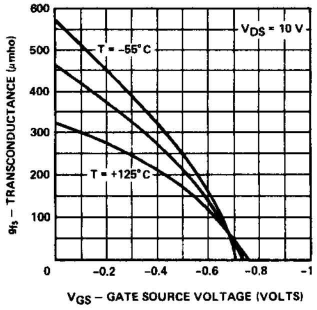
Transfer Characteristics
High $V_{GS(off)}$ Unit (2.5 V)



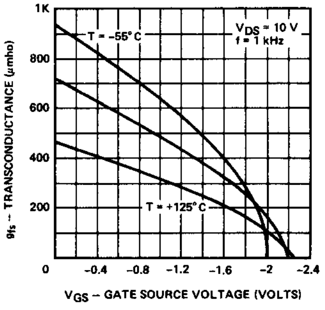
Forward Transconductance vs
Gate Source Cutoff Voltage



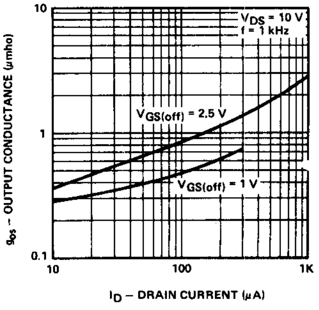
Transconductance vs Gate Source Voltage
Low $V_{GS(off)}$ Unit (1.0 V)



Transconductance vs Gate Source Voltage
High $V_{GS(off)}$ Unit (2.5 V)

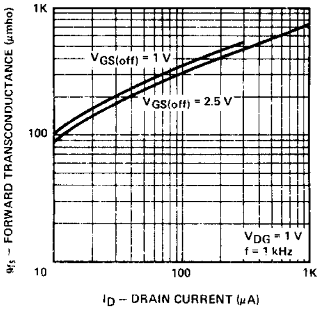


Common-Source Output Conductance
vs Drain Current

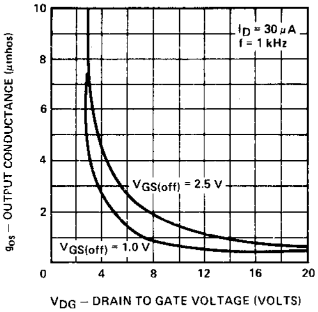


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

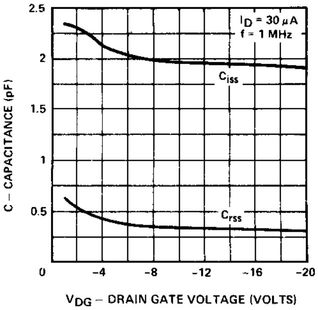
Forward Transconductance vs Drain Current



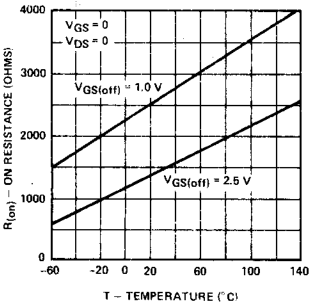
Output Conductance vs Drain to Gate Voltage



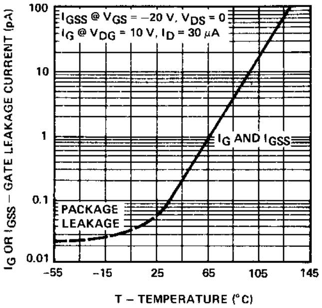
Capacitance vs Drain Gate Voltage



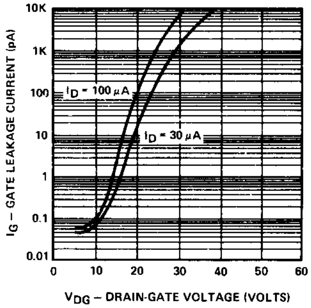
On Resistance vs Ambient Temperature



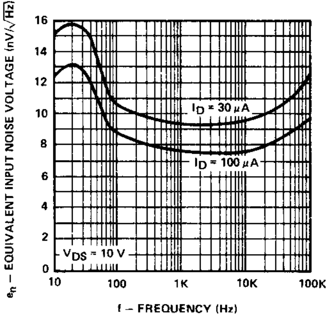
Leakage Current vs Temperature



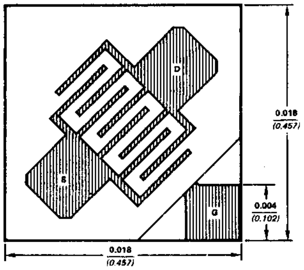
Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency



GATE ALSO BACKSIDE CONTACT
S AND D ARE SYMMETRICAL



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET *designed for . . .*

Siliconix

- **Small Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**
- **Switches**

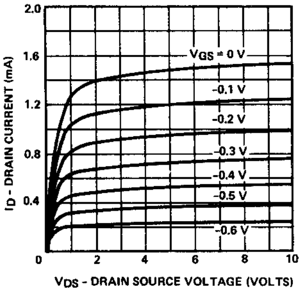
BENEFITS:

- **Wide Input Dynamic Range**
  High I_G Breakpoint Voltage
- **High Gain**
- **Low Insertion Loss Switches**

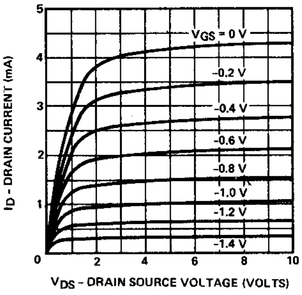
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3821-4, 2N4220-2, 2N4220A-22A 2N4223-24, 2N5556-58
Single	TO-92	2N3819, 2N5457-9, MPF109, MPF111
Dual	TO-71	2N3921-2, 2N4084-5, 2N5045-7, U401-6
Single	Chip	All of the above except 2N3819

PERFORMANCE CURVES (25°C unless otherwise noted)

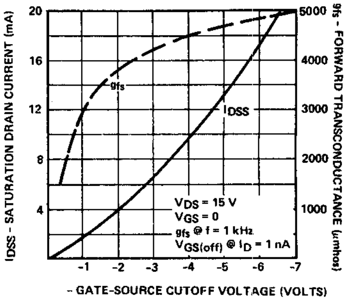
Output Characteristic



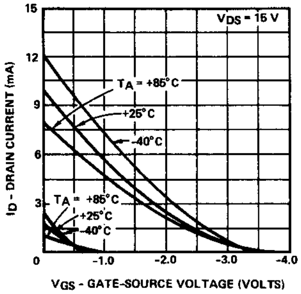
Output Characteristic



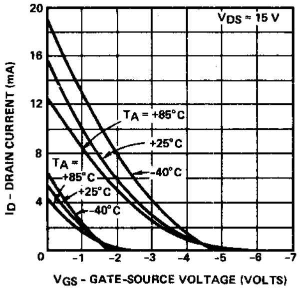
Drain Current & Transconductance vs Gate-Source Voltage



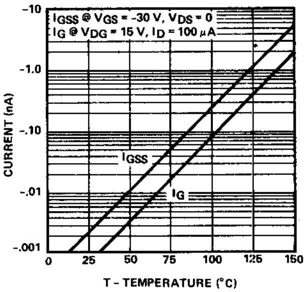
Transfer Characteristic



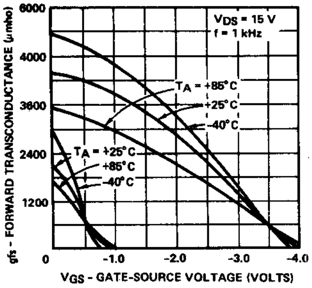
Transfer Characteristics



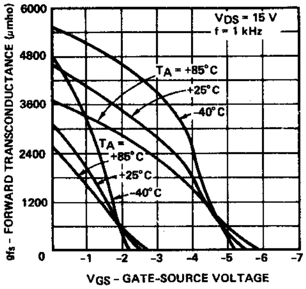
Leakage Currents vs Ambient Temperature



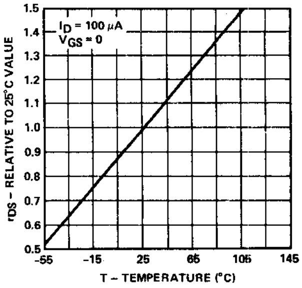
Transconductance Characteristics



Transconductance Characteristics

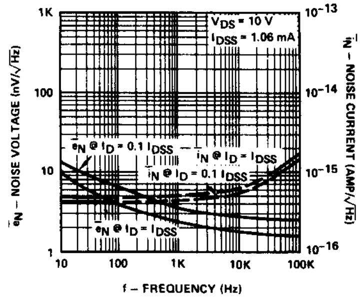


'ON' Resistance vs Ambient Temperature

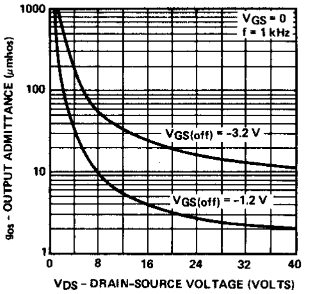


PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

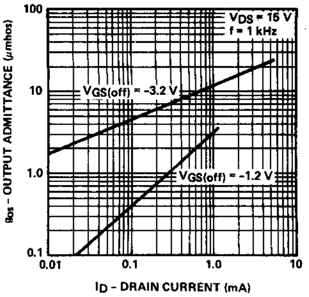
Equivalent Input Noise Voltage and Noise Current vs Frequency



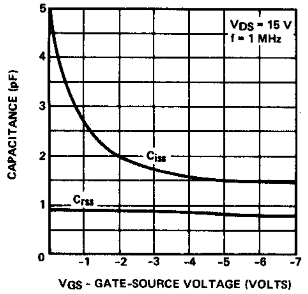
Common-Source Output Admittance vs Drain-Source Voltage



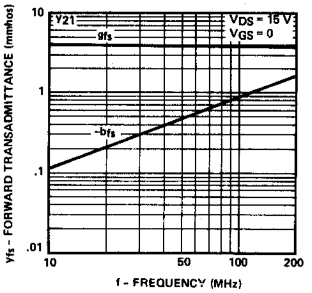
Common-Source Output Admittance vs Drain Current



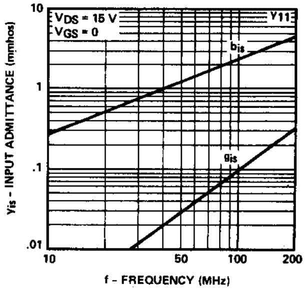
Common-Source Capacitances vs Gate-Source Voltage



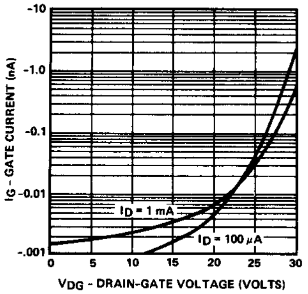
Common-Source Forward Transadmittance vs Frequency



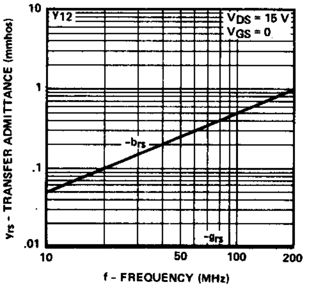
Common-Source Input Admittance vs Frequency



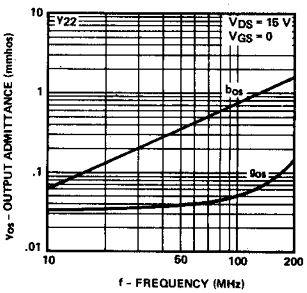
Gate Operating Current vs Drain-Gate Voltage



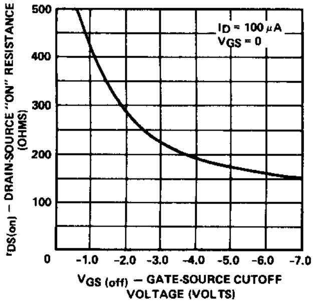
Common-Source Reverse Transfer Admittance vs Frequency



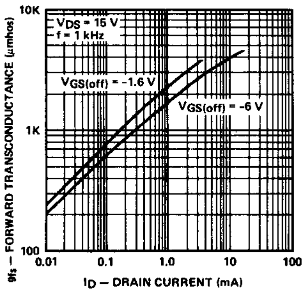
Common-Source Output Admittance vs Frequency



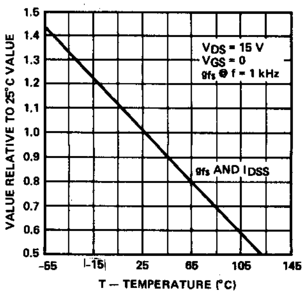
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



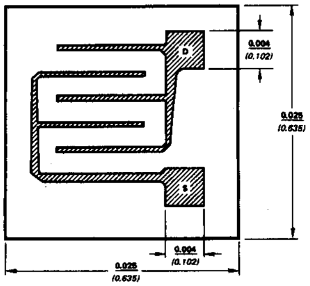
Common-Source Forward Transconductance vs Drain Current



Drain Current and Transconductance vs Ambient Temperature



GATE IS BACKSIDE CONTACT
S AND D ARE SYMMETRICAL



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET designed for . . .

Siliconix

- Low Noise Amplifiers
- Single and Differential Amplifiers

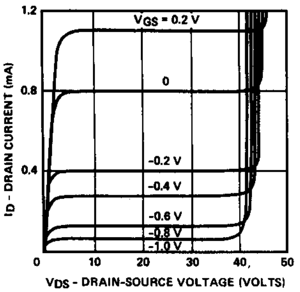
BENEFITS:

- Simplifies Amplifier Design
- Low Output Conductance
- Low 1/f Noise

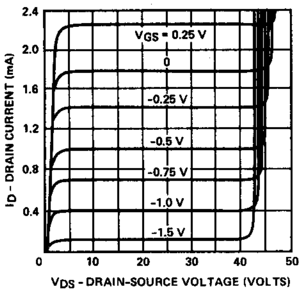
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N5515-24
Single	TO-72	2N4867-9, 2N4867A-69A
Single	TO-92	J230-32
Single	TO-92 Lead-form	J230-18 - 232-18
Dual	Chip	2N5518CHP-9CHP, 2N5523CHP-4CHP
Single	Chip	All of the above single devices

PERFORMANCE CURVES (25°C unless otherwise noted)

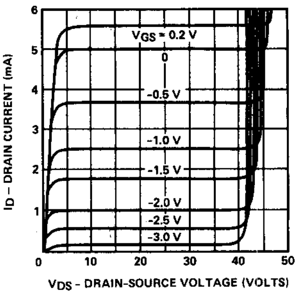
Output Characteristics



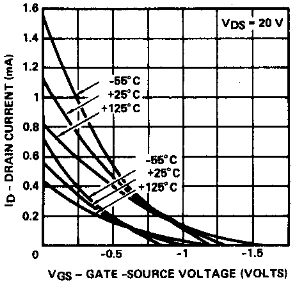
Output Characteristics



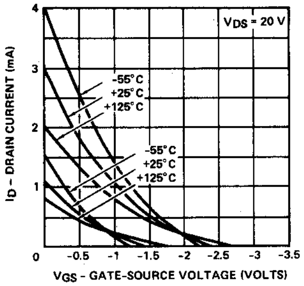
Output Characteristics



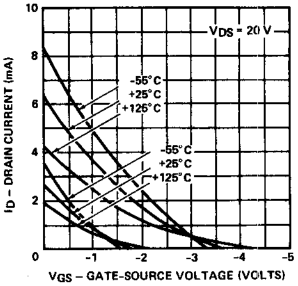
Transfer Characteristics



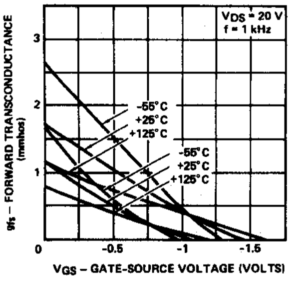
Transfer Characteristics



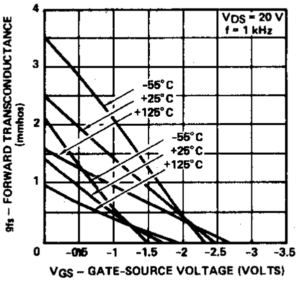
Transfer Characteristics



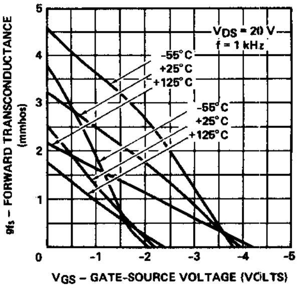
Transconductance Characteristics



Transconductance Characteristics

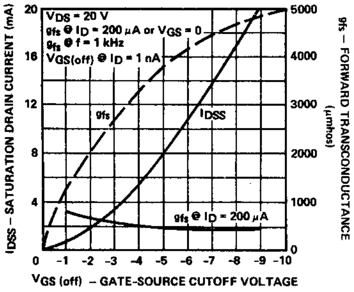


Transconductance Characteristics

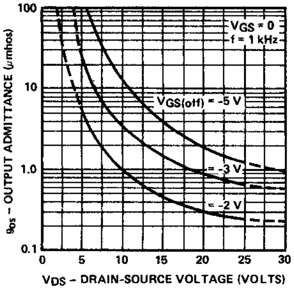


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

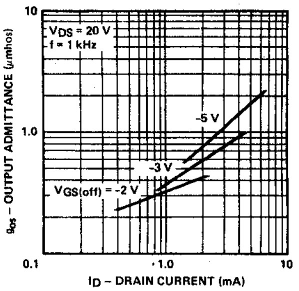
Saturation Drain Current and Forward Transconductance vs. Gate-Source Cutoff Voltage



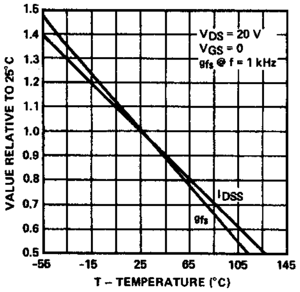
Common-Source Output Conductance vs Drain-Source Voltage



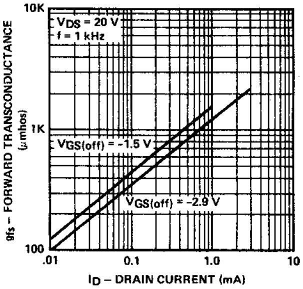
Common-Source Output Conductance vs Drain Current



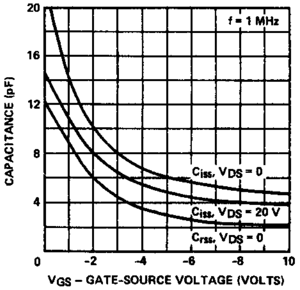
Drain Current & Transconductance vs Ambient Temperature



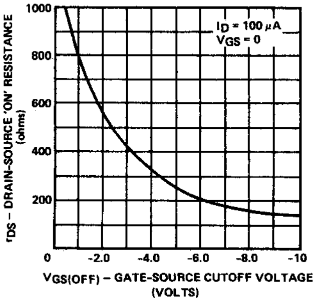
Common-Source Forward Transconductance vs Drain Current



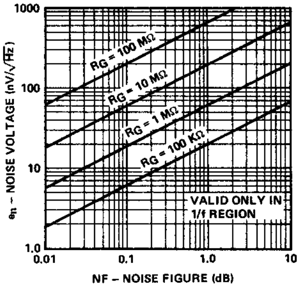
Common-Source Capacitance vs Gate-Source Voltage



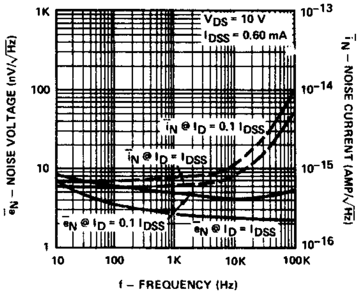
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



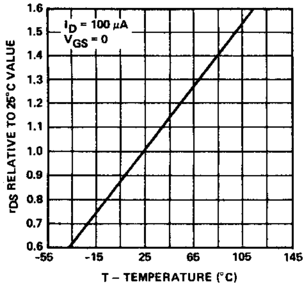
Approximate Noise Figure vs Input Noise Voltage



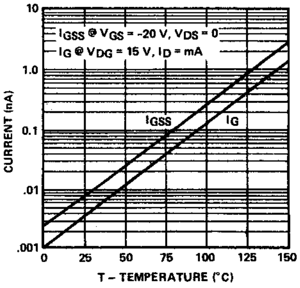
Equivalent Input Noise Voltage and Noise Current vs Frequency



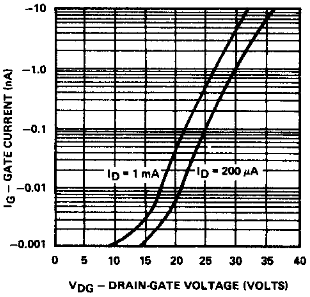
Drain-Source 'ON' Resistance vs Ambient Temperature

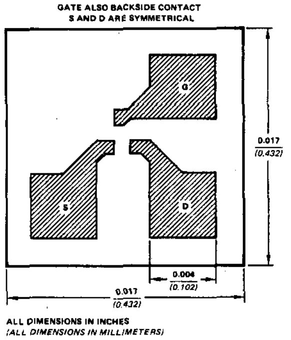


Leakage Currents vs Ambient Temperature



Gate Operating Current vs Drain-Gate Voltage





n-channel JFET

designed for . . .

Siliconix

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **pH Meters**
  - **Smoke Detectors**

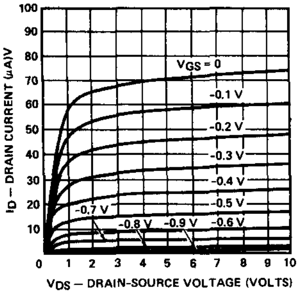
BENEFITS:

- **Low Power**
  $I_{DSS} < 90\ \mu A$ (2N4117)
- **High Input Impedance**
  $I_G < 1$ pA (2N5906-09)

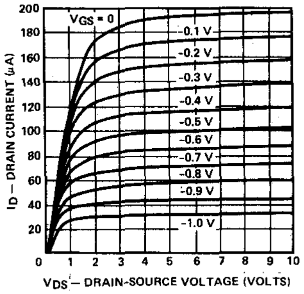
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N4117-9, 2N4117A-9A, VCR7N
Dual	TO-78	2N5902-9
Single	Chip	2N4117CHP-9CHP, 2N4117ACHP-9ACHP, VCR7NCHP
Dual	Chip	2N5905CHP, 2N5909CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

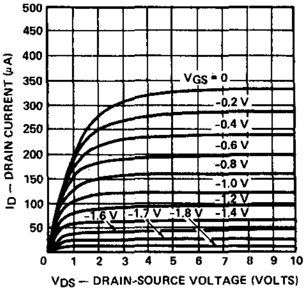
Output Characteristic



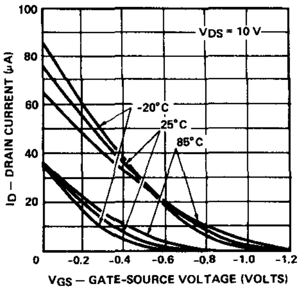
Output Characteristic



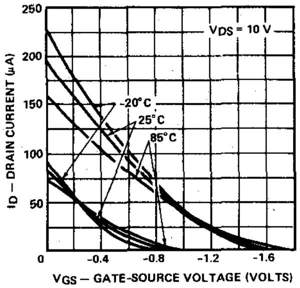
Output Characteristic



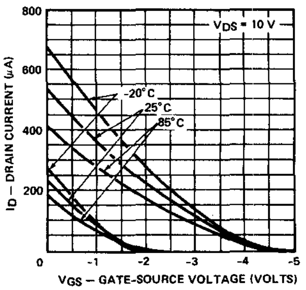
Transfer Characteristics



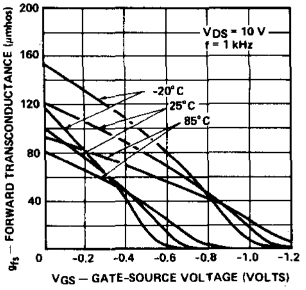
Transfer Characteristics



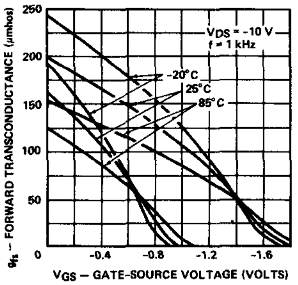
Transfer Characteristics



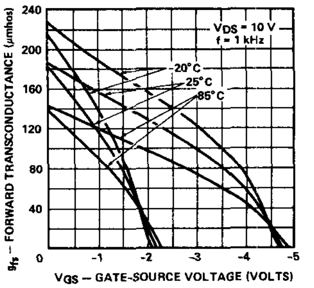
Transconductance Characteristics



Transconductance Characteristics

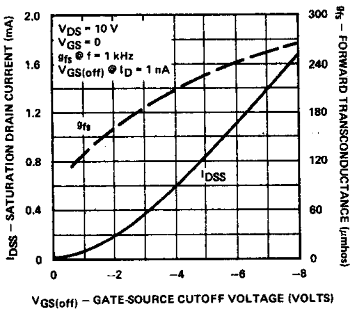


Transconductance Characteristics

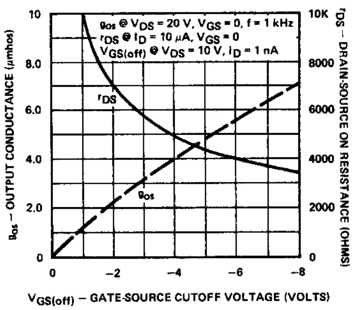


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

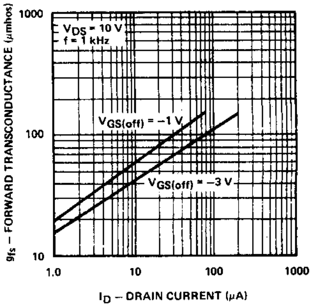
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



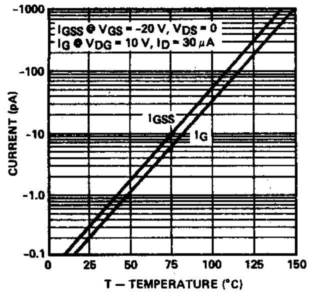
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



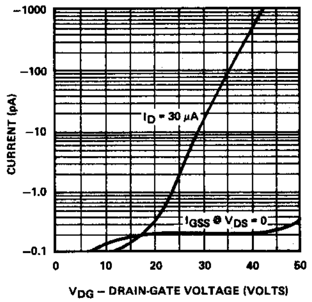
Common-Source Forward Transconductance vs Drain Current



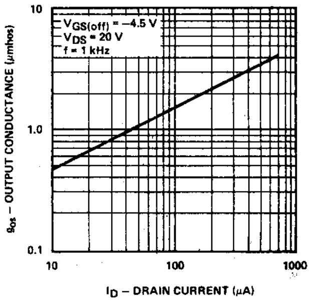
Leakage Currents vs Ambient Temperature



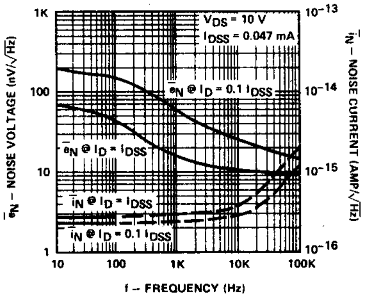
Leakage Currents vs Drain-Gate Voltage

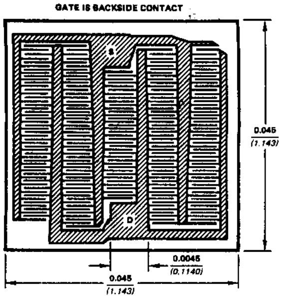


Common-Source Output Conductance vs Drain Current



Equivalent Input Noise Voltage and Noise Current vs Frequency





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**

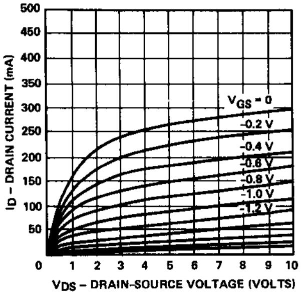
BENEFITS:

- **Very Low Insertion Loss** $R_{DS(on)} < 2.5$ **Ohms (U290)**
- **High Off-Isolation**

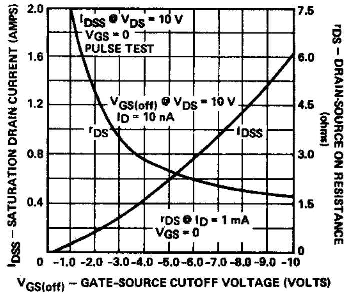
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U290-1
Single	TO-92	J105-7
Single	TO-92 Lead-form	J105-18 - 107-18
Single	Chip	U290CHP-1CHP, J105CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

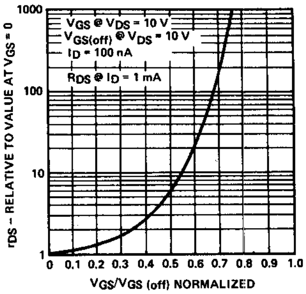
Output Characteristic



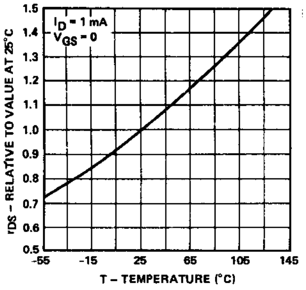
Saturation Drain Current and Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



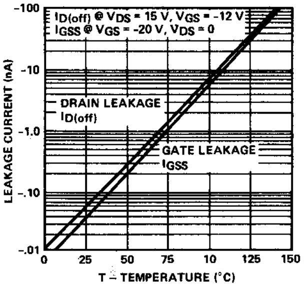
Drain-Source Resistance vs Normalized Gate-Source Voltage



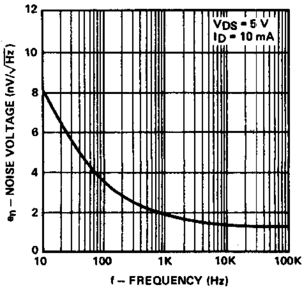
Drain-Source 'ON' Resistance vs Ambient Temperature



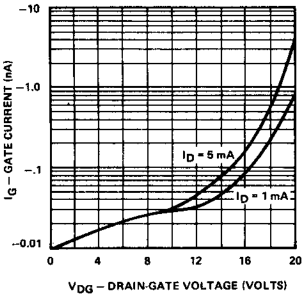
Leakage Currents vs Ambient Temperature



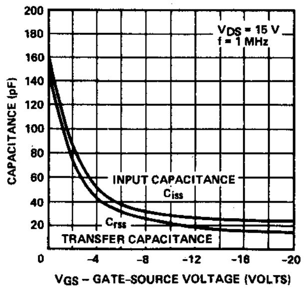
Equivalent Input Noise Voltage vs vs Frequency

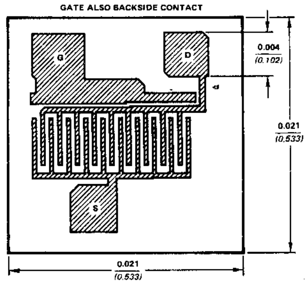


Leakage Current vs Drain-Gate Voltage



Common-Source Capacitance vs Gate-Source Voltage





ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- VHF/UHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

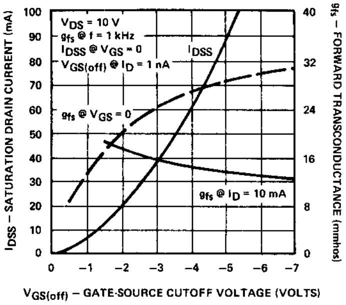
BENEFITS

- Industry Standard
- High Power Gain
  16 dB at 100 MHz, Common Gate
  11 dB at 450 MHz, Common Gate
- Low Noise
  3 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater Than 100 dB
- 75 Ohm Input Match Common Gate

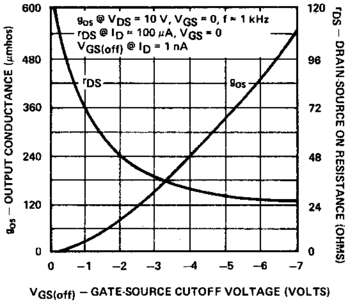
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U308-10
Single	TO-72	U311
Single	TO-92	J308-10
Dual	TO-99	U430-1
Single	TO-92 Lead-form	K308-18 -310-18
Single	Chip	J308CHP-10CHP, U308CHP-10CHP, U311CHP
Dual	Chip	U430CHP-1CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

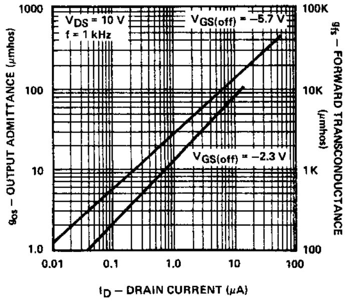
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



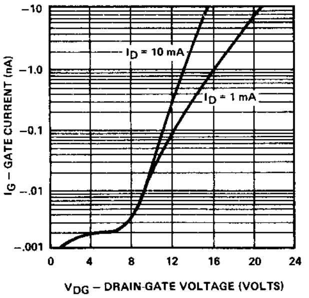
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



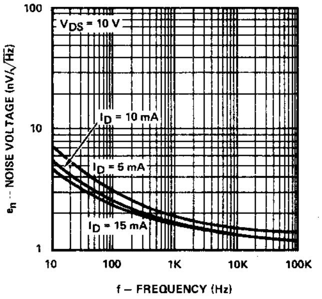
Common-Source Output Conductance vs Drain Current



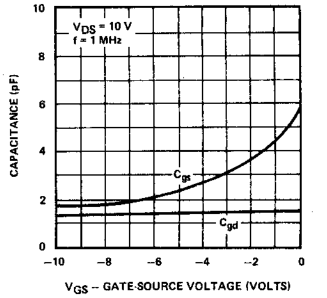
Gate Operating Current vs Drain-Gate Voltage



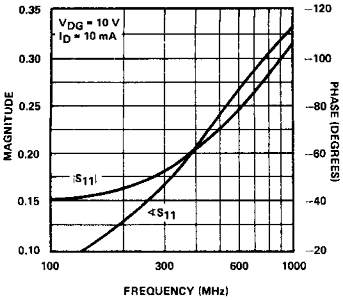
Equivalent Input Noise Voltage vs Frequency

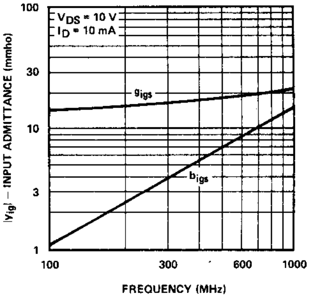


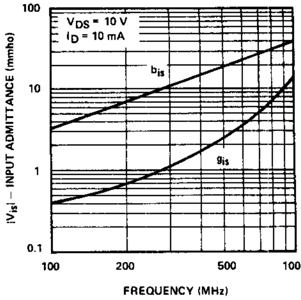
Junction Capacitance vs Gate-Source Voltage

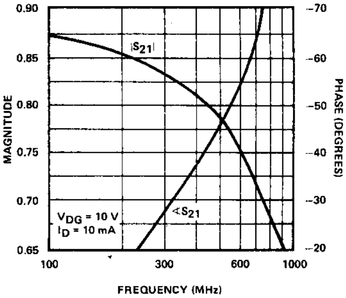


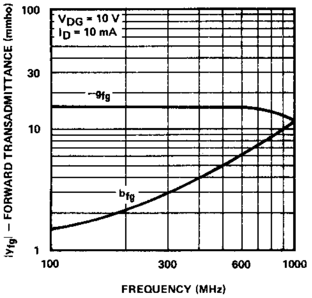
PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

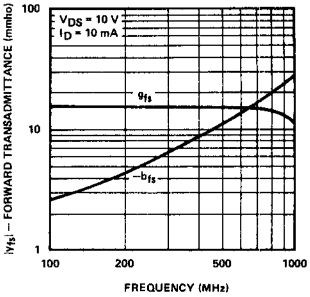

Forward Reflection Coefficient Common Gate

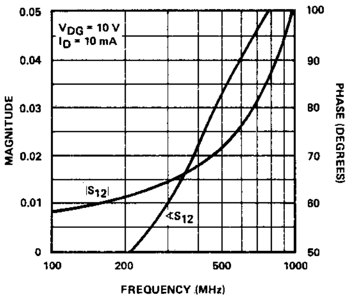

Input Admittance Common Gate

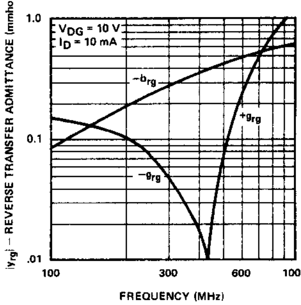

Input Admittance Common Source

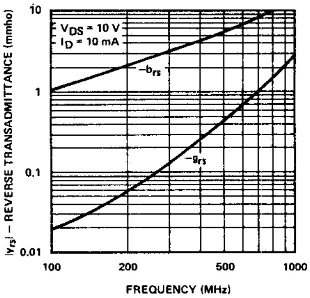

Forward Transmission Coefficient Common Gate

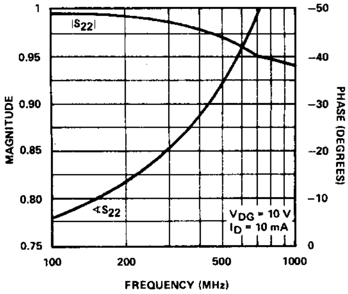

Forward Transfer Admittance Common Gate

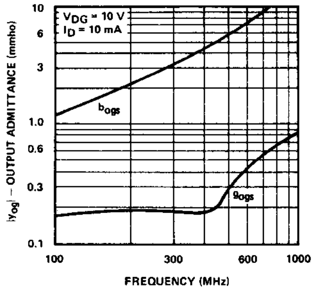

Forward Transfer Admittance Common Source

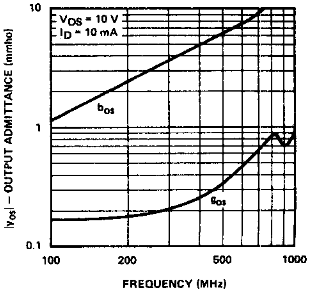

Reverse Transmission Coefficient Common Gate

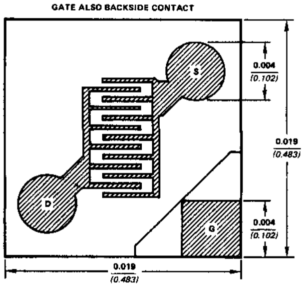

Reverse Transfer Admittance Common Gate


Reverse Transfer Admittance Common Source


Reverse Reflection Coefficient Common Gate


Output Admittance Common Gate


Output Admittance Common Source



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

n-channel JFET
designed for . . .

Siliconix

- **High Frequency Amplifiers**
- **Mixers**
- **Oscillators**

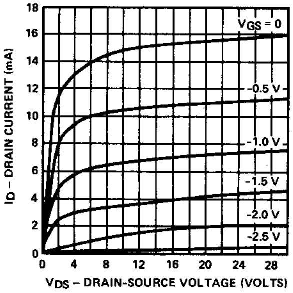
BENEFITS:

- **High Power Gain**
- **Low Input Capacitance**

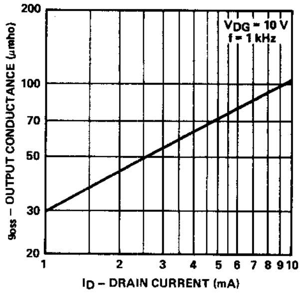
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U312
Dual	TO-78	2N5911-12, U257
Dual	TO-71	U440-41
Single	Chip	U312CHP
Dual	Chip	2N5912CHP, U257CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

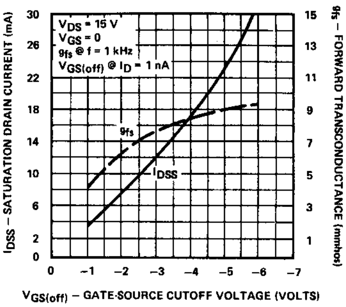
Output Characteristic



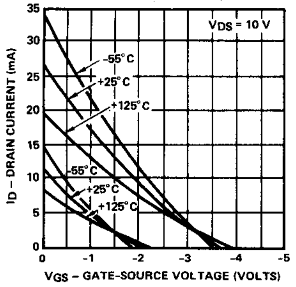
Common-Source Output Conductance vs Drain Current



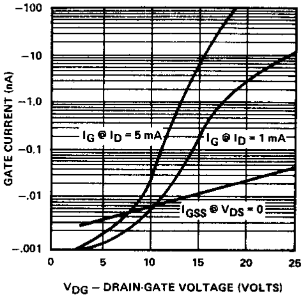
Saturation Drain Current and Forward Transconductance vs Gate-Source Cutoff Voltage



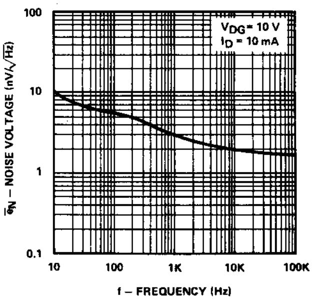
Transfer Characteristics



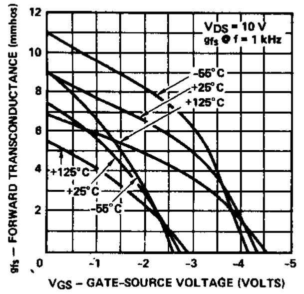
Leakage Currents vs Drain-Gate Voltage



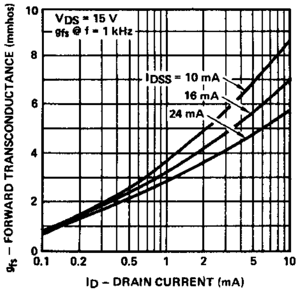
Equivalent Input Noise Voltage vs Frequency



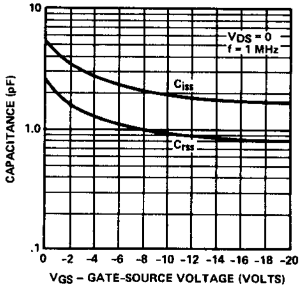
Transconductance Characteristics



Forward Transconductance vs Drain Current

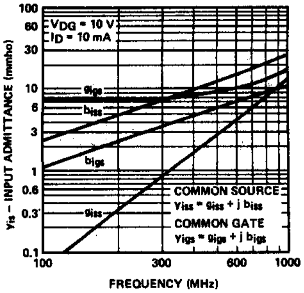


Common-Source Capacitances vs Gate-Source Voltage

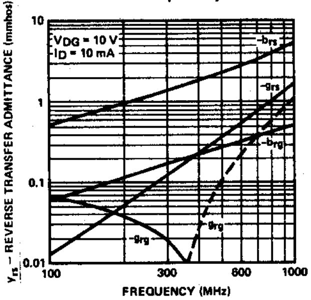


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

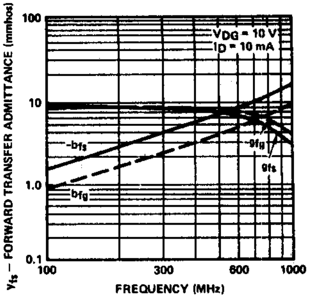
Input Admittance vs Frequency



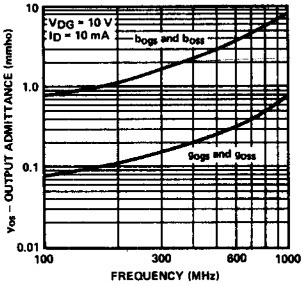
Reverse Transfer Admittance vs Frequency



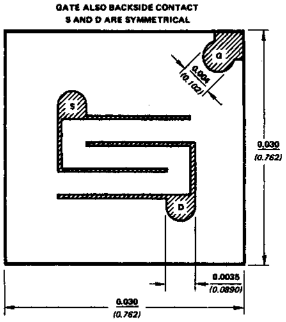
Forward Transfer Admittance vs Frequency



Output Admittance vs Frequency



GATE ALSO BACKSIDE CONTACT
S AND D ARE SYMMETRICAL



ALL DIMENSIONS IN INCHES
(ALL DIMENSIONS IN MILLIMETERS)

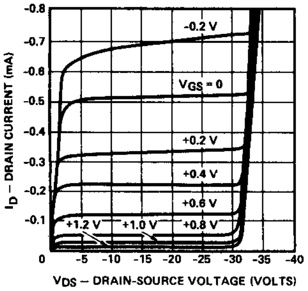
p-channel JFET
designed for . . .

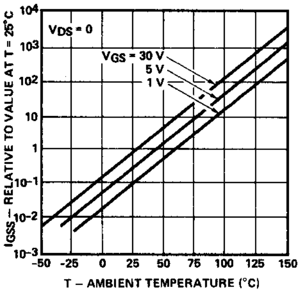
Siliconix

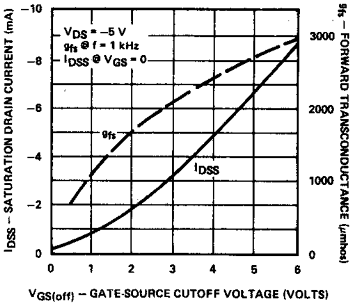
- General Purpose Amplifiers and Attenuators

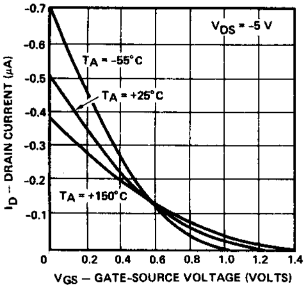
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N2608, 2N2608JAN, 2N2843
Single	TO-72	2N3329-32, 2N3909, VCR5P
Single	Chip	2N2608CHP, 2N2843CHP, 2N3329CHP-32CHP, 2N3909CHP VCR5PCHP

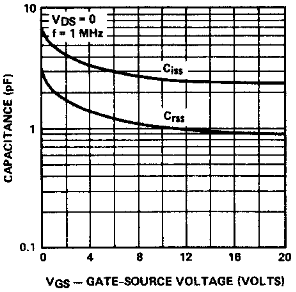
PERFORMANCE CURVES (25°C unless otherwise noted)

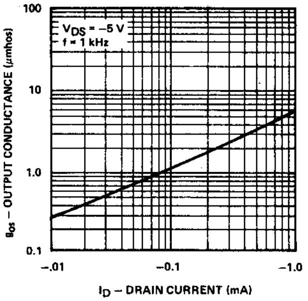

Output Characteristic

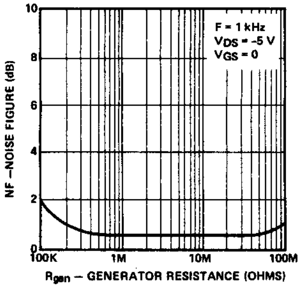

Gate Reverse Current vs Ambient Temperature

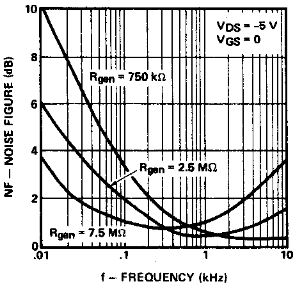

Drain Current & Transconductance vs Gate-Source Voltage

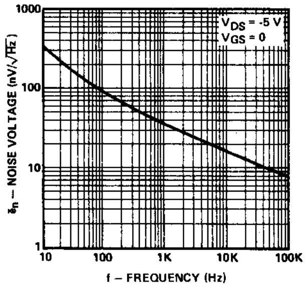

Transfer Characteristic

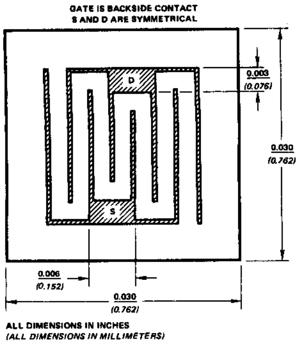

Common-Source Capacitances vs Gate-Source Voltage


Common-Source Output Conductance vs Drain Current


Noise Figure vs Generator Resistance


Noise Figure vs Frequency


Equivalent Input Noise Voltage vs Frequency



p-channel JFET
designed for . . .

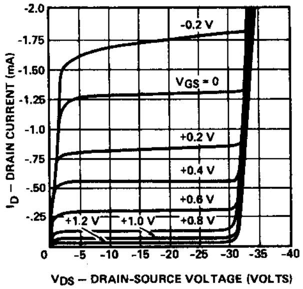
Siliconix

- General Purpose Amplifiers

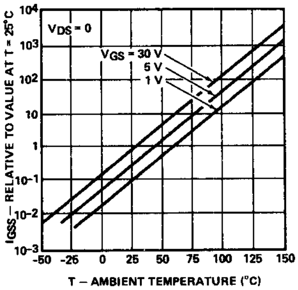
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N2609, 2N2609JAN, 2N2844
Single	Chip	2N2609CHP, 2N2844CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

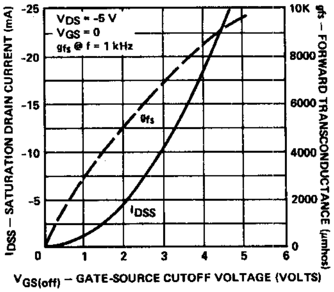
Output Characteristic



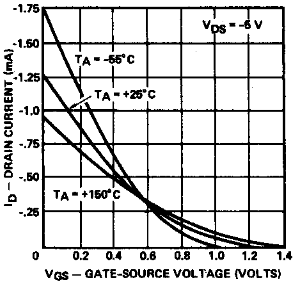
Gate Reverse Current vs Ambient Temperature



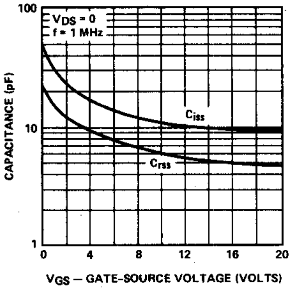
Drain Current & Transconductance vs Gate-Source Voltage



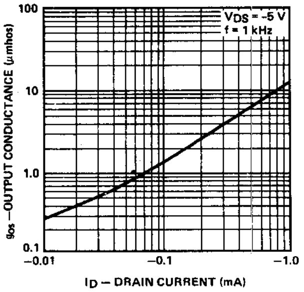
Transfer Characteristic



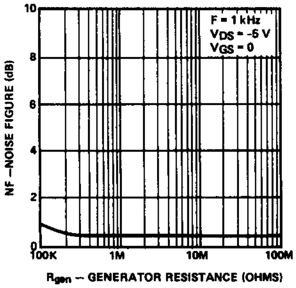
Common-Source Capacitance vs Gate-Source Voltage



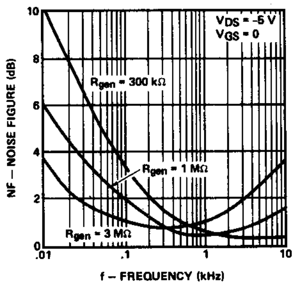
Common-Source Output Conductance vs Drain Current



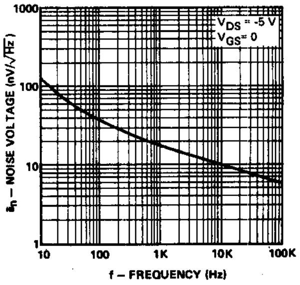
Noise Figure vs Generator Resistance

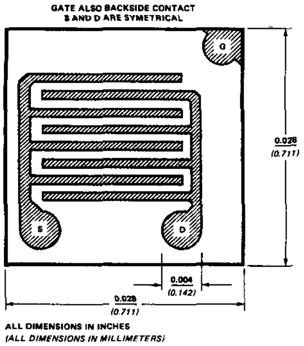


Noise Figure vs Frequency



Equivalent Input Noise Voltage vs Frequency





p-channel JFET
designed for . . .

Siliconix

- General Purpose Amplifiers
- Switches

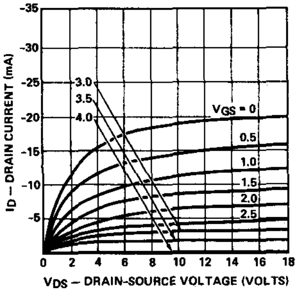
BENEFITS:

- Wide Range of Transconductance

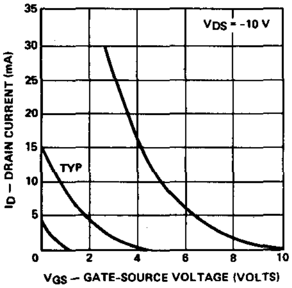
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3382, 2N3384, 2N3386, VCR3P
Single	Chip	2N3382CHP-86CHP, VCR3PCHP

PERFORMANCE CURVES (25°C unless otherwise noted)

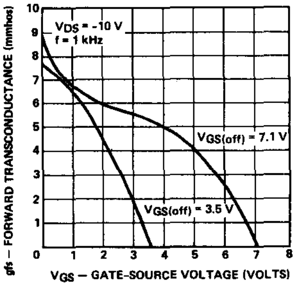
Output Characteristic



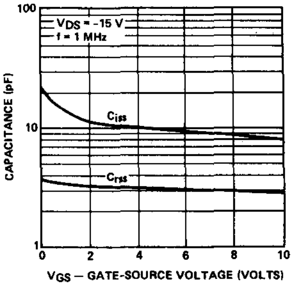
Transfer Characteristics



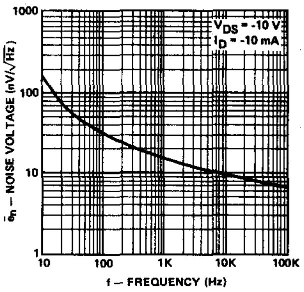
Transconductance Characteristics



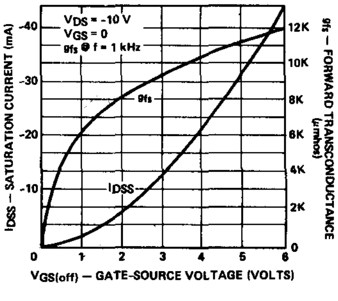
Common-Source Capacitances vs Gate-Source Voltage

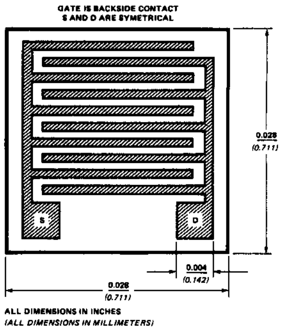


Equivalent Input Noise Voltage vs Frequency



Drain Current & Transconductance vs Gate-Source Voltage





p-channel JFET
designed for . . .

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

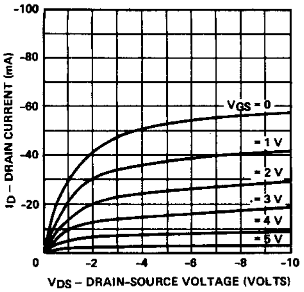
BENEFITS:

- **Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)**
- **Short Sample and Hold Aperture Time $C_{rss} < 7$ pF**
- **High Off-Isolation $I_{D(off)} < 500$ pA**

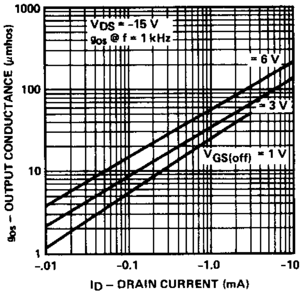
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	2N5018-19, 2N5114-16, U304-6
Single	TO-92	J174-7, J270-1, P1086-87, P1086E
Single	TO-92 Lead-form	J174-18 - 177-18, J270-18 - 271-18 P1086-18 - 87-18
Single	Chip	2N5018CHP-19CHP, 2N5114CHP-16CHP U304CHP-6CHP, P1086CHP-87CHP J270CHP-271CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

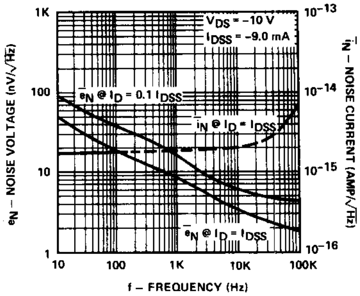
Output Characteristic



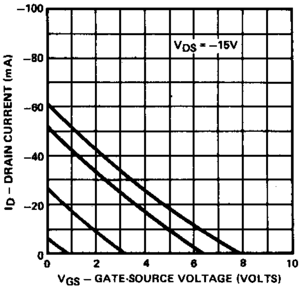
Common-Source Output Conductance vs Drain Current



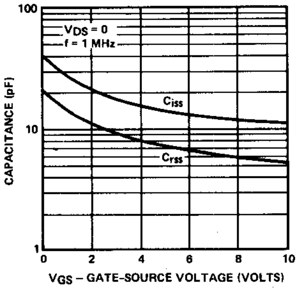
Equivalent Input Noise Voltage and Noise Current vs Frequency



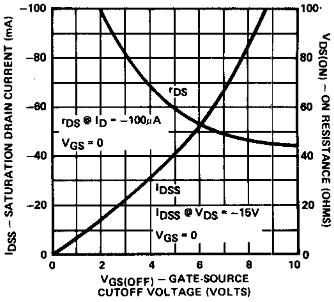
Transfer Characteristics



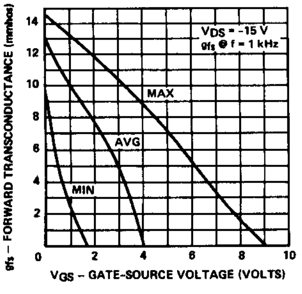
Common-Source Capacitance vs Gate-Source Voltage



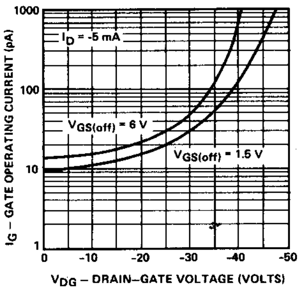
Saturation Drain Current and Drain-Source ON Resistance vs. Gate-Source Cutoff Voltage



Transconductance Characteristics



Gate Operating Current vs Drain-Gate Voltage



APPLICATION NOTE

An Introduction to FETs

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J.E. Lilenfeld's patent of 1925. The theoretical description of a FET made by Schockley in 1952 paved the way for development of a classic electronic device which provides the designer with the means by which he can accomplish nearly every circuit function. The field-effect transistor earlier was known as a "unipolar" transistor, and the term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology and parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

Amplifiers
- Small Signal
- Low Distortion
- High Gain
- Low Noise
- Selective
- D.C.
- High-Frequency

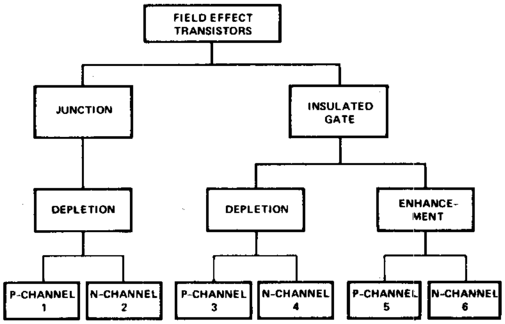
Switches
- Chopper-type
- Analog Gate
- Commutator

Current Limiters
Voltage-Controlled Resistors
Mixers
Oscillators

This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics – which are very different from those of bipolar devices – can often make possible the design of technically superior (and sometimes cheaper) circuits. This comment applies not only to networks employing discrete devices and conventional components such as resistors and capacitors, but also extends to both linear and digital integrated circuits. In fact, FET technology today allows a greater packaging density in large-scale integrated circuits (LSI) than would ever be possible with bipolar devices.

(Although there is no industry-accepted definition of LSI, apparently when the equivalent circuit of an IC contains more than 1,000 active elements (500 gates) or is "very complex", the end product may be called LSI. With a typical LSI chip measuring less than 200 x 200 mils, this is high-density packaging indeed.)

The family tree of FET devices (Figure 1) may be divided into two main branches, junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, *metal-oxide-silicon field-effect transistors*). Junction FETs are inherently depletion-mode devices, and are available in both P- and N-Channel configurations. MOSFETs are available in both enhancement or depletion modes, and exist as both N- and P-Channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.

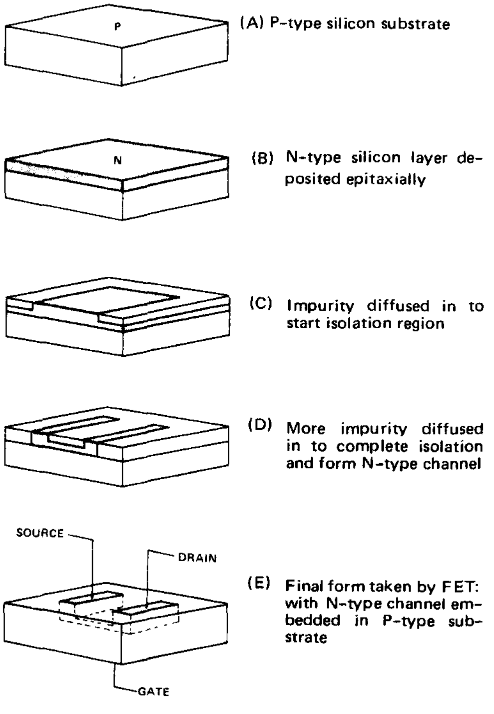


FET Family Tree
Figure 1

Junction FETs

In its most elementary version, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a *gate*, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the fundamental difference between FET and bipolar devices: when the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The FET is a high input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, N-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, P-type material will be formed and the channel current will consist of holes. N-Channel devices have greater conductivity than P-Channel types, since electrons have higher mobility than do holes; thus N-Channel FETs tend to be more efficient conductors than their P-Channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, N-type silicon is deposited epitaxially (single-crystal condensation surface) onto monocrystalline P-type silicon, so that crystal integrity is maintained. Then a layer of silicon dioxide is grown on the surface of the N-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a P-type annulus has been formed in the layer on N-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of N-type material within the substrate.



(A) P-type silicon substrate

(B) N-type silicon layer deposited epitaxially

(C) Impurity diffused in to start isolation region

(D) More impurity diffused in to complete isolation and form N-type channel

(E) Final form taken by FET: with N-type channel embedded in P-type substrate

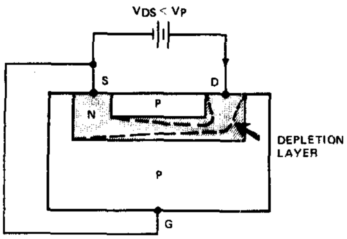
Idealized Manufacture of an N-Channel Junction FET
Figure 2

In addition to the channel material, a FET contains two ohmic (non-rectifying) contacts, the *source* and the *drain*. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized FET chip, it is immaterial which contact is called the source and which is called the drain; the FET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

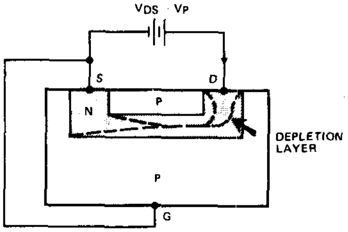
(For certain FET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

Figure 2E also shows how the N-Channel is embedded in the P-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the FET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the PN junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a *depletion* layer, where almost all the electrons present in the N-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (*Drain-to-Source* current with the gate *Shorted* to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

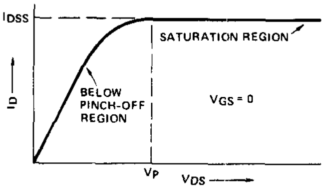
Figure 3C shows the output characteristics of an N-Channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be *pinched off.* The physical meaning of this term leads to one definition of *pinch-off voltage*, V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.



(A) N-channel FET working below saturation ($V_{GS} = 0$).
(Depletion shown only in channel region).



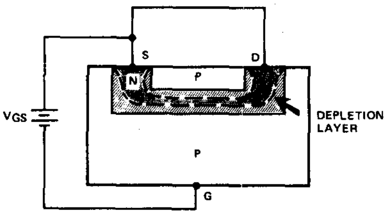
(B) N-channel FET working in saturation retion ($V_{GS} = 0$)



(C) Idealized output characteristic for $V_{GS} = 0$.

Figure 3

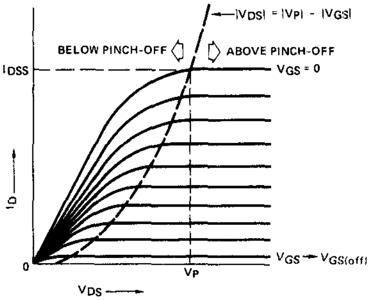
In Figure 4, consider the case where $V_{DS} = 0$, and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for $V_{GS} = 0$. In fact, at a value of $|V_{GS}| \geqslant |V_P|$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_P or by $V_{GS(off)}$. V_P has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off. $V_{GS(off)}$ and V_P, strictly speaking, are equal in magnitude but opposite in polarity.



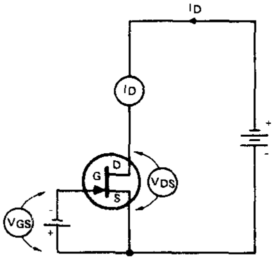
N-channel FET Showing Depletion Due To Gate-Source Voltage ($V_{DS} = 0$)
Figure 4

The mechanisms of Figure 3 and 4 react together to provide a family of output characteristics as shown in Figure 5A. The area below the pinchoff voltage locus is known as the triode or "below pinchoff" region; the area above pinchoff is often referred to as the pentode or saturation region. FET behavior in these regions is comparable to that of a power grid vacuum tube, and for this reason FETs operating in the saturation region may be used as excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.

Figure 5B relates the curves of Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.



(A) Family of output characteristics for N-channel FET

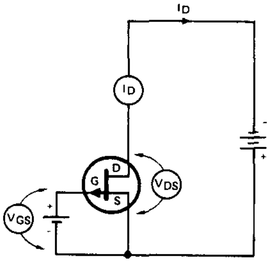


(B) Circuit arrangement for N-channel FET

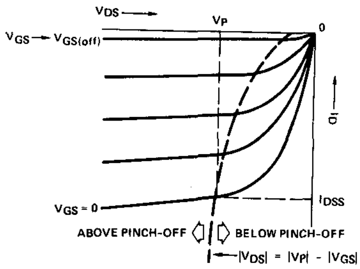
Figure 5

The P-Channel FET works in precisely the same way as does the N-Channel FET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto N-type silicon, and the donor impurity diffused later to form a second N-type region and leave a P-type channel. In the P-Channel FET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a P-Channel FET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the N-Channel FET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_P, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit arrangement for P-channel FET

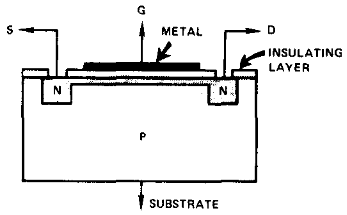


(B) Family of output characteristics for P-channel FET

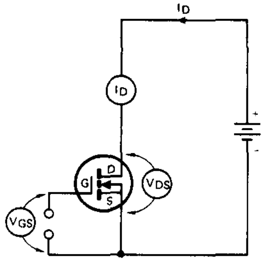
Figure 6

MOSFETs

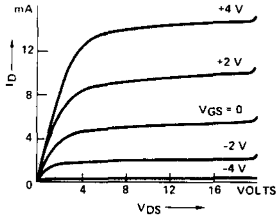
The metal-oxide-silicon FET (MOSFET) depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the P-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate at the interface, spontaneously forming an N-type channel. Thus a conducting path exists between the diffused N-type source and drain regions. Further, the MOSFET will behave in a manner similar to the N-Channel junction FET when a voltage of the correct polarity is applied to the channel, as in Figure 7B.



(A) Idealized cross-section through an N-channel depletion-type MOSFET



(B) Circuit arrangement for N-channel depletion MOSFET



(C) Family of output characteristics for the Siliconix 2N3631 N-channel depletion MOSFET

Figure 7

Output characteristics of an N-Channel MOSFET are shown in Figure 7C. Because there is no junction involved, V_{GS} can be reversed without engendering a gate current; the gate may be made either positive or negative with respect to the source. Under these circumstances, still more free electrons will be attracted to the channel region, and I_D will become greater than I_{DSS}. This mode of operation is represented by the higher members of the family of ourput characteristics. Because the application of a negative gate voltage causes the channel to be depleted of free electrons – thus reducing I_D – the device just described is called a *depletion-mode* MOSFET.

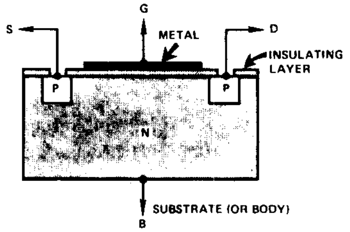
The foregoing has established that the depletion-mode MOSFET is a "normally-ON" device: when $V_{GS} = 0$, a conducting path exists between source and drain. In many circuits a "normally-OFF" device would be useful, a condition which leads to the concept of an *enhancement-mode* MOSFET. In the latter device, an increasing voltage applied to the gate will enhance channel conduction, and depletion will never occur, I_D being zero when $V_{GS} = 0$.

A P-Channel enhancement-mode MOSFET is shown in Figure 8. Here, an acceptor impurity has been diffused into an N-type substrate to form P-type source and drain regions. No conducting channel exists between the source and the drain, because no matter how the drain-source voltage is applied one of the PN junctions will always be reverse-biased. On the other hand, if a negative voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layer of the substrate and produce a P-type channel. A family of output characteristics for a typical MOSFET is shown in Figure 8C. The idealized cross-section illustrated in Figure 8A may be used to show how the characteristics of Figure 8C come about. Refer to Figure 9 for an extension of this phenomenon.

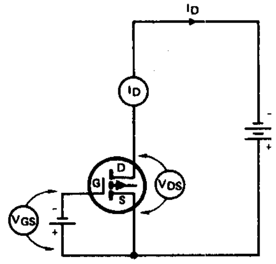
If a constant (negative) gate voltage, ($V_{GS(K)}$) is applied, then an essentially-uniform P-Channel depletion layer will be induced, as in Figure 9A. If a negative drain voltage is applied, then current, I_D, will flow through the drain. As $|V_{DS}|$ increases, I_D also increases. However, the voltage between the drain and the gate decreases, so that the thickness of the channel at the drain end is reduced as in Figure 9B. Therefore, the relationship of I_D versus V_{DS} will eventually reach a limiting value when $V_{DS} = V_{GS}$, and the channel becomes pinched off. This condition is shown in Figure 9C.

Different values of V_{GS} give rise to limiting values of I_D, so that the characteristic family of output curves which was shown in Figure 8 is realized. Characteristics of depletion-mode MOSFETs also come about for the same reason, except that members of the output characteristics family also exist for V_{GS} values of zero or reversed polarity. The P-Channel enhancement-mode MOSFET is currently the most popular member of the FET family in current use, and is in fact the basic element in many LSI integrated circuits.

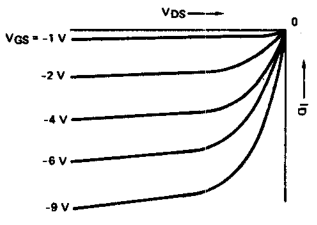
In principle it is possible to manufacture the remaining two members of the MOSFET family, the P-Channel depletion-mode and the N-Channel enhancement-mode devices. Because of the spontaneous formation of an N-Channel at a silicon/silicon-dioxide interface, the fabrication processes involved become quite difficult on a volume production basis. Much work has gone into the development of practical MOSFET processes for these devices, and N-Channel depletion-mode types are now becoming generally available.



(A) Idealized cross-section through a P-channel enhancement MOSFET

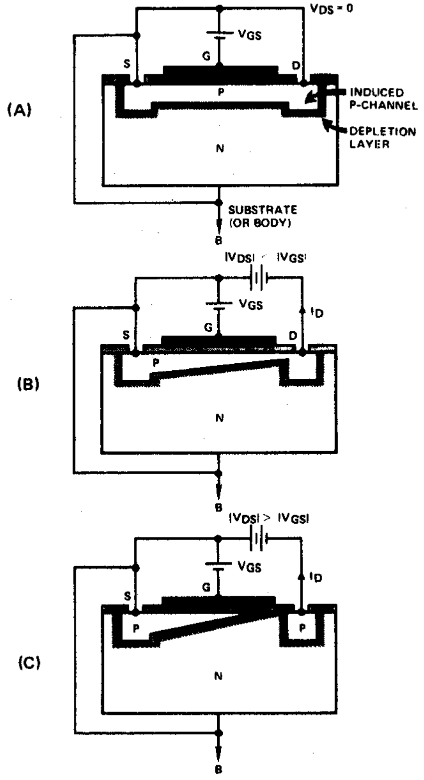


(B) Circuit arrangement for P-channel enhancement MOSFET



(C) Family of output characteristics for a P-channel enhancement MOSFET

Figure 8



Idealized approach of pinch-off,
(A) $V_{DS} = 0$, (B) $|V_{DS}| < |V_{GS}|$, (C) $|V_{DS}| > |V_{GS}|$

Figure 9

FET Characteristics

The FET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range (> 100 dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a FET approximates to a square-law response, and the second and higher-order derivatives of g_m are near zero; thus strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a FET is simply the impedance of a reverse-biased PN junction, which is on the order of 10^{10} to 10^{12} Ω. In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency; for example, in a 2N4416 FET, the input impedance would be 22K Ω at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The FET has very high dynamic range, in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

FET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on FET electrical quantities and parameters – in particular, the most important parameters, and the means by which they can be measured. The following discussion will define specific FET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- I_{DSS} – Drain current with the gate shorted to the source
- $V_{GS(off)}$ – Gate-source cutoff voltage
- I_{GSS} – Gate-to-source current with the drain shorted to the source
- BV_{GSS} – Gate-to-source breakdown voltage with the drain shorted to the source
- g_{fs} – Common-source forward transconductance
- C_{gs} – Gate-source capacitance
- C_{gd} – Gate-drain capacitance

Special attention should be given to the subscript "s" because it has two different meanings and three possible uses. In FET notations, an "s" for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an "s" for the third subscript does not refer to the FET source terminal. It is an abbreviation for "shorted", and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term I_{GSS} refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the FET, four-pole admittance equations are commonly used to describe electrical characteristics of the FET:

$$I_1 = Y_{11} V_{11} + Y_{21} V_{22} \qquad (1)$$

When Y_{11}, Y_{21}, Y_{12} and Y_{22} are defined as the input, reverse transfer, forward transconductance, and output admittances respectively, Equation 1 reduces to

$$\begin{aligned} i_1 &= y_i v_{11} + y_r v_{22} \\ i_2 &= y_f v_{11} + y_o v_{22} \end{aligned} \qquad (2)$$

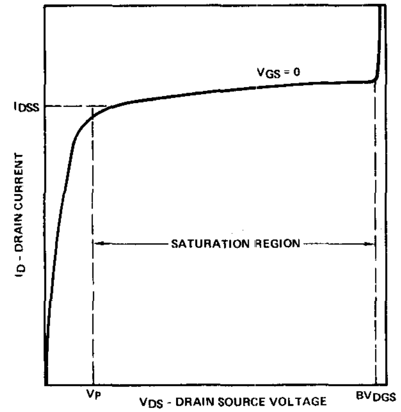
For a three-lead FET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

$$\begin{aligned} i_i &= y_{is} v_{gs} + y_{rs} v_{ds} \\ i_o &= y_{fs} v_{gs} + y_{os} v_{ds} \end{aligned} \qquad (3)$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.

I_{DSS} – Drain Current at Zero Gate Voltage (I_D at $V_{GS} = 0$)

By itself, I_{DSS} merely refers to the drain current that will flow for any applied V_{DS} with the gate shorted to the source. However, when a particular value for V_{DS} is given, equal to or greater than V_P (see Figure 10), I_{DSS} indicates the drain saturation current at zero gate voltage. Some FET data sheets label I_{DSS} for V_{DS} greater than V_P as $I_{D(on)}$.



FET Characteristic at $V_{GS} = 0$
Figure 10

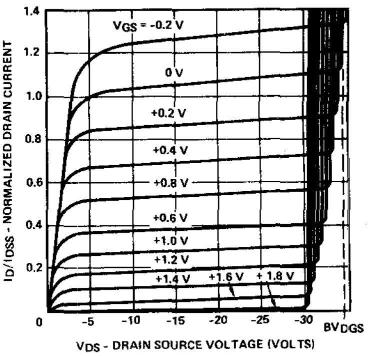
$V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by $R = \rho L/A$, where

ρ = resistivity
L = length of the channel
A = W x T = cross-sectional area of channel

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come in contact, and the a-c or incremental channel resistance, r_{DS}, approaches infinity. As earlier noted, this condition is referred to as "pinch-off" or "cutoff" because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in V_{DS} (up to the junction reverse-bias breakdown) will cause little change in I_D. Accordingly, the pinch-off region is also referred to as the pentode or "constant-current" region.

In Figure 10, pinch-off occurs with $V_{GS} = 0$. In Figure 11, V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D, and smaller values of V_{DS} necessary to reach the "knee" of the curve. The current scale in Figure 11 has been normalized to a specific value of I_{DSS}.



FET I_D vs V_D Output Characteristics
Figure 11

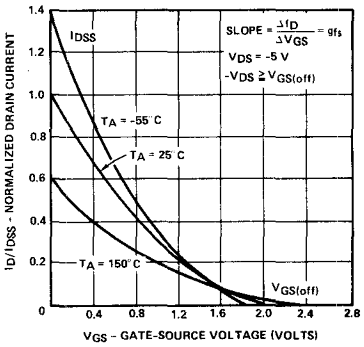
The knee of the curve is important to the circuit designer because he must know what minimum V_{DS} is needed to reach the pinch-off region with $V_{GS} = 0$. When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow; V_{DS} has no effect until breakdown occurs. The specific amount of V_{GS} that produces pinch-off is known as the gate-source cutoff voltage, $V_{GS(off)}$.

$V_{GS(off)}$ Test Procedure

Although the magnitude of $V_{GS(off)}$ is equal to the pinch-off voltage, V_P, defined by the pinch-off knee in Figure 10, rapid curvature in the area makes it difficult to define any precise point as V_P. Taking a second derivative of V_{DS}/I_D would yield a peak corresponding to the inflection point at the knee, which approximates V_P. However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the I_D versus V_{GS} characteristic. This is easier than trying to specify the location of the knee of the I_D versus V_{DS} output characteristic.

A typical transfer characteristic I_D versus V_{GS} is shown in Figure 12. The curve can be closely approximated by

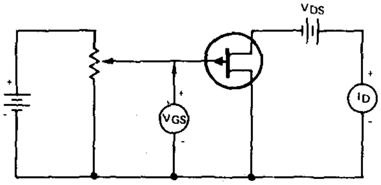
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (4)$$



Typical I_D vs V_{GS} Transfer Characteristic
Figure 12

Equation 4 and Figure 12 indicate that at $V_{GS} = V_{GS(off)}$, $I_D = 0$. In a practical device, this cannot be true because of leakage currents. If I_D is reduced to less than 1 percent of I_{DSS}, V_{GS} will be within 10 percent of the $V_{GS(off)}$ value indicated by Equation 4. If I_D is reduced to 0.1 percent of I_{DSS}, the indicated $V_{GS(off)}$ error will be reduced to about 3 percent. For a true indication of $V_{GS(off)}$, and a realistic picture of the parameters of Figure 12, care must be taken that leakage currents do not result in an error in the $V_{GS(off)}$ reading. Typically, *at room temperature, 1 percent of* I_{DSS} is still well above leakage currents but is low enough to give a fairly accurate value of $V_{GS(off)}$.

A typical circuit for measuring $V_{GS(off)}$ is shown in Figure 13. At $V_{GS} = 0$, the value of I_{DSS} can be measured. Then, by increasing V_{GS} until I_D is 0.01 percent of I_{DSS}, the value of $V_{GS(off)}$ is obtained. From a production standpoint, it is more convenient to specify I_D at some fixed value (such as 1 nA), rather than as a certain percentage of I_{DSS}. Thus a pinchoff voltage specification may be given as indicated in Table I.



Circuit for Measuring $V_{GS(OFF)}$
Figure 13

Table I
Typical Pinch-Off Voltage Specification

Characteristic		Min	Max	Units
$V_{GS(off)}$	Gate-source pinch-off voltage of: $V_{DS} = -5$ V, $I_D = -1$ μA	1	4	Volts

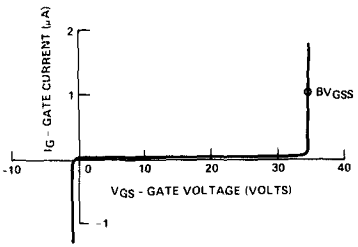
Another method which provides an indirect indication of the maximum value of $V_{GS(off)}$ is shown in Table II. The characteristic specified is $I_{D(off)}$, whereas the parameter of interest is $V_{GS} = 8$ volts. The specification does say that the maximum $V_{GS(off)}$ is approximately 8 volts, but no provision is made for stating a *minimum* $V_{GS(off)}$, as was done in Table I. Therefore, another test must be made if $V_{GS(off)\,(min)}$ is to be specified.

Table II
Indication of Maximum V_p

Characteristic		Test Conditions	Min	Max	Unit
$I_{D(off)}$	Pinch-off drain current	$V_{DS} = -12$ V, $V_{GS} = 8$ V		−10	μA

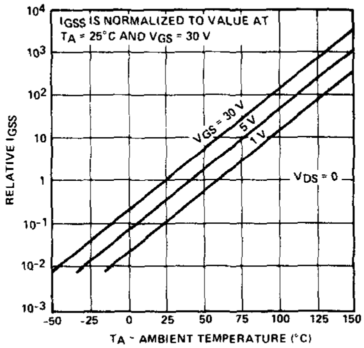
I_{GSS} – Gate-Source Cutoff Current

The input gate of a P-Channel FET appears as a simple PN junction; thus the input d-c input characteristic is analogous to a diode V-I curve, as is shown in Figure 14.



P-Channel FET Input Gate Characteristic
Figure 14

In the normal operating mode, with V_{GS} positive for a P-Channel device, the gate is reverse-biased to a voltage between zero and $V_{GS(off)}$. This results in a d-c gate-source resistance which is typically more than 100M Ω. The gate current is both voltage- and temperature-sensitive. Figure 15 shows this relationship for I_{GSS} versus temperature and V_{GS}.



I_{GSS} vs Temperature
Figure 15

If the gate-source junction becomes forward-biased, (negative voltage in a P-Channel device) or if V_{GS} exceeds the reverse-bias breakdown for the junction, the input resistance will then become very low.

The FET is normally operated with a slight reverse bias applied to the gate-source; hence a good measure of the d-c input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are three common measurements of gate current: I_{GDO}, I_{GSO}, and the combined measurement I_{GSS}. These measurement circuits are shown in Figure 16.

The question is, should I_{GDO} and I_{GSO} be measured separately, or will one measurement of I_{GSS} suffice? One thing is certain: $I_{GSO} + I_{GDO} > I_{GSS}$, because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most FETs, if V_G is greater than $V_{GS(off)}$, the difference between $(I_{GSO} + I_{GDO})$ and I_{GSS} is small; therefore, the measurement of I_{GSS} is a realistic means of controlling both I_{GDO} and I_{GSO}.

In a circuit, V_{GD} may be biased between zero and BV_{GDS}, while V_{GS} will be between zero and $V_{GS(off)}$: therefore, I_G is not necessarily the same as I_{GSS}.

BV_{GSS} – Gate-Source Breakdown Voltage

FET input terminals have been previously described as having NP or PN junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

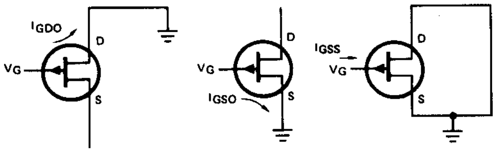
A useful equivalent circuit for a FET is the distributed constant network shown in Figure 17, for a P-Channel FET. If an N-Channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus the gate-drain breakdown rating is most important. However, it is also possible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 17, when a high negative voltage is applied from drain to source, CR_1 will break down while CR_n becomes forward-biased).

Some device manufacturers use a BV_{GDO} rating, which means they are only checking diode CR_1. A better method is to use a BV_{GSS} rating (gate-source breakdown with the drain shorted to the source), because it checks both CR_1 and CR_n, in addition to exposing the *weakest* breakdown path along the entire gate-channel junction. The BV_{GSS} test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

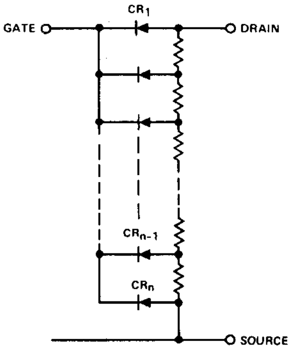
Admittedly, a BV_{GSS} test will reject some units which might pass a BV_{GDO} test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

Test Procedures for BV_{GSS}

Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 18).



Three Common Measurement of Gate Current
Figure 16



A Useful FET Equivalent Circuit
Figure 17

SOFT KNEE (FAILING)

SHARP BREAKDOWN

Examples of Soft Knee and Sharp Knee Breakdown
Figure 18

g_{fs} – Transconductance

Transconductance, g_{fs}, is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}\ ,\ V_{DS} = \text{constant} \qquad (5)$$

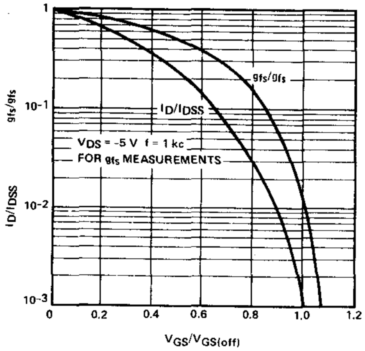
The interrelation of g_{fs} to the parameters I_{DSS} and $V_{GS(OFF)}$ should be noted. Equations 4, 6 and 7 describe the value of I_D and g_{fs} in a FET for any value of V_{GS} between zero and $V_{GS(OFF)}$.

$$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \qquad (6)$$

$$g_{fso} = -\frac{2I_{DSS}}{V_{GS(off)}} \qquad (7)$$

where g_{fso} is the value of g_{fs} at $V_{GS} = 0$ and I_{DSS} is the value of I_D at $V_{GS} = 0$. With these equations, the value of g_{fs} can be calculated with a fair degree of accuracy (20 percent) if I_{DSS} and $V_{GS(off)}$ are known.

Figure 19 shows normalized curves for I_D and g_{fs} as functions of V_{GS} in a P-Channel FET. These curves were obtained from actual measurements on typical diffused channel FETs, such as the 2N2606. The curves agree very well with Equations 4 and 6 until $V_{GS(off)}$ is approached. For these curves, $V_{GS(off)}$ was assumed to be the value of V_{GS} where $I_D/I_{DSS} = 0.001$.



Normalized Curves for I_D and g_{fs} as Functions of V_{GS}
Figure 19

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_D/\text{triode} = I_{DSS}\left(\frac{V_{DS}}{V_{GS(off)}}\right)^{1/2} \qquad (8)$$

Specifications for g_{fs} are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the N-Channel 2N3823 and the P-Channel 2N3329. The gate voltage for the 2N3823 is established as zero. This means that g_{fs} is measured at $I_D = I_{DSS}$, as in Table III.

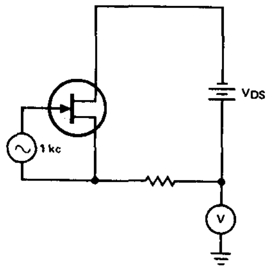
Table III (2N3823)

Characteristic		Test Conditions	Min	Max	Unit
g_{fs}	Small-signal common-source forward transconductance	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	3,500	6,500	μmho

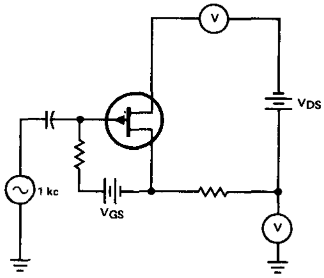
Table IV (2N3329)

Characteristic		Test Conditions	Min	Max	Unit
y_{fs}	Common-source forward transfer admittance	V_{DS} = −10 V, I_D = −1 mA f = 1 kHz		20	μmho

The test conditions shown in Table IV specify a certain value for I_D (−1 mA for the 2N3329). This means that for each unit tested, V_{GS} is adjusted until I_D equals the specified value. The conditions specified in Table III simplify testing of the g_{fs} parameter by eliminating the necessity of adjusting V_{GS}. Figures 20 and 21 show typical test setups for the two methods.



Test Circuit for g_{fs} with V_{GS} = 0
Figure 20



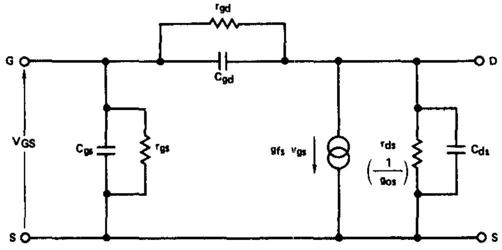
Test Circuit for g_{fs} with I_D Specified
Figure 21

Junction FET Capacitances

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometric distribution are functions of the applied voltages V_{GS} and V_{DS}. Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances, C_{gs} and C_{gd}, exist between the gate and the source and drain, respectively. (A much smaller capacitance, C_{ds}, also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of C_{gs} and C_{gd} as the result of changing conditions of V_{DS}, V_{GS} and temperature. If these data are not presented, an estimate of inter-electrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the -2.2 mV/°C change in junction potential difference.

Assuming that the FET is properly biased – that is, that the d-c conditions are met by the external circuitry – it is possible to construct an incremental equivalent circuit from which the small-signal or a-c performance may be predicted. Such an equivalent circuit is shown in Figure 22.



NOTE: $C_{gss} = C_{iss} = C_{gs} + C_{gd}$

$C_{oss} = C_{gd} + C_{ds} \cong C_{gd} = C_{rss}$

Incremental Equivalent Circuit for the Junction FET
Figure 22

The equivalent capacitance from the gate to the source, C_{gs}, is shunted by a very large input resistance, r_{gs}, with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd}. (For most purposes, r_{gs} and r_{gd} may be neglected, and the gate impedance of the FET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance C_{ds} – which stems from the header material – is shunted by the incremental channel resistance, r_{ds}. This resistance is capable of wide variations, depending on bias conditions. Since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition, r_{ds} will be on the order of megohms.

The incremental channel current is given by the transconductance, g_{fs}, multiplied by the incremental gate voltage. For the small signal, v_{gs}, *this is manifested in the equivalent* circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the FET, in a "positive" direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of g_{fs} adn r_{ds} can be measured as previously mentioned; there remains only the requirement to establish the methods of determining C_{gs} and C_{gd}.

First, assume that the FET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to a-c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gss} \text{ (or } C_{iss}) = C_{gs} + C_{gd} \qquad (9)$$

Second, assume that the gate and source are short-circuited to a-c in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss} \text{ (or } C_{oss}) \approx C_{gd} \qquad (10)$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for C_{gd} is C_{rss}, which refers to the "reverse" capacitance.

In data sheets, it is customary to state (= C_{iss}) C_{gss} and C_{dss} (= C_{oss}). C_{rss} is often given in place of C_{oss} because if $C_{ds} \ll C_{oss}$, which is usually the case, then $C_{rss} \cong C_{oss}$. Equations (9) and (10) can be used in those instances where it is necessary to extract C_{gs} and C_{gd}, as in

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss} \qquad (11)$$

and

$$C_{gd} = C_{rss} \qquad (12)$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the values given in the data sheet for the Siliconix E202 N-channel FET. They are given as

$$C_{iss} \text{ (at } V_{DS} = 20 \text{ V and f} = 1 \text{ MHz)} = 5 \text{ pF max.}$$

and

$$C_{rss} \text{ (at } V_{DS} = 20 \text{ V and F} = 1 \text{ MHz)} = 2 \text{ pF max.}$$

Hence, at a drain-source voltage of 20 V and a frequency of 1 MHz, $C_{gs} = 5 - 2 = 3$ pF maximum. Even though the FET is physically symmetrical, bias conditions have forced the capacitances to be unequal.

Siliconix

APPLICATION NOTE

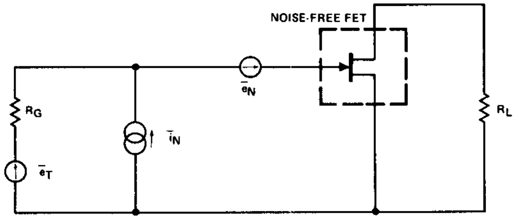
Audio-Frequency Noise Characteristics of Junction FETs

INTRODUCTION

The purpose of this application note is to identify and characterize audio frequency noise in junction field-effect transistors. Emphasis is placed on basic device characteristics rather than on end applications, since it is important for the circuit designer to know the salient noise behavior of the FET, and how those characteristics may be specified by production-oriented test parameters.

Defining FET Noise Figure

For analysis, it is convenient to represent noise in a FET by assuming that an ideal noise-free device has two external noise sources, $\bar{e}_N$ and $\bar{i}_N$. These noise sources are chosen to have the same output as would an actual noisy FET. An equivalent circuit is shown in Figure 1.



Representing Noise in an Ideal FET
Figure 1

A noise factor (F) is a Figure of Merit of a device with respect to the resistance of a generator. To calculate a noise factor, a source resistor R_G, with a thermal noise voltage $\bar{e}_T$, is added to the circuit.

A noise factor (F) may be defined as

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to thermal noise of } R_G}$$

or

$$F = \frac{\text{Noise power output due to } R_G + \text{noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Gain X noise power of FET referred to input}}{\text{Gain X noise power due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power of FET referred to input}}{\text{Noise power due to } R_G}$$

The thermal noise voltage across R_G is(1)

$$\bar{e}_T = \sqrt{4kTR_GB} \qquad (1)$$

where k = 1.380 x 10^{-23} Joules/°K (Boltzmann's Constant), T = temperature in °K, and B = bandwidth in Hz. Therefore noise power due to R_G is

$$\frac{\bar{e}_T{}^2}{R_G} = \frac{4kTR_GB}{R_G} = 4kTB \qquad (2)$$

The noise power of the FET referred to the input is

$$\frac{\overline{e_N}^2}{R_G} + i_N^2 \cdot R_G \qquad (3)$$

When expressions for the noise power of both the FET and R_G are substituted, the noise factor becomes

$$F = 1 + \frac{\overline{e_N}^2 + \overline{i_N}^2 R_G^2}{4kTR_G B} \qquad (4)$$

A noise figure (NF) expressed in dB indicates the presence of added noise power from the FET or another active device. The noise figure is always given with reference to a standard, specifically the generator resistance R_G:

$$NF = 10 \log_{10} [F] \qquad (5)$$

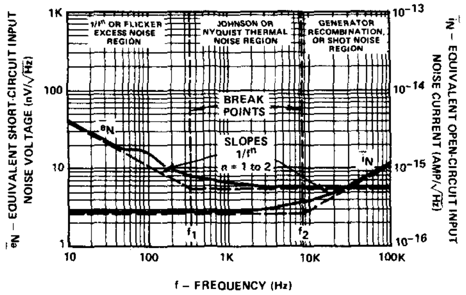
The noise figure of the FET is

$$NF = 10 \log_{10} \left[1 + \frac{\overline{e_N}^2 + \overline{i_N}^2 R_G^2}{4kTR_G B} \right] \text{dB} \qquad (6)$$

When junction FET noise is expressed in terms of the noise figure (NF), an inherent disadvantage arises in that the noise figure value is dependent upon the value of the generator resistance, R_G. Therefore, the $\overline{e_N}$, $\overline{i_N}$ method remains as the best way to quantitatively express the noise characteristics of the FET itself.

Describing Junction FET Noise Characteristics

Junction FET $\overline{e_N}$ and $\overline{i_N}$ characteristics are frequency-dependent within the audio noise spectrum, and take a form as shown in Figure 2.



Characteristics of Junction FET Noise
Figure 2

$\overline{e_N}$, the equivalent short circuit input noise voltage (with the exception of the $1/f^n$ region), is defined as[2]

$$\overline{e_N} = \sqrt{4kTR_N B} \qquad (7)$$

where $R_N \cong 0.67/g_{fs}$, the equivalent resistance for noise. The $\overline{e_N}$, except in the $1/f^n$ region, closely approximates the equivalent thermal noise voltage of the channel resistance.

In the so-called $1/f^n$ region, $\overline{e_N}$ is expressed as

$$\overline{e_N} = \sqrt{4KR_N B(1 + f_1/f^n)} \qquad (8)$$

where n varies between 1 and 2 and is device- and lot-oriented.

The characteristic bulge in $\overline{e_N}$ in the $1/f^n$ region has been observed to some extent in all junction FETs submitted to test. The breakpoint or corner frequency shown as f_1 in Figure 2 is lot- and device design-oriented, and varies from about 100 Hz to 1 kHz.

As indicated in Equations (7) and (8), $\overline{e_N}$ is inversely proportional to the square root of the transconductance of the FET ($\overline{e_N} \propto 1/\sqrt{g_{fs}}$). $\overline{e_N}$ can be lowered by a factor of $1/\sqrt{N}$ if N devices with matched electrical characteristics are connected parallel. For example, when

$$N = 2 \qquad (9)$$

let

$$\overline{e_{N1}} = \overline{e_{N2}} \qquad (10)$$

and let

$$g_{fs1} = g_{fs2} \qquad (11)$$

Thus,

$$g_{fs}\text{TOTAL} = 2\ g_{fs1} \text{ or } 2\ g_{fs2} \qquad (12)$$

From Equation (7)

$$\overline{e_{N1}} = \sqrt{4kT(0.67/g_{fs1})B} \qquad (13)$$

and

$$\overline{e_N}\text{TOTAL} = \sqrt{4kT(0.67/2g_{fs1})B} \qquad (14)$$

Thus,

$$\overline{e_N}\text{TOTAL} = \frac{1}{\sqrt{2}}\, \overline{e_{N1}} \qquad (15)$$

A second way to achieve low $\overline{e_N}$ is to use a device with a large gate area. Empirically, $\overline{e_N}$ is inversely proportional to the square of the gate area ($\overline{e_N} \propto 1/A_G^2$), independent of g_{fs}. This large gate area philosophy has been followed in the design of the Siliconix 2N4867A FET, and noise performance of the device is discussed later in this Application Note. A major advantage of this type of design is that $\overline{e}_N$ is significantly lowered and $\overline{i}_N$ also remains at a low value.

The equivalent open-circuit input noise current, $\overline{i}_N$, with the exception of the shot noise region shown in Figure 2, is due to thermally-generated reverse current in the gate channel junction. It is defined as

$$\overline{i}_N = \sqrt{2qI_GB} \qquad (16)$$

where $q = 1.602 \times 10^{-19}$ coulomb (the magnitude of the electron charge), I_G is the measured DC operating gate current in amperes, and B is bandwidth in Hz. The expression is accurate only when the measured gate current is the result of bulk device conductance. It is possible for the measured gate current to be due to conductance stemming from contamination across the leads of the semiconductor package.

At higher frequencies, as in the shot noise region shown in Figure 2, $\overline{i}_N$ can be approximated as being equal to the Nyquist thermal noise current generated by a resistor:(3)

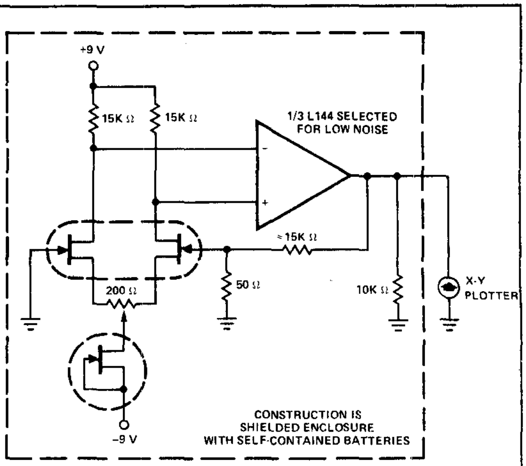
$$\overline{i}_N = \sqrt{\frac{4kTB}{R_p}} \qquad (17)$$

where R_p is the real part of the gate-to-source input impedance. The breakpoint or corner frequency f_2 in Figure 2 is lot- and device design-oriented and can vary from 5 kHz to 50 kHz.

Another form of noise found in junction FETs is known as "popcorn" or burst noise; the term popcorn noise was originated in the hearing aid industry because of noise or level shifts which are present in input stages, and which resemble the sound of corn popping.

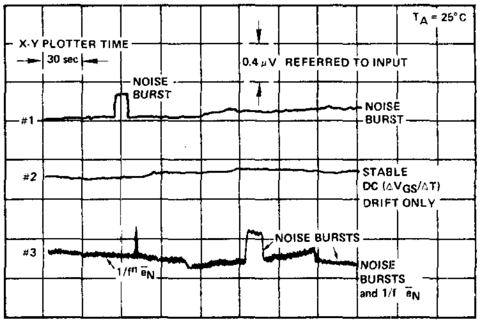
Popcorn noise is a form of random burst input noise current which remains at the same amplitude, and which is confined to frequencies of 10 Hz or lower. The suitability of a FET device is dependent on the amplitude of the burst, its duration, and its repetition rate. The origins of popcorn noise are not completely identified, but are believed to be caused by intermittent contact in aluminum-silicon interfaces and by contamination in the oxidation processes.

A test circuit to measure popcorn noise in differential junction FET amplifiers is shown in Figure 3. In practice, popcorn noise is evaluated on an engineering basis, and not on a production-line basis. No correlation between $1/f^n$ noise at 10 Hz and popcorn noise has yet been found in junction FETs. However, if the amplitude of the burst is large and occurs frequently, then $1/f^n$ noise voltage ($\overline{e}_N$) is masked and difficult to evaluate at 10 Hz.



Test Circuit to Measure Popcorn Noise
Figure 3

The graph in Figure 4 shows "moderate" burst noise observed in a group of junction FET differential amplifiers which were measured in the test circuit.



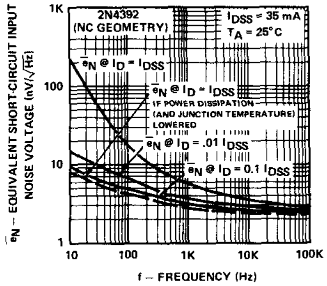
Popcorn Noise in Differential Amplifiers
Figure 4

Operating Point Considerations

Unlike bipolar transistors, where $\overline{e}_N$ and $\overline{i}_N$ characteristics vary directly with change in collector current (I_C), similar characteristics in junction FETs will vary only slightly as drain current (I_D) is varied. This is true so long as the FET is biased so that the drain-source voltage is greater than the pinch-off voltage ($V_{DS} > V_p$ or $V_{GS(off)}$).

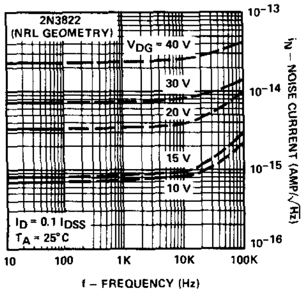
The $\overline{e}_N$ in junction FETs will be lowest when the devices are operated at $V_{GS} = 0$ ($I_D = I_{DSS}$), where transconductance (g_{fs}) is at its highest value. This will be true only if device dissipation is maintained very low in relation to the total dissipation capability of the FET.

The curves in Figure 5 illustrate changes in $\bar{e}_N$ as the operating drain current (I_D) is varied. Note that the lowest $\bar{e}_N$ did not occur at $V_{GS} = 0$, because of high power dissipation and a resultant rise in junction temperature at the operating point.



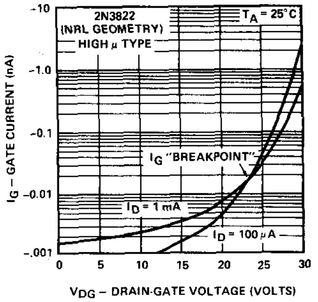
$\bar{e}_N$ Changes vs I_D Variations
Figure 5

The optimum (lowest) $\bar{i}_N$ in depletion-mode junction FETs should occur at $V_{GS} = 0$ ($I_D = I_{DSS}$). In practice, very little change will be seen in $\bar{i}_N$ when the operating point is changed, provided that the drain-gate voltage is maintained below the gate current (I_G) breakpoint and power dissipation is kept at a low level. The curves in Figure 6 illustrate $\bar{i}_N$ characteristics as a function of drain-gate voltage at points below, on, and above the I_G breakpoint voltage.

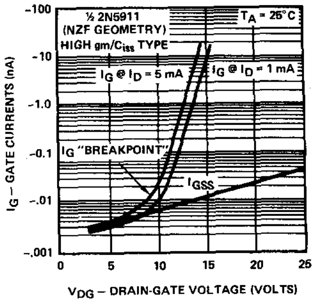


$\bar{i}_N$ Characteristics as Function of Drain-Gate Voltage
Figure 6

In circuit design, particular attention must be paid to drain-gate voltage (V_{DG}) to minimize gate current (I_G) under operating conditions. The critical drain-gate voltage (I_G breakpoint voltage) can be anywhere from 8 to 40 V, depending on device design.[4] Gate operating current (I_G) should not be considered equal to gate reverse current (I_{GSS}) in linear amplifier applications. I_{GSS} is only an indication of reverse-biased junction leakage under non-operating conditions. The Curves in Figures 7 and 8 show how I_G breakpoint is related to basic device design. Device designs with a high g_{fs}/C_{iss} ratio have low breakpoint voltages, typically at V_{DG} = 10 V, whereas high μ devices ($\mu = r_{ds} \cdot g_{fs}$). have much higher I_G breakpoints, typically V_{DG} = 20 – 30 V.



Gate Operating Current vs Drain-Gate Voltage
Figure 7

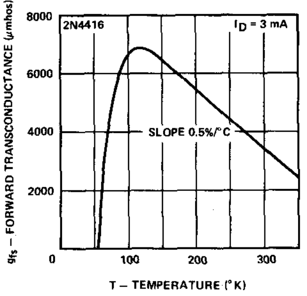


Gate Currents vs Drain-Gate Voltage
Figure 8

Characteristics of $\bar{e}_N$ and $\bar{i}_N$ at Low Temperature

Three equations presented earlier ((7), (16) and (17)) show that $\bar{e}_N$ and $\bar{i}_N$ are temperature dependent. $\bar{e}_N$ and $\bar{i}_N$ are proportional to $\sqrt{T}$, and both will be reduced if the temperature is lowered. In Equation (16), $\bar{i}_N$ is proportional to $\sqrt{I_G}$; I_G will halve for each temperature drop of 10 to 11°C. $\bar{e}_N$ is also proportional to $\sqrt{R_N}$, where $R_N \cong 0.67/g_{fs}$. Thus when g_{fs} is increased, which is typical of junction FETs operating at low temperature, $\bar{e}_N$ will also lower.

In Figure 9, g_{fs} has been plotted vs temperature for a silicon junction FET, and the low temperature limitation caused by a dropoff in g_{fs} is clearly shown.



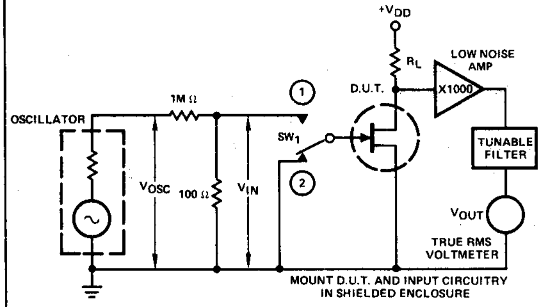
g_{fs} vs Temperature
Figure 9

In connection with the plot of g_{fs} vs temperature, note that the relationship can vary from approximately 0.2% to 1% per degree C. The g_{fs} slope depends upon the basic design of the FET, and upon the proximity of the drain current operating point to I_{DZ}, the zero temperature coefficient point.

The major application for junction FETs at low temperature is in charge-sensitive amplifiers.(5) For best performance in this type of application, a high g_{fs}/C_{iss} ratio is required. Recommended Siliconix FET types for such applications are the 2N4416 (NH geometry) and the U311 (NZA geometry).

Test Measurements

By definition, $\overline{e}_N$ and $\overline{i}_N$ are referred to the input of the device under test. To measure $\overline{e}_N$, the test circuit shown in Figure 10 will prove useful.



Test Circuit to Measure $\overline{e}_N$
Figure 10

The following procedure should be used to make the $\overline{e}_N$ test:

1. Set tunable filter to required f_{low} and f_{high}. Adjust oscillator to mean center frequency ($f_{mean} = [f_{low} \cdot f_{high}]^{1/2}$).
2. Set V_{osc} to 100 mV with Switch 1 in position①. Compute $V_{in1} = 10^{-1} \times \frac{10^2}{10^6} = 10^{-5}\ \mathrm{V} = 10\ \mu\mathrm{V}$.
3. Measure V_{out1}. Compute overall gain as $A_v = \frac{V_{out1}}{V_{in1}} = \frac{V_{out1}}{10\ \mu V}$.
4. Set Switch 1 to position②and measure V_{out2}. Compute V_{in2}, the equivalent short-circuit input noise voltage ($\overline{e}_N$), using A_v from Step 3. $V_{in2} = \frac{V_{out2}}{A_v} = \overline{e}_N$ in volts over bandwidth f_{low} to f_{high}.

An alternate method of performing the above test is to use a Quan-Tech Transistor Noise Analyzer consisting of a Model 2173 Control Unit and a Model 2181 Filter. The analyzer has provision for measuring $\overline{e}_N$ and determining NF with various values of R_G in FET and bipolar devices with selectable test conditions. The measuring system has a constant gain of 10,000. The analyzer records output noise at selected frequencies between 10 Hz and 100 kHz in the device under test, with the scale shown as the actual output divided by 10,000. This is then the output noise referred to the input. The equivalent bandwidth for testing is 1 Hz.

There are certain instances where the test circuit or the Transistor Noise Analyzer are not adequate to measure $\overline{e}_N$ at certain frequencies over certain bandwidths in the $1/f^n$ region. The rms noise over a bandwidth from f_{low} to f_{high}, where there is a $1/f^n$ characteristic over the entire range, can be computed as

$$\overline{e}_N = \left[\overline{e}_N \text{ known}\right] \cdot \left[f_{known} \cdot \ln\left(\frac{f_{high}}{f_{low}}\right)\right]^{1/2n} \tag{18}$$

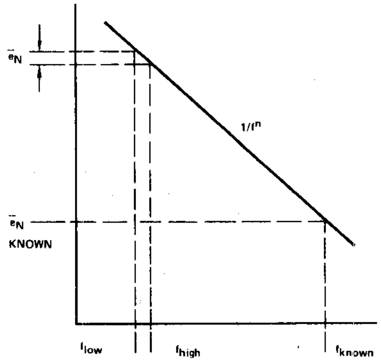
Figure 11 represents this equation graphically. For example, $\overline{e}_N$ known = $70 \times 10^{-9}\ \mathrm{V}/\sqrt{\mathrm{Hz}}$ at 10 Hz. How much noise is in the band from 4.5 to 5.5 Hz? The noise has a $1/f^1$ characteristic over the entire range. Thus

$$\overline{e}_N = \left[70 \times 10^{-9}\right] \cdot \left[10 \cdot \ln\left(\frac{5.5}{4.5}\right)\right]^{1/2} \text{ Volts} \tag{19}$$

or

$$\overline{e}_N = 99.16 \times 10^{-9}\ \mathrm{V}/\sqrt{\mathrm{Hz}} \ @\ 4.975\ \mathrm{Hz}, \tag{20}$$

4.975 Hz is the mean center frequency where $f_{mean} = (f_{low} \cdot f_{high})^{1/2}$.



Computing rms Noise Over a Bandwidth
Figure 11

$\overline{i}_N$ measurements are difficult to implement at best. At frequencies below f_2 in Figure 2, $\overline{i}_N$ is assumed to have a constant level or "white" noise characteristic which may be correlated to gate current, I_G. From Equation (16) I_G is established as the measured bulk gate current. Because measured gate current (I_G) is the result of all conductances at the gate, the resultant gate current and the computed $\overline{i}_N$ due to bulk material can be assumed to be this value or less.

The total equivalent input noise of the FET can be approximated by(6)

$$\overline{e}_{ni}{}^2 = \overline{e}_T{}^2 + \overline{e}_N{}^2 + \overline{i}_N{}^2 \cdot R_G{}^2 \qquad (21)$$

where $\overline{e}_T{}^2$ is the thermal noise of the generator resistance R_G and $\overline{e}_{ni}{}^2$ is the total noise referred to the input. This approximation assumes that the equivalent noise voltage and the current generators vary independently. Equation (21) implies that $\overline{i}_N{}^2$ can be calculated if $\overline{e}_N{}^2$, $\overline{e}_T{}^2$ and total noise $\overline{e}_{ni}{}^2$ are known. The difficulty here is that in MOS or junction FETs, the R_G must be very large to detect the anticipated small value of $\overline{i}_N$. However, when R_G is very large $\overline{e}_T{}^2$ is much greater than $\overline{i}_N{}^2 \cdot R_G{}^2$. For example, over a 1 Hz bandwidth at 25°C, if R_G is equal to 100 MΩ, then

$$\overline{e}_T{}^2 = 4kTR_G = 4 \times 1.38 \times 10^{-23} \times 2.95 \times 10^2 \times 10^8 = 1.63 \times 10^{-12}\ \mathrm{V}/\sqrt{\mathrm{Hz}}. \qquad (22)$$

Anticipated $\overline{i}_N$ is

$$\overline{i}_N \approx 10^{-15}\ \mathrm{Amperes}/\sqrt{\mathrm{Hz}} \qquad (23)$$

and

$$\overline{j}_N{}^2 = 10^{-30}\ \mathrm{Amperes}/\sqrt{\mathrm{Hz}}. \qquad (24)$$

Thus

$$\overline{i}_N{}^2 \cdot R_G{}^2 = 10^{-30} \cdot 10^{16} = 10^{-14}\ \mathrm{V}/\sqrt{\mathrm{Hz}}. \qquad (25)$$

Therefore, $\overline{i}_N{}^2 \cdot R_G{}^2$ is much less than $\overline{e}_T{}^2$, which renders this method of finding $\overline{i}_N$ impractical for most common MOS FETs or junction FETs.

An improved method of measuring $\overline{i}_N{}^2$ is to substitute a low-loss mica capacitor for resistor R_G. The mica capacitor by definition does not have equivalent thermal noise voltage, and thus Equation (21) becomes

$$\overline{e}_{ni}{}^2 = \overline{e}_N{}^2 + \overline{i}_N{}^2 \cdot X_C{}^2 \qquad (26)$$

(where X_C = capacitive reactance)

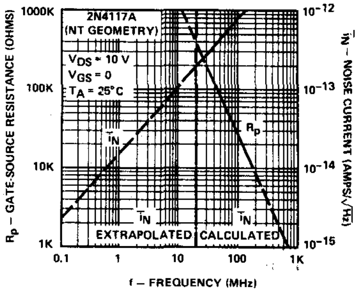
or

$$\overline{i}_N = \frac{(\overline{e}_{ni}{}^2 - \overline{e}_N{}^2)^{1/2}}{X_C} \qquad (27)$$

When a 10 pF mica capacitor was used in the evaluation circuit (up to a frequency of 100 Hz) a correlation of from 80 to 90% was obtained when compared to $\overline{i}_N{}^2$ computed from measured gate current readings.

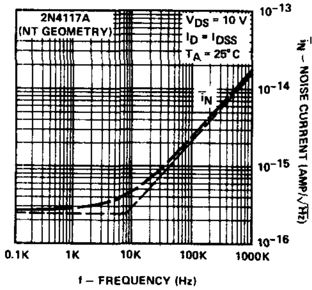
At frequencies above 100 Hz direct computation of $\overline{i}_N$ via the capacitor method becomes unwieldy because of the rapid decrease in capacitor reactance at these frequencies.

In calculating $\overline{i}_N$ at higher frequencies, an alternate method is to measure (R_p) the real part of the gate-source impedance of the FET.(7) When R_p is measured at various frequencies, the equivalent short-circuit input noise current ($\overline{i}_N$) can be computed as a function of frequency (See Equation (17)). A convenient instrument to measure R_p is the Hewlett-Packard Type 250A Rx meter or equivalent. The Type 250A Rx meter can measure R_p accurately up to 200K ohms. As is shown in Figure 12, this establishes the low frequency limit of 20 MHz for $\overline{i}_N$ computed via direct measurement of R_p for the Siliconix FET Type 2N4117A. For frequencies between 100 Hz and 20 MHz, $\overline{i}_N$ must be extrapolated, as is shown in Figures 12 and 13. For FET types with lower R_p (such as the Siliconix 2N4393) $\overline{i}_N$ can be computed down to 2 MHz, and hence extrapolated $\overline{i}_N$ between 100 Hz and 100 kHz is more accurate.



Low Frequency Limit for Calculated $\overline{i}_N$

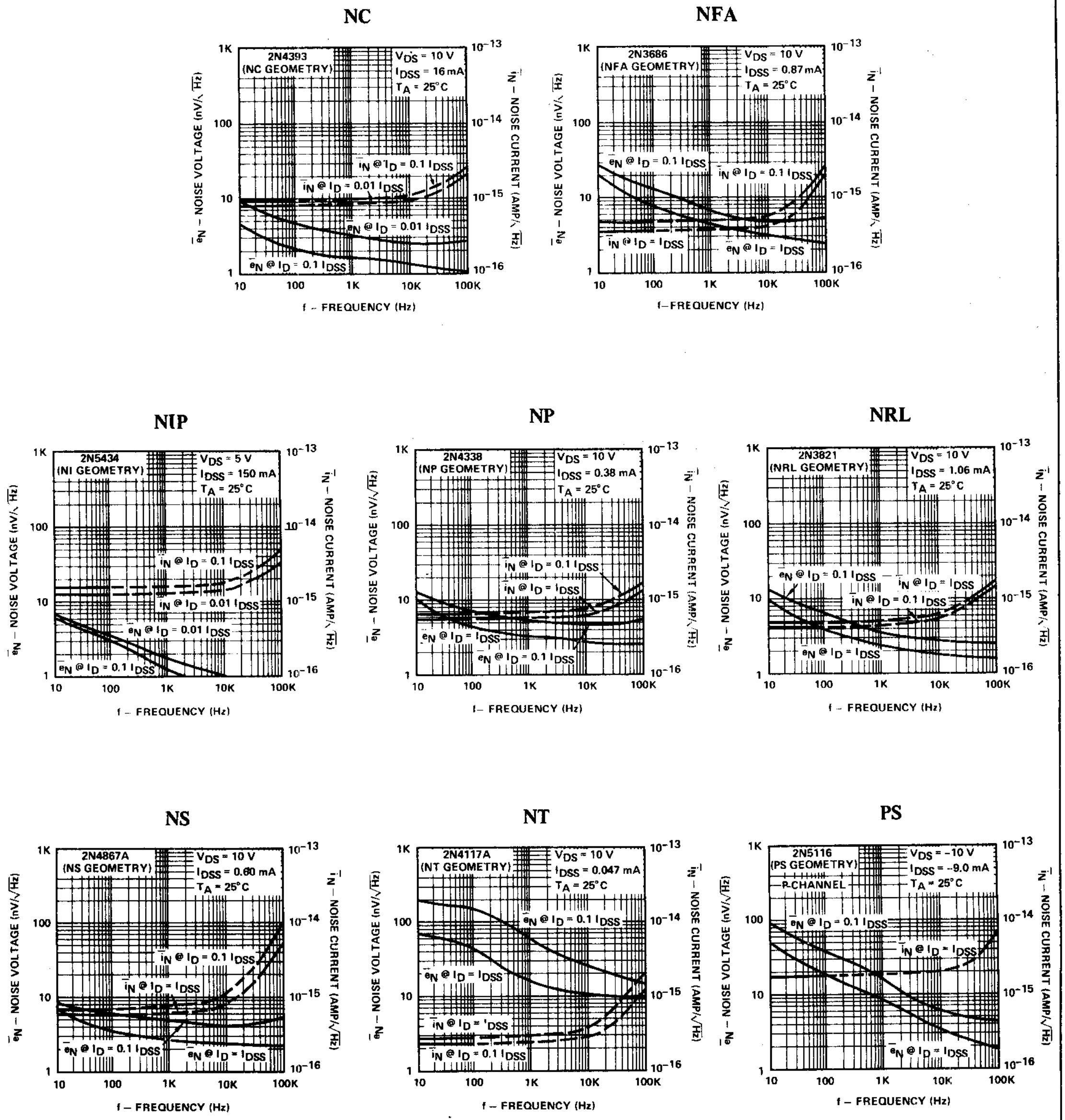
Figure 12



Extrapolated $\overline{i}_N$ vs Frequency

Figure 13

The following are representative $\overline{e_N}$, $\overline{i_N}$ curves for Siliconix J-FET products. Of particular importance is the geometry which by its design governs the basic noise characteristics of product types derived from it.



FET Noise Characteristics by Geometry
Figure 14

CONCLUSION

Contemporary junction FETs have noise voltages ($\overline{e}_N$) equal to those found in low-noise bipolar transistors. Each type of device has a different operating mechanism: the FET is voltage-actuated, while the bipolar transistor is current-actuated. Hence, FETs have an inherently lower noise current ($\overline{i}_N$) and are preferred over bipolar devices in most audio-frequency applications where low-noise performance is a design requirement.

When bias points are properly selected, as described in this Application Note, the excellent low-noise characteristics of high g_{fs} junction FETs can be realized.

The curves shown in Figure 14 are representative of $\overline{e}_N$ and $\overline{i}_N$ performance of Siliconix junction FETs. Of particular importance in these curves is the process geometry by which the basic design of the FET governs the noise characteristics of product types derived from it. Readers are invited to refer to the Siliconix FET catalog for full geometry performance data, and for specific part numbers stemming from the generic process geometries.

In the measurement section of this Application Note, it was shown that direct $\overline{e}_N$ measurements can readily be made. $\overline{i}_N$ can be guaranteed at frequencies below 100 Hz by measuring the DC operating gate current (I_G). When I_G is known, $\overline{i}_N$ can be extrapolated from frequencies below 100 Hz to predict noise performance at frequencies to 100 kHz.

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(4) MacDonald, Charles L., "Behavior of FET Gate Current," Siliconix incorporated Application Note, April, 1969.

(5) Radeka, V., "Field-Effect Transistors in Charge-Sensitive Amplifiers," National Academy of Sciences, National Research Council Publication 1184.

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Siliconix

APPLICATION NOTE

FETs for Video Amplifiers

INTRODUCTION

The field-effect transistor lends itself well to video amplifier applications. Gain bandwidth products in excess of 250 MHz may be easily achieved using simple one or two transistor circuits. DC input resistances in the tens of megohms range may also be easily achieved while input capacitances may be significantly reduced to less than 1 pF by well known circuit techniques. Video amplifiers have applications in communications and pulse amplifying circuits and normally operate up to 100 MHz.

Behavior of FET Input Resistance

A prime FET parameter, input impedance, has a large effect in determining the frequency response of a FET video amplifier. It is not a simple RC network but one in which the real and imaginary parts are a function of frequency.

The voltage generator source resistance R_g and the FET input impedance Z_{in} form a frequency sensitive attenuation network. The larger the R_g, the worse will be the frequency response, and vice versa. Examining this in greater detail, consider the input equivalent circuit of a FET connected in the common source configuration,

where

R_{gs} and R_{gd} = bulk series gate resistance
C_{gs} and C_{gd} = bulk series gate capacitance
G_{OSS} = output conductance

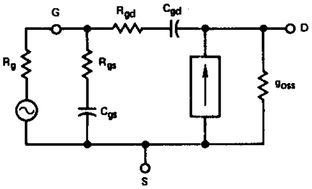


Figure 1

For this analysis the gate source leakage resistance has been ignored due to its high value. Redrawing the input equivalent circuit as a simple parallel RC combination results in

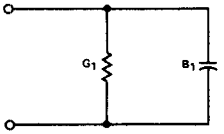


Figure 2

where

$$G_1 = \mathrm{Re}\,|Y_{in}| = \frac{\omega^2[T_1C_1(1+\omega^2T_2^2) + T_2C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2+\omega^2(T_1^2+T_2^2)} \quad (1)$$

and

$$B_1 = \mathrm{Im}\,|Y_{in}| = \frac{\omega[C_1(1+\omega^2T_2^2) + C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2+\omega^2(T_1^2+T_2^2)} \quad (2)$$

where

$$T_1 = C_{gd}R_{gd}$$
$$T_2 = C_{gs}R_{gs} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4) while the input reactance is inversely proportional to the frequency (see Figure 3).

In common-source circuits, $1/G_1$ will typically fall to < 2K ohms at 100 MHz while C_1 remains substantially constant at least up to 1000 MHz. Figures 3 and 4 below exhibit these relationships.

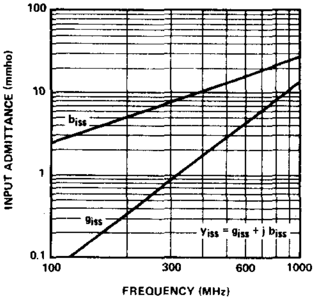
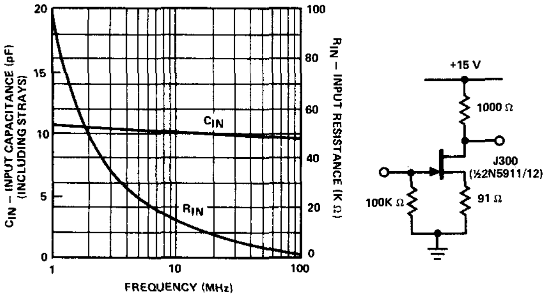


Figure 3



(A) (B)

Figure 4

To maintain low input capacitance, and thus a high input impedance over a wide frequency range, feedback may be applied to most circuits. Such techniques are explored in "FET and Bipolar Cascade" section (page 5). The effect of R_g on the frequency response is shown in Figures 6, 9, 11, 13 where various amplifier configurations are investigated.

Circuits to Consider

Five video amplifier circuits are considered. They are:

- Common-Source Configuration
- Shunt-Peaked Common-Source Configuration
- Source Follower
- Cascode Amplifier
- FET and Bipolar Cascade

Common-Source Circuit[1]

The circuit of Figure 5 features high input impedance and high voltage gain. The drain resistor is set at 560 ohms to maintain good bandwidth which, with 50-ohm generator impedance, is determined primarily by the drain load components. These are:

$$R_D = 560\,\Omega \tag{4}$$

$$C_T = C_{gd} + C_D + C_S \tag{5}$$

C_{gd} = 2.0 pF, C_D the VTVM probe, 2.0 pF, and C_S is circuit stray capacitance of 3 pF.

$$C_T = 2 + 2 + 3 = 7\text{ pF} \tag{6}$$

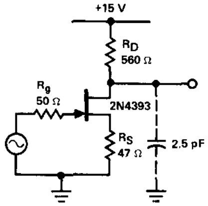


Figure 5

The 3-dB frequency ω_3 is given by:

$$\omega_3 = \frac{1}{C_T R_D} \tag{7}$$

$$= \frac{1}{7 \times 10^{-12} \times 560} \tag{8}$$

$$\omega_3 = 255 \times 10^6 \tag{9}$$

$$f_3 = 39\text{ MHz} \tag{10}$$

The low frequency voltage gain for this configuration is given by:

$$A_V = \frac{g_{fs} R_D}{1 + g_{fs} R_S} \tag{11}$$

$$A_V = 4.9 \tag{12}$$

where

g_{fs} = 15 mmho when I_D = 12 mA, the quiescent current

$$R_D = 560\,\Omega \tag{13}$$

$$R_S = 47\,\Omega \tag{14}$$

Measured Performance

Figure 6 shows the frequency response of the circuit. The low-frequency gain was measured at 4.5 and the 3-dB bandwidth at 44 MHz giving a gain bandwidth product of 197 MHz. This compares with a calculated gain bandwidth of 191 MHz.

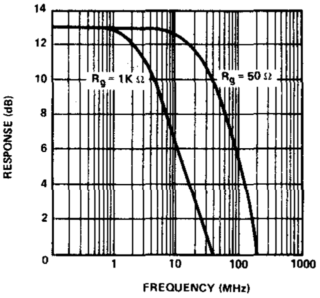


Figure 6

Effect of Increasing Generator Impedance

If the generator resistance R_g is increased to 1K ohm, the input time constant of the FET is increased. The bandwidth of the amplifier is now determined primarily by the input time constant which consists of generator impedance (R_g = 1K ohm) shunted by C_{in} (see Figure 7).

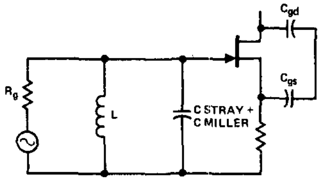


Figure 7

where

$$C_{in} = \left(1 + \frac{g_{fs}R_D}{1 + g_{fs}R_S}\right) C_{gd} + \left(1 - \frac{g_{fs}R_S}{1 + g_{fs}R_S}\right) C_{gs} + \text{Strays}$$

$$= (5.9 \times 3.5) + (0.6 \times 10) + 3. \qquad (15)$$

$$C_{in} = 30\text{ pF} \qquad (16)$$

where

$$C_{gd} = 3.5\text{ pF} \qquad (17)$$

$$C_{gs} = 10\text{ pF} \qquad (18)$$

The corresponding 3-dB frequency is given by:

$$\omega_3 = \frac{1}{C_{in}R_g} \qquad (19)$$

$$= \frac{1}{30 \times 10^{-12} \times 10^3} = \frac{10^9}{30} \qquad (20)$$

$$f_3 = 5.3\text{ MHz} \qquad (21)$$

which agrees closely with the measured bandwidth as shown in Figure 6.

Shunt-Peaked Common-Source Circuit

The frequency response of the resistance-loaded common-source circuit may be significantly extended by shunt peaking at the gate and/or drain. Consider first the gate circuit. Here an inductor may be connected in shunt with the gate and set to such a value that it forms a tuned circuit with the FET input capacitance. The frequency of resonance is determined by:

$$f_0 = \frac{1}{2\pi\sqrt{LC_{in}}} \qquad (22)$$

where

$$C_{in} = C_{iss} + C_{Stray} + C_{Miller} \qquad (23)$$

The response of an input signal of frequency f_0 will then be boosted to an extent depending on the loaded Q of the tuned circuit; the loaded Q in turn is dependent on the unloaded Q of inductor L, R_g and the FET input resistance.

Next consider shunt peaking in the drain circuit. In Figure 8 the inductor L is set to such a value that a low Q tuned circuit is formed; the resonating capacitance C is the parallel combination of C_{gd} plus stray and load capacitances. For a flat response, the LC circuit is tuned to the 3-dB frequency of the resistance loaded circuit of Figure 5. (See Appendix.)

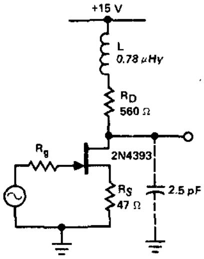


Figure 8

The required value of L is:

$$L = \frac{R_D{}^2C}{2}\text{, and for the circuit in Figure 8.} \qquad (24)$$

$$= 0.78\ \mu\text{H} \qquad (25)$$

where

$$R_D = 560\ \Omega \qquad (26)$$

$$C = C_{gd} + C_{Stray} + C_{VTVM\ PROBE} \qquad (27)$$

$$C = 1.2 + 1.3 + 2.5 = 5\text{ pF} \qquad (28)$$

Due to the low circuit Q (about 5), the value of L is not critical.

The 3-dB bandwidth shown in Figure 9 now extends to 67 MHz giving a gain bandwidth product of:

$$67 \times 4.2 = 281\text{ MHz} \qquad (29)$$

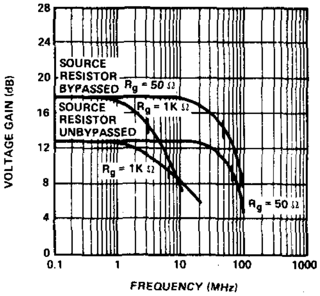


Figure 9

When R_S is bypassed by a 0.1 capacitor, the low frequency voltage gain is given simply by:

$$A_V = g_{fs}R_D \tag{30}$$

$$= 15 \times 10^{-3} \times 560 \tag{31}$$

$$= 8.4\,(18.5\text{ dB}) \tag{32}$$

The gain bandwidth product tends to remain constant whether R_S is bypassed or not and this effect is shown in Figure 9.

Source-Follower Circuit^2

A J300 is used in the FET source-follower circuit, Figure 10, because of its low input capacitance and high g_{fs} which remains high at the frequency range of interest. A source follower exhibits a high input impedance and low output impedance. The real part of the output impedance is the reciprocal of g_{fs} which is independent of frequency up to about 600 MHz. The input capacitance is $C_{gd} + C_{gs}(1 - A_V)$ which, in this case, is approximately 1.5 pF maximum. The input capacitance is also independent of frequency and independent of load when the load is larger than the output resistance R_o.

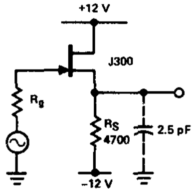


Figure 10

The frequency response is dependent mainly on the generator internal impedance. For example, when R_g is increased to 1K ohm the bandwidth falls to 80 MHz. In this particular circuit, the low-frequency voltage gain is 0.94.

The input resistance is proportional to $1/f^2$ as explained in the section, "Behavior of Input Resistance," and at some high frequency will go negative, particularly if the source resistor is large. For example, with the circuit in Figure 10, the input resistance is high at 10 MHz but in the negative resistance region at 100 MHz. However, when R_S is 1000 ohms, the input resistance is real at this frequency.

The voltage gain of a source follower is given by:

$$A_V = \frac{g_{fs}R_S}{1 + g_{fs}R_S} \tag{33}$$

Thus A_V is almost independent of R_S when R_S is large. Using typical values for the J300 (or ½ 2N5912) in Figure 10, the drain current is 3 mA, g_{fs} is 5 mmho and R_S 4700 ohms,

$$A_V = 0.96$$

which is near the measured value of 0.94. Measured performance is shown in Figure 11. The output resistance of this source follower is given by:

$$R_o = \frac{1}{g_{fs}} = \frac{1}{5 \times 10^{-3}} = 200\,\Omega \tag{34}$$

and in this circuit, R_o was measured at 165 ohms. The source follower is a useful versatile circuit which may be used as an impedance converter, level shifter, buffer stage, or as an input circuit to an op amp or feedback amplifier.

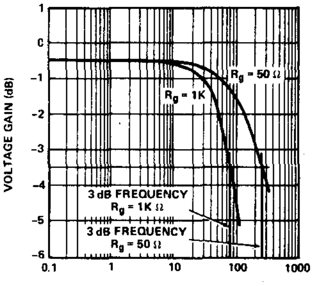


Figure 11

Cascode Circuit

The cascode circuit has applications as a buffer amplifier for use with high stability oscillators or in low level power amplifiers^2 mainly due to its low reverse transfer characteristics. The advantages and considerations of this configuration, Figure 12, are similar to those listed for the common-source circuit. An extra advantage exists in the cascode circuit, namely the low input capacitance:

$$C_{in} = C_{gs} + (1 - A_V)\,C_{dg} \tag{35}$$

$$C_{in} = C_{iss} + C_{gd} \tag{36}$$

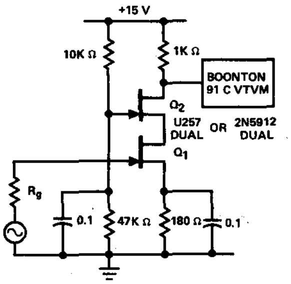


Figure 12

where A_V is the voltage gain from Q_1 gate to Q_1 drain which is essentially unity. C_{iss} for the U257 dual FET is 5 pF and C_{dg} is 1 pF, therefore

$$C_{in} = 5 + 1 = 6\text{ pF, excluding strays of 4 pF}$$

Thus Miller effect is minimized and a good gain bandwidth product is achieved.

Figure 13 shows cascode frequency response. The voltage gain at low frequency is 15 dB (x 5.6) and the bandwidth is 24.5 MHz with a generator impedance of 50 ohms. Gain bandwidth product is 137 MHz.

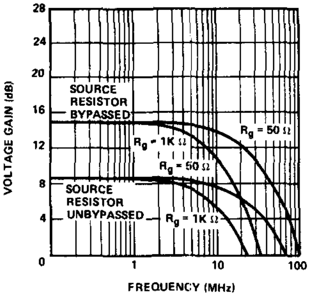


Figure 13

FET and Bipolar Cascade

The FET and bipolar transistor combination of Figure 14 makes a good video amplifier because the FET input provides the voltage gain thus obtaining a superior gain bandwidth product. The feedback capacitor a-c couples the emitter to the drain. The a-c voltage at the gate is nearly equal to that at the source. This source voltage is d-c coupled to the base. This produces an a-c voltage at the emitter whose amplitude is almost equal to that at the base. Thus at the FET, $v_g \cong v_s \cong v_d$ and all three signals are in phase. In this way Miller effect capacitance is largely eliminated.

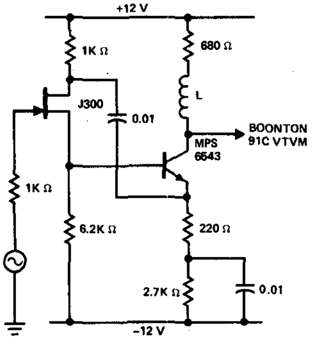


Figure 14

The frequency response of this circuit is controlled by the output time constant if f_t of the transistor is much greater than the amplifier bandwidth. In the circuit shown the a-c load is 2.5 pF.

CONCLUSION

The input resistance of a FET is inversely proportional to the frequency squared, while the input capacitance remains constant to at least 1000 MHz.

Several video amplifier configurations are considered. The common-source circuit is considered first: in the example, the low frequency gain is 4.5 and the 30-dB bandwidth 44 MHz (gain bandwidth 197 MHz). By shunt peaking in the drain circuit, gain bandwidth is increased to 260 MHz. The simple source-follower circuit gives a gain near unity with GBW almost 300 MHz and an output resistance of $1/g_{fs}$. The cascode circuit features a low input capacitance and GBW of 137 MHz. The circuit featuring the best gain bandwidth is the FET and bipolar combination. A gain of 11 dB and bandwidth of 90 MHz is achieved.

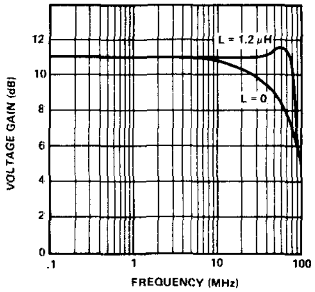


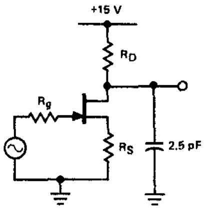
Figure 15

APPENDIX

Selection of Video Amplifier Designs with Performance Summary

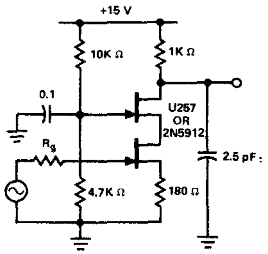
Note. All output voltages measured with Boonton 91C VTVM.

Common Source Stage



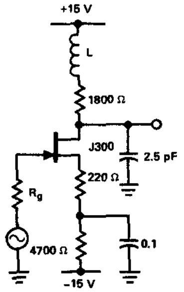
Device	Rg Ω	RS Bypassed	RS Ω	RD Ω	Gain	dB	Cin pF	BW MHz	GBW MHz
2N4393	50		47	560	4.5	13.0		44	197
	50	x	47	560	7.5	17.5		40	300
	1K		47	560	4.5	13.0		5.0	22
	1K	x	47	560	7.5	17.5		3.5	26
J300	50		91	1K	3.8	11.6	11.0	27.5	103
½	50	x	91	1K	6.3	16.0	14.5	30.0	189
2N5912	1K		91	1K	3.8	11.6	11.0	9.5	36
	1K	x	91	1K	6.3	16.0	14.5	6.5	41
2N4416	50		120	1.5K	3.9	11.8	11.5	25	98
	50	x	120	1.5K	6.2	15.8	13	19	118
	1K		120	1.5K	3.9	11.8	11.5	8	31
	1K	x	120	1.5K	6.2	15.8	13	7	44

Cascode



Rg Ω	RS Bypassed	Gain	dB	Cin pF	BW MHz	GBW MHz
50		2.7	8.5	9	27	73
50	x	5.6	15	11.5	27	151
1K		2.7	8.5	9	9.5	73
1K	x	5.6	15	11.5	9.0	51

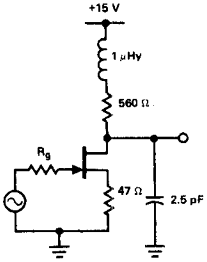
Common-Source Circuit



Rg Ω	L μH	Gain	dB	Cin pF	BW MHz	GBW MHz
50	0	3.5	11	2	20	70
1K	0	3.5	11	2	11	38.5
50	8	3.5	11	2	37	130
1K	15	3.5	11	2	17	60

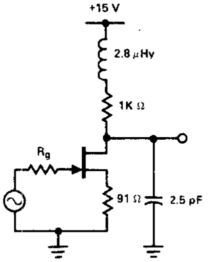
Shunt-Peaked Common-Source Stage

2N4393



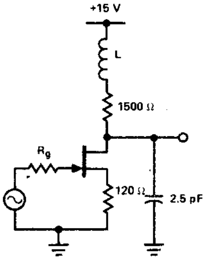
R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		4.2	12.5	66	277
50	x	7.5	17.5	54	405
1K		4.2	12.5	6.0	25
1K	x	7.5	17.5	3.5	26

J300
(½2N5911/12)



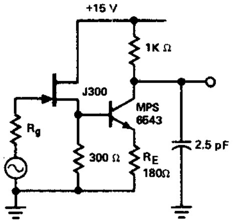
R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		3.9	11.8	67	262
50	x	6.3	16.0	67	421

2N4416

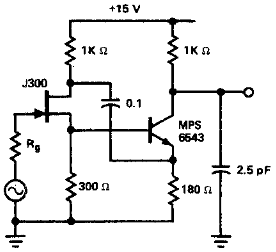


R_g Ω	L µH	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50	4		3.9	11.8	45	175
50	4	x	6.2	15.8	40	248
50	5	x	6.2	15.8	45	279

Common-Drain Common-Emitter Stage

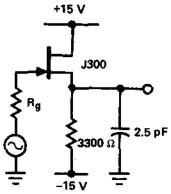


R_g Ω	R_E Bypassed (0.1 µF)	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		3	9.5	2.0	39	117
50	x	25	28	2.0	21	525
1K		3	9.5	2.0	13	39
1K	x	25	28	2.0	11	275



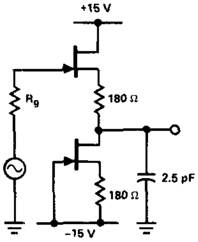
R_g Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	5.6	15	1.0	32	179
1K	5.6	15	1.0	15	84

Source-Follower Circuit



R_g Ω	Gain	C_{in} Stray pF	C_{in} Total pF	R_o Ω	BW MHz	GBW MHz
50	0.92	2.2	2.7	165	350	326
1K	0.92	2.2	2.7	165	55	50

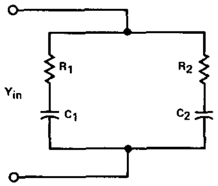
Note. R_o = output resistance of the source follower.



Dual FET	R_g Ω	Offset (Max) (Input to Output) mV	Gain	BW MHz	GBW MHz
U257	50	100	0.98	70	69
2N5912	1K	100	0.98	15	14.7
U232	50	10	0.98	85	83
	1K	10	0.98	13	12.7

Derivation of Input Admittance Terms

where



$R_1 = R_{gs} \quad C_1 = C_{gs} \quad (1)$

$R_2 = R_{gd} \quad C_2 = C_{gd} \quad (2)$

$s \;= j\omega$

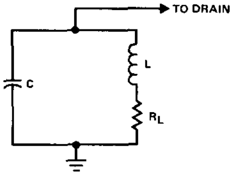
$$Y_{in} = \frac{sC_1}{R_1C_1\,s+1} + \frac{sC_2}{R_2C_2\,s+1} \tag{3}$$

$$= \frac{-\,\omega^2C_1C_2\,(R_1+R_2)+s(C_1+C_2)}{(1-\omega^2R_1R_2C_1C_2)+s(C_1R_1+C_2R_2)} \tag{4}$$

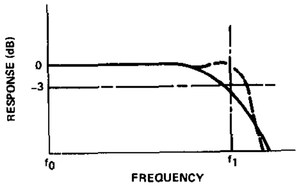
Derivation of Shunt Peaking Formula

The equivalent circuit of the drain load is shown in the Figure below. The total impedance seen by the drain is given by:

$$Z = \left[\frac{R_L{}^2+\omega^2L^2}{(1-\omega^2LC)^2+\omega^2C^2R_L{}^2}\right]^{\frac{1}{2}} \tag{5}$$



The response below shows the "normal" 3-dB frequency without peaking -- f_1. It is now required to raise the response at f_1 by 3 dB to achieve a maximally flat response. Therefore, under these conditions the total impedance seen by the drain at f_1 must equal the impedance seen by the drain at f_o. Also at f_1, $X_C = R_L$. Substituting for X_C in Equation 5:



$$R_L{}^2 = \frac{R_L{}^2+\omega^2L^2}{\left(1-\frac{\omega L}{R_L}\,^{2}+1\right)} \tag{6}$$

$$R_L{}^2 - 2\omega LR_L + \omega^2L^2 + R_L{}^2 = R_L{}^2 + \omega^2L^2 \tag{7}$$

$$R_L{}^2 = 2\omega LR_L \tag{8}$$

$$R_L \;= 2\omega L \tag{9}$$

$$L \;= \frac{R_L}{4\pi\,f_1} \tag{10}$$

and

$$f_1 \;= \frac{1}{2\pi\,R_LC}\;,\therefore\; L = \frac{R_L{}^2C}{2} \tag{11}$$

REFERENCES

1. Sherwin, J.S., "Liberate Your FET Amplifier," Electronic Design, May 1970.
2. Siliconix Application Tip, "FET Cascode Circuits Reduce Feedback Capacitance," August 1970.

Siliconix

APPLICATION NOTE

FETs in Balanced Mixers

Ed Oxner

INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than

Table I

Characteristic	MIXER TYPE		
	Single-Ended	Single Balanced	Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative IM Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L.O. Power	0 dB	+3 dB	+6 dB

Table II

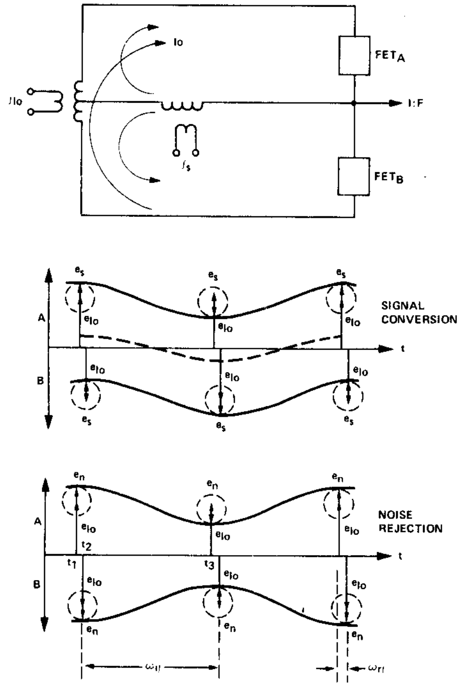
DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L.O. Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain not possible at Optimum Square Law Response Level High L.O. Power
Dual-Gate MOS FET	Low IM Distortion AGC Square Law Characteristic	High Noise Figure Poor Burnout Level Unstable

those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).



Signal and Noise Vectors
Figure 1

Energy conversion into the intermediate frequency (IF) passband is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{ift}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{lo}) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2, the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° (ω_{ift}) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise.(1)

The analysis of the conversion of the signal to the IF passband is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2, the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{lo}. The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a *prototype* balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

(1) Intermodulation and Cross-Modulation
(2) Conversion Gain
(3) Noise Figure
(4) Selecting the Proper FET
(5) Local Oscillator Injection
(6) Designing the Input Transformer
(7) Designing the IF Network

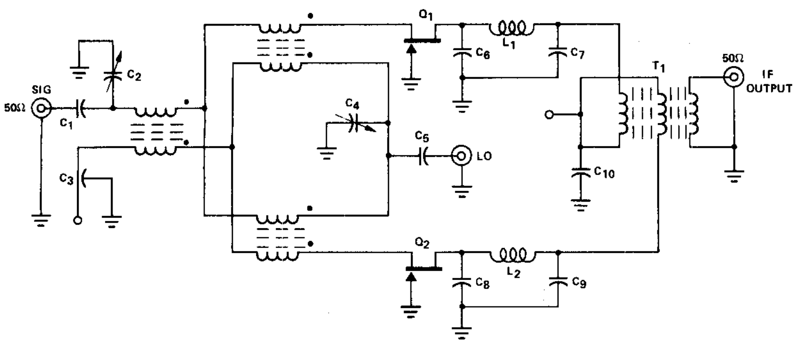
Intermodulation and Cross-Modulation

A basic aim in mixer design is to avoid the effects of intermodulation product distortion and crossmodulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both crossmodulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest.(2)

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an N-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c, is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs}, of the FET when used as an amplifier.



C1, C5 – .01 μfd
C2, C4 – 1 - 10 pF
C3 -- 1000 pF
C6, C8 – 30 pF
C7, C9 – 68 pF
C10 – 0.1 μF
L1, L2 – 1.3 μHy
Q1, Q2 – U310 (2) or U430
T1 – RELCOM BT-9

Prototype Active Balanced Mixer
Figure 2

Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_V, as:

$$A_V = g_c R_L \tag{1}$$

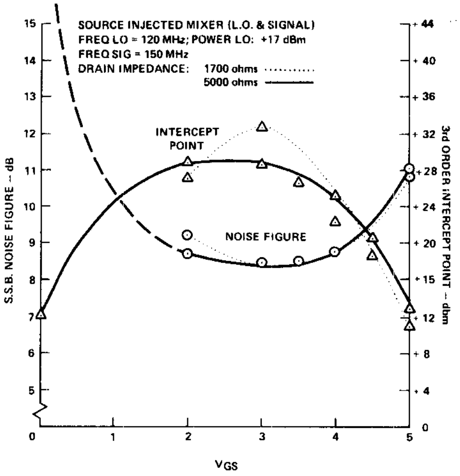
where g_c is the conversion transconductance and R_L is the FET drain load.

An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion – particularly intermodulation product distortion.

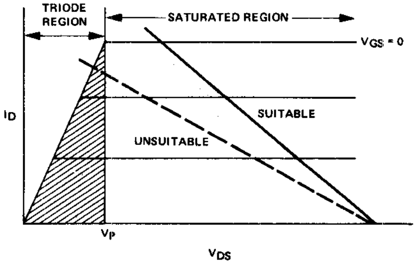
Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted crossmodulation signals.(3) A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 18 through 20.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-source voltage can cause a change in parasitic capacitance, C_{rss}, and give rise to harmonics.(4) A FET tends to be voltage-dependent when the drain voltage falls appreciably below 6 volts. If the source voltage (from the power supply) is also low and the drain load impedance is high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.



Comparison of Mixer IM Characteristics
Figure 3



Plotting Drain Load Lines
Figure 4

Conversion Gain

In a FET, forward transconductance is defined as(5)

$$g_{fs} = \frac{dI_D}{dV_{gs}} \tag{2}$$

and conversion transconductance is defined as(6)

$$g_c = \frac{dI_{D(\omega i)}}{dV_{gs(\omega r)}} \tag{3}$$

where ωi = the intermediate frequency and ωr = the signal frequency.

The effects of time-varying local oscillator voltage, V_2, and the much smaller signal voltage, V_1, must be considered:

$$v_{gs} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \tag{4}$$

For square law operation(7)

$$V_2 + V_{GS} \leqslant V_{GS(off)} \tag{5}$$

Drain current is approximately defined by (8)

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \tag{6}$$

or (9)

$$I_D \approx \frac{g_{fso} V_{GS(off)}}{2} \left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \tag{7}$$

or

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \left[V_{GS(off)} - v_{gs}\right]^2 \tag{8}$$

then(10)

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \text{ (complex Taylor expansion)} \tag{9}$$

which can be reduced to

$$I_{D(IF)} \approx \frac{g_{fso}}{2V_{GS(off)}} V_1 V_2 \cos(\omega_1 - \omega_2)t \tag{10}$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2V_{GS(off)}} |V_2| \tag{11}$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

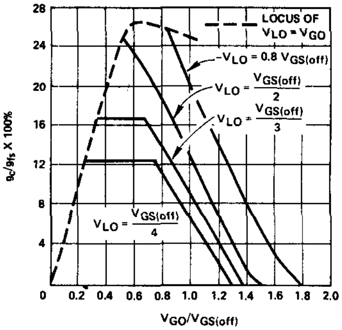
Thus

$$2\, V_2 \text{ peak} \leqslant V_{GS(off)} \tag{12}$$

or

$$V_2 \text{ peak} \leqslant \frac{V_{GS(off)}}{2} \tag{13}$$

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.

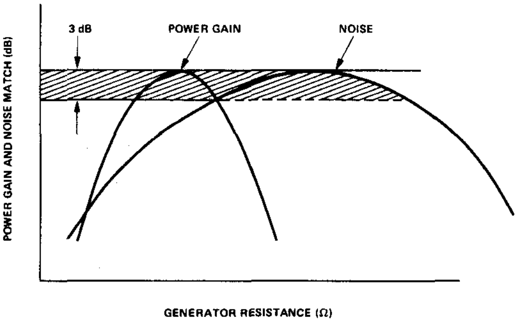


Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$
(from "FET RF Mixer Design Technique", S.P. Kwok, WESCON Convention Record (1970) 8/1, p.2.)
Figure 5

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g.(11) A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{igs}, which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.



Power Gain and Noise Matching
Figure 6

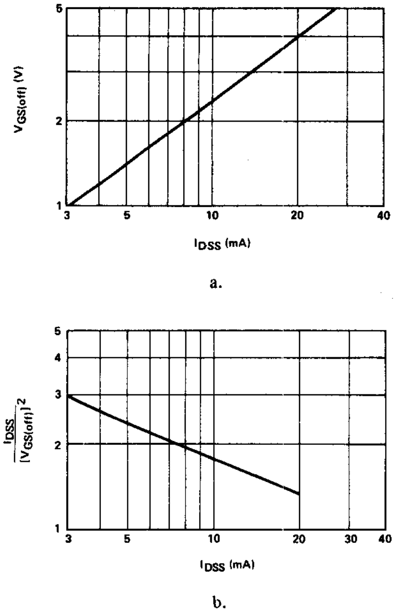
How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c, which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS}, and the gate cutoff voltage, $V_{GS(off)}$:

$$g_c = \frac{I_{DSS}}{V_{GS(off)}^2} |V_2| \qquad (14)$$

$$\approx \frac{g_{fso}}{2V_{GS(off)}} \qquad (15)$$

Equation 15 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7A and 7B show that devices from a family selected for high I_{DSS} do *not* provide high conversion transconductance, but actually produce a lower value of g_c.



Relationship of I_{DSS} and $V_{GS(off)}$
Figure 7

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS}, for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 20,000 μmhos max at V_{DS} = 10 V, I_D = 10 mA, and f = 1 kHz.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach — the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember, however, that conversion transconductance, g_c, can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a number of possible alternatives to the U310.

Table III

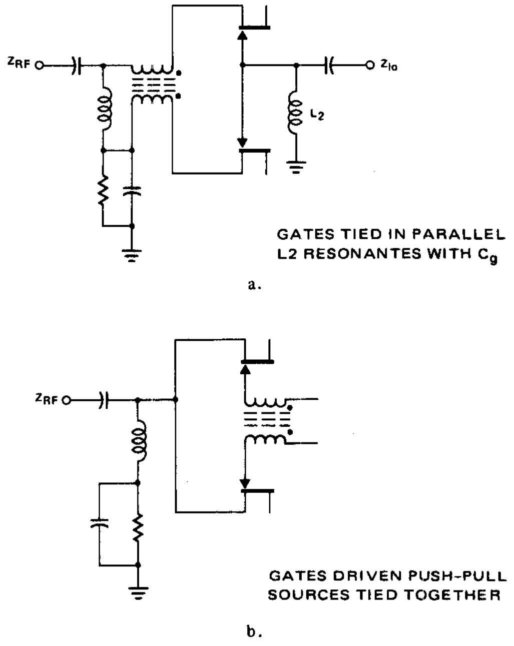
Typical Characteristic	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	14K	6K	5K	3.5K
I_{DSS}	40 mA	15 mA	10 mA	10 mA

*Similar devices are also available in plastic packages:
U310 (J310)
2N5397 (K300-18)
2N4416 (2N5486, K304-18)

Local Oscillator Injection

Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing, Two circuits to obtain direct gate coupling are suggested in Figure 8.



Alternate Forms of L.O. Injection
Figure 8

The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer. best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-ohm load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

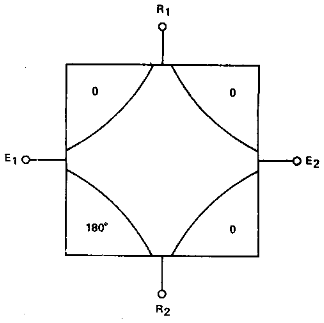
(1) Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B

(2) Offer a match between either input to a symmetrical balanced load

(3) Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)

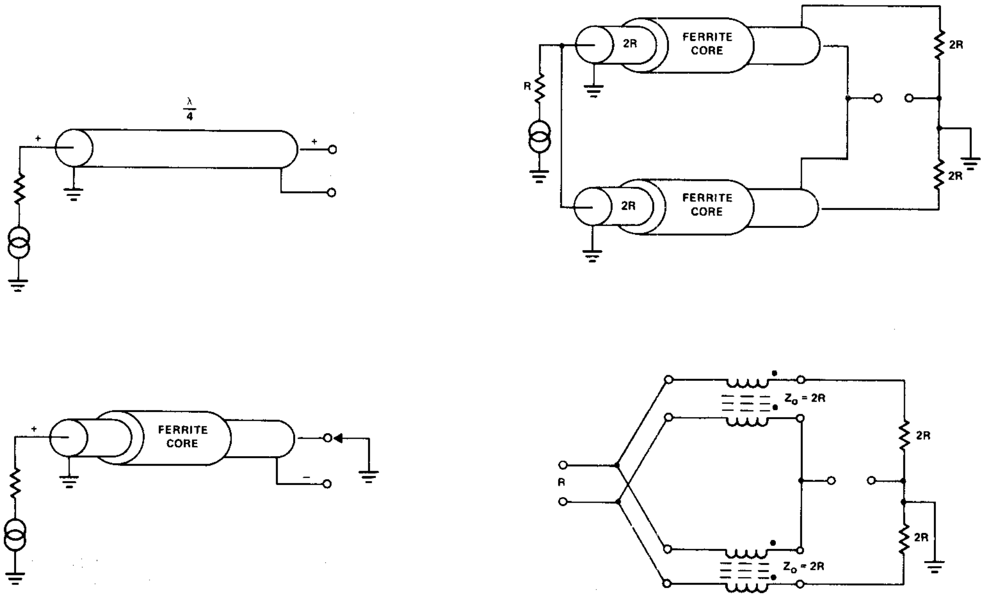
(4) Maintain a differential phase of 180° across the symmetrical balanced loads

(5) Introduce the least possible amount of loss



4-Port Hybrid with Phase and Isolation
Figure 9

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite.(12) The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff.(13)



Hybrid Input Coupling Transformer
Figure 10

Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis.(14) The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{upper}} \text{ (inches)} \tag{16}$$

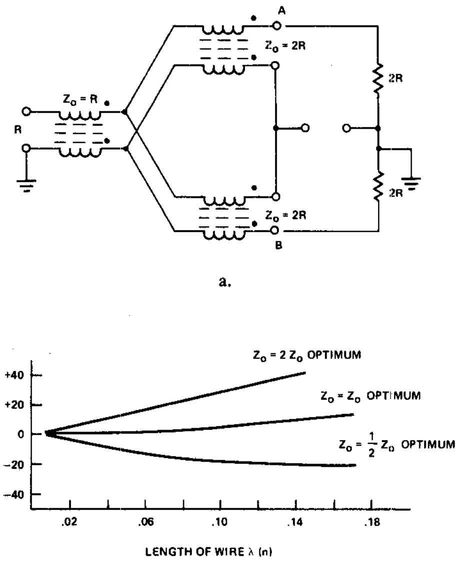
$$\text{min length} = \frac{20\, R_L}{(1 + \mu/\mu_o)\, f_{lower}} \text{ (inches)} \tag{17}$$

where R_L = the load impedance, μ/μ_o = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q.

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium.(15) A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line condcutors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_o, is to be preferred over a higher Z_o. Both 50-ohm and 100-ohm transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide Z_o = 100 ohms. Each core is wound with 2 inches of the proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 16, 17).

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4, Figure 2).(16) A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ±2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.



a.

b.

Toroid Coil Winding Data
Figure 11

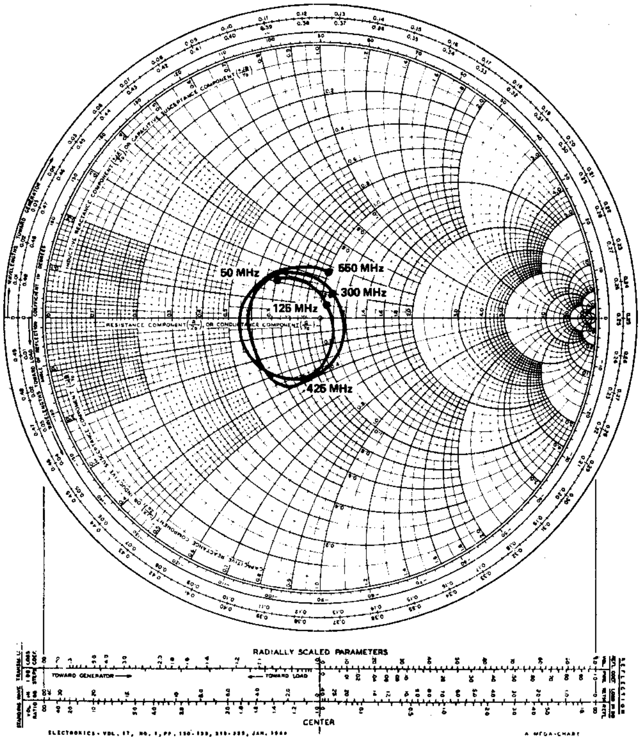
Designing the IF Network

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network.(17) This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_o.(18, 19) This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and crossmodulation will be



50Ω – 200Ω Balun

Figure 12

both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors.(20) If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2\,V_{GS(off)}}{i_d} \qquad (18)$$

where

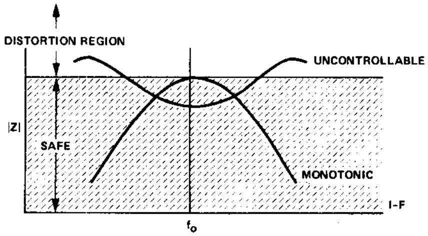
$$i_d = I_{DSS}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \qquad (19)$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \qquad (20)$$

For the U310 FET, the optimum drain load impedance is established at slightly less than 2000 ohms, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-ohm CT to 50-ohm trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 ohms on each FET; excellent



Pi (π) Match Filter Function

Figure 13

IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Mixer Performance

Tests of the operational prototype FET balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table IV (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point.(21) With two signals 300 kHz apart, the balanced mixer suppressed third-order products −89 dB with both signals at −10 dBm, representing an intercept point of +32 dBm.

Table IV

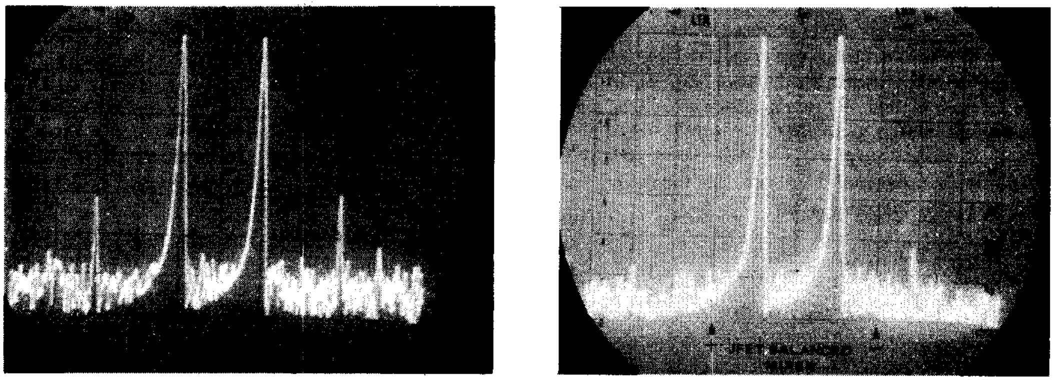
50-250 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dBm	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	−6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

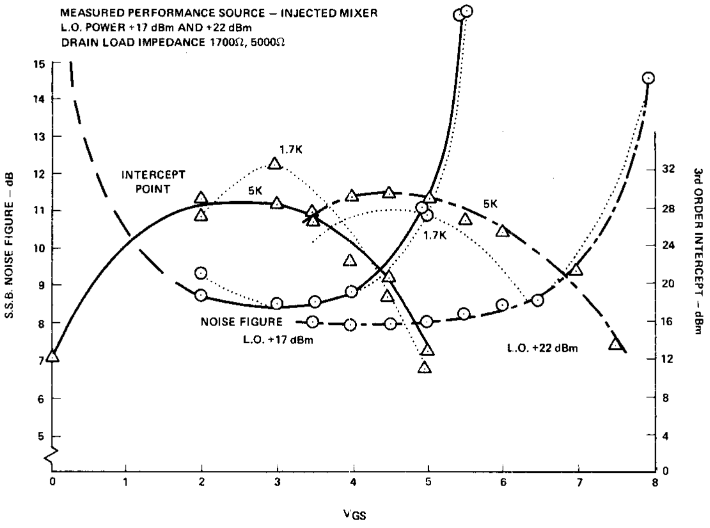
†Estimated *Conservative minimum

Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.



Comparison of 3rd Order IM Products
Figure 14



Noise Figure and intercept Point Performance
Figure 15

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 16 and 17) are equally applicable to trifilar as they are for bifilar.

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Siliconix

APPLICATION NOTE

FETs As Voltage-Controlled Resistors

INTRODUCTION

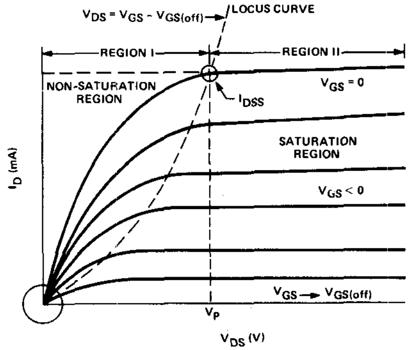
The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage, V_{GS}, and the net drain-source voltage, V_{DS}.

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.(1) Maximum drain-source current, I_{DSS}, and minimum resistance, $r_{DS(on)}$, will exist when the gate-source voltage is equal to zero volts ($V_{GS} = 0$). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.(2) The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.

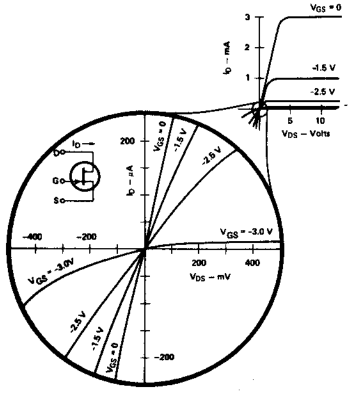


Typical N-Channel JFET Operating Characteristics
Figure 1

Resistance Properties of FETs

The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{ds}, is essentially the same as that of d.c. resistance, r_{DS}, and is a function of V_{GS}.$^{(3)}$

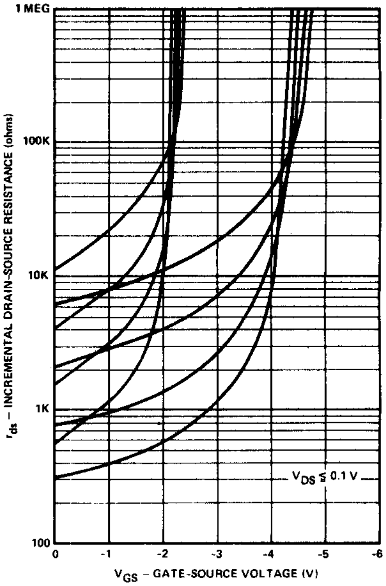
Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $\Delta I_D/\Delta V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS}, usually expressed as $r_{DS(on)}$, occurs at $V_{GS} = 0$ and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS}. Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.



N-Channel JFET Output Characteristic Enlarged Around V_{DS} = 0
Figure 2

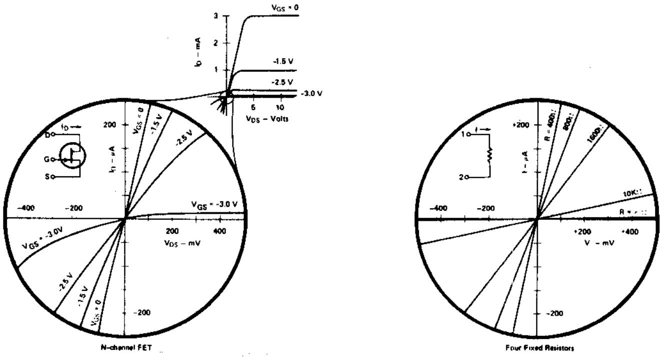
Figure 3 extends the r_{ds} characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.

Typical r_{DS} curves for several Siliconix N-channel JFETs are plotted in Figure 4.$^{(4)}$ The graphs are useful in estimating r_{DS} values at any given value of V_{GS}. All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefor deisrable to convert Figure 4 to a normalized plot. This has been done in Figure 5. The resistance is normalized to its specific value at V_{GS} = 0 V. The dynamic range of r_{DS} is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.



Incremental Drain-Source Resistance for Typical N-Channel FETs
Figure 4

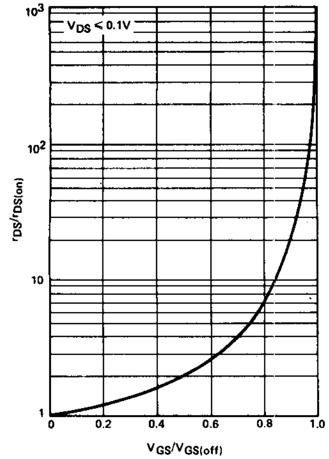
Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω (Figure 7).



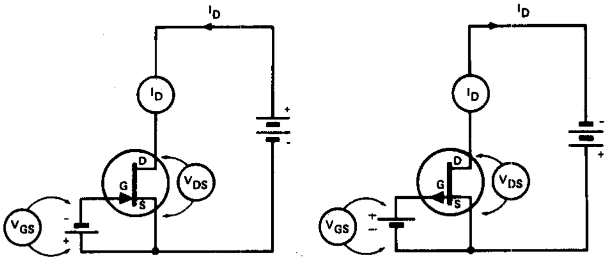
N-channel FET

Four Fixed Resistors

Comparison of FET and Resistor Characteristics
Figure 3



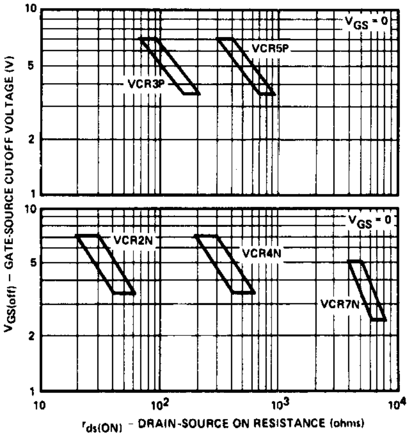
Normalized r_{ds} Data
Figure 5



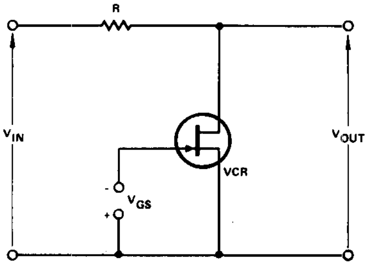
(a) N-channel FET

(b) P-channel FET

Circuit Arrangement for Both an N and P Channel FET
Figure 6



$r_{ds(on)}$ (Drain-Source Resistance at $V_{DS} = V_{GS} = 0$)
Varies as an Inverse Function of $V_{GS(off)}$
Figure 7



Simple Attenuator Circuit
Figure 8

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.$^{(5)}$

The output voltage is

$$v_{OUT} = \frac{V_{in}\, r_{DS}}{R + r_{DS}} \qquad (1)$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which v_{OUT} can assume is

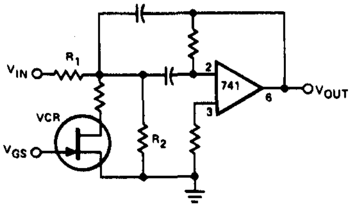
$$v_{OUT(min)} = \frac{V_{in}\, r_{DS(on)}}{R + r_{DS(on)}} \qquad (2)$$

The highest value is

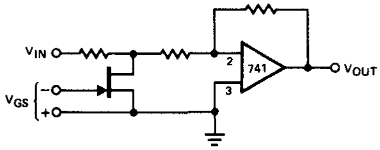
$$v_{OUT(max)} = v_{in} \tag{3}$$

since r_{DS} can be extremeley large.

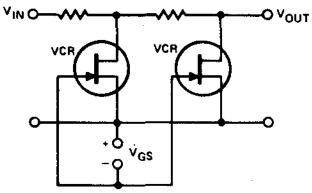
A number of other FET VCR applications are shown in Figures 9-16.



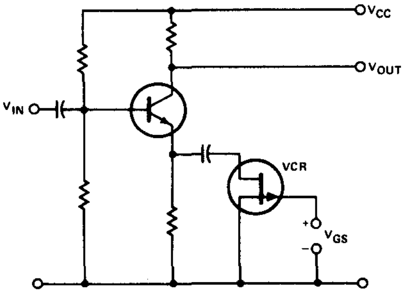
Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET $V_{GS(off)}$ and Tuned by R_2. Upper Frequency is Controlled by R_1
Figure 9



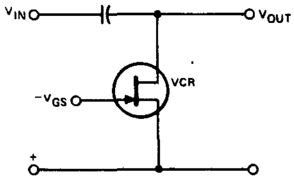
Electronic Gain Control
Figure 10



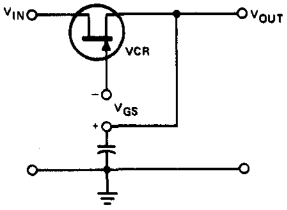
Cascaded VCR Attenuator
Figure 11



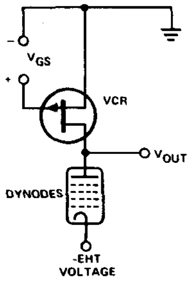
Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level
Figure 12



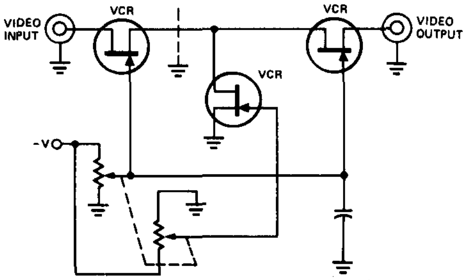
VCR Phase Advance Circuit
Figure 13



VCR Phase Retard Circuit
Figure 14



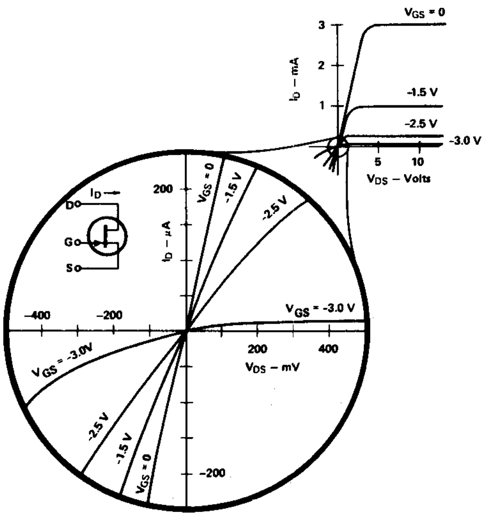
P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually < 1 μA) Implies that VCR will Always Perform in Linear Region Near Origin
Figure 15



Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides for Optimum Dynamic Linear Range Attenuation
Figure 16

Signal Distortion: Causes

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS}, and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current, so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 17B shows how the current has an opposite effect in the third quadrant, rising negatively with an increasingly negative V_{DS}. This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 17A

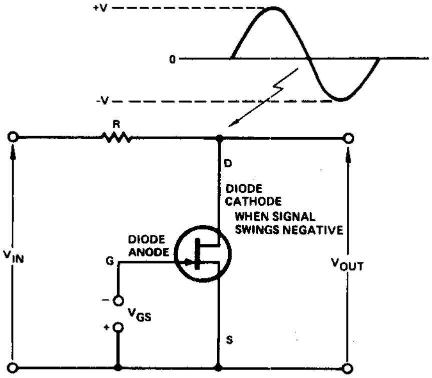


Figure 17B

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

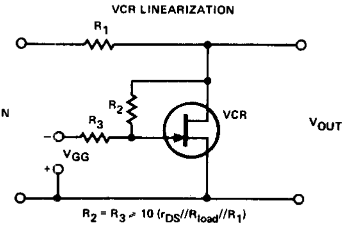


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geqslant 10\ [R_1 \,||\, r_{ds}(\text{max}) \,||\, R_L] \qquad (4)$$

Typically, 470K Ω resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)} \,||\, R_L$ to $[(r_{DS(on)} \,||\, R_L) + R_1]$ gives the desired output voltage, or:

$$e_o = e_i \; \frac{r_{DS(on)} \,||\, R_L}{(r_{DS(on)} \,||\, R_L) + R_1} \qquad (5)$$

The feedback technique used in Figure 18 requires that the gate control voltage, V_{GG}, be twice as large as V_{GS} in Figure 17B for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

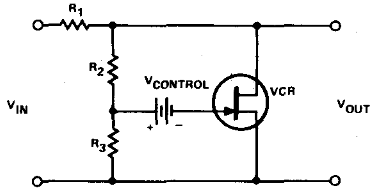


Figure 19

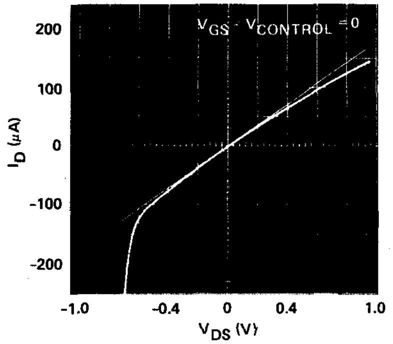
Experimental Results

Figures 20 through 23 show low voltage output characteristic curves for a typical Siliconix N-Channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 20 shows a two-volt peak-to-peak signal on the V_{GS} = 0 V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.

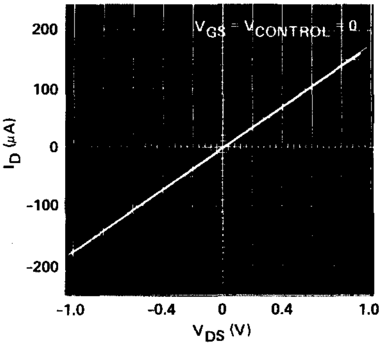
The forward-biased gate-drain PN junction may be seen at approximately −0.6 V, and bending of the bias curve is apparent in the third quadrant. The photo also demonstrates the comparison between a fixed resistor (the linear line superimposed on the bias curve) and the distortion apparent in the VCR without feedback compensation; the VCR signal is unusable with the indicated amount of distortion.

In Figure 21, the same VCR7N FET is shown operating with the addition of the feedback resistors. Distortion has been reduced to less than 0.5%, and the characteristics of the VCR are now closely comparable to those of a fixed resistor.

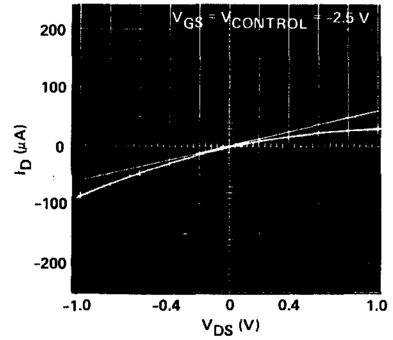
In Figures 22 and 23, the same VCR FET characteristics are shown, with V_{GS} adjusted for higher r_{DS}. No feedback network is employed in Figure 22, and measured distortion is greater than 8%. In Figure 23, the feedback resistors have been added and distortion has been reduced to less than 0.5%.



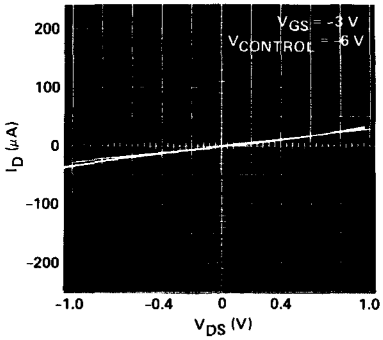
VCR7N with No Feedback
Figure 20



VCR7N with Feedback
Figure 21

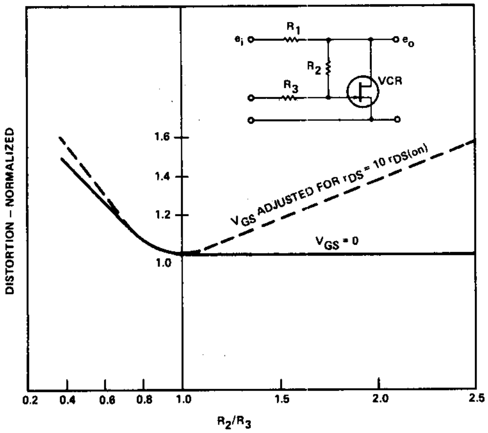


VCR7N with No Feedback
Figure 22



VCR7N with Feedback
Figure 23

Some degree of non-linearity will be experienced in both the first and third quadrants as V_{GS} approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants. Figure 24 shows a curve of distortion vs R_2/R_3, in both quadrants.



Distortion vs R_2/R_3
Figure 24

Distortion resulting from changes in temperature are also minimized by the feedback resistor technique. r_{DS} will change with temperature in an inverse manner to the behavior of FET drain current. Table I presents the result of VCR laboratory performance tests of distortion vs temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

Table I

Temperature (°C)	Without Feedback		With Feedback	
	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\, r_{DS(on)}$	$r_{DS} = r_{DS(on)}$	$r_{DS} = 10\, r_{DS(on)}$
+125	>13%	>6%	<0.5%	<0.5%
+ 25	>10%	>5%	<0.5%	<0.5%
− 55	3.9%	3.2%	<0.5%	<0.5%

SUMMARY

This Application Note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no DC bias voltage in the signal loop, an ideal characteristic for many applications.

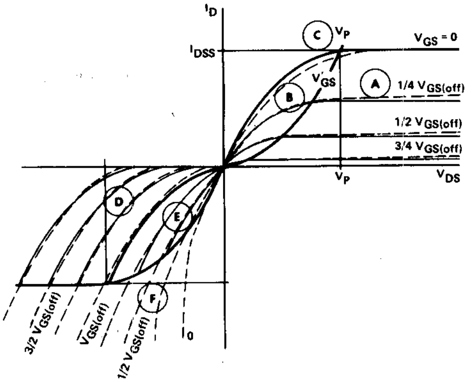
Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high $V_{GS(off)}$ will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high $V_{GS(off)}$ (compatible with the desired r_{DS} value) if large signal levels are to be encountered.

APPENDIX A – From proceedings of the IEEE, October, 1968, pp. 1718-1719.

Abstract – An analytical approximation of FET characteristics for positive and negative voltages is presented. The distortion in an application as a controlled attenuator is calculated, and a method of reducing distortion by a factor of more than 50 is described.

Controlled resistors are used in oscillators, controlled amplifiers, and attenuators.(6,7) The possible control range is much larger for field-effect transistors (FET) than for other elements with comparable time constants (e.g., diodes). The signal-to-noise ratio is considerably improved.



Comparison Between Mathematical Approximation of FET Characteristics (Solid Lines) and Measured Curves (Broken Lines) for a Typical N-Channel JFET
Figure 25

Figure 25 shows idealized and real FET characteristics. In region A (above pinch-off) I_D is independent of V_{DS}:(8)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (1)$$

Region B, where $V_{DS} < (V_{GS} - V_P)$, is the so-called triode region. (In the following discussion all the signs (+, −) will be valid for N-Channel FETs.) The characteristics can be approximated by a quadratic function, of which the maximum and a second point (the origin) are known. The approximation is

$$I_D = I_{DSS}\left[\left(1 - \frac{V_{GS}}{V_P}\right)^2 - \left(1 - \frac{V_{GS} - V_{DS}}{V_P}\right)^2\right]$$

$$= \frac{2I_{DSS}}{(V_P)^2}\, V_{DS}\left(V_{GS} - V_P - \frac{V_{DS}}{2}\right) \qquad (2)$$

This is the same function that can be found by a simple analysis based on semiconductor theory. The less negative of the two voltages across the junction (V_{GS}, V_{GD}) controls the channel conductance. Under the condition that the FET is symmetrical (drain and source interchangeable), the following consideration is true. If V_{GD} were the controlling voltage and $V_{DS} < 0$, $I_D < 0$, then the characteristics would be the same as in the first quadrant:

$$-I_D = -\frac{2I_{DSS}}{V_P^2}\, V_{DS}\left(V_{GD} - V_P + \frac{V_{DS}}{2}\right) \qquad (3)$$

Since the controlling voltage for both regions (B and E) is V_{GS},

$$V_{GD} = V_{GS} - V_{DS} \qquad (4)$$

Substituting (4) into (3), we get (2); the same approximation can be used in B and E. The limits of region E where (2) is valid are $V_{GD} = 0$ and $V_{GD} = V_P$. The characteristics in region D can be found from (1) with the same consideration:

$$I_D = -I_{DSS}\left(1 - \frac{V_{GS} - V_{DS}}{V_P}\right)^2 \qquad (5)$$

The mathematical approximation is compared with the measured characteristic in Figure 25. In the regions C and F the junction is forward biased. The characteristics are dependent on the internal resistance of the gate voltage source since gate current flows.

The FET as a controlled resistor works in region B and E. The higher the resistance, the more non-linear are the characteristics. For most applications this is undesirable. Based on the simple approximation (2), the relation between distortion, control range, and maximum to minimum attenuation will be described for a simple voltage divider [Figure 26(a)]. Most applications can be based on this simple example. The conductance in any point of region B or E is

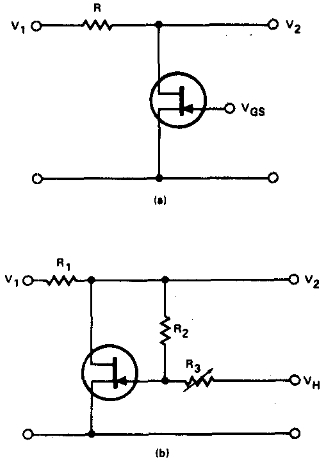
$$G_{DS} = \frac{I_D}{V_{DS}} = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$-\frac{I_{DSS}}{(V_P)^2}\, V_{DS} = g_{DS} + \frac{g_{DSS}V_{DS}}{2V_P} \qquad (6)$$

where g_{DS} is the differential conductance at the origin; when $V_{GS} = 0$, then $g_{DS} = g_{DSS}$. The attenuation for the circuit of Figure 26(a) is

$$\frac{V_2}{V_1} = \frac{1}{1 + Rg_{DS}}$$

$$= \left[1 + Rg_{DS} + \frac{Rg_{DSS}V_1}{2V_P\left(1 + Rg_{DS} + \frac{2Rg_{DS}V_1}{2V_P(1 + Rg_{DS})}\right)}\right]^{-1} \qquad (7)$$



(a) Controlled JFET Attenuator. (b) Controlled Attenuator with "Feedback" Making Characteristics Linear and Symmetrical
Figure 26

To reduce (7) to a more tractable form, the following inequality is introduced:

$$\frac{V_1\, Rg_{DSS}}{2V_P\,[1 + Rg_{DS}]^2} \ll 1$$

so that (7) can now be approximated by the expansion

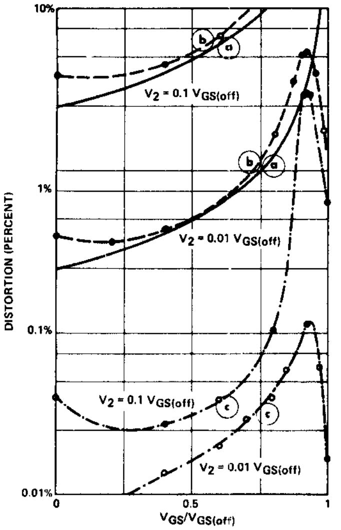
$$V_2 = \frac{V_1}{1 + g_{DS}R}\left(1 - \frac{Rg_{DS}V_1}{2V_P\,[1 + Rg_{DS}]^2} + \ldots\right) \qquad (8)$$

Only the second harmonic will be considered for the distortion since the third is much smaller. For small distortion ($d \ll 1$ and $Rg_{DSS} \gg 1$),

$$d = \frac{V_1\, Rg_{DSS}}{4\,|V_P|\,[1 + Rg_{DS}]^2} \qquad (9)$$

If V_2 is held constant,

$$d = \frac{V_2\, Rg_{DS}}{4\,|V_P|\,[1 + Rg_{DS}]} \approx \frac{V_2}{4\,|V_P - V_{GS}|} \qquad (10)$$



Distortion as a Function of $V_{GS}/V_{GS(off)}$ for Two Different $V_2/V_{GS(off)}$. (a) Theoretical for Figure 26(a). (b) Measured with Circuit of Figure 26(a). (c) Measured with Circuit of Figure 26(b)

Figure 27

Figure 27 shows a comparison of measured and calculated distortion. If V_{GS} approaches V_P, the above restrictions are violated; the expression for the distortion can no longer be applied. If $V_{DS} < 0$, $V_{GS} = 0$, then the FET works in region F; the distortion will be higher than predicted. From (10) we get for a prescribed maximum distortion a maximum amplitude as a function of V_{GS}:

$$V_{2max} = 4d_{max} |V_P - V_{GS}| \tag{11}$$

For a given d_{max} and V_{2max} the ratio of minimum to maximum attenuation is

$$\frac{A_{min}}{A_{max}} = m = \frac{1 + Rg_{DSS}}{1 + Rg_{DSS} \dfrac{V_{2max}}{4d_{max} |V_P|}} \approx \frac{4d_{max} |V_P|}{V_{2max}} \tag{12}$$

valid only for m > 1. Note that the maximum distortion is reached only for minimum attenuation. Examples:

$d_{max} = 10$ percent $V_{2max} = 0.001\ V_P$ $m = 400$

$d_{max} = 1$ percent $V_{2max} = 0.01\ V_P$ $m = 4$

Although these relations are only first-order approximations, they give a good estimate of FET attenuator characteristics. The maximum amplitude is proportional to V_P. FETs with high V_P are desirable for attenuator applications. Unfortunately, the majority of commercially available FETs are made with low V_P for use in amplifiers.

There are several means of reducing distortion. By connecting two identical FETs in antiparallel or antiseries, nonlinearities can be cancelled out to a certain extent. A better linearization is possible by using one FET with "feedback". It has been shown above that the characteristics would be symmetrical if V_{GD} were the control voltage in the third quadrant. By adding 0.5 V_{DS} to the control voltage, the two voltage V_{GS} and V_{GD} interchange when V_{DS} changes sign:

$$\begin{aligned} V_{GS} &= V_H + 0.5\ V_{DS} \\ V_{GD} &= V_H - 0.5\ V_{DS} \end{aligned} \tag{13}$$

then (13) used in (2) gives

$$I_D = \frac{2I_{DSS}}{V_P^2} V_{DS} (V_H - V_P) \tag{14}$$

The resulting characteristic is linear and symmetrical in B and E. The improvement in distortion performance can be seen in Figure 27. A distortion of 12 percent for $V_2 = 0.1\ V_P$ at $V_{GS} = 0.8\ V_P$ is reduced through linearization to 0.1 percent. Figure 26(b) shows a possible circuit. The frequency range of the controlled signal must be much higher than that of the controlling signal V_H to keep the direct interference of V_H on V_2 small. R_3 is set for minimum distortion. If V_2 and V_H are in the same frequency range, a high impedance amplifier must be used. V_2 is at the input; the output is connected to the FET gate. The amplification is approximately 0.5 (adjustable). The control voltage is introduced through a second input so that no direct interference with V_2 occurs.

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(6) W. Gosling, "Voltage Controlled Attenuators Using Field-Effect Transistors," IEEE Trans Audio, Vol. AU-13, pp. 112-120, Sept.-Oct., 1965.

(7) J.S. Sherwin, "Voltage Controlled Resistors (FET)," Solid State Design, pp. 12-14, Aug. 1965.

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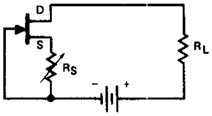
DESIGN IDEA

The FET Constant Current Source

INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant current source. An adjustable current source may be built with a FET, a variable resistor and a small battery, Figure 1. For good thermal stability, the FET should be biased near the zero T.C. point.[1]



Field-Effect Transistor Current Source
Figure 1

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant current source at any current below its saturation current I_{DSS}.

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)} \left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/k}\right] \qquad (1)$$

where k can vary from 1.7 to 2.0, depending upon device geometry. The series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \qquad (2)$$

A change in supply voltage, or change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss}.

$$\Delta I_D = \Delta V_{DS} g_{oss} \qquad (3)$$

The value of g_{oss} is an important consideration in the accuracy of a constant current source. As g_{oss} may range from less than 1 μmho to more than 50 μmho according to the FET type, the dynamic impedance can be greater than 1 megohm to less than 20K. This corresponds to a current stability range of 1 μA to 50 μA per volt. The value of g_{oss} depends also on the operating point, being highest at I_{DSS} and at low V_{DS}. Output conductance g_{oss} decreases approximately linearly with I_D, becoming less as the FET is biased toward cut-off. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \qquad (4)$$

where

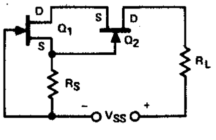
$$g_{oss} = g'_{oss} \qquad (5)$$

when

$$V_{GS} = 0 \qquad (6)$$

So as $V_{GS} \rightarrow V_{GS(off)}$, $g_{oss} \rightarrow$ zero. For best regulation, I_D must be considerably less than I_{DSS}.

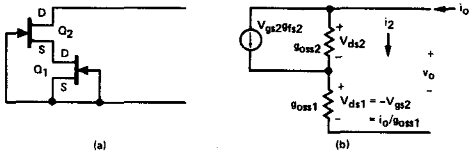
It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs as shown in Figure 2.



Cascade FET Current Source
Figure 2

Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The d-c value of I_D is controlled by R_S and Q_1. However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

Figure 2 is redrawn in Figure 3 for the condition $V_{GS1} = 0$.



(a) (b)

Figure 3

$$i_o = i_2 + v_{gs2}g_{fs2} = v_{ds2}g_{oss2} - i_o\frac{g_{fs2}}{g_{oss1}} \qquad (7)$$

$$i_o = \frac{v_{ds2}g_{oss2}g_{oss1}}{g_{oss1} + g_{fs2}} \qquad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \qquad (9)$$

$$v_o = v_{ds2}\,\frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \qquad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1}g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \qquad (11)$$

If $g_{oss1} = g_{oss2}$ (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs}/g_{oss}} \qquad (13)$$

When

$R_S \neq 0$ as in Figure 2 (14)

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S\,(g_{fs}^2 + g_{oss}g_{fs} + g_{oss}^2)} \qquad (15)$$

$$\approx \frac{g_{oss}^2}{g_{fs}\,(1 + R_Sg_{fs})} \qquad (16)$$

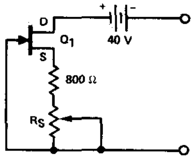
In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably less than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage V_{DG}. That is,

$$V_{DG} > V_{GS(off)},\ \text{preferably } V_{DG} > 2\,V_{GS(off)} \qquad (17)$$

If $V_{DG} < 2\,V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A 2N4340 has typical $g_{oss} = 4$ µmho at $V_{DS} = -20$ V and $V_{GS} = 0$. At $V_{DS} \approx -V_{GS(off)} = 2$ V, $g_{oss} \approx 100$ µmho.

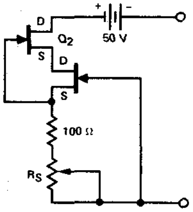
The best FETs for current sources are those having long gates and consequently very low g_{oss}. The Siliconix 2N4869 exhibits typical $g_{oss} = 1$ µmho at $V_{DS} = 20$ V. A single 2N4869 in the circuit of Figure 4 will yield a current source adjustable from 5 µA to 1 mA with internal impedance greater than 2 megohms.



$R_S = 1$MΩ, 2W

Adjustable Current Source
Figure 4

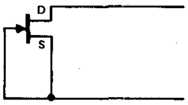
The cascade circuit of Figure 5 provides a current adjustable from 2 µA to 1 mA with internal resistance greater than 10 megohms.



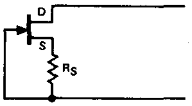
$Q_1 = 2N4340$
$Q_2 = 2N4341$
$R_S = 1$MΩ, 2W

Cascade FET Current Source
Figure 5

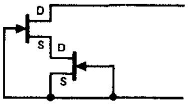
For each circuit discussed, g_{oss} is represented by the following equations:



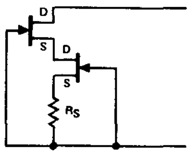
$g_o = g_{oss}$



$$g_o \approx \frac{g_{oss}}{1 + R_Sg_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}\,(1 + R_Sg_{fs})}$$

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Siliconix

DESIGN IDEA

Wideband UHF Amplifier with High-Performance FETs

Ed Oxner

INTRODUCTION

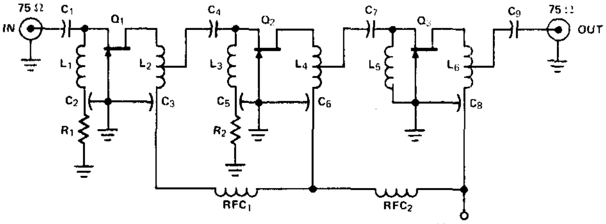
A new freedom in UHF amplifier design is possible with high-performance "Super FETs" such as the Siliconix U310 Junction FET. Typical advantages include a closely-matched 75 ohm input for extremely low return loss in cable systems, and high spurious response rejection with the 3rd order IM intercept measured at +29 dB.(1)

Additionally, the high common-gate forward transconductance of the U310 (20,000 μmho maximum) makes it possible to design an amplifier with wide bandwidth and good gain, since the figure of merit (g_m/C) of the FET is 2.35 x 10^9 typical – higher than any other known UHF Junction FET.

The amplifier circuit in Figure 1 is designed for 225 MHz center frequency, 1 dB bandwidth of 50 MHz, low input VSWR in a 75-ohm system, and 24 dB gain. Three stages of U310 FETs are used, in a straight forward design.

Typical parameters are taken from the U310 data sheet:

Forward Transconductance		14 mmhos
Input Admittance at 225 MHz	g_{igs}	13 mmhos
	b_{igs}	4 mmhos
Output Admittance at 225 MHz	g_{ogs}	0.27 mmhos
	b_{ogs}	2.6 mmhos



C_1, C_4, C_7, C_9 = 68 pF
C_2, C_5 = 500 pF
C_3, C_6, C_8 = 1000 pF
Q_1, Q_2, Q_3 = Siliconix U310
L_1, L_3, L_5 = 120 nHy
L_2, L_4, L_6 = 222 nHy
RFC_1, RFC_2 = 2.2 nHy
R_1, R_2 = 51 Ω

Figure 1

Input match is simplified because the FET input (real) impedance is nearly 77 ohms. A coupling capacitor is used in the amplifier, rather than a tuned circuit, and thus the values may be determined:

$$R_s\sqrt{\frac{R_{ig}}{R_s}-1} = X_s = 75\sqrt{\frac{77}{75}-1} = 11.85\ \Omega$$

$$C_s = \frac{1}{\omega X_s} \approx 68\ \text{pF}$$

$$X_P = \frac{R_sR_p}{X_s} = \frac{75 \times 77}{11.85} = 488\ \Omega$$

$$C_P = 1.47\ \text{pF}$$

$$C_T = 4.4\ \text{pF}\ (C_T = C_P + C_{igs})$$

$$L_s = \frac{1}{\omega^2 C_T} = 120\ \text{nHy}$$

Figure 2 shows that the measured input VSWR in the 75-ohm system indicated an available bandwidth considerably greater than that required for the amplifier design criteria.

Three cascaded synchronous single-tuned stages are used to achieve the desired gain, and thus stage bandwidth and Q are determined:(2)

$$\frac{B/W}{f} = \frac{1}{Q}\sqrt{\left(\frac{E_o}{E}\right)^2 - 1}$$

where:

$$\frac{\text{Bandwidth of 3 Stages}^{(3)}}{\text{Bandwidth of 1 Stage}} = \sqrt{2^{1/3} - 1}$$

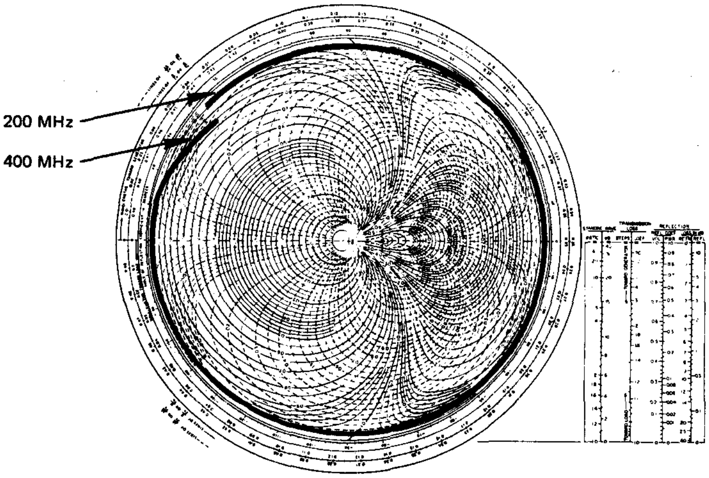
and

$$\left(\frac{E_o}{E}\right) = 1.122\ (1\ \text{dB})$$

giving

$$B/W\ (1\ \text{dB}) = 98\ \text{MHz}$$

$$Q = 1.15$$



Blanchard Chart (Inverted Circle Impedance Chart)
Figure 2

With a FET output impedance of 3700 ohms shunted by approximately 2.5 pF (with 0.5 pF allowed for stray capacitance), the total parallel resistance necessary to obtain the desired bandwidth is:

$$Q = \omega C R_t$$

$$R_t = \frac{1.15}{1.415 \times 10^9 \times 2.5 \times 10^{-12}} = 330\,\Omega$$

The tank circuit impedance appearing in shunt with the FET, is therefore calculated to be about 365 ohms. From this, the inductance is:

$$L = \frac{R}{\omega Q} = \frac{365}{\omega 1.15} = 222 \text{ nHy}$$

with a turns ratio of 2.3:1 to match to 75 ohms. Since each stage is designed for 75 ohm input and output, three cascaded stages complete the amplifier design.

The computed voltage gain per stage is approximately $g_{fs} R_{t/n}$ or 2.22 (7 dB). Measured gain for all three stages is 24 dB. The U310 FET in the final stage operates at I_{DSS}, and thus accounts for the higher measured gain. The gain/bandwidth response of the amplifier is shown in Figure 3.

The 3rd order spurious intercept point is plotted graphically in Figure 4.(4) The importance of a high intercept point becomes apparent in a crowded high-level area of the spectrum where signal purity is of utmost priority.

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(1) "Don't Guess the Spurious Level," ELECTRONIC DESIGN, February 1, 1967, pp. 70-73.

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(3) Valley and Wallman, VACUUM TUBE AMPLIFIERS, MIT Rad. Lab. Series, Vol. 18, pp. 172-173.

(4) Op. cit., "Don't Guess the Spurious Level."

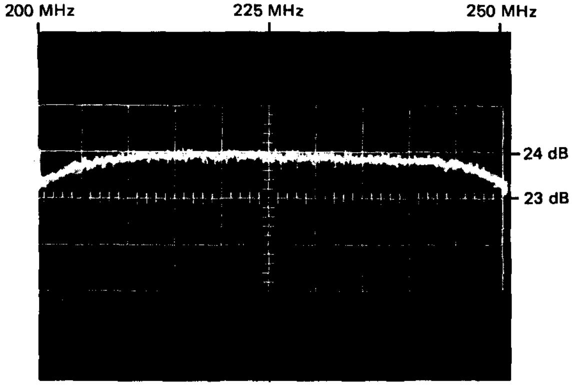


Figure 3

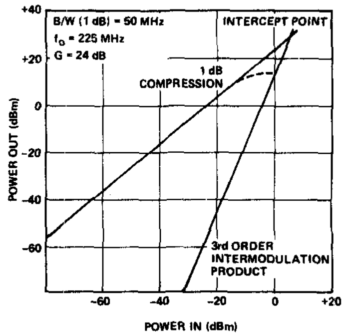


Figure 4

DESIGN IDEA

High-Performance FETs In Low-Noise VHF Oscillators

Ed Oxner

Most communications receivers are limited in their dynamic range because of saturation in the early stages of RF amplifiers or mixers. However, some receiver designs are available which overcome this limitation by using parametric amplifiers and converters to achieve spectacular increases in dynamic range. There still remain certain limitations in dynamic range which cannot be remedied by parametric devices. In these cases, the problem lies in the heterodyning of noise sidebands which appear on the receiver local oscillator, entering the passband through strong interfering signals.

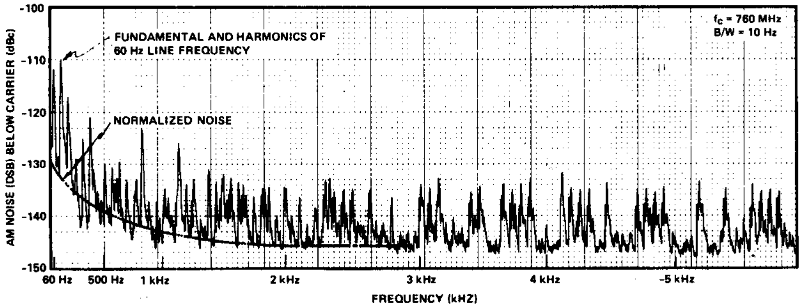
Common Types of Noise

Although noise is often difficult to characterize because of its random or nondeterministic nature, it is possible to differentiate various forms of noise through an understanding of the Gaussian distribution of noise about an RF carrier. Briefly stated, the three major forms of noise are (1) low-frequency noise ($1/f$); (2) thermal noise ($4kTRB$); and "shot" noise (i_n). Further, these types of noise can be identified from their relationship to the main RF carrier. For example, low-frequency noise predominates very close to the carrier, and falls to insignificant levels when it is displaced more than 250 Hz from the carrier. Low-frequency noise is associated with surface contamination and other irregularities, such as gate current leakage.

Thermal noise plays the predominant role in the region from the $1/f$ decay point to approximately 20 kHz from the carrier, and is commonly associated with equivalent resistance where the rms value of noise voltage of the Thevenin generator becomes the classic $(4kTBR)^{1/2}$. Noise appearing beyond the 20 kHz is known as Shot noise, and is directly attributable to noise current. Because of the typically uniform distribution of shot noise it is also referred to as "white noise."

Origins of Oscillator AM Noise

Although an oscillator tends to produce a wave that is nearly sinusoidal, there are other fluctuations present. When the energy in the frequency domain close to the carrier is observed on a spectrum analyzer, noise appears as a modulation phenomenon. This observation would be greatly enhanced if the noise contribution was coherent and consisted of discrete sideband frequencies. Without a doubt, the major component of AM noise is the contribution of low-frequency noise ($1/f$). Both thermal and shot noise are relatively insignificant segments of AM noise when compared to $1/f$. A graph of AM noise vs frequency removed is shown in Figure 1.

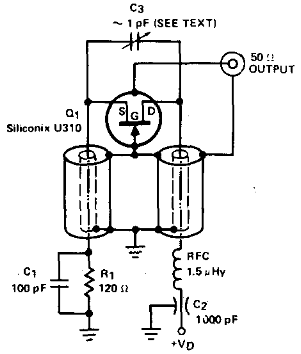


AM Noise vs Frequency Removed from the Carrier
Figure 1

Design of a VHF Oscillator

The important design considerations for best oscillator performance include using a FET with high forward transconductance, maintaining the gate at ground potential, and keeping a high unloaded tank Q. The high transconductance is necessary to reduce the effective noise resistance. The grounded gate reduces the noise voltage contributions to those of the gate leakage current and the series gate resistance. The high tank circuit Q serves as an effective filter for the sideband noise energy.

The oscillator design is somewhat extraordinary for a circuit employing a FET. The FET chosen was the Siliconix U310, which has a forward transconductance value higher than 18 mmho at zero bias ($V_{GS} = 0$). The oscillator basically consists of two coaxial resonators, one for the FET source and the other for the drain. Oscillation is established by capacity coupling between the two resonators; output coupling is derived from the magnetic coupling which exists at the open ends of the resonators. Optimum resonator Q is achieved by designing the coaxial resonators for a characteristic impedance of 75 ohms. The oscillator circuit is shown in Figure 2, and construction details are shown in Figure 3.



Oscillator Circuit
Figure 2

Oscillator Construction Details
Figure 3

The technique to establish the proper resonator length for the desired frequency is somewhat tricky, and requires a first-order approximation of the anticipated capacitive fringing which derives from both the FET and the feedback network. A short circuited coaxial transmission line is theoretically resonant at a quarter-wave length of the resonating frequency, except for the effects of fringe field capacitance. At resonance

$$X_L = X_C \tag{1}$$

If the fringe capacitance is known, X_C can be calculated as

$$X_C = \frac{1}{\omega C} \tag{2}$$

From this, the resonator length can be determined as

$$X_C = \tan \beta \ell \tag{3}$$

In making these calculations, a Smith chart is invaluable, as is shown in the following illustration:

Frequency of oscillation = 760 MHz
FET b_{igs} (from data sheet) = 16 mmho
Capacitance from b_{igs} C_{gs} = 3.4 pF
Allow for stray capacitance and
 the feedback network $\underline{C_s = 1.5 \text{ pF}}$
4.9 pF

Thus X_C = j 0.57 (normalized to 75 Ω)

Locate 0.57 on the Smith chart. The wavelength toward the load = 0.081 λ. Since a wavelength at 760 MHz is 39.5 cm., then the resonator cavity length is simply

$$39.5 \times 0.081 = 3.20 \text{ cm } (1.26 \text{ inches}) \tag{4}$$

In the completed FET coaxial oscillator circuit, the output coupling loop consists of a single turn made fast to the cavity by the BNC flange and the FET itself. Although the feedback network appears somewhat crude, it can be replaced by a small trimmer capacitor for similar operation.

Conclusions

Measured performance of the oscillator is shown in Table IA; AM noise measurements in a 10 Hz bandwidth are shown in Table IB.

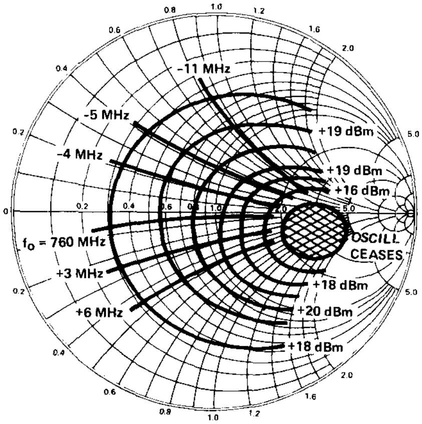
TABLE IA
Oscillator Measured Performance @ 25°C

V_{DD}(V)	+10	+15	+20	+25
I_D (mA)	15	16.2	18.2	21
P_{out} (dBm)	+6.6	+15.2	+18.3	+20
Frequency (MHz)	725	742.7	754.7	762.9

TABLE IB
AM Noise Measurement

Frequency Displaced From Carrier	dBc
50 Hz	-130
500 Hz	-139
1 kHz	-143.5
5 kHz	-146

The Reike diagram shown in Figure 4 makes possible the accurate prediction of expected power output and operating frequency with the oscillator feeding directly into a mismatched load. Expansion of the Reike diagram to show frequency vs transmission line length (in degrees) will allow prediction of the long-line effect on oscillator stability.



Reike Diagram
Figure 4

Siliconix

TECHNICAL ARTICLE

FET Biasing

James Sherwin

INTRODUCTION

Engineers often design FET amplifiers that are unnecessarily sensitive to device characteristics because they may not be familiar with proper biasing methods.

One way to obtain consistent circuit performance in spite of wide device variations is to use a combination of constant-voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme, particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the V_{GS} = −0.4 V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage, V_{DD}, of 30 V and a drain resistance, R_D, of 39K Ω are being used.

The quiescent drain-to-source voltage, V_{DSQ}, is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of ±0.2 V will produce output voltage swings of ±7.0 V – a voltage gain of 35.

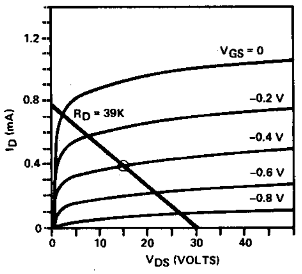


Figure 1. A large dynamic range is provided by the operating point at V_{DSQ} = 15 V, I_{DQ} = 0.39 mA and V_{GSQ} = −0.4 V. The output characteristics are for a typical 2N4339.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for V_{GG} = constant on the transfer characteristic of the FET.

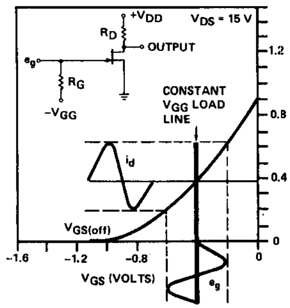


Figure 2. Constant-voltage bias is maintained by the V_{GG} supply as shown on this typical 2N4339 transfer curve. Input signal e_g moves the load line horizontally.

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The transfer characteristic is a plot of I_D vs V_{GS} for constant V_{DS}. Since the curve doesn't change much with changes in V_{DS}, *it is quite useful in establishing operating bias points.* In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

The heavy vertical line at $V_{GS} = -0.4$ V establishes the Q-point of Figure 1. No voltage is dropped across resistor R_G because the gate current is essentially zero. R_G serves mainly to isolate the input signal from the V_{GG} supply.

Excursions of the input signal, e_g, combine in series with V_{GS} so that they add algebraically to the fixed value of -0.4 V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. For an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no resultant gate-source voltage excursion. This bias technique is therefore limited to source followers, source-coupled *differential amplifiers, and to ac amplifiers where* the source terminal is bypassed to ground at the signal frequency.

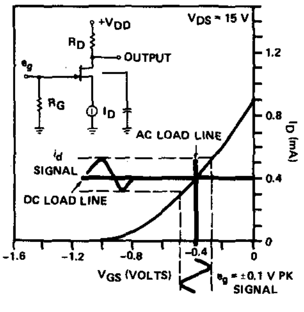

Figure 3. Constant-current bias fixes the output voltage for any R_D. Hence, input signals cannot affect the output unless the current source is bypassed.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to $-(1/X_C) = -\omega C$ (Figure 4).

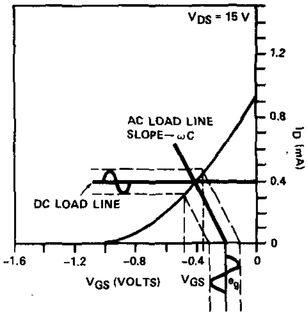

Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from e_g.

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal, e_g, is reduced by the drop across the capacitor:

$$v_{gs} = e_g - v_S = e_g - i_S X_C \tag{1}$$

It is clear from Figure 4 that the input signal only shifts the operating point by an amount equal to V_{gs}, the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

Self Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor, R_S, to the gate. Since no voltage is dropped across R_S when $I_D = 0$, the self-bias load line passes through the origin. Its slope is given by $-1/R_S$. Therefore, the desired Q-point is established by setting $-1/R_S = I_{DQ}/V_{GSQ}$.

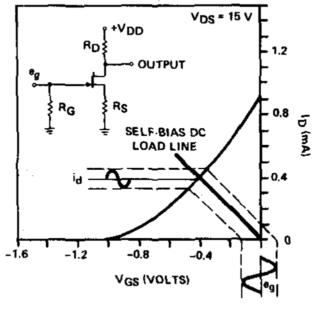

Figure 5. The self-bias load line passes through the origin with a slope $-1/R_S$. Bypassing R_S will steepen the slope and increase the gain of the circuit.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equa*tion 1 with X_C replaced by R_S. The ac gain of the circuit* can be increased by shunting R_S with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope $-(1/Z_S) = -(\omega C + 1/R_S)$.

The circuit is biased automatically at the desired Q-point, requires no extra power supply and provides a degree of current stabilization not possible with constant-voltage biasing.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing V_{GG}. (The bias line intercepts the V_{GS} axis at V_{GG}.) The larger V_{GG} is made, the larger R_S will be and the better will be the approximation to constant-current biasing.

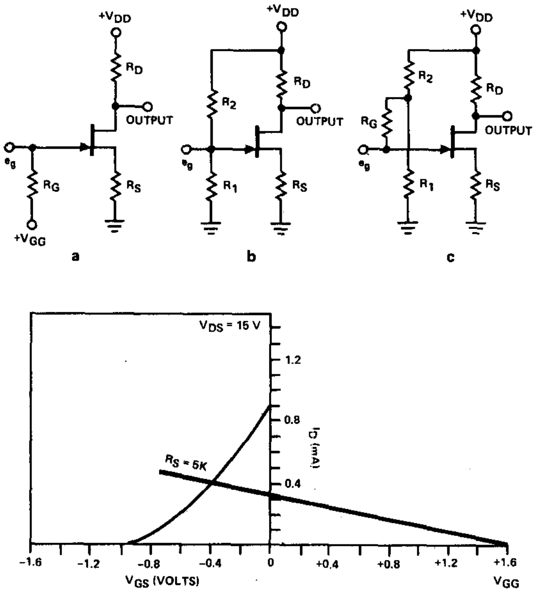

Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

All three circuits in Figure 6 are equivalent. Circuit 6(a) requires an extra power supply. The need for an additional supply is avoided in 6(b) by deriving V_{GG} from the drain supply. R_1 and R_2 are simply a voltage divider. To maintain the high input impedance of the FET, R_1 and R_2 must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired V_{GG} in every circuit application. Circuit 6(c) overcomes this problem by placing a large R_G between the center point of the divider and the gate. This allows R_1 and R_2 to be small, without lowering the input impedance.

One point of caution worth remembering is that as V_{GG} is increased, V_S increases, and V_{DS} decreases. Therefore with low V_{DD}, there may be a significant decrease in the allowable output voltage swing.

Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7

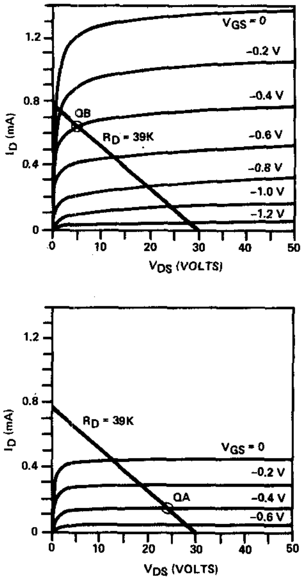

Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

where two limiting sets of output characteristics, representing the actual min-max spread of the Siliconix 2N4339, are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8. (See next page.)

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance – for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating I_{DQ} for the extreme limit devices. At $V_{GS} = -0.4$ V, the range of I_{DQ} is 0.13 to 0.69 mA, and V_{DSQ} for a given R_D will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with $R_D = 39K\ \Omega$ and $V_{DD} = 30$ V, V_{DSQ} varies from near saturation (5 V) to 25 V.

An apparently excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets V_{DSQ} to $V_{DD} - I_{DQ}R_L$ for any device in the production spread. V_{GS} automatically finds a value to set the appropriate I_{DQ} = constant for all devices. For the constant-current bias plot of Figure 8, with $I_{DQ} = 0.39$ mA, V_{GS} would range from –0.11 to –0.67 V.

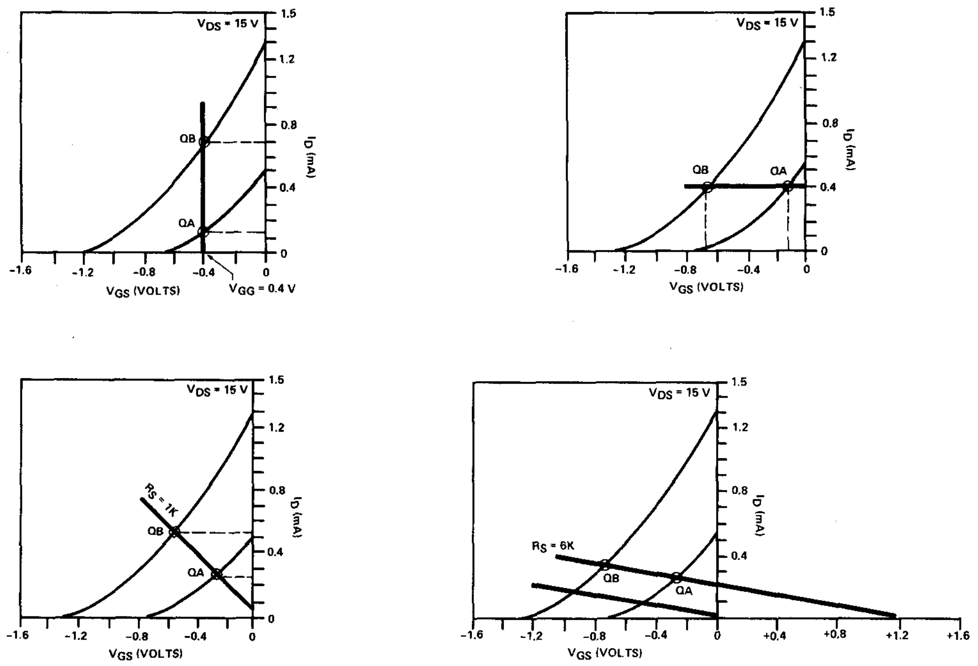

Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Output characteristics are not needed as long as I_{DQ} is chosen to be below the minimum I_{DSS}. With R_D = 39K Ω and V_{DD} = 30 V, V_{DSQ} is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance, g_{fs}, of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high R_S.

An appropriate choice of I_{DQ} limits can be made by using the pair of limiting transfer curves. For example, for R_S = 1K Ω, the load line shown on the self-bias curve of Figure 8 is established. The maximum I_D is 0.52 mA, and the minimum I_D is 0.24 mA. The operating range of V_{DSQ} may be calculated for any value of V_{DD} and R_D. Clearly, for R_D = 39K Ω, the maximum-limit device (device B) would operate with V_{DSQ} = 9.8 V and the minimum-limit device (device A) would operate with V_{DSQ} = 20.6 V. This results in fairly satisfactory operation for all devices. However, such a variation in I_{DQ} imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with V_{GG} = 1.2 V. The range of I_{DQ} for this bias condition is 0.25 mA to 0.32 mA. A similar minimum difference in I_{DQ} could be achieved with R_S = 6K Ω and V_{GG} = 0, (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows v_{gs} = ±1.8 V (limited by I_{DSSA}), while the lower line allows a v_{gs} of only ±0.7 V (limited by $V_{GS(off)A}$). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with R_D = 62K Ω, the V_{DSQ} would range only between 10 and 15 V.

For this circuit, R_D should be chosen to allow the largest output signal swing for I_{DQ} midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across R_D at one-half of (V_{DD} − $2V_{GS(off)typ}$) or 14 V, yields R_D = (14 V/0.285 mA) = 49K Ω.

It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.

Minimize the Gain Variations

Leaving R_S unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).

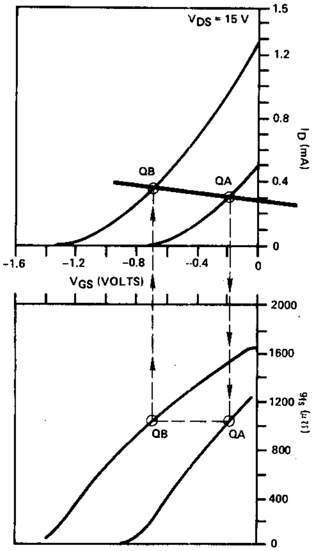

Figure 9. Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal g_{fs} (bottom).

As Figure 9 shows, it is possible to find an R_S and a V_{GG} that will set I_{DQA} and I_{DQB} to values so that g_{fsQ} will be the same for both devices. The g_{fsQ} of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

The design procedure is as follows:

Step 1. Select a desired I_{DQA} below I_{DSSA}. A good value, allowing for temperature variations, is 60% of I_{DSSA}. This will allow for decreasing I_{DSS} due to temperature variation and for reasonable signal excursions in load current.

Step 2. Enter the transfer curves at $I_{DQA} \cong 0.6\ I_{DSSA}$ (0.3 mA) to find V_{GSQA}. This $V_{GSQA} \cong 0.2$ V for the 2N4339.

Step 3. Drop vertically at V_{GSQA} to the minimum limit transconductance curve to find g_{fsQA}. The value as read from the plot is approximately 1000 µmho.

Step 4. Travel across the g_{fs} plot to the maximum curve to find V_{GSQB} at the same value of g_{fs}. This is $V_{GSQB} \cong -0.7$ V.

Step 5. Travel vertically up to the maximum limit transfer curve to find I_{DQB} at V_{GSQB}. This is $I_{DQB} \cong 0.36$ mA.

Step 6. Construct an R_S bias line through points Q_A and Q_B on the transfer curves. The slope of the line is $1/R_S$, and the intercept with the V_{GS} axis is the required V_{GG}.

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can then be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB})/(I_{DQB} - I_{DQA}) \qquad (2)$$

and the bias voltage is

$$V_{GG} = R_S\, I_{DQB} + V_{GSQB} \qquad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. (For n-channel FETs, V_{GS} is negative and I_D is positive. For p-channel units, the signs are reversed.)

If the transconductance curves of Figure 9 are not available, g_{fs} can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the I_D and V_{GS} axes. The slope and g_{fs} are given by:

$$\text{slope} = g_{fs} = I_{D(\text{intercept})}/-V_{GS(\text{intercept})} \qquad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point Q_A and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is Q_B.

Designing Without Output Curves

Although the transfer characteristic has been seen to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish V_{DSQ}. However, if a set of output curves is not available, V_{DSQ} can be determined or selected from the transfer curve by using the following procedure:

Step 1. Establish R_S and limiting values of I_{DQ}, V_{GSQ} and g_{fsQ} from the transfer curve.

Step 2. Establish V_{DD} as available, but in no case greater than BV_{GSS} nor less than several times $V_{GS(off)}$. There are special cases where V_{DD} will be below this limit, but in no case should instantaneous v_{dg} be allowed to fall below 2^{*} x $V_{GS(off)}$ if minimum distortion is to be achieved.

Step 3. Set V_{DSQ} approximately midway between V_{DD} and 2 x $V_{GS(off)}$; lower if large output signals will not be handled.

Step 4. Select R_D to give the appropriate V_{DSQ}. The formula is:

$$R_D = [(V_{DD} - V_{DSQ})/0.5\ I_{DQA} + I_{DQB}] - R_S \qquad (5)$$

In the example of Figure 8, this procedure would have yielded $V_{DSQ} = (30\text{-}3)/2 = 13.5$ V and $R_D = (30 - 13.5)/0.5\ (0.52 + 0.24)$ mA - 1K Ω = 42.5K Ω.

Step 5. Check to ensure that with this R_D, device B is not in a saturated condition – $V_{DQB} = V_{DD} - I_{DBQ} R_D > 2V_{GS(off)} + R_S I_{DBQ}$.

Decrease R_D if this condition is not met.

An alternate method, that selects R_D to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

Step 3. Determine required stage gain, A_v, and set $R_D = A_v/g_{fsQ}$.

Step 4. Calculate V_{DSQ} to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S)\,I_{DQ} \qquad (6)$$

Step 5. If necessary, change I_{DQ}, V_{DD}, A_v and/or R_D to obtain an optimum compromise. ■■

FET SOURCE-FOLLOWER CIRCUITS

Too little knowledge of biasing methods for FET amplifiers sometimes keeps engineers from making maximum use of FETs in circuit designs. The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors. By considering 10 circuits, which represent virutally every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10(a) through 10(e) have no gate feedback; their input impedances, therefore, are equal to R_G. Circuits 10(f) through 10(k) employ feedback to their gates to increase the input impedance above R_G.

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, d and f can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.
- Circuits d, e and k employ FETs as current sources. In circuit d, Q_2 must have a lower cut-off voltage, $V_{GS(off)}$, and a lower zero gate-voltage drain current, I_{DSS}, than Q_1.
- Circuits e, g, h and k employ a source resistor, R_S, which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

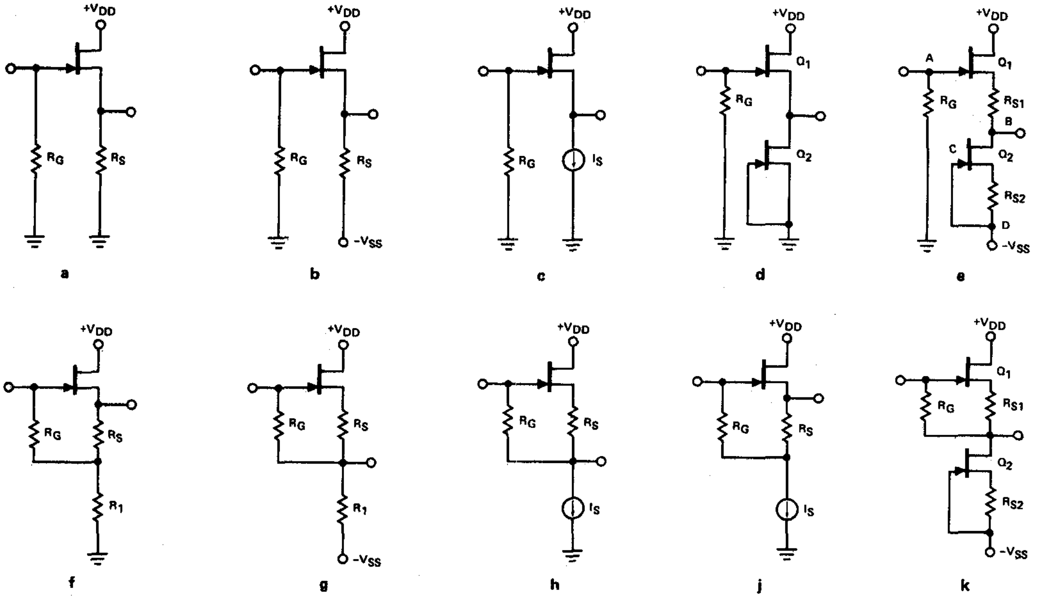

Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

Biasing Without Feedback is Simple

The no-feedback circuits of Figure 10 (circuits 10(a) through 10(e) use simple biasing techniques (see the earlier article). Circuit 10(a) is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G. Since no gate-to-source voltage, V_{GS}, can be developed when $I_D = 0$, the self-bias load line passes through the origin (Figure 11). For the 2N4339 FET, whose limiting transfer characteristics are used throughout this article, the quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1K Ω source resistor is used. The quiescent output voltage lies between +0.25 and +0.55 V.

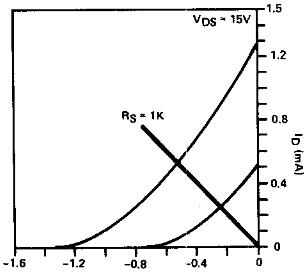

Figure 11. Self biasing (Figure 10a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

Circuit 10(b) is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 10(a) is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Figure 12, one for $V_{SS} = -15$ V and the other $V_{SS} = -1.6$ V. For the first case, the quiescent output voltage lies between +0.18 and +0.74 V. For the second, it lies between +0.3 and +0.82 V.

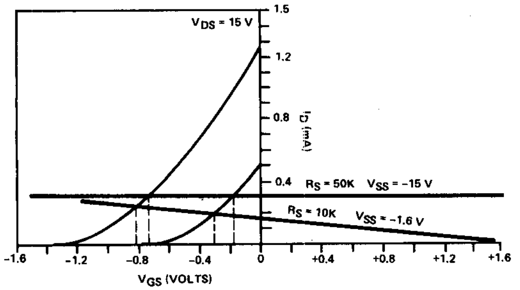

Figure 12. Adding a V_{SS} supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the V_{GS}-axis is at $V_{GS} = -V_{SS}$. Bias lines are shown for $V_{SS} = -15$ V and $V_{SS} = -1.6$ V.

The bias load line for circuit 10(c) is just a horizontal line (I_D = constant). The quiescent output voltage is between +0.15 and 0.7 V for $I_D = 0.3$ mA.

Circuit 10(d) is similar to 10(c) except that the $V_{GS} = 0$ output characteristic of FET Q_2 is used as a current source. As seen in Figure 13, Q_2 does not supply constant current when its V_{DS} gets very small. This technique should therefore be used only to bias FETs whose $V_{GS(off)}$ is significantly higher than the equivalent $V_{GS(off)}$ of the current-source FET diode.

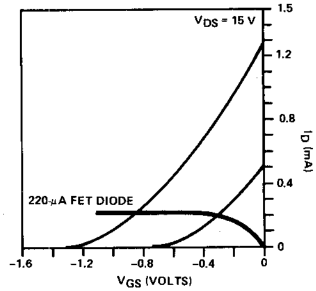

Figure 13. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Figure 10d). Therefore, Q_1 should have a significantly larger $V_{GS(off)}$ than Q_2 does.

A pair of matched FETs is used in the circuit of Figure 10(e), one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2}, as indicated by the load line of Figure 14. The drain current may be anywhere from 0.20 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

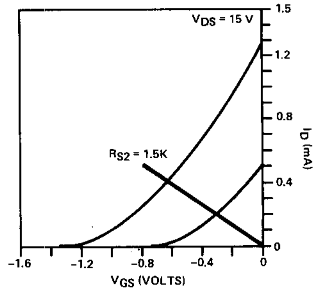

Figure 14. This load line is set by R_{S2} and Q_2 which acts as a current source (Figure 10e). If its components are properly matched, the circuit will have zero or near-zero offset.

Since $I_{D1} = I_{D2}$ and $V_{GS1} = V_{GS2}$, choosing $R_{S1} = R_{S2}$ will ensure that the voltage from point A to B equals the voltage point from point C to D (Figure 10(e)). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D, the source follower will exhibit zero or near-zero temperature drift.

Biasing With Feedback Increases Z_{in}

Each of the feedback-type source followers (Figure 10(f) through 10(k)) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G. If R_S is chosen so that R_G is returned to zero dc volts (except in circuit 10(f), then the input/output offset is zero. R_1 is usually much larger than R_S.

Circuit 10(f) is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Figure 15). The output load line, however is determined by the sum of $R_S + R_1$. The feedback voltage V_{FB}, measured at the junction of R_S and R_1, is determined by the intercept of the $R_S + R_1$ load line with the V_{GS} axis. The quiescent output voltage is $V_{FB} - V_{GS}$.

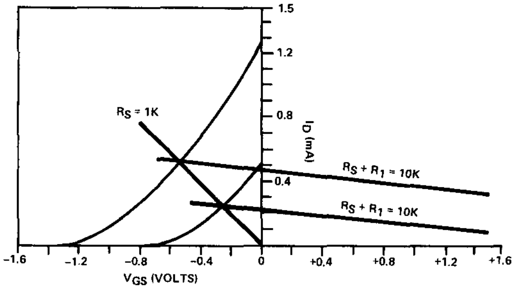

Figure 15. The bias load line is set by R_S but the output load line is determined by $R_S + R_1$ when gate feedback is employed (Figure 10f). The feedback V_{fb} is determined by the intercept of the $R_S + R_1$ load line and the V_{GS} axis.

In the circuit of Figure 10(g), R_S can be trimmed to provide zero offset. As the curves show (Figure 16), R_S will be between 670 ohms and 2.5K Ω. R_S is much less than R_1. The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

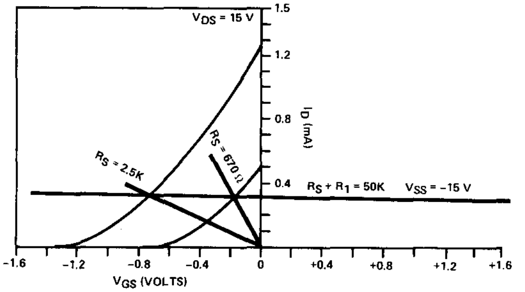

Figure 16. R_S can be trimmed to provide zero offset at some point between 670 ohms and 2.5K Ω (Figure 10g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of −1/50K, because the current source is not perfect; it has a finite impedance.

Circuit 10(h) is almost the same as 10(g); the difference is that resistor R_1 is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of circuit 1(h) differs from that of Figure 10(g) (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of −1/50k.

Circuit 10(j) is similar to 10(h) except that the output is taken from the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work at all properly.

In Figure 17, the constant-current load line represents a 0.3-mA current source, and the effect of a 1K Ω source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For R_S = 1K Ω, V_{FB} will be between −0.1 V and +0.45 V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

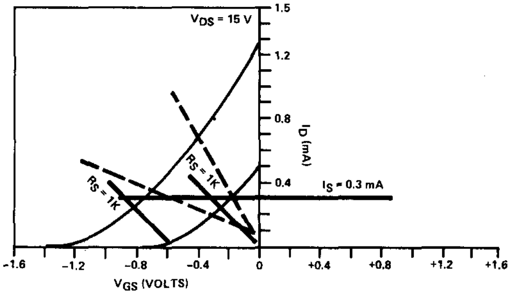

Figure 17. If R_S is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

This can be done by trimming R_S, as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10(h).

Biasing for circuit 10(k) is identical to that for circuit 10(e) (Figure 14) except that feedback is added to raise the input impedance.■■

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(1) Sherwin, J.S., "How, Why and Where to Use FETs," *Electronic Design,* May 17, 1966, p. 94.

(2) Sherwin, J.S., "Knowing the Cause Helps to Cure Distortion in FET Amplifiers," *Electronics,* Dec. 12, 1966, pp. 99-105.

Siliconix

APPLICATION NOTE

Don't Trade Off Analog Switch Specs. VMOS–A Solution to High Speed, High Current, Low Resistance Analog Switches

Walt Heinzer

INTRODUCTION

For analog switches, Vertical MOS (VMOS) transistors give you a nearly ideal combination of characteristics–without the tradeoffs required by the more conventional components. These devices are now available from two American suppliers: Siliconix and its licensee, Semtech.

Unlike the commonly used N-channel JFETs, VMOS chips that handle more than a few hundred milliamps are also small enough for economical production. Smaller chips lead to lower inherent capacitances. Moreover, the basic VMOS structure provides lower ON resistance.

Some analog switches use relays, bipolar transistors and even triacs. Although electromechanical relays offer the lowest ON resistance initially, their ON resistance will vary with current and degrade with use. Also, relays suffer from mechanical limitations.

Bipolar transistors require base-drive current that causes offset in the switched analog signal. Triacs are only suitable for switching raw power; for analog switching, they introduce too much offset and non-linearity although they easily handle high power.

VMOS Offers High Performance

VMOS devices aren't limited by any of these disadvantages. They can switch 10 W, linearly, over a wide dynamic range. In addition, VMOS input impedance is very high, and only input voltage (no current) turns the transistors OFF or ON. And since the drain-to-source channel is purely resistive while ON, you get low distortion.

VMOS transistors in analog switches offer several more advantages, including

- 1.8 Ω ON resistance, which results in low insertion loss in low-impedance systems
- 2.0 A DC current capability–paralleling three VMOS devices increases this capability to 6.0 A and unlike other devices, paralleled VMOS do not require power-wasting ballast resistors
- 3 A peak current, which makes VMOS super for driving capacitive lines and quickly charging and discharging capacitors in high speed A/D converters, sample and hold circuits, and integrators
- 60 dB isolation at 10 MHz and 500 nA DC leakage in the OFF state
- Enhancement-mode operation with a 0.8 to 2.0 V threshold, which gives VMOS direct compatibility with CMOS and TTL. And the logic gates aren't loaded by the VMOS.
- Linear ON resistance, which results in low total harmonic and intermodulation distortion

What's more, all these capabilities come in a TO-202AA package.

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Examine the output characteristics of a low resistance VMOS device like the Siliconix VN46AF. A look at the transfer characteristic in Figure 1A reveals that varying the gate-to-source voltage from 0 to +10 V switches the VN46AF from OFF to ON–with a 3 Ω ON resistance. From the curve you can see that the device turns OFF well before zero volts, which eases interfacing with logic.

In the VN46AF schematic in Figure 1B, note that the body and source are internally connected. Figure 1C and 1D, respectively, show simplified models of the VN46AF's OFF and ON states. Diode D_1 is the body-to-drain PN junction. When the VN46AF is OFF, its drain current vs drain-to-source voltage characteristics (Figure 1E) is essentially the curve for D_1.

The breakdown for D_1 is 40 V, and the diode exhibits forward conduction for drain-to-source potential as low as −0.6 V. This diode therefore constrains the analog voltage, which a simple switch (one VMOS transistor) can handle, to between −0.6 and +40 V.

When the VN46AF is ON, a 2 Ω resistance is in parallel with D_1. Maximum continuous current in either direction is 2.0 A, even though the diode is forward-biased for currents over 0.5 A.

One VMOS Device Makes an Analog Gate

VMOS characteristics are put to good use in the analog switch of Figure 1F. In the ON state, the gate of the VN46AF is positive with respect to the source. In the OFF state, the gate-to-source voltage is zero. The 2.0 A capability and the 3 Ω ON resistance of the VMOS transistor can be fully exploited in this circuit. The input signal, however, is restricted to positive voltages and must always be greater than the output voltage. Otherwise, OFF isolation is impaired.

Both ON and OFF switching takes 200 ns; charge feed-through during the ON-to-OFF transition is 80 pC with a 50 Ω load. Charge transfer is, of course, especially important in sample and hold systems. For example, 80 pC into 0.01 μF causes an offset of 8 mV.

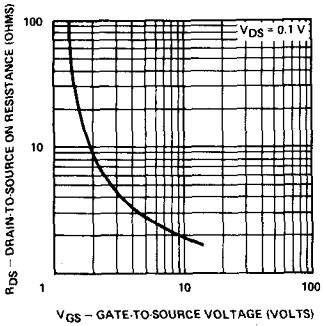
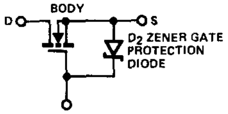
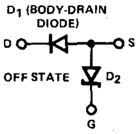


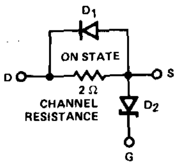
Figure 1A



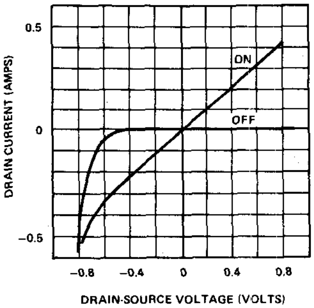
Schematic Symbol of VN46AF
Figure 1B



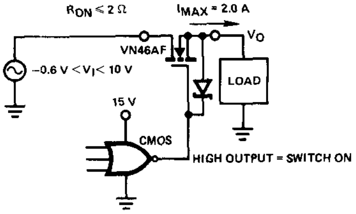
Equivalent OFF Condition (V_{GS} = 0)
Figure 1C



Equivalent ON Condition
(V_{GS} = 10 V)
Figure 1D



Small Signal Characteristics of VN46AF
Figure 1E



A Simple Unidirectional VMOS Analog Switch ($v_i \geq v_o$)
Figure 1F

The VN46AF switches from OFF to ON with a 3 Ω drain-to-source resistance, when its gate-to-source potential swings from 0 to +10 V. The device turns OFF at about 1 V(A). Some VMOS transistors (B) carry an on-board zener diode that protects the gate-to-source junction. A VMOS transistor is equivalent to two diodes in the OFF state (C), when the gate-to-source voltage is less than the threshold value. The equivalent diode, D_1 is shunted by 3 Ω when the VMOS device is ON (D), with the gate-to-source potential at +10 V. The small signal drain-to-source voltage vs current characteristic (E) is essentially determined by the body-to-drain diode. The input is restricted to positive voltages in the single-VMOS analog gate (F).

Figure 1

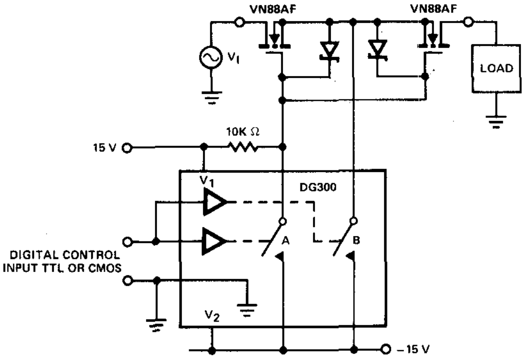
In Series, They Switch Both Polarities

To increase the switch's dynamic range, connect two VN88AF's in series (Figure 2A). In the ON state, both halves of the DG300 analog switch are open, so the gates of both VN88AF's are pulled to +15 V through the 10K Ω resistor. The ON resistance of this analog switch is twice as high as the drain-to-source resistance of a single VN88AF. The maximum current that this two-transistor switch can handle is the same as that for a single-transistor switch (2.0 A).

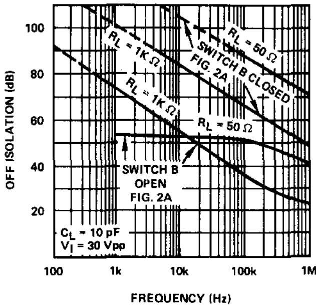
The switch is turned OFF by shorting the gates to the negative supply, thereby reducing the gate-to-source voltage to less than the threshold of 0.8 V. The second section of the DG300 adds 30 dB OFF isolation by shunting the signal-leakage path (through both sources) to the negative supply. OFF-isolation curves (Figure 2B) show that the DG300 raises the circuit's isolation and that decreasing the load resistance increases isolation.

Since the two transistors are back-to-back, one body-to-drain diode is always reverse-biased. This eliminates the OFF-state problem caused by forward-biasing the diode.

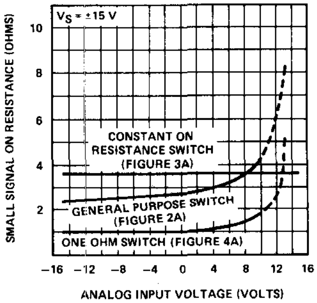
Since the bidirectional switch's gate drive is referenced to a fixed supply, its ON resistance varies with the input analog voltage (Figure 2C). This variation introduces distortion when you're driving low-impedance loads such as speakers or transmission lines. For constant ON resistance, use the circuit in Figure 3A.



A General Purpose Bidirectional Analog Switch
Figure 2A



OFF Isolation vs Frequency
Figure 2B



Small Signal ON Resistance vs Analog Input Voltage
Figure 2C

ON resistance is doubled in the two-VMOS switch (A), but inputs of both polarities are handled without losing isolation. The DG300 analog gate (B) raises the circuit's isolation by 30 dB. Decreasing load resistance also improves isolation. With the gate drive referenced to a fixed voltage (C), the ON resistance varies undesirably with the input, and generates distortion, especially with low impedance loads like speakers and transmission lines.

Figure 2

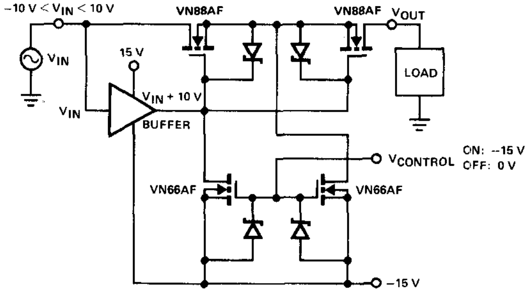
Bootstrapping Adds Linearity

In the ON state, a bootstrap voltage that tracks the input drives the gates of the VN88AF's. This bootstrapping keeps the VMOS's gate-to-source voltage constant and independent of the input signal. So, changes in the input-signal level do not modulate the ON resistance of the switch.

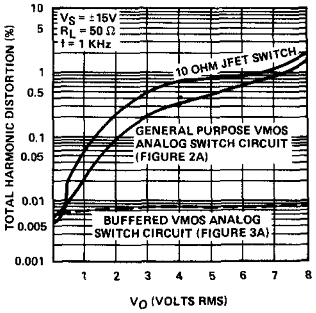
The buffer circuit reduces the computed total harmonic distortion from 1.5% to 0.005%, for 8 Vrms at 1 kHz into 50 Ω (Figure 3B). The popular 10 Ω DG186 JFET analog switch generates a higher total harmonic distortion of about 2%.

The two buffer circuits shown in Figures 3C and 3D isolate the input signal and employ a zener diode to provide a fixed gate-to-source voltage. The general-purpose buffer of Figure 3C has a flat frequency response of up to 300 kHz and accepts inputs ranging between ±15 V. The buffer of Figure 3D, VN66AK source follower, has its frequency response extended to 50 MHz and, when operated from ±30 V supplies, increases the signal range to ± 30 V.

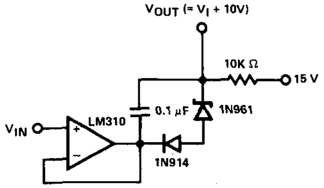
The VN66AK and VN88AF do not have on-board zener diodes like the VN66AF transistor. At the expense of the diode protection, the VN66AK and VN88AF gain lower capacitance from gate-to-source and reduced DC "see through" from driver to signal path. Bootstrapping the switch's gate circuits with a buffer permits the switch to operate with low distortion even as the signal amplitude comes close to the positive supply voltage.



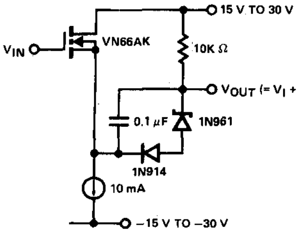
Low Distortion Constant ON Resistance Switch
Figure 3A



Distortion Improvement Using the Buffered Analog Switch
Figure 3B



General Purpose Buffer
Figure 3C



High Speed Buffer
Figure 3D

Bootstrapping the gate and input cuts distortion by holding the ON resistance constant (A). The buffered bootstrap circuit (A) distorts less than either a JFET or a nonbootstrapped VMOS analog switch (B). A general-purpose buffer (C) using the LM310 op amp is suitable for low speed switches, but when you need a fast analog switch, use the VN66AK buffer (D). In addition to speed, this buffer gives you increased isolation.

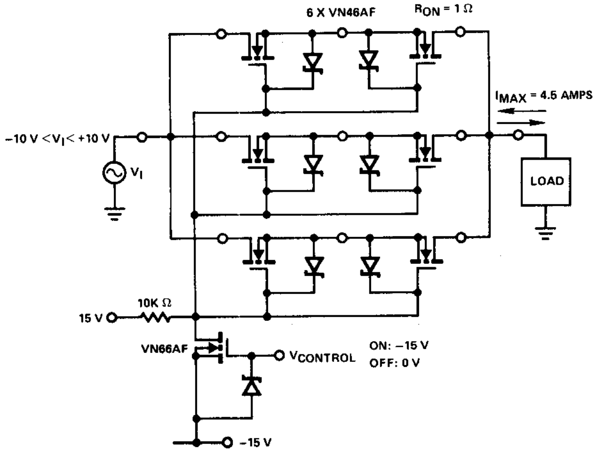
Figure 3

VMOS Devices Parallel Without Padding

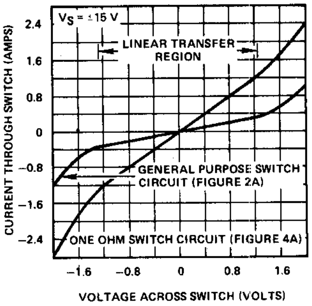
Paralleling devices lowers the total ON resistance. For example, three paralleled legs, each with two VN46AF's in series, make a 1 Ω switch (Figure 4A). Because VMOS devices are immune to current hogging, no ballast or balance resistors are needed. Negative tempcos, a VMOS feature, cause these devices to draw less current as they heat up. As a result, excess current is automatically shared by paralleled VMOS devices.

Paralleling three VN46AF's not only decreases ON resistance, but also increases the current capability to 6.0 A and extends the linear range of the large signal transfer characteristic from 0.3 to 1.2 A (Figure 4B).

The voltage range of the basic analog switch can also be increased. Simply use a higher breakdown VMOS unit (Figure 5). The VN98AK's have a 90 V breakdown, which allows up to ±40 V of voltage swing capability. However, these higher voltage devices do carry a penalty—the ON resistance is higher: 3.5 Ω vs 3.0 Ω for the VN46AF. Zener diode D_1 limits the gate-to-source potential to 30 V, and thereby prevents a possible gate-oxide rupture. Diode CR110 limits the current from the 50 V gate-bias supply.



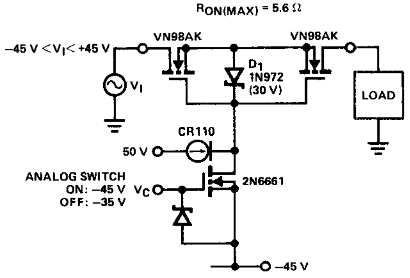
Ultra Low Resistance Switch (1 Ohm)
Figure 4A



Large Signal Transfer Characteristics
Figure 4B

No ballast or balance resistors are needed when VMOS devices are paralleled (A) because negative tempcos immunize them from current hogging. Paralleling extends the linear range from 0.3 to 1.2A (B) as it decreases the ON resistance of the analog switch to 1 Ω and increases its current-handling capability to 4.5 A.

Figure 4



90 V Peak to Peak Analog Switch

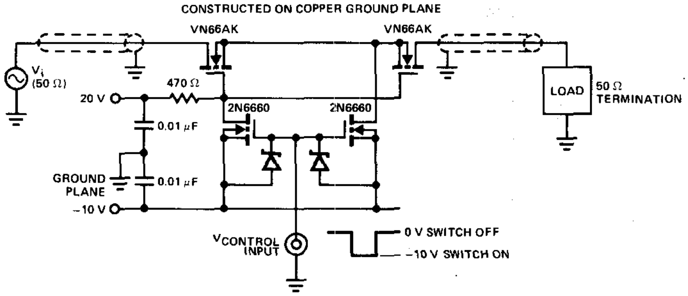
You pay for 90 V breakdown in the VN98AK with 3.0 Ω ON resistance, which allows swings of ±40 V. The zener diode limits the gate to-source potentials to 30 V.

Figure 5

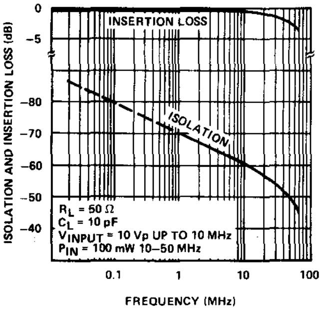
For the Ultimate in Switching Speed

The high power RF switch shown in Figure 6A performs very well up to 50 MHz–with turn-ON and turn-OFF times of 50 ns. At 10 MHz, isolation is 60 dB with a 20 V pk-pk input signal. Insertion loss is only 1 dB with a 50 Ω load (Figure 6B). The gain vs input power curve in Figure 6C shows that the RF analog switch using VN66AK's can put 1 W into a 50 Ω load at 14 MHz. The two-tone, third order, intermodulation product curves show a 42 dB intercept point with 1 dB of gain compression at 25 dBm input power.

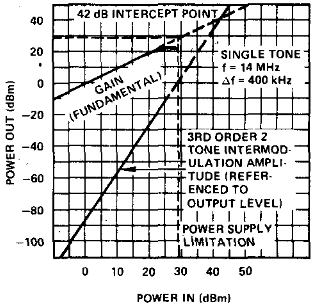
Turn-ON time of the switch (Figure 6D) is determined by the passive pull-up resistor combined with the capacitance at the gates of the VN66AK's. The negative turn-OFF transient is caused by charge-coupling to the output through the output capacitance of the VN66AK.



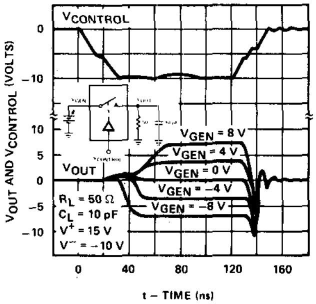
RF Analog Switch
Figure 6A



Insertion Loss and Isolation vs Frequency of RF Analog Switch
Figure 6B



Gain and Two Tone 3rd Order Intermodulation
Figure 6C



Switching Response of RF Switch into 50 Ohm Load
Figure 6D

The VN66AK switches high power at RF (A). At 10 MHz, a 20 V pk-pk signal is attenuated by 60 dB and the insertion loss is only 1 dB into 50 Ω and 10 pF (B). Third-order intermodulation distortion is given by the 42 dB intercept point, and 1 dB gain compression occurs at 25 dBm input for 14 MHz (C). The negative turn-OFF transient (D) is caused by charge-coupling to the output through the output capacitance of the VN66AK.

Siliconix

APPLICATION NOTE

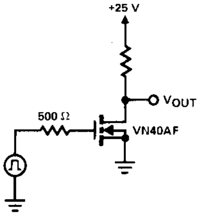
Driving VMOS Power FETs

Dave Hoffman
January 1979

INTRODUCTION

Using VMOS Power FETs you can achieve performance never before possible–if you drive them properly. This article describes circuits and suggests design methods to be used in order to obtain the performance from VMOS that you need.

When designing with VMOS there are some facts that must be kept in mind in order to get optimum results with every circuit. The first fact is that VMOS is a very high frequency device. The cut-off frequency for all VMOS FETs is several hundred megahertz. Most power designers are not used to designing with extremely high frequency devices because with bipolars the frequency response decreases as the power increases. The very high frequency response of VMOS is the basis for many of its advantages but it must be kept in mind while designing. With improper circuit design VMOS can oscillate. This oscillation can be eliminated, though, by exercising two simple precautions. First, minimize lead and trace lengths whenever possible, especially leads associated with the gate of the FET. If it is not possible to have short leads to the gate place a ferrite bead on the gate lead or a small resistor in series with the gate. The ferrite bead or the resistor must be very close to the gate. Second, because of the extremely high input impedance of VMOS (in excess of $10^{12}\ \Omega$) drive circuits may be designed which are very high impedance. Under these conditions it is possible for the gate node to get enough positive feedback from the gate-to-drain capacitance or just from stray fields in the circuit to cause oscillation. This must be kept in mind in the design of the circuit.



A Typical VMOS Switching Circuit
Figure 1

When driving VMOS it must be kept in mind that the dynamic input impedance is very different than the static input impedance. The input of a VMOS device is capacitive. The DC input impedance is very high but the AC input impedance varies with frequency. Because of this effect, the rise and fall times of VMOS are dependent on the output impedance of the circuit driving it. The first approximation of the rise or fall time is simply

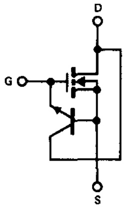
$$t_r \text{ or } t_f = 2.2 \cdot R_{OUT} \cdot C_{iss} \qquad (1)$$

where R_{OUT} is the output impedance of the drive circuit. This equation is valid only if the drain load resistance is much larger than R_{OUT}. Knowing this fact, along with the fact that there is no storage or delay time with VMOS, it is very easy to calculate the rise and fall times and set them to any desired value. For example, if you wanted to calculate the 10% to 90% rise or fall time for the circuit shown in Figure 1 using Equation 1 the rise time is equal to:

$$t_r = (2.2)\,(500)\,(50 \times 10^{-12}) = 55 \text{ nsec}$$

The dynamic input characteristics of VMOS are covered very thoroughly in Siliconix' application note AN79-3.[1]

A last thing to remember when you are driving VMOS is the input protection zener diode. When putting a positive voltage on the gate with respect to the source, the maximum voltage rating of the zener diode should not be exceeded. It is more important, however, that you do not forward bias the zener diode by putting a negative voltage on the gate while the VMOS is operating in a circuit. The reason for this is most easily explained by referring to Figure 2. As can be seen in the figure, the zener diode is actually the base-emitter junction of a bipolar transistor. If a negative voltage greater than 0.6 V is placed on the gate, the base-emitter junction of the bipolar will be forward biased which will turn on the bipolar transistor. When the bipolar is turned on, current will flow from the drain through the bipolar and out the gate. This operating condition is very likely to be destructive. If negative voltages must be placed on the gate it is recommended that you use a VMOS part that does not have an input zener diode. Non-zenered equivalents are available for most of Siliconix' zenered devices.



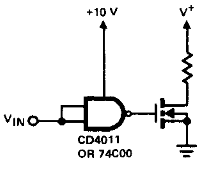
A Parasitic NPN Transistor in Zener Protected MOSFETS
Figure 2

Of all operating modes the common-source configuration is the simplest to drive. Because of the high input impedance of VMOS it can be driven directly from many logic families. When driving from a CMOS gate as shown in Figure 3, rise and fall times of about 60 nsec can be expected due to the limited source and sink currents available from the CMOS gate.[2] If faster rise and fall times are required there are several ways to obtain them. One easy way is if there are extra gates in the package that is driving the VMOS simply put the extra gates in parallel with the gate already being used. The additional current available will cut down the rise and fall times. If no extra gates are available an emitter-follower buffer can be used as shown in Figure 4. With this circuit the current available to the VMOS will be the output current of the CMOS multiplied by the beta of the bipolars. Because the bipolars are operating as emitter-followers there will still be no storage time to worry about and the frequency limit will be determined by either the CMOS gate or the f_T of the bipolars, whichever comes first.

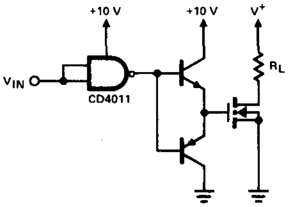
VMOS can also be driven directly from TTL gates. Because the output voltage of TTL is limited, the output current of the VMOS will be limited to some value less than its maximum rated current. The output current that can be expected can be determined from the transfer characteristic of the device being used. For example, if a TTL gate is driving VN46AF the minimum output current of the VMOS will be approximately 250 mA. This value was obtained by using the minimum output voltage of the TTL gate (3.2 V) for a high level output and referring to the transfer characteristic for the VNAZ which is the VMOS geometry used in the VN46AF. If more than 250 mA is required the output of a standard VMOS gate can be pulled up to the 5 V rail as shown in Figure 5. With a full 5 V on the gate the VN46AF will typically sink 600 mA.

For very high speeds a capacitive driver such as the MH0026 can be used as shown in Figure 6. With this drive configuration typical rise and fall times are less than 10 nsec.

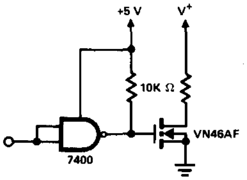
When operated in the common-drain mode VMOS is somewhat more difficult to drive than when in the common-source mode. Because of VMOS' high input impedance, though, it is considerably easier to drive common-drain than a bipolar would be when operated common collector. Common-drain circuits can be used when the load needs to be connected to ground, when an active pull-up and pull-down is required (totem pole circuit), or in bridge type circuits. For the purpose of this discussion all examples will be shown with totem pole circuits.



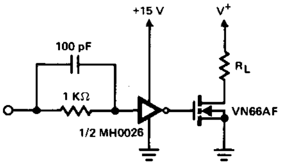
Driving VMOS with a CMOS Gate
Figure 3



An Emitter-Follower Circuit Will Decrease VMOS Rise and Fall Times
Figure 4

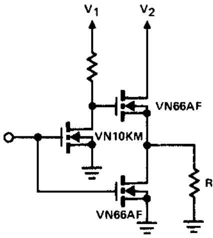


Pulling Up a TTL Output Will Increase the Sink Current of the VMOS
Figure 5



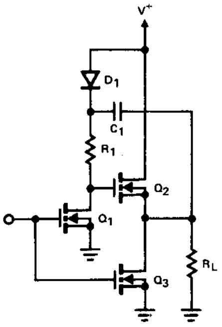
Using an MOS Clock Driver to Drive VMOS
Figure 6

The difficulty with common-drain circuits occurs because as the voltage across the load increases the enhancement voltage of the common-drain device decreases. Referring to Figure 7, as the voltage across R_L approaches V_2 the enhancement voltage for the upper VN66AF decreases. If V_1 is not greater than V_2 then the voltage across R_L can never reach V_2. For this reason whenever a common-drain circuit is used it is always necessary to have or to generate a voltage that is greater than the voltage which is desired to be impressed across the load. The amount the voltage has to be above the desired drain voltage is dependent upon the current the VMOS must source and can be determined from the transfer characteristic of the VMOS being used. If no supply voltage is available other than the one the load is to be pulled up to, one can be generated. This can be done very easily because of the very low drive current requirements of the VMOS.

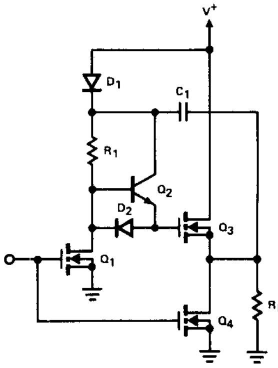


VMOS in Totem-Pole Configuration
Figure 7

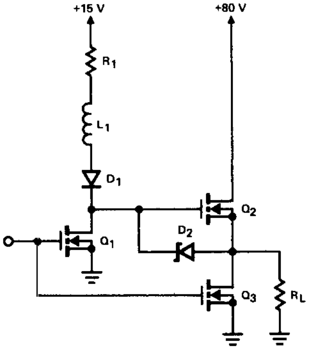
One way of generating the required gate voltage is the bootstrap circuit shown in Figure 8. In the circuit, when Q_1 and Q_3 are on, C_1 is charged to the supply rail through D_1. When Q_1 and Q_3 are turned off, the gate voltage on Q_2 goes to the supply rail. As the source of Q_2 begins to pull R_L up, the voltage across C_1 will be maintained, therefore, the gate-to-source voltage of Q_2 will be maintained. The size of C_1 should be large enough so that when it charges the gate capacitance of Q_2 a minimum voltage equal to the required enhancement voltage of Q_2 will be maintained across it. A good rule of thumb is to make C_1 equal to ten times the C_{iss} of the FET. Figure 9 shows the same bootstrap circuit with some added components to improve the rise and fall times. In the circuit Q_2 acts as an emitter-follower to increase the peak gate current to Q_3. D_2 will be forward biased when Q_1 turns on and serves as a low impedance path to discharge the gate of Q_3.



VMOS Bootstrap Circuit
Figure 8



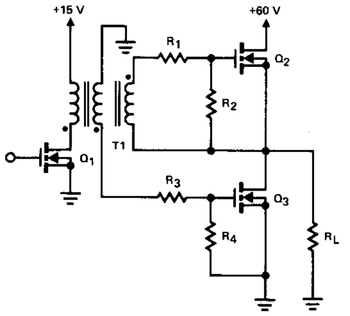
Bootstrap Circuit with Emitter-Follower
for Improved Rise Times
Figure 9



Inductive Kickback Drive Circuit
Figure 10

Another method to drive a common-drain VMOS FET is shown in Figure 10. Rather than charging a capacitor and then feeding a signal back from the output as was done in the bootstrap circuit, this circuit stores the required charge in an inductor. When Q_1 is turned off a flyback voltage is generated across the inductor. This voltage is used to maintain an enhancement voltage equal to the voltage of zener diode D_2 across the VMOS FET. Once the Q_2 has been fully turned on and the voltage on R_L is at the rail a negligible amount of energy is required to keep Q_2 on. Q_2 will remain on until Q_1 is turned on, or until the leakage currents of Q_1 and D_2 discharge the gate capacitance of Q_2.

Another method that can be used to drive a common-drain VMOS is transformer drive. A transformer drive circuit is shown in Figure 11. In this circuit the transformer is used in the flyback mode when turning on the upper FET. R_1 and R_3 are used to suppress ringing and R_2 and R_4 are used to assist with turn-off of the FETs. When driving with a transformer, care must be taken to design the transformer so that the secondary inductance in conjunction with the input capacitance of the FET does not create ringing of oscillation problems.



Transformer Drive Circuit for VMOS
Figure 11

SUMMARY

The very high input impedances of VMOS Power FETs greatly simplify the drive requirements as compared to bipolars. The input drive requirements for both common-source and common-drain configurations were discussed in detail. With common-source circuits the requirement that needs to be kept in mind is the rise and fall time required. With common-drain circuits a method of maintaining an adequate enhancement voltage must be considered in addition to required rise and fall time requirements.

REFERENCES

1. A. Evans, D. Hoffman, "Dynamic Input Characteristics of a VMOS Power Switch" AN79-3.
2. D. Hoffman, L. Schaeffer, "VMOS – A Breakthrough in Power MOSFET Technology" AN76-3.

Publications Index

Application Notes

Document Number	Title
AN70-1	FET Cascode Circuits Reduce Feedback Capacitance
* AN70-2	FETs for Video Amplifiers
AN71-1	A High Resolution CMRR Test Method
* AN72-1	FETs in Balanced Mixers
* AN72-2	FETs as Analog Switches
AN73-1	FETs as Voltage-Controlled Resistors
AN73-2	IC Multiplexer Increases Analog Switching Speeds
AN73-3	Switching High-Frequency Signals With FET Integrated Circuits
AN73-4	Junction FETs in Active Double-Balanced Mixers
AN73-5	Driver Circuits for the JFET Analog Switch
* AN73-6	Function/Application of the L144 Programmable Micro-Power Triple Op Amp
* AN73-7	An Introduction to FETs
* AN74-1	Function/Application of the LD110/LD111 3½ Digit A/D Converter Set
AN74-2	Analog Switches in Sample and Hold Circuits
AN74-3	Designing Junction FET Input Op Amps
* AN74-4	Audio-Frequency Noise Characteristics of Junction FETs
* AN75-1	CMOS Analog Switches—A Powerful Design Tool
AN76-1	Measuring High Frequency S-Parameters on the Dual Gate MOSFET
* AN76-2	Function/Application Problem Solving with the DF215 Dual Set Point Timer
* AN76-3	VMOS—A Breakthrough in Power MOSFET Technology
* AN76-4	Function/Application of the LD110/LD114 3½ Digit A/D Converter Set
* AN76-5	Function/Application of the LD130 ±3 Digit Converter
* AN76-6	DG300 Series Analog Switch Applications
* AN76-7	Function/Application of the L161 Industry's First Programmable Micropower Comparator
* AN77-1	Function/Application of the LD120/LD121 4½ Digit A/D Converter Set in Measurement Systems
* AN77-2	Don't Trade off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches
* AN77-3	Function/Application of the LD120/LD121 4½ Digit A/D Converter Interfaced with an 8080A Microprocessor
* AN77-4	Function/Application of the DF331/DF332 New Companding Converter Chip Set
* AN79-1	A 500 KHz Switching Inverter for 12 V Systems
* AN79-2	Stepping Motor Controller
* AN79-3	Dynamic Input Characteristics of VMOS Power Switch
* AN79-4	Driving VMOS Power FETs

Design Aids

Document Number	Title
* DA74-1	Design Aid of the LD110/LD111 3½ Digit DVM Demonstrator Board
* DA76-1	The VMOS Power FET Audio Amplifier
* DA76-2	Design Aid of the LD130 ±3 Digit DVM Demonstrator Board
DA76-3	Design Aid of the LD130 ±3 Digit Auto-Ranging DMM
* DA77-1	Design Aid to Build a Portable 0 to 99.9°F LCD Display Thermometer using the DF411
* DA77-2	Design Aid of the LD120/LD121 4½ Digit DVM
* DA77-3	Design Aid to Build a Smoke Alarm Demonstrator with the SM110 Detector IC
* DA77-4	Design Aid to Build a Piezoelectric Smoke Alarm Demonstrator with the SM110 Detector IC
* DA77-5	Design Aid for a Versatile Darkroom Timer using the DF215
* DA78-1	Design Aid to Build a CODEC Evaluation Demonstrator with the DF331/DF332/DF334
* DA78-2	Considerations for the Filtering of Analog Signals in DF331/DF332/DF334 CODEC Converter Applications
DA78-4	Design Aid to Build a Smoke Detector with the SM110 IC

Design Ideas

Document Number	Title
DI71-1	The FET Constant Current Source
DI71-4	Wideband Mixer-Preamplifer Using FETs
DI71-5	A FET Frequency Doubler
DI71-6	Using FETs in Selective VHF Amplifiers
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* DI71-9	Wideband UHF Amplifier with High Performance FETs
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Document Number	Title
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* TA73-2	Designing with Monolithic FET Switches
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Catalogs

Document Number	Title
______	Analog Switch Data Book
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______	Telecommunications Data Book
______	VMOS Power FET Design Catalog
______	OEM Pricing/Product Information Selector Guide

Reprints & Reports

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______	Designing with Codec's: Know your A's and μ's. Thomas J. Mroz, *EDN* 5/76
______	Log Data under μ Control. Gary Grandbois, *Electronic Design* 5/76
______	Higher Power Ratings Extend VMOS FETs' Dominion. Arthur D. Evans, David C. Hoffman, Edwin S. Oxner, Walter Heinzer and Lee Shaeffer. *Electronics* 6/78
______	Siliconix, Inc. Annual Report. 1979

glossary of terms and abbreviations

1. Upper case letters indicate DC voltages and currents.
2. Lower case letters indicate AC voltages and currents.
3. Subscripts can refer to the terminals used in the measurements, i.e., V_G = Gate Voltage; or simply help define the symbol, i.e., t_f = Fall Time, t_r = Rise Time.
4. Triple subscripts are used for terminal references only. The first subscript is the object terminal. The second subscript is the common terminal. The third gives the condition of the remaining terminal(s). S = Short, 0 = open and X = neither open nor short (refer to the test conditions). Example: BV_{GSS} = Breakdown Voltage from gate to source with the drain shorted to the source.

b_{fg} = Common-Gate Forward Susceptance

b_{fs} = Common-Source Forward Susceptance

b_{igs} = Common-Gate Input Susceptance

b_{iss} = Common-Source Input Susceptance

b_{ogs} = Common-Gate Output Susceptance

b_{oss} = Common-Source Output Susceptance

b_{rg} = Common-Gate Reverse Susceptance

b_{rs} = Common-Source Reverse Susceptance

BV_{DGO} = Drain-Gate Breakdown Voltage

BV_{DSS} = Drain-Source Breakdown Voltage

BV_{SDX} = Drain-Source Breakdown Voltage

BV_{G1G2} = Gate-Gate Breakdown Voltage

BV_{G1SS} = Gate 1 to Source Breakdown Voltage

BV_{G2SS} = Gate 2 to Source Breakdown Voltage

BV_{GBS} = Gate-Body Breakdown Voltage

BV_{GSS} = Gate-Source Breakdown Voltage

BV_{SDS} = Source-Drain Breakdown Voltage

BV_{SGO} = Source-Gate Breakdown Voltage

C_{db} = Drain-Body Capacitance

C_{dgo} = Drain-Gate Capacitance

C_{gb} = Gate-Body Capacitance

C_{gd} = Gate-Drain Capacitance

C_{gs} = Gate- Source Capacitance

C_{iss} = Common-Source Input Capacitance

C_{oss} = Common-Source Output Capacitance

C_{rss} = Common-Source Reverse Transfer Capacitance

C_{sb} = Source-Body Capacitance

C_{sd} = Source-Drain Capacitance

C_{sgo} = Source-Gate Capacitance

D = Drain

$\bar{e}_N$ = Equivalent Short Circuit Input Noise Voltage

f_m = Figure of Merit

G = Gate

g_{fg} = Common-Gate Forward Transconductance

g_{fs} = Common-Source Forward Transconductance

g_{fso} = Common-Source Forward Transconductance @ $V_{GS} = 0$

g_{fs1}/g_{fs2} = Common-Source Forward Transconductance Ratio

g_{ig} = Common-Gate Input Conductance

g_{is} = Common-Source Input Conductance

g_{og} = Common- Gate Output Conductance

g_{os} = Common-Source Output Conductance

g_{oss} = Common Source Output Conductance @ $V_{GS} = 0$

$g_{os1}-g_{os2}$ = Differential Output Conductance

G_{pg} = Common-Gate Power Gain

G_{ps} = Common-Source Power Gain

$I_{D(off)}$ = Drain Cutoff Current

$I_{D(on)}$ = Drain ON Current

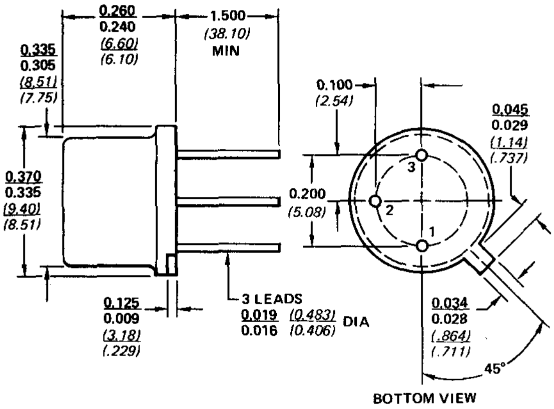
I_{DGO} = Drain-Gate Leakage

glossary of terms and abbreviations (cont'd)

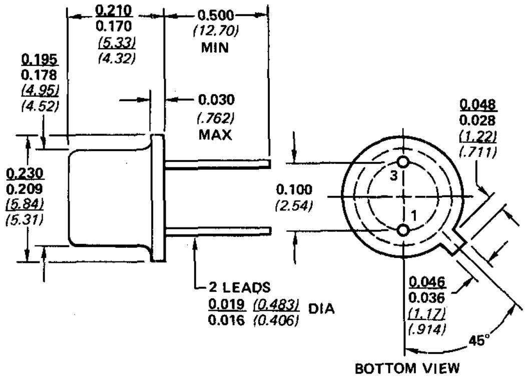
I_{DSS} = Saturation Drain Current
I_{DSS1}/I_{DSS2} = Saturation Drain Current Ratio
I_F = Forward Current
I_G = Gate Operating Current
I_{G1G2} = Gate to Gate Leakage Current
$|I_{G1}-I_{G2}|$ = Differential Gate Operating Currents
I_{GBS} = Gate to Body Leakage Current
$I_{G(f)}$ = Gate Forward Current
I_{GSS} = Gate Reverse Current
I_{G1SS} = Gate 1 to Source Leakage Current
I_{G2SS} = Gate 2 to Source Leakage Current
I_{G1SSR} = Gate 1 to Source Reverse Leakage Current
I_{G2SSR} = Gate 2 to Source Reverse Leakage Current
$\bar{i}_n$ = Equivalent Open-Circuit Noise Current
I_P = Pinch-Off Current
NF = Noise Figure
P_D = Continuous Power Dissipation
P_{OV} = Peak Operating Voltage
$r_{ds(on)}$ = Drain-Source ON Resistance
$r_{DS(on)}$ = Static Drain-Source ON Resistance
Re (Y_{fg}) = Common-Gate Forward Transconductance
Re (Y_{fs}) = Common-Source Forward Transconductance
Re (Y_{ig}) = Common-Gate Input Conductance
Re (Y_{is}) = Common-Gate Output Conductance
Re (Y_{os}) = Common-Source Output Conductance
Re (Y_{rg}) = Common-Gate Reverse Transconductance
Re (Y_{rs}) = Common-Source Reverse Transconductance
r_{GS} = Common-Source Input Resistance
S = Source
t_d = Delay Time
$t_{d(off)}$ = Turn-Off Delay Time
$t_{d(on)}$ = Turn-On Delay Time
t_f = Fall Time
T_j = Junction Temperature
t_{off} = Turn-Off Time
t_{on} = Turn-On Time
T_l = Lead Temperature
t_r = Rise Time
T_{stg} = Storage Temperature
V_B = Body Voltage
V_{BB} = Body Supply Voltage
V_D = Drain Voltage
V_{DD} = Drain Supply Voltage
$V_{DS(on)}$ = Drain-Source ON Voltage
V_G = Gate Voltage
V_{GG} = Gate Supply Voltage
V_{GS} = Gate-Source Voltage
$|V_{GS1}-V_{GS2}|$ = Differential Gate-Source Voltage
ΔV_{GS} = Differential Gate-Source Voltage
$\frac{\Delta|V_{gs1}-V_{gs2}|}{\Delta T}$ = Differential Gate-Source Voltage Change with Temperature
$V_{GS(f)}$ = Gate-Source Forward Voltage
$V_{GS(th)}$ = Gate Threshold Voltage
$V_{GS(off)}$ = Gate Source Cutoff Voltage
$V_{G1S(off)}$ = Gate 1 to Source Cutoff Voltage
$V_{G2S(off)}$ = Gate 2 to Source Cutoff Voltage
V_S = Source Voltage
V_{SS} = Source Supply Voltage
Z_d = Dynamic Impedance
Z_k = Knee AC Impedance
θ_I = Current Temperature Coefficient
θ_{J-A} = Junction to Ambient Thermal Resistance
θ_{J-C} = Junction to Case Thermal Resistance

mechanical data

Siliconix



TO-5



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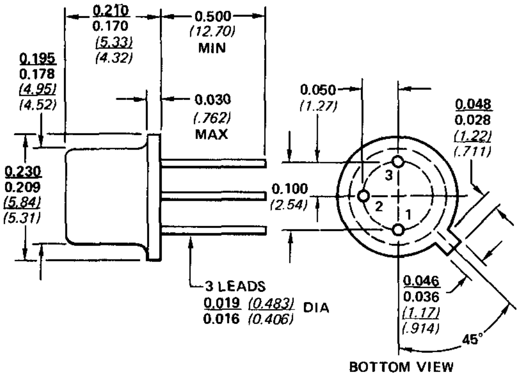
(2 PIN)



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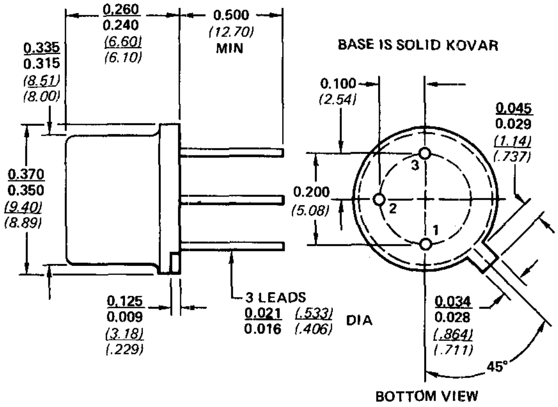

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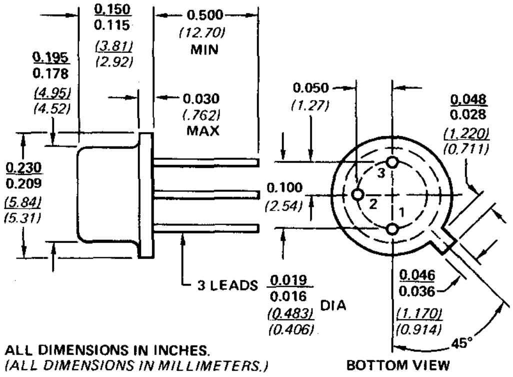
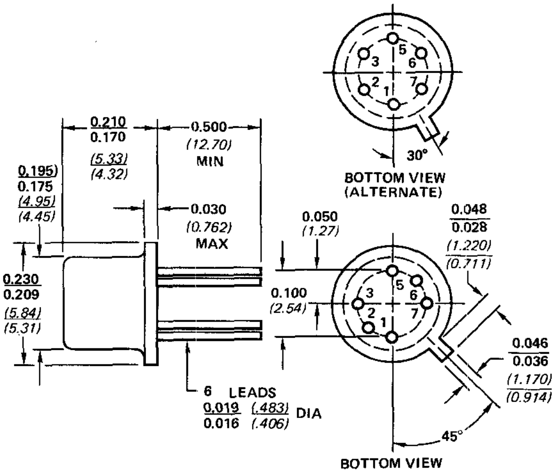


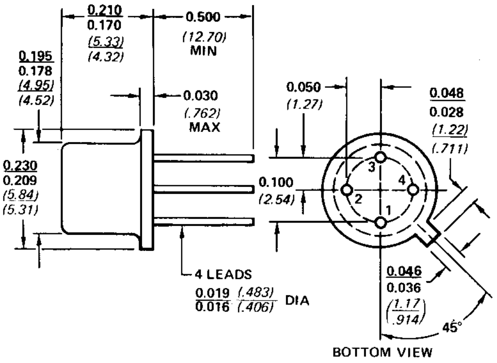
ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

TO-52



TO-71

mechanical data (cont'd)



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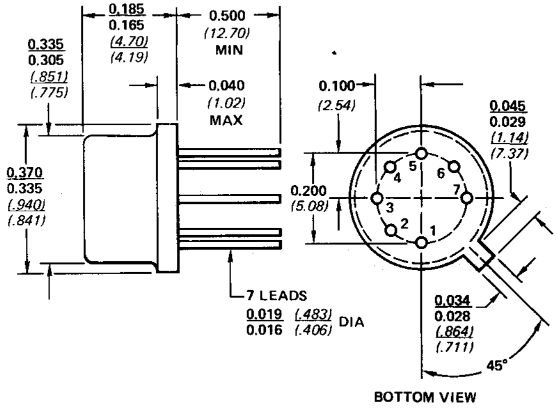

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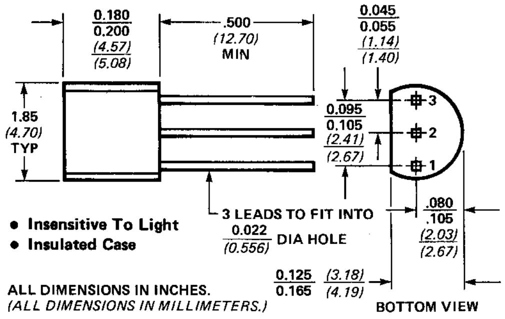
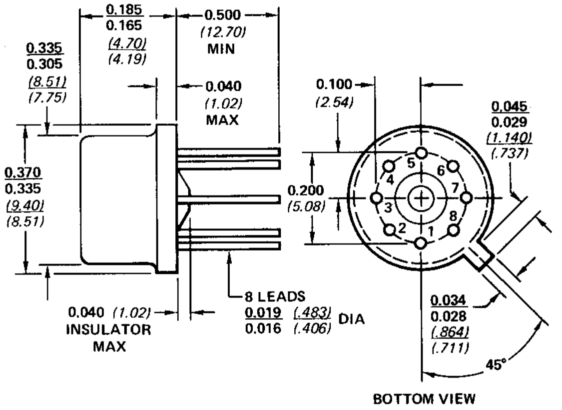


- **Insensitive To Light**
- **Insulated Case**

ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

TO-92



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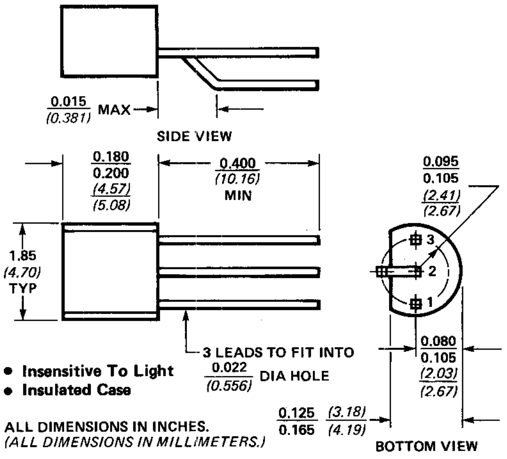

- **Insensitive To Light**
- **Insulated Case**

ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS.)

TO-92 LEAD FORM
(–18)

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(913)888-6680
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Tlx: 7-255 553

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Tel: (08152) 7774
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Tlx: 27249

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Komponentbolaget NAXAB
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S-17104 Solna
Tel: 08.985140
Tlx: 17912 KOMP

SWITZERLAND

Kontron Electronic AG
Bernerstrasse Sud 169
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Altrincham, CHESHIRE WA145RZ
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Cable: CANNONLEC - MELBOURNE

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867-Cj 22
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Seoul
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Tlx: K24123

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Mexel
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Tlx: MEXEL 0177 3197

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