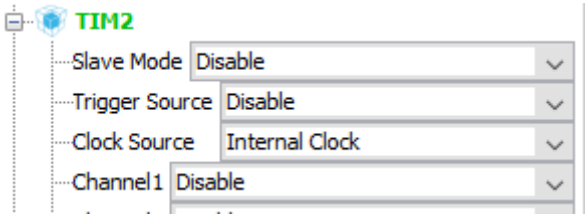
3.2 Master configuration

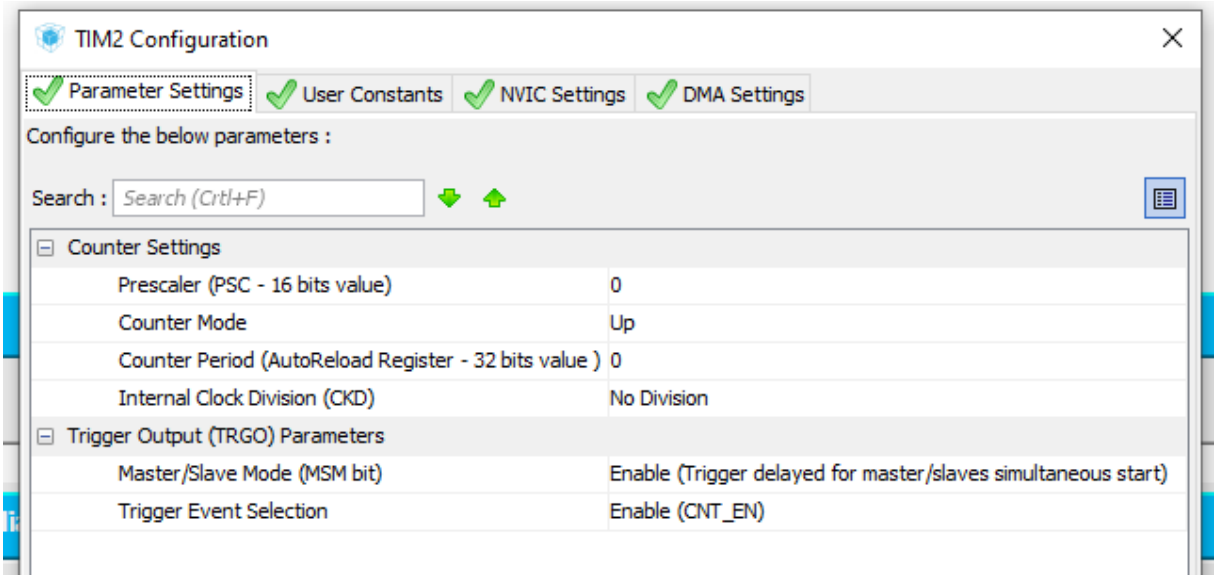
When a timer is selected as a master timer, the corresponding trigger output signal is used by the slave internal trigger (when configured). The trigger output can be selected from the following list:

- **Reset**: the UG bit from the TIMx_EGR register is used as a trigger output (TRGO);
- **Enable**: the counter enable signal is used as a trigger output (TRGO) to start several timers at the same time, or to control a window in which a slave timer is enabled;
- **Update**: the update event is selected as trigger output (TRGO). For example, a master timer can be used as a prescaler for a slave timer;
- **Compare pulse**: the trigger output sends a positive pulse when the CC1IF flag is to be set (even if it was already high) as soon as a capture or a compare match occurs;
- **OC1Ref**: OC1REF signal is used as trigger output (TRGO);
- **OC2Ref**: OC2REF signal is used as trigger output (TRGO);
- **OC3Ref**: OC3REF signal is used as trigger output (TRGO);
- **OC4Ref**: OC4REF signal is used as trigger output (TRGO).

To configure a timer in master mode:

1. Configure the timer
2. Select the trigger output to be used, by writing the MSM (Master /Slave Mode selection) bits in TIMx_CR2 register
3. Enable the MSM (Master/Slave Mode) bit in the SMCR register to allow a perfect synchronization between the current timer and its slaves (through TRGO).





3.3 Slave configuration

The slave timer is connected to the master timer through the input trigger. Each ITRx is connected internally to another timer, and this connection is specific for each STM32Fx/Gx/Hx/Lx//Wx series product as stated on the first page.

The slave mode can be:

- **Reset mode**: rising edge of the selected trigger input (TRGI) reinitializes the counter and generates an update of the registers
- **Gated mode**: the counter clock is enabled when TRGI is high. The counter stops (but is not reset) as soon as the trigger becomes low. Both counter start and stop are controlled
- **Trigger mode**: the counter starts at a rising edge of the trigger TRGI (but it is not reset). Only the counter start is controlled
- **External clock mode** 1: rising edges of the selected trigger TRGI clock the counter
- **Combined reset + trigger mode**: rising edge of the selected TRGI reinitializes the counter, generates an update of the registers and starts the counter. This feature is not available in the original series. See *Section 1: Overview* for more details.

To configure a timer in slave mode:

1. Select the slave mode to be used by writing SMS (slave mode selection) bits in SMCR register
2. Select the internal trigger to be used by writing TS (trigger selection) bits in SMCR register.

For more details on using the timer in this mode, refer to the examples provided in the STM32Cube package:

`Examples\TIM\TIM_CascadeSynchro,\TIM_ExtTriggerSynchro\TIM_Synchronization and \TIM_ParallelSynchro folders.`

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Table 108. TIMx Internal trigger connection

Slave TIM	ITR0 (TS = 000)	ITR1 (TS = 001)	ITR2 (TS = 010)	ITR3 (TS = 011)
TIM1	TIM5	TIM2	TIM3	TIM4
TIM8	TIM1	TIM2	TIM4	TIM5