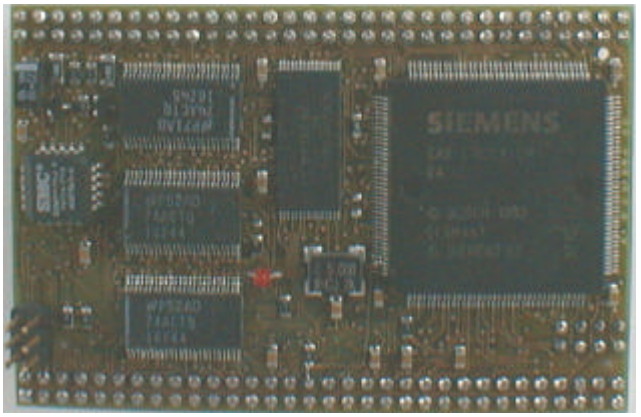


TQC - Microcontroller - Minimodul

TQM167/167C

Hardware - Manual

Hardware Manual for:

TQM167/167C Rev100

Rev200

Rev300

Rev400

Rev500

Rev600

Contents

1. Introduction

Top Quality embedded Microcontroller Systems

High integration and high reliability are what set the TQ-Components industrial microcontroller modules apart from the rest. TQ-Components Minimoduls from credit-card to half credit-card size are unbeatable in various applications. With an ever-expanding product line and clear technology migration path, TQ-Components offers OEMs uncompromising excellence in microcontroller modules. In a variety of industrial measurements, process regulations and control developments engineers confronted with the task of developing a complex monitoring / control system under time constraints are the prime beneficiaries of our microcontroller devices. Compare the advantage of the implementing a TQ-Components module to the total cost of a completely new circuitry design.

Time to market

TQ-Components microcontroller modules provide a drop-in CPU solution, with complete CPU kernel functionality on board. This enables engineers to take a project from concept to prototype or market in weeks, rather than in months or longer.

Reliability

TQ-Components modular embedded microcontroller Minimoduls have proven to be reliable and rugged in numerous demanding and critical applications. Our highly knowledgeable team of electonic engineers has wide experience in designing embedded microcontroller Moduls. The team‘s commitment to quality and reliability is evident througout the whole TQ-Components product line.

Upgradability

Thanks to the flexibilty of TQ’s product architectures, you will be able to enhance your products by taking advantage of a new technology when it becomes available. Our products offer a migration path so you can upgrade features or performance without major redesign.

TQ-Minimodules offers you ...

☑ **Best price-performance relationship**

- uncompromising use of most modern production-technology
- low price through high production quantity
- Custumized Versions on requests

☑ **Maximum performance on small footprint**

- double-sided SMT Technology
- Fine Pitch Multilayer Printed Circuit Boards
- using latest chip technology
- using latest Flash Memory technology

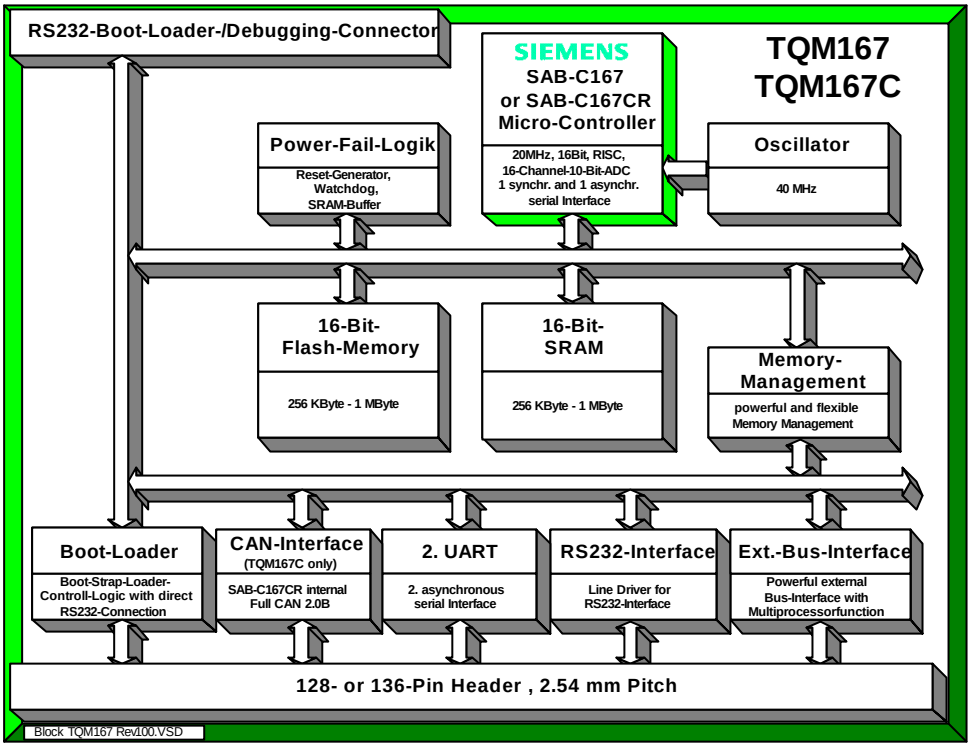
☑ **save time and money in your development**

- complete CPU kernel functionality on board
- immediate start through particular monitor-program
- works with most modern Software Development Tools such as compilers and debuggers
- Design-In Support through the manufacturer

☑ **save time and money in your production and service**

- Download-Function for development, production and service
- simple Firmware-Updates through Download-Function
- Download over Standard RS232-Interface without additional switches and jumpers
- Service-friendly modular construction

2. TQM167/167C Overview



2.1 Microcontroller SAB-C167-LM / SAB-167CR-LM

- High Performance 16 Bit-CPU
- 100 ns Instruction Cycle Time at 20 MHz CPU
- Up to 16 MByte Linear Address Space for Code and Data
- On-Chip CAN Interface (Version 2.0B) (*only SAB-C167CR-LM)
- 16-channel 10-bit A/D Converter
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with five 16-bit Timers
- Programmable Watchdog Timer
- Two Serial Channels (Synchronous/Asynchronous and High-Speed Synchronous)
- On-Chip Bootstrap Loader

Details see Siemens / Infineon User's Manual SAB-C167

2.2 Memory

2.2.1 Flash-Memory

- 256 kByte or 1 MByte
- organization 128k*16 or 512k*16
- 90 ns access time
- on Board programmable
- Standard: 256 kByte

2.2.2 SRAM-Memory

- 256 kByte or 1 MByte
- organization 128k*16 or 512k*16
- 70 ns access time
- external battery backup
- Standard: 256 kByte

2.3 Reset-Logic

- CPU internal Watchdog
- External Watchdog
- Switchable by Software (Optional)
- Power-Fail Logic with MAX691

2.4 Interface

2.4.1 Serial-Interface

- one internal asynchronous (integrated in the processor)
  - used unbuffered as RxD0 and TxD0
  - with RS232 Driver as RxD0# and TxD0#
- one external asynchronous (external UART COM81C17)
- one internal synchronous (integrated in the processor)

2.4.2 Bus-Interface

- Address Bus
- Data Bus
- Control Bus
- Fast 74ACTQ Drivers

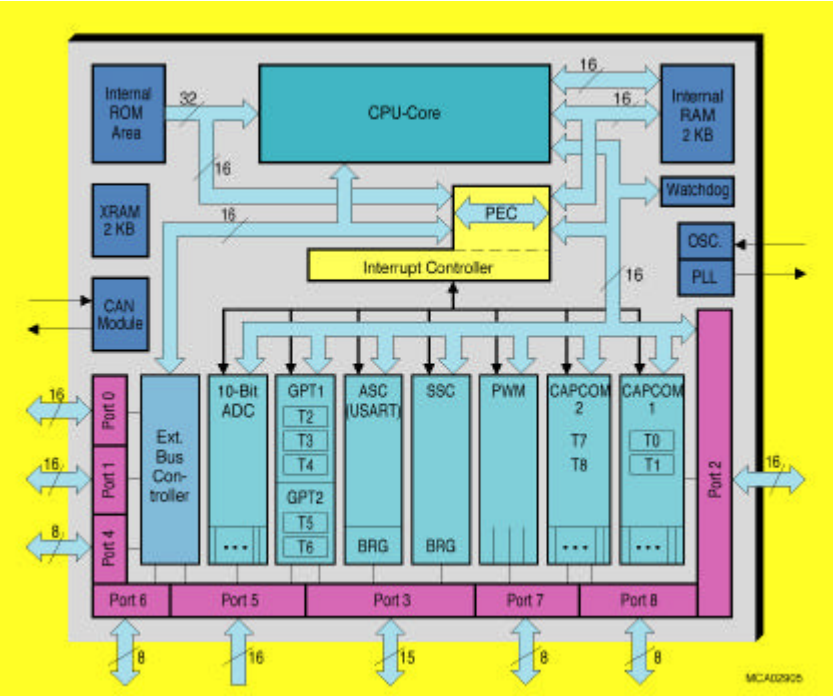
2.4.3 Internal Bootstrap Loader

- Download via serial Interface
- Download via Bootstrap Loader Connector
- Powerful Download Tools
- Download to SRAM or Flash

2.5 Internal LED

The LED installed on the top of the module is connected to the reset output RSOUT# of the module. It lights when RSOUT# is active, i.e. until the EINF command has been executed after a reset.

3. Microcontroller



- High Performance 16-bit CPU with 4-Stage Pipeline
- 100 ns Instruction Cycle Time at 20 MHz CPU Clock
- Enhanced Boolean Bit Manipu-lation Facilities
- Additional Instructions to Support HLL and Operating Systems
- Register-Based Design with Multiple Variable Register Banks
- Single-Cycle Context Switching Support
- Clock Generation via on-chip PLL or via direct clock-input
- Up to 16 MBytes Linear Address Space for Code and Data
- 4 KBytes On-Chip SRAM (2 KB Internal RAM, 2 KBytes Extension RAM)
- Programmable External Bus Characteristics for Different Address Ranges
- 8-bit or 16-bit External Data Bus
- Five Programmable Chip-Select Signals
- Hold- and Hold-Acknowledge Bus Arbitration Support
- 1024 Bytes On-Chip Special Function Register Area
- Idle and Power Down Modes
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40 ns
- 16-Channel 10-bit A/D Converter with 9.7 µs Conversion Time
- Two 16-Channel Capture/Compare Units
- 4-Channel PWM Unit
- Two Multi-Functional General Purpose Timer Units with five 16-bit Timers
- Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- On-Chip CAN Interface 2.0 B active with 15 Message Objects (Full-CAN/Basic-CAN) (*only SAB-C167CR-LM / TQM167C)
- Programmable Watchdog Timer
- Up to 111 General Purpose IO Lines, partly with Selectable Input Thresholds and Hysteresis
- On-Chip Bootstrap Loader

Details see Siemens / Infineon User's Manual SAB-C167

4. Memory

The flexible memory management of the TQM167 is different from most microcontroller modules of the same generation. The handling of the configuration of this module is more simple and flexible than in almost any other module.

The installed processor is equipped with 5 freely programmable Chip Select outputs which access the respective system components. This allows a completely open memory configuration of the minimodule.

In addition, it is possible to open "windows" of external memory in the flash EPROM or SRAM areas.

The memory management is described in detail in ⇨ Section 4.3.

4.1 Flash-Memory

4.1.1 Flash-Memory structure

Depending on the module variant, the non-volatile memory of the module is implemented with two 8-bit flash EPROMs with variable storage capacity. This results in a possible memory space of 128K*16 or 512K*16, representing as memory capacity of 256 KByte or 1024 KByte. The module TQM167 is therefore available with a maximum non-volatile memory of 1 MByte.

For exact technical data of the applied memory chips, please refer to ⇨ Section 10.

Details on programming are to be found in ⇨ Section 4.1.2 / 4.3.5

Depending on the equipping, the following memory configurations are possible:

Flash1	Flash2	Capacity:	Address space:
128 KByte	128 KByte	256 KByte	128K x 16
512 KByte	512 KByte	1024 KByte	512K x 16

* Due to the 16-bit data and address buses, both memory chips are always installed *

4.1.2 Flash EPROM access times

The access time of the flash EPROMs is 90 ns. The maximum access period is therefore 100 ns.

According to the data sheets of the SAB-C167, 2 wait states are necessary during memory access for reliable operation under worst-case conditions.

In strict compliance with the specifications for 90ns flash EPROMs, the following configuration is possible:

Field in BUSCON:	Value:	Delay:
MCTC [BUSCONx.0..3]	1101b	2 Waitstates (100ns)
RWDC [BUSCONx.4]	1b	Delay 0 ns
MTTC [BUSCONx.5]	1b	No Delay

The associated C command could then be as follows:

➔ BUSCONx = 0x04BD

4.2 SRAM-Memory

4.2.1 SRAM-Memory structure

Depending on the module variant, the static memory of the module is also implemented by two 8-bit SRAMs with variable storage capacity. This results in a possible memory space of 128K*16 or 512K*16, representing a memory capacity of 256 KByte or 1024 KByte. The module TQM167 is therefore available with a maximum static memory of 1 MByte. The SRAM can be protected against data loss by a battery buffer. The associated connections are provided on the module.

For exact technical data of the applied memory chips, please refer to ⇨ Section 10.

Details on programming are to be found in ⇨ Section 4.2.2 / 4.3.6

Depending on the installed chips, the following memory configurations are possible:

SRAM1	SRAM2	Capacity:	Address space:
128 KByte	128 KByte	256 Kbyte	128K x 16
512 KByte	512 KByte	1024 Kbyte	512K x 16

* Due to the 16-bit data and address buses, both memory chips are always installed *

4.2.2 SRAM access times

The static RAMs installed in the modules have a maximum access time of 70 ns and thereby guarantee a clock frequency of 20 MHz in conjunction with two logic ICs with a maximum access period of 93 ns.

According to the data sheets of the SAB-C167, 1 wait state is necessary during memory access for reliable operation under worst-case conditions. The access speed can be programmed by the fields MCTC (Memory Cycle Time Control), MTTC (Memory Tri-State Time Control) and RWDC (Read/Write Delay Control) of the respective BUSCON register.

In strict compliance with the specifications, the following configuration is therefore possible:

Field in BUSCON:	Value:	Delay:
MCTC [BUSCONx.0..3]	1110b	1 Waitstate (50 ns)
RWDC [BUSCONx.4]	1b	Delay 0 ns
MTTC [BUSCONx.5]	1b	No Delay

The associated C command could then be as follows:

➔ BUSCONx = 0x04BE

However, practical tests have shown that, under normal conditions (room temperature, Vcc=5V±0.25V) operation is also possible without wait states with the following configuration:

Field in BUSCON:	Value:	Delay:
MCTC [BUSCONx.0..3]	1111b	0 Waitstates
RWDC [BUSCONx.4]	1b	Delay 0 ns
MTTC [BUSCONx.5]	1b	No Delay

➔ BUSCONx = 0x04BF

4.3 Memory Management

This section contains all details and the know-how necessary for optimum usage of the memory installed in the module. The memory range management and configuration (memory management) can be implemented entirely by software. The address ranges can be programmed flexibly with the 5 freely programmable CS outputs of the processor and the associated configuration registers.

4.3.1 Principle of operation

The microcontroller SAB-C167 is equipped with 5 freely programmable Chip Select outputs which allow access to the respective periphery. For each address block allocated to a Chip Select output, it is also possible to select an individual configuration of the system bus. For this, the bus type, bus width, wait states and also the memory block can be allocated to a CS signal.

CS0 addresses all memory blocks of the addressable range not allocated to CS1-CS4. This makes it possible to manage non-sequential memory blocks without further measures. After a reset, the Chip Select lines CS1-CS4 of the processor are inactive. In this case, CS0 is active for the entire memory range.

To allow programs in the flash EPROM to be started, CS0 is used to address these memory chips after a reset CS0.

4.3.2 Chip Select allocation

The memory configuration applicable in most cases is works-adjusted by the manufacturer:

- CS0 addresses the flash EPROMs,
- CS1 the SRAMs.

If external memory is to be superimposed on the address range of the SRAM or flash EPROM, the SRAM / flash EPROM must be accessed through CS0 because it is only possible to open "windows" on memory blocks accessed by CS0.

To switch between the CS lines CS0 and CS1, an external register names XREG is implemented. XREG is accessed by CS2# and address line A8. Switching is performed with the data lines D0 and D1.

For programming, please refer to ⇨ Section 4.3.4 of this description.

Standard settings by TQ-Components:

Control line	Connected chip		
CS0#	On-board flash EPROM or on-board SRAM *)		
CS1#	On-board flash EPROM or on-board SRAM *)		
CS2#	Additional asynchronous interface and XREG		
CS3#	External memory		
CS4#	External memory		
CS0#	Reset configuration	000000_h- $FFFFFF_h$	Flash EPROM

*) Switchable with XREG (⇨ Section 4.3.4)

4.3.3 Programming of the Chip Select lines

The Chip Select lines are programmed by software via the registers BUSCON0..4 and ADDRSEL1..4.

The BUSCON registers define the hardware configuration of the system bus, the ADDRSEL registers the scope and size of memory.

In this, it must be observed that ADDRSEL0 does not exist because, as described in Sect. xx, all memory space outside the defined ranges of CS1-CS4 is allocated to the Chip Select line CS0.

BUSCON registers:

The BUSCON registers are all adjustable by software. These are not preset apart from the BUSCON0 register.

The following parameter can be set individually through the BUSCON registers for each memory block initialised with the respective CS lines:

- Bus width:
  The system bus can be selected with a width of 8 or 16 bits. If an 8-bit bus is selected, first the Low byte and then the High byte are transferred through the data lines D0-D7.
- Bus type:
  This allows the selection of a multiplexed or non-multiplexed bus.
- Wait states:
  Up to 15 wait states, memory tristates and a R/W delay can be specified.
- Miscellaneous:
  The length of the ALE signal and the functions of RD# and WR# can also be influenced here.

The exact programming is to be found in the processor manual.

ADDRSEL registers:

The division of the memory range is performed with the ADDRSEL registers. For this, the starting address of the memory block and the memory size must be specified:

ADDRSELx:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Range Start Address												Range Size Selection			

- **Range Start Address (RGSAD):**
  specifies the starting address of the memory block for the respective CS line (only integer multiples of the adjusted block size (RGSZ) are valid as the starting address; see table).

- **Range Size Selection (RGSZ):**
  Specifies the memory size as shown in the table below.

The following table is intended to simplify programming.

RGSZ:	Memorysize	RGSAD:	Startaddress
0 0 0 0	4 Kbyte	$RRRRRRRRRRRR_b$	$RRRRRRRRRRRR_b$ * 4KByte
0 0 0 1	8 Kbyte	$RRRRRRRRRRRx_b$	$RRRRRRRRRRR0_b$ * 4KByte
0 0 1 0	16 Kbyte	$RRRRRRRRRRxx_b$	$RRRRRRRRRR00_b$ * 4KByte
0 0 1 1	32 Kbyte	$RRRRRRRRRxxx_b$	$RRRRRRRRR000_b$ * 4KByte
0 1 0 0	64 Kbyte	$RRRRRRRRxxxx_b$	$RRRRRRRR0000_b$ * 4KByte
0 1 0 1	128 Kbyte	$RRRRRRRxxxxx_b$	$RRRRRRR00000_b$ * 4KByte
0 1 1 0	256 Kbyte	$RRRRRRxxxxxx_b$	$RRRRRR000000_b$ * 4KByte
0 1 1 1	512 Kbyte	$RRRRRxxxxxxx_b$	$RRRRR0000000_b$ * 4KByte
1 0 0 0	1 MByte	$RRRRxxxxxxxx_b$	$RRRR00000000_b$ * 4KByte
1 0 0 1	2 MByte	$RRRxxxxxxxxx_b$	$RRR000000000_b$ * 4KByte
1 0 1 0	4 MByte	$RRxxxxxxxxxx_b$	$RR0000000000_b$ * 4KByte
1 0 1 1	8 MByte	$Rxxxxxxxxxxx_b$	$R00000000000_b$ * 4KByte
Rest:	Not defined		

R: used bit; x: unused bit

☞ *Example:*

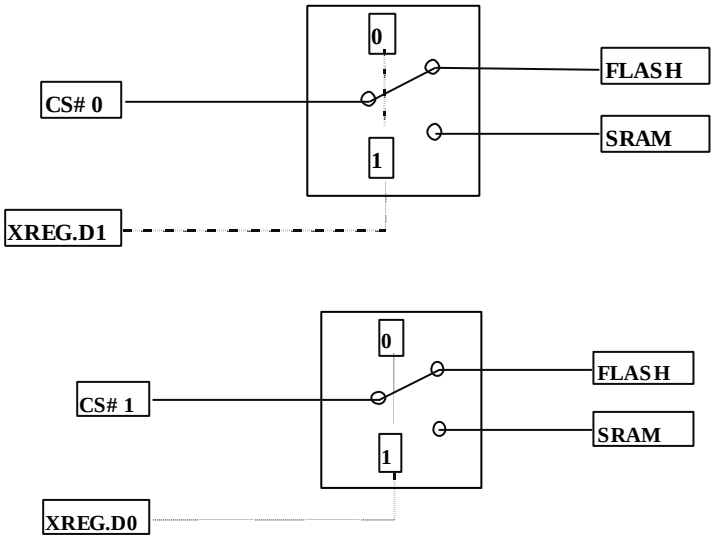
ADDRSEL4 = 0x1A42; (= 0001 1010 0100 0010_b)

Specifies a 16 KByte block of memory from address $1A4000_h$ for access to external memory.

4.3.4 Programming the XREG register

With the aid of the external register XREG, it is possible to switch between the Chip Select lines CS0# and CS1#.

The register XREG is selected when both the address line A8 and the Chip Select line CS2# reach a Low state. Only then is it possible to program the two Chip Select lines by the data lines D0 and D1. In this, XREG.D0 switches CS#1 and XREG.D1 switches CS#0:



The following table is intended to simplify programming:

XREG D1	XREG D0	CS-Line: CS0#	CS-Line: CS1#	
0	0	Flash	Flash	
0	1	Flash	SRAM	Default-Value
1	0	SRAM	Flash	
1	1	SRAM	SRAM	

XREG can only be changed after it has been initialised by EINIT (machine command, see processor manual) (RSTOUT# ≡ High). If XREG is accessed in word mode, the High byte must also contain the value of XREG because CS2# is initialised as an 8-bit bus and the High byte is also written to XREG.

XREG access times

The configuration register XREG is implemented with a simple JK flipflop and can only be accessed for writing. XREG cannot be read. Access is fully uncritical and can therefore be executed with 0 wait states.

ATTENTION:

When XREG is switched, it must be ensured that the program does not "shut out" its own memory medium.

ATTENTION:

Because the external UARTs are located at memory locations in which CS2# and A9 have Low states, it is advisable to access the UARTs with an address offset of 100_h (A8 ≡ High state) and XREG with an address offset of 200_h (A9 ≡ High state) because it is otherwise possible to access XREG and the UARTs simultaneously.

Example:

ADDRSEL2 = 2000h

then:

UART address = 200100h
XREG address = 200200h

☞ *Example:*

The program is located in the SRAM and is accessed via CS1#. CS0# is to be selected:

XREG	= 1 1	CS0# and CS1# access the SRAM.
BUSCON0	= < SRAM configuration >	Prepares switching for CS0#
ADDRSEL1	= < Flash memory range >	Deactivates the address range for CS1#
		==> Program "runs" via CS0#
BUSCON1	= <Flash configuration >	Access to the flash is initialised
XREG	= 0 1	CS1# is allocated to the flash

4.3.5 Programming the flash EPROMs

Due to the 16-bit data bus, it is possible to program both memory chips simultaneously. However, initialisation addresses differing from those specified by AMD result from the memory range allocation:

Bit A0 of the flash EPROM is connected to A1 of the address bus, which doubles the value of the initialisation address. However, it is basically possible to address both memory chips simultaneously by word access.

☞ *Example:* Byte Program

	1st Buscycle		2nd Buscycle		3rd Buscycle		4th Buscycle	
	Addrerss	Data	Address	Data	Address	Data	Address	Data
Standard	5555H	AAH	2AAAH	55H	5555H	A0	PA	Data
TQM167	AAAAH	AAAAH	5554H	5555H	AAAAH	A0A0	PA	Data

PA: the address to be programmed is equal in both cases because the code is distributed between the two flash EPROMs in the minimodule TOM167.

4.3.6 Examples of memory configurations

4.3.6.1 Memory allocation used by the monitor program MON16X

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-0FFFFFh	SRAM	1	$048C_h$	0008_h
100000h-1FFFFFh	Flash-EPROM	0	$048C_h$	-------
200000h-200FFFh	Exteral UART	2	0400_h	2000_h
300000h-3FFFFFh	External Memory	3	0480_h	3008_h

4.3.6.2 memory allocation after a download to the RAM

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-0FFFFFh	SRAM	1	$048C_h$	0008_h
100000h-FFFFFFh	Flash-EPROM	0	$048C_h$	-------

These are two concrete proposals of memory configurations which ensure stable operation:

- Variant for a program in flash memory
- Variant for a program in SRAM

4.3.6.3 Proposals for applications in the flash EPROM

XREG register=01_b

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-0FFFFFh	Flash-EPROM	0	$048C_h$	-------
100000h-1FFFFFh	SRAM	1	$048C_h$	1008_h
200000h-200FFFh	External UART	2	0400_h	2000_h
300000h-3FFFFFh	External Memory	3	0480_h	3008_h

4.3.6.4 Proposal for an application in the SRAM

XREG register=10_b

Memory-Area	Chip	CS#	BUSCON-Register	ADDRSEL-Register
000000h-0FFFFFh	SRAM	0	$048C_h$	-------
100000h-1FFFFFh	Flash-EPROM	1	$048C_h$	1008_h
200000h-200FFFh	External UART	2	0400_h	2000_h
300000h-3FFFFFh	External Memory	3	0480_h	3008_h

5. Interface

5.1 Serial Interface

The module is equipped with three serial interfaces:

- one internal asynchronous (integrated in the processor)
- one external asynchronous (external UART COM81C17)
- one internal synchronous (integrated in the processor)

5.1.1 Internal asynchronous interface

Initialisation:

The internal asynchronous interface operates directly with the processor clock. For programming, please refer to the initialisation recommended in the manual.

Hardware configuration:

The interface is equipped with triple connections on the module:

- Unbuffered as RxD0 and TxD0.
- With RS232 driver as RxD0# and TxD0#.
- With a 6-pole connector strip on the upper side of the module, the so-called bootstrap loader plug. With this, the flash memory chips can be programmed directly from a PC (⇨ Section 5.3).

5.1.2 External asynchronous interface

Initialisation:

The clock frequency of the external UART is generated by the PWM register of port P7.0. This saves additional hardware. The UART is accessed in the block starting at CS2# + 100h (see also ⇨ Section 4.3).

The initialisation of the UART is described in the data sheet of the COM81C17 (⇨ Section 11).

Because the chip is not operated with its intended clock frequency of 5.0688 MHz, a baud rate error occurs, which is partially compensated by the internal error of the UART. The chip is operated at 5.00MHz.

Baudrate	Error of 80C167	Error of 81C17	Total Error
4800	-1.36%	0%	-1.36%
9600	-1.36%	0%	-1.36%
19200	-1.36%	+3.125%	+1.77%
38400	-1.36%	+3.125%	+1.77%

The application XSIODEMO.C can be used as an example of programming.

Hardware configuration:

The interface is equipped with double connections on the module:

- Unbuffered as RxD1 and TxD1
- With RS232 driver as RxD1# and TxD1#

Access times for the external UARTs

The COM81C17 must be initialised 50 ns before the falling flank of RD#. This results in the following bus configuration:

Field in BUSCON:		Value:	Delay:
MCTC	[BUSCON2.0..3]	1101b	2 Waitstates (100ns)
RWDC	[BUSCON2.4]	0b	Delay 25 ns
MTTC	[BUSCON2.5]	0b	Delay 25 ns
ALECTRL	[BUSCON2.9]	1b	extended ALE-Signal

The associated C command could be as follows:

➔ BUSCON2 = 0x060D

5.1.3 Internal synchronous interface

Initialisation:

See ⇨ Section 5.1.1

Hardware configuration:

The conductors of the synchronous interface are connected to port 3 and can be used without limitations.

P3.8 MRST
P3.9 MTSR
P3.13 SCLK

5.2 Bus interface for external access

Fast bus drivers both for unidirectional and bidirectional data exchange are installed in the module, which can be used as required. This achieves a maximum degree of feedback tolerance and speed. The module is protected against undesired "external effects".

Use in multiprocessor systems is possible through the common data and address buses.

The performance of the applied driver chips is described in ⇨ Section 10 / 11 of this description.

The module is available with or without an external bus interface.

5.2.1 Access times for components outside the module

On the basis of the bus interface, external components must attain the following times:

Max. access time = 20 ns + 50 ns * <number of wait states>

If 90 ns SRAMs are used and taking account of all maximum delays, 2 wait states are therefore necessary: 20 ns + 2 * 50 ns = 120 ns (temperature range 0 - 70 °C)

Bus configuration:

Field in BUSCON:		Value:	Delay:
MCTC	[BUSCONx.0..3]	1101b	2 Waitstates (100ns)
RWDC	[BUSCONx.4]	1b	Delay 0 ns
MTTC	[BUSCONx.5]	1b	No Delay

The associated C command could be as follows:

➔ BUSCONx = 0x04BD

5.2.2 Properties of the bus drivers

The applied bus drivers 74ACTQ16244/74ACTQ16245 which buffer the address, data and control buses have the following properties:

Symbol	Parameter	V_{cc}	T_A = -40°C bis +85°C	Units	Conditions
U_{IH}	Minimum High Input Voltage	4.5	2.0	V	U_{OUT} = 0.1V or
		5.5	2.0	V	U_{CC} - 0.1V
U_{IL}	Maximum Low Input Voltage	4.5	0.8	V	U_{OUT} = 0.1V or
		5.5	0.8	V	U_{CC} - 0.1V
U_{OH}	Minimum High Output Voltage	4.5	4.4	V	I_{OUT} = -50µA
		5.5	5.4	V	
					U_{IN} = U_{IL} or U_{IH}
		4.5	3.76	V	I_{OH} -24 mA
		5.5	4.76	V	I_{OH} -24 mA
U_{OL}	Maximum Low Output Voltage	4.5	0.1	V	I_{OUT} = 50µA
		5.5	0.1	V	
					U_{IN} = U_{IL} or U_{IH}
		4.5	0.44	V	I_{OL} 24 mA
		5.5	0.44	V	I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND

The following signals are buffered to the exterior of the module:

- D0 .. D15
- A0 .. A23
- RD#, WD#, ALE#, BHE#, CSE#, CSE1#, CSE2#, RSOUT#

5.3 Internal bootstrap loader

The installed processor is equipped with a bootstrap loader which, in conjunction with the periphery implemented in the module, makes programming of the EPROMs unnecessary.

The downloading of a program to the module can be performed via the serial interface or via the separate connector (see also ⇨ Section 5.4.3) on the top of the TQM167 module. The download interface is connected directly to the serial interface of a PC.

In this way, programs can be downloaded from a PC without additional hardware, either to the SRAM or to the flash EPROM.

Because the internal bootstrap loader of the processor can only process 32 bytes, it is necessary to transfer programs in several blocks into the memory of the module.

Functional sequence:

1. To activate the bootstrap loader, a reset must first be initiated (RTS and DTR active = 1).
2. The reset is enables after approx. 10 ms, the DTR line remains active.
3. The processor then enters the bootstrap loader mode and waits for a Null byte transmitted via ASC0.
4. The processor then returns an acknowledgement byte ($A5), which can be used to identify the processor.
5. 32 bytes are then transmitted by the PC, which are loaded directly into the internal RAM of the processor.

To allow convenient downloading of programs with larger memory requirement, TQ has developed the program BOOT16x (DOS Version) and TQLoad (Windows Version).
The program BOOT16x provides user-friendly control of the entire loading operation.
More detailed explanations and examples of this are to be found in the Software Manual.

The following signal lines of the serial interface are used (by the PC) for the download:

TQM167			PC (DSUB-9)		PC (DSUB-25)	
Signal	Pin		Pin	Signal	Pin	Signal
RESINS#	1	↔	7	RTS	4	RTS
TXD0#	2	↔	2	RxD	3	RxD
GND	3	↔	5	GND	7	GND
GND	4	↔	5	GND	7	GND
BOOTSTR#	5	↔	4	DTR	20	DTR
RXD0#	6	↔	3	TxD	2	TxD

5.4 Brief description of the Minimodul Interface

These tables specify all important connections with their abbreviations and a brief description. Input and output signals are specified as such.

The tables apply to the fully equipped module (full version). Not all connections are actually installed in all versions.

For an exact description of the port lines, please refer to the Microcontroller User's Manual.

5.4.1 Connector X1

Des.:	I/O	Function, Comments:
Vcc		Supply voltage +5V ± 5%, current consumption < 300 mA
Vbat		SRAM buffer voltage +3V (2.5..4V), < 40µA max.
Varef		A/D converter reference voltage +4V < Varef < Vcc+0.1V
DGND		Digital ground (Vss)
AGND		Analogue ground
RSIN#	I	Reset input, active low; internally connected through 4.7Kohm to Vcc
RSOUT#	O	Reset output, active low, buffered
NMI#	I	Non-maskable interrupt, active low, internally connected through 10KOhm to Vcc
READY#	I	READY# input of the 80C167, active low, internally connected through 10KOhm to Vcc
RD#	O	Read signal, active low, buffered
WR#	O	Write signal, active low, buffered
BHE#	O	High byte enable signal, active low, buffered
ALE	O	Address latch enable signal, active high, buffered
CSE#	O	Chip select external output, active low, buffered. Low state indicates access to an address in the external memory range.
CSE1#	O	Chip select external output, active low, buffered. Low state indicates access to an address in the external memory range, accessed by CS3#
CSE2#	O	Chip select external output, active low, buffered. Low state indicates access to an address in the external memory range, accessed by CS4#
RESINS#	I	Reset input to initiate resets via the serial interface. Negative voltage: reset enabled; positive voltage: reset is initiated.
BOOTSTR#	I	Bootstrap loader input to activate the bootstrap loader mode via the serial interface. Positive voltage: bootstrap mode active
CP1#	I	Universal input of the external UART
CP2#	I/O	Universal I/O of the external UART
D0 .. D15	I/O	Data bus lines D0 .. D15, buffered
A0 .. A19	O	Address bus lines A0 .. A19, buffered
A20 .. A23	O	Address bus lines A20 .. A23, buffered; in the variant with CAN controller, the address bus lines A20 .. A23 are not available
P2.0 .. 15	I/O	I/O port with capture/compare registers
P3.0 .. 15	I/O	I/O port with diverse functions; P3.11, P3.12, P3.14 not for universal use
P5.0 .. 15	I	Input port, analogue inputs AN0 .. AN15, Vagnd < Vain < Varef
P6.5 .. 7	I/O	I/O port, alternative: HOLD#, HLDA#, BREQ#
P8.0 .. 7	I/O	I/O port; alternative: capture/compare register
TXD0#	O	RS232 data output of the internal serial interface ASC0, level adjustment by MAX233
RXD0#	I	RS232 data input of the internal serial interface ASC0, level adjustment by MAX233
TXD1	O	RS232 data output of the external UART, not buffered
RXD1	I	RS232 data input of the external UART, not buffered
TXD1#	O	RS232 data output of the external UART, level adjustment by MAX233
RXD1#	I	RS232 data input of the external UART, level adjustment by MAX233
NC		Not Connected: pin is not connected and should not be used

= active low or inverted signal (RS232)

5.4.2 Extension connector X2

Des:	I/O	Function, Comments:
P7.0	I/O	I/O port; if equipped with the external UART: used as clock generator
P7.1 .. 3	I/O	I/O port; alternative: PWM output
P7.4 .. 5	I/O	I/O port; alternative: capture/compare register
P7.6	I/O	I/O port; alternative: capture/compare register; optional external watchdog
P7.7	I/O	I/O port; alternative: capture/compare register; optional interrupt input of the external UART

5.4.3 Bootstrap loader Connector X3

Des:	I/O	Function, Comments:
TXD0#	O	RS232 data output of the internal serial interface ASC0, level adjustment by MAX233
RXD0#	I	RS232 data input of the internal serial interface ASC0, level adjustment by MAX233
RESINS#	I	Reset input to initiate a reset via the serial interface. Negative voltage: reset enabled; positive voltage: reset is initiated.
BOOTSTR#	I	Bootstrap loader input to activate the bootstrap loader mode via the serial interface. Positive voltage: bootstrap mode active
DGND		Digital ground

= inverted signal (neg. voltage = logical "1", pos. voltage = logical "0")

6. Reset-Logik

6.1 Power fail supervisor

The MAX691 chip is installed as a power fail supervisor. This monitors the supply voltage and initiates a controlled reset of the module if the voltage falls. Special hardware (power fail logic) is implemented in the module for this purpose.

Another task of the chip is to protect the SRAMs against data loss. For this, the chip switches the supply voltage of the SRAMs to the battery supply and protects the SRAM against uncontrolled access by the processor.

6.2 Description of the optional external watchdog:

In principle, a watchdog is nothing more than a resettable timer which automatically counts backwards from a specified value to 0. If zero is reached, watchdog initiates a reset. To prevent this, the timer is reset to its initial counter value regularly by a signal delivered by the µP. If the microprocessor is unable to issue this signal, e.g. because it is "trapped" in an endless loop, the watchdog initiates a reset, returning the module to a defined initial state:

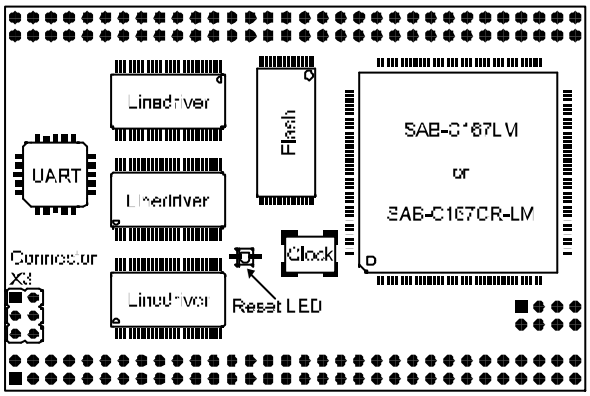
- To prevent the external watchdog from executing a reset of the entire microcontroller module, port P7.6 must change its state (toggle) within the watchdog timeout period, typically 100ms (min. 70ms, max. 140ms). If the external watchdog is used, it must therefore be ensured that the interval at which the module software accesses port P7.6 is less than 70ms.
- The first timeout period directly after a reset is typically 1.6s (min. 1s, max. 2.25s)
- To deactivate the external watchdog, port P7.6 must be set as an input.

  (The external watchdog is a optional function. **See Section 10** (Model No. and Order Code)

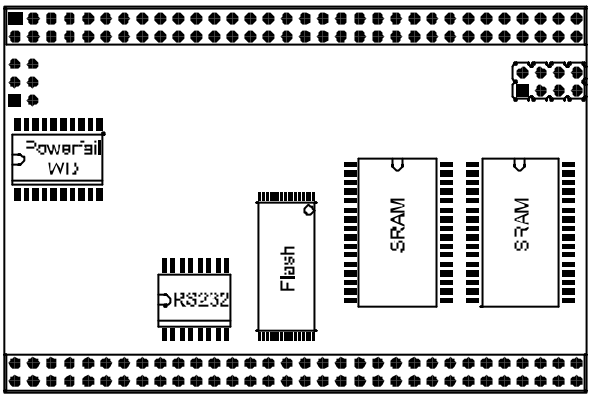
7. Technical Data

- PCB-Material: FR4
- PCB-Layout: double sided SMT
- PCB-Layer: 6 Layer
- Dimension: 81,6 x 54 mm²
- Ambient Operating Temperature: 0°C - 70°C
- Storage Temperature Range: -20°C - +85°C
- Power Supply: 5 VDC ± 5%
- Power Dissipation typ. 250 mA

7.1 View



TQM167/TQM167C Top-View



TQM167/TQM167C Bottom-View

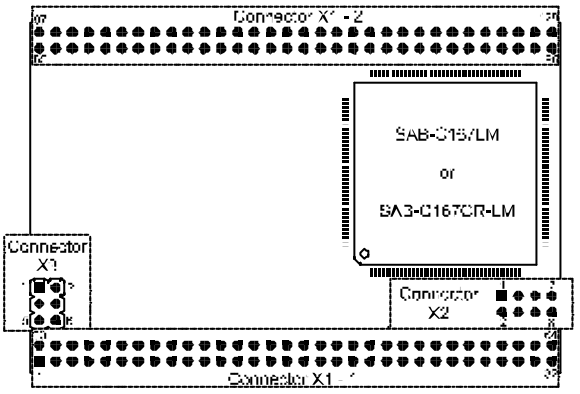
8. Mechanical Data and Pin Configuration

8.1 Connector

8.1.1 Connector Reference No.

Minimodul Side			Customer Board Side	
X1: 64 Pin Header 2.54 mm Pitch			64 Pin Receptacle 2.54 mm Pitch	
Fischer Elektronik Berg AMP Molex or compatible	SL22/124 64 G 77313-170-64 3-829394-2 10-96-7645		Fischer Elektronik Berg AMP Molex or compatible	BL6 64 G 87606-332 3-215313-2 15-44-3264
X2: 8 Pin Header 2.54 mm Pitch			8 Pin Receptacle 2.54 mm Pitch	
Fischer Elektronik Berg AMP Molex or compatible	SL22/124 8 G 77313-170-08 0-829394-4 10-96-7085		Fischer Elektronik Berg AMP Molex or compatible	BL6 8 G 87606-304 0-215313-4 15-44-3208
X3: 6 Pin Header 2.54 mm Pitch			6 Pin Receptacle 2.54 mm Pitch	
Fischer Elektronik Berg AMP Molex or compatible	SL22/124 6 G 77313-170-06 0-829394-3 10-96-7065		Fischer Elektronik Berg AMP Molex or compatible	BL6 6 G 87606-303 0-215313-3 15-44-3206

8.1.2 Connector Location



TQM167/TQM167C Topview

8.1.3 Pin Configuration

8.1.3.1 Extension Connector X2

No.:	Function	No.:	Function	No.:	Function	No.:	Function
1	P7.0	**3**	P7.2	**5**	P7.4	**7**	P7.6
2	P7.1	**4**	P7.3	**6**	P7.5	**8**	P7.7

8.1.3.2 Bootstraploader Connector X3

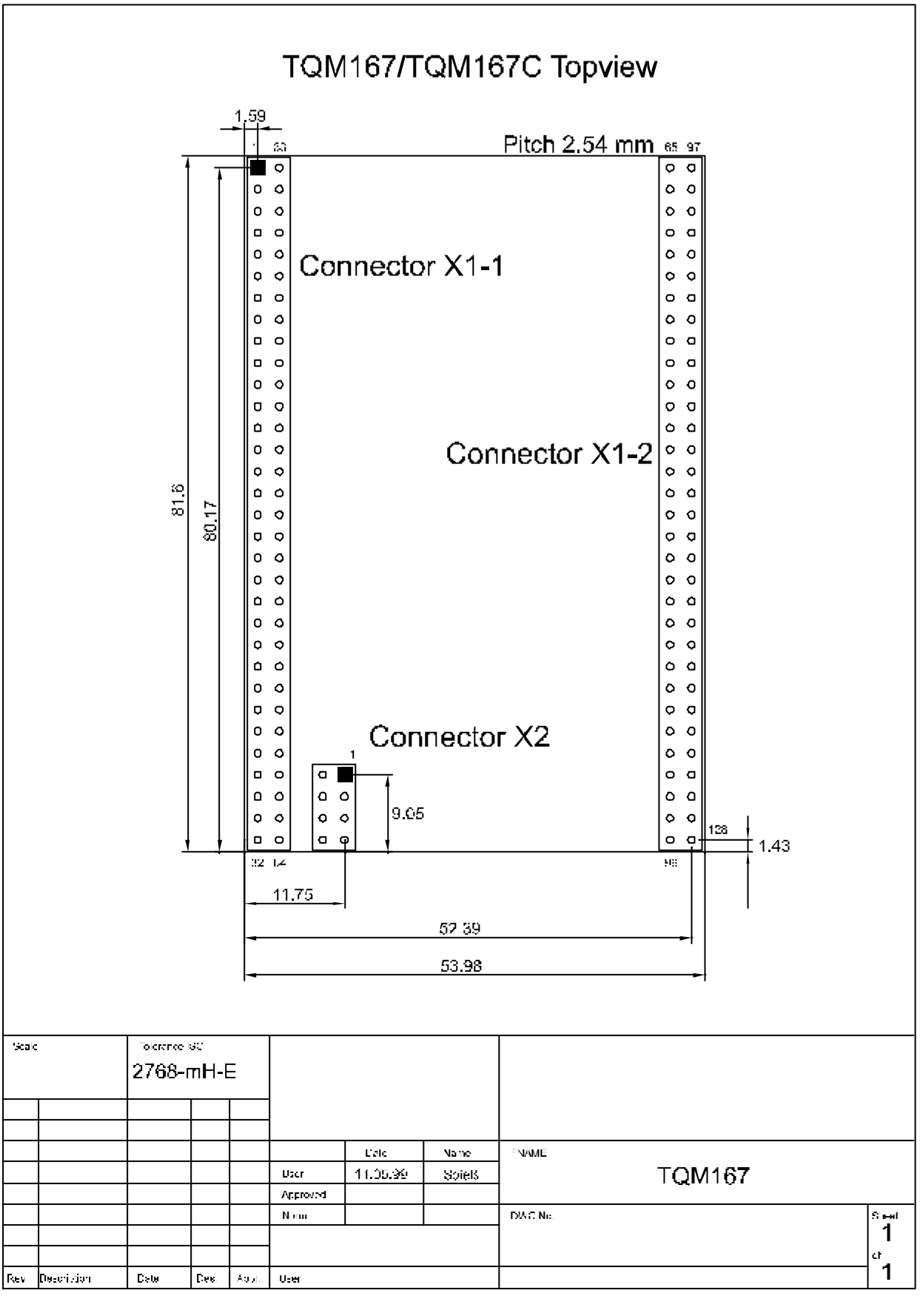
No.:	Function	No.:	Function	No.:	Function
1	RESINS#	**3**	DGND	**5**	BOOTSTR#
2	TxD0#	**4**	DGND	**6**	RxD0#

8.1.3.3 Interface Connector X1

Pin-No.:	Function	Pin-No.:	Function	Pin-No.:	Function	Pin-No.:	Function
128	P3.1/T6OUT	**96**	P3.0/T0IN	**64**	DGND	**32**	DGND
127	P3.3/T3OUT	**95**	P3.2/CAPIN	**63**	P5.8	**31**	P5.9
126	P3.5/T4IN	**94**	P3.4/T3EUD	**62**	P5.6	**30**	P5.7
125	P3.7/T2IN	**93**	P3.6/T3IN	**61**	Varef	**29**	AGND
124	RXD1	**92**	TXD1	**60**	P5.4	**28**	P5.5
123	P3.11/RXD0	**91**	P3.10/TXD0	**59**	P5.2	**27**	P5.3
122	READY#	**90**	NC	**58**	P5.0	**26**	P5.1
121	P3.15	**89**	P2.1	**57**	P5.15	**25**	RSIN#
120	P2.0	**88**	P2.3	**56**	P5.13	**24**	P5.14
119	P2.2	**87**	P2.5	**55**	P5.11	**23**	P5.12
118	P2.4	**86**	P2.7	**54**	NC[1]/CAN_RXD[2]	**22**	P5.10
117	P2.6	**85**	P2.9	**53**	NC[1]/CAN_TXD[2]	**21**	Vbat
116	P2.8	**84**	P2.11	**52**	P8.7	**20**	P8.6
115	P2.10	**83**	P2.13	**51**	P8.5	**19**	P8.4
114	P2.12	**82**	P2.15	**50**	P8.3	**18**	P8.2
113	P2.14	**81**	A17	**49**	P8.1	**17**	P8.0
112	A16	**80**	WR#	**48**	NMI#	**16**	RSOUT#
111	RD#	**79**	ALE	**47**	P6.5/HOLD#	**15**	P6.7/BREQ#
110	BHE#	**78**	P3.8/MRST	**46**	A7	**14**	P6.6/HLDA#
109	P3.13/SCLK	**77**	P3.9/MTSR	**45**	A6	**13**	A5
108	D7	**76**	D6	**44**	A4	**12**	A3
107	D5	**75**	D4	**43**	A2	**11**	A1
106	D3	**74**	D2	**42**	A0	**10**	A23[1]
105	D1	**73**	D0	**41**	CSE#	**9**	A22[1]
104	CSE1#	**72**	CSE2#	**40**	A21[1]	**8**	A20[1]
103	RESINS#	**71**	BOOTSTR#	**39**	A19	**7**	A18
102	CP1#	**70**	CP2#	**38**	A15	**6**	A14
101	D14	**69**	D15	**37**	A13	**5**	A12
100	D12	**68**	D13	**36**	A11	**4**	A10
99	D10	**67**	D11	**35**	A9	**3**	A8
98	D8	**66**	D9	**34**	TXD0#	**2**	RXD0#
97	Vcc	**65**	Vcc	**33**	TXD1#	**1**	RXD1#

[1] = only for TQM167
[2] = only for TQM167C

9. Mechanical Drawing



Scale		Tolerance ISO 2768-mH-E						
						Date	Name	NAME TQM167
					User	11.05.99	Spieß	
					Approved			
					Norm			DWG No.
								Sheet 1 of 1
Rev.	Description	Date	Des.	Appr.	User			

10. Model No. and Order Code

TQM167 C X Y Minimodul

Optional Function		total
No Option **(Standard)**	add 0	
External Watchdog activ	add 1	
Without RS232 Driver	add 2	
Without 2. Serial Interface	add 4	
Without Connector X2 for P7.x lines	add 8	
Without external Address lines A0...A15	add 16	
Without external Bus Interface	add 32	
Summary	**Y =**	

Memory X =	256 kByte SRAM	1 Mbyte SRAM
256 kByte FLASH	**A***	**B**
1 Mbyte FLASH	**C**	**D**

* Standard

CAN Configuration	**C =**
With SAB-C167LM / without CAN	Blank
With SAB-C167CR-LM / with CAN	C

STK167A0-EU	Starterkit with TQM167A0 Minimodul, EVA-Board, 220V Power Supply, Cable
STK167A0-US	Starterkit with TQM167A0 Minimodul, EVA-Board, 110V Power Supply, Cable
STK167D0-EU	Starterkit with TQM167D Minimodul, EVA-Board, 220V Power Supply, Cable
STK167D0-US	Starterkit with TQM167A0 Minimodul, EVA-Board, 110V Power Supply, Cable
STK167CA0-EU	Starterkit with TQM167CA0 Minimodul, EVA-Boad, 220V Power Supply, Cable
STK167CA0-US	Starterkit with TQM167CA0 Minimodul, EVA-Boad, 110V Power Supply, Cable
STK167CD0-EU	Starterkit with TQM167CD0 Minimodul, EVA-Board, 220V Power Supply, Cable
STK167CD0-US	Starterkit with TQM167CD0 Minimodul, EVA-Board, 110V Power Supply, Cable
TQMDWLK	Download Cable 2m, Sub-D 9-pin (PC COM Port) to Receptacte 6-pin (X3)
BOOT16x	Download Software (DOS Version)
TQLOAD	Download Software (Windows Version)

11. References

SAB-C167 / SAB-C167C Microcontroller

http://www.infineon.com/products/index.htm
Microcontrollers
C167 Users Manual

AM29F010 / AM29F040 Flash EPROM

http://www.amd.com/products/products.html
Non Volatile Memory
Flash – 5V only Flash Memory
Data Sheet AM29F010 / AM29F040

74ACTQ16244 / 74FCT16244 / 74ACTQ/16245 / 74FCT16245 Line Driver

http://www.national.com/pf/master.html
Master Selection Guide / 54
Data Sheet 54ACTQ/74ACTQ16244 / 54ACTQ/74ACTQ16245

http://www.idt.com/products/pages/Logic.html
FCT Logic / 5V Double Density with High Drive
Data Sheet IDT74FCT16244ATPV / IDT74FCT16245ATPV

MAX233 RS232 Driver

http://www.maxim-ic.com
Products / Data Sheets
Data Sheet MAX233ACWP

COM81C17 UART

http://www.smsc.com

Rev No.	Designed by:	Date	Approved by:	Date:	Changes:
100	Heifi				1sk Version
101	KOZ	03.02.00			2nd Version (Layout)
102	KOZ	20.03.99			3rd Version (Layout)

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