VLSI Projects for M.Tech

URL:

https://takeoffprojects.com/VLSI-Projects-for-MTech

Description:

The main aim of this project is to assist with image coding so as to supply high accurate images without losing any information. The plan of this VLSI Project for M.Tech is to implement a modified booth encoder using a 4 bit SFQ multiplier which gives better performance as compared to the conventional booth encoder.

An Area-Efficient Universal Cryptography Processor for Smart Cards: This project implements both private and public key supported three cryptography algorithms for open-end credit applications to supply highly secured user authentication and data communication.
A High-Speed/Low-Power Multiplier using Spurious Power Suppression Technique: This project is meant to filter the useless spurious signals of arithmetic units so as to avoid useless transmission of knowledge.

A Lossless Data Compression and Decompression Algorithm and Its Hardware Architecture: the target of this project is to implement a two-stage hardware architecture supporting the features of Parallel dictionary LZW .This project reduces the general energy consumption during transmission of knowledge of wireless sensor networks by decomposing LUT-Log-BCJR algorithm into fundamental Add Compare Select (ACS) operations.

An Efficient VLSI Architecture for Removal of Impulse Noise in Image: This project aims to reinforce the visual quality of images and to avoid chances of being corrupted by impulse noise by implementing an efficient VLSI architecture using edge preserving filters.
A Processor-In-Memory Architecture for Multimedia Compression: This project presents the implementation of a coffee complexity processor-in Â–memory architecture that supports multimedia applications like video and compression by applying very large command word and single-instruction and multiple data concepts.

This has added new capabilities and features, however, most of the time, the implementations are proprietary and networking isn't always possible. Control is communicated to the FPGA from a mobile through its Bluetooth interface. This leads to an easy, cost-effective, and versatile system, making it an honest candidate for future smart home solutions.

A robotic arm may be a type normally programmable mechanical arm, which may be wont to pick and place various objects within the industries from one place to a different place. It could also be the sum of the mechanism or may be a part of a more complex robot. The FPGA based project is executed using Spartan Project Kit and Robotic ARM kit.

To connect modern complex control systems communication demands, the project presents a multi-channel UART controller supported FIFO (First in First Out) technique and FPGA (Field Programmable Gate Array). It can also be wont to reduce synchronization error between sub-

systems during a system with several subsystems. The controller is reconfigurable and scalable.

By integrating multiplication with accumulation and devising a hybrid type adder the performance was improved. The modified booth encoder will reduce the amount of partial products generated by an element of two. Fast multipliers are essential parts of digital signal processing systems. The speed of multiply operation is of great importance in digital signal processing also as within the general purpose processors. The number to be added is that the multiplicand, the amount of times that it's added is that the multiplier, and therefore the results the merchandise.