

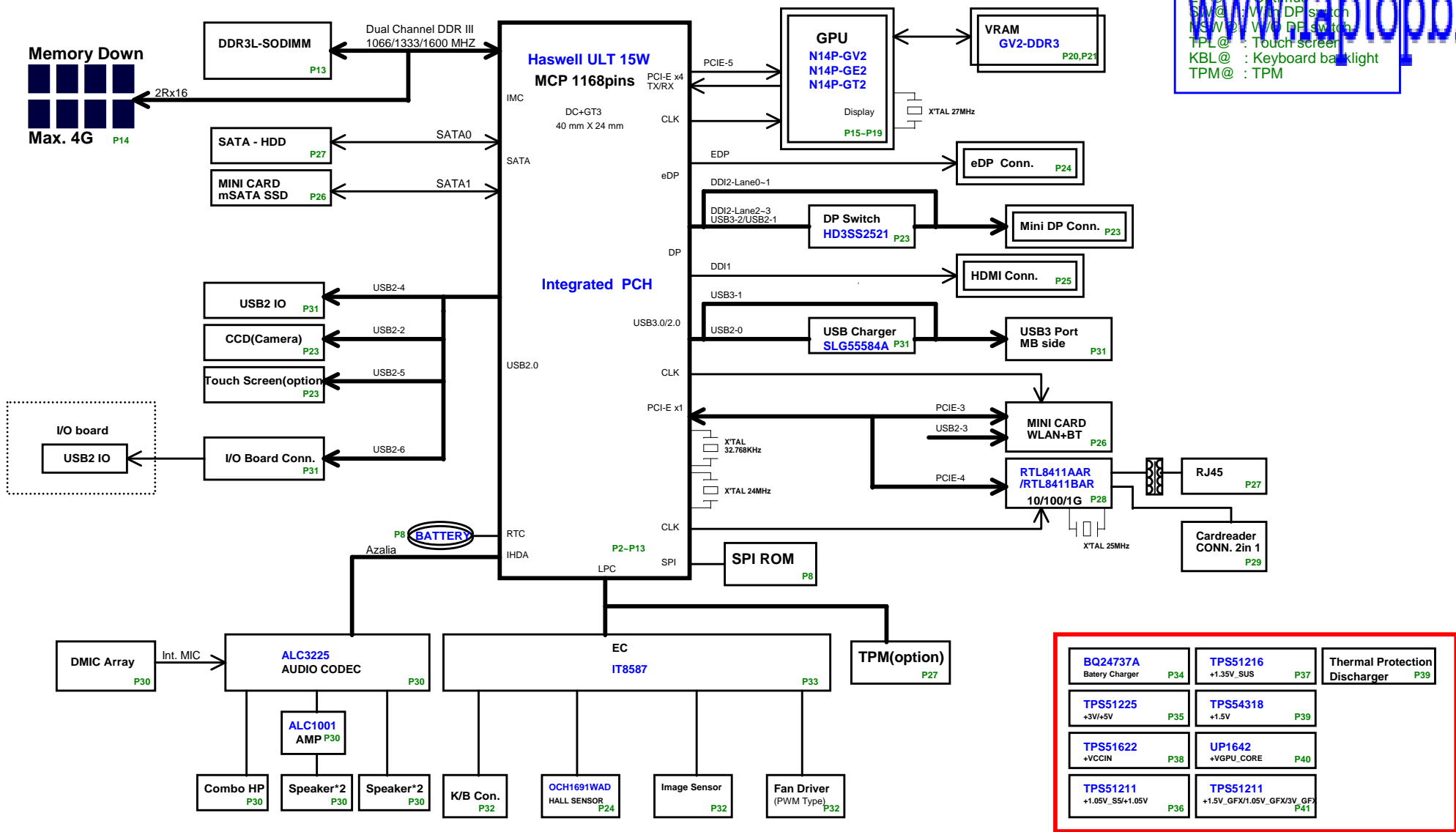
ZRQ_GDDR3_SHB_ULT_SYSTEM_BLOCK_DIAGRAM

BOM

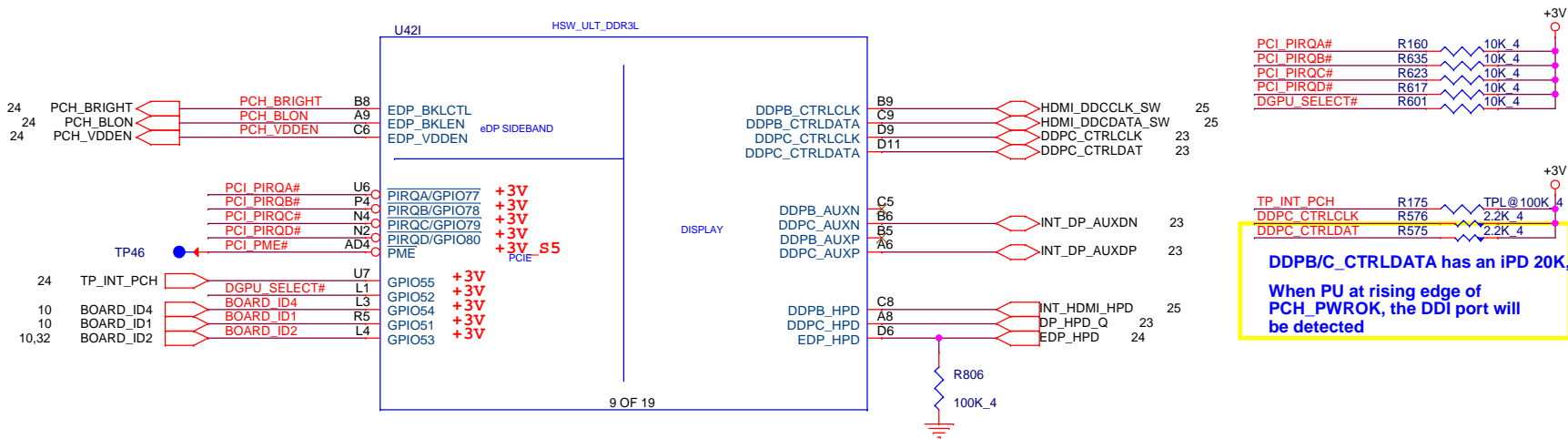
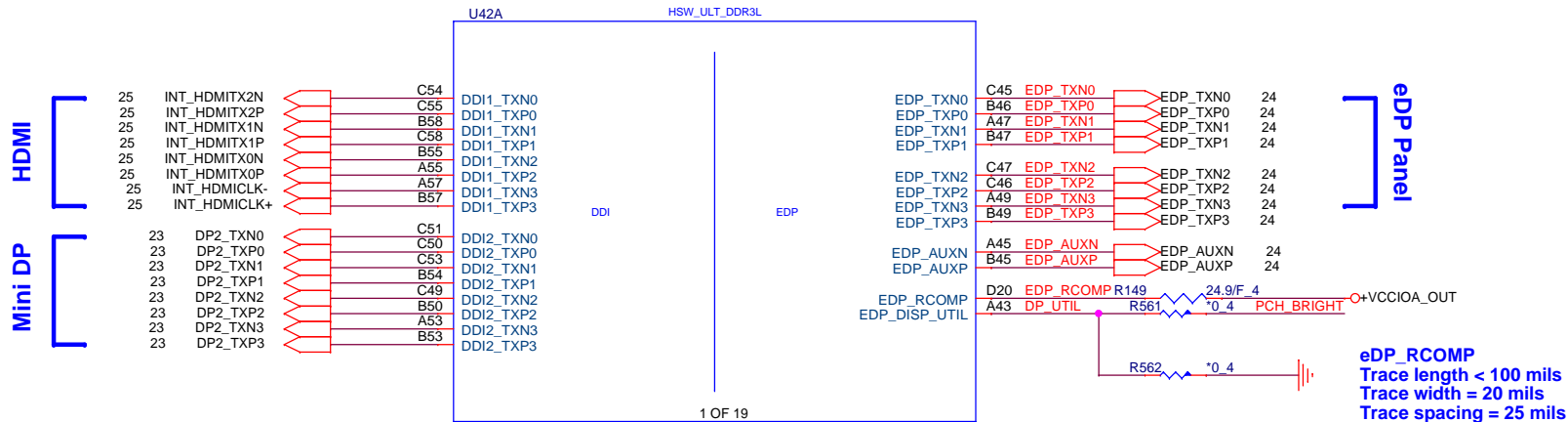
01

IV@ : iGPU
 SW@ : iGPU
 SW@ : Win DP switch
 NSW@ : Win DP switch
 TPL@ : Touch screen
 KBL@ : Keyboard backlight
 TPM@ : TPM

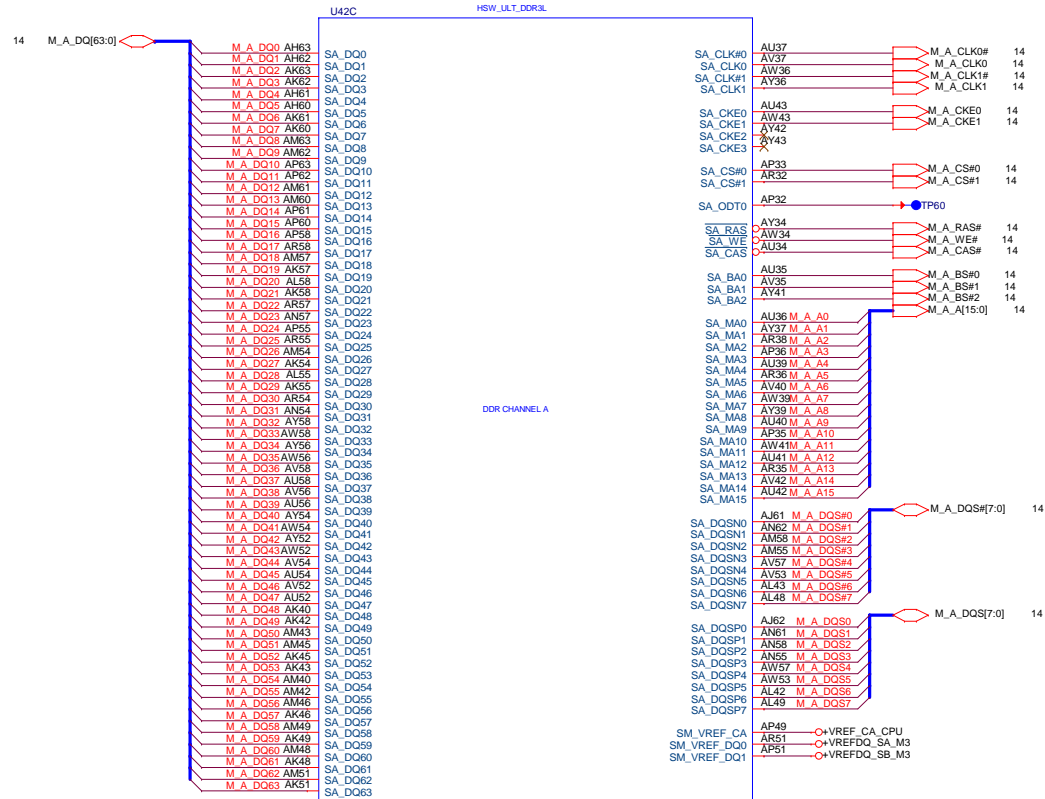
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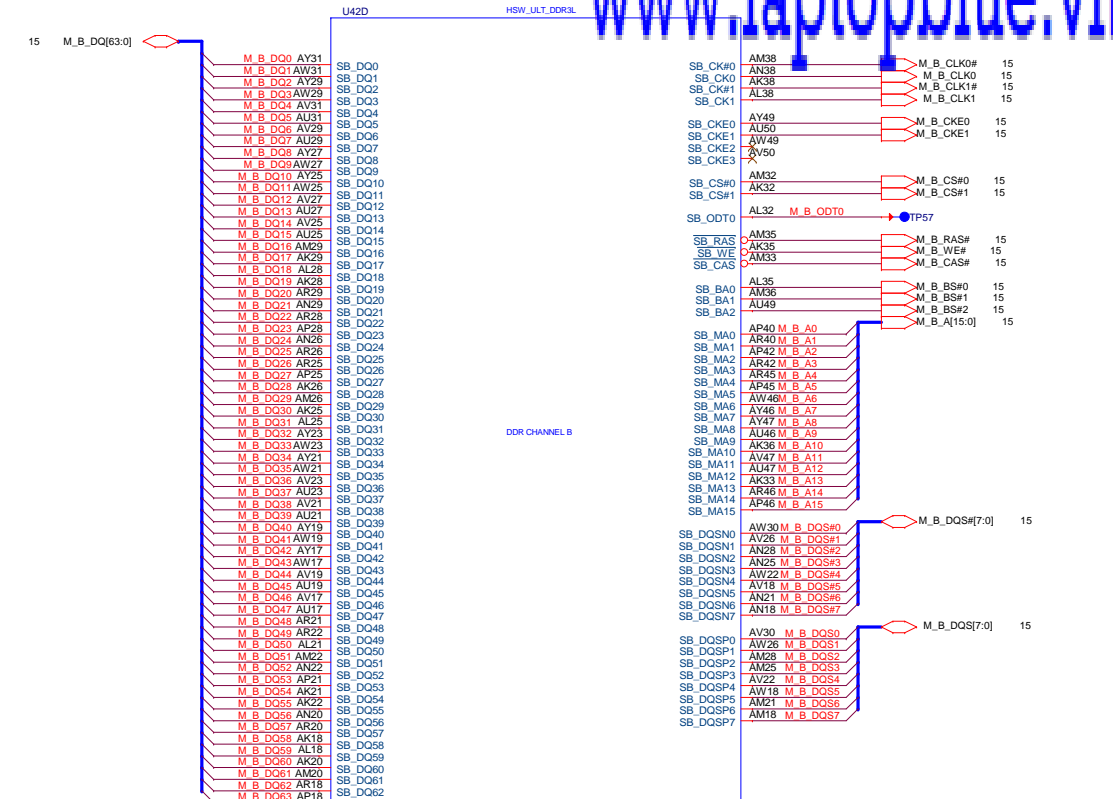
Haswell ULT (DISPLAY,eDP)



Haswell ULT (DDR3L)



Haswell Processor (DDR3)



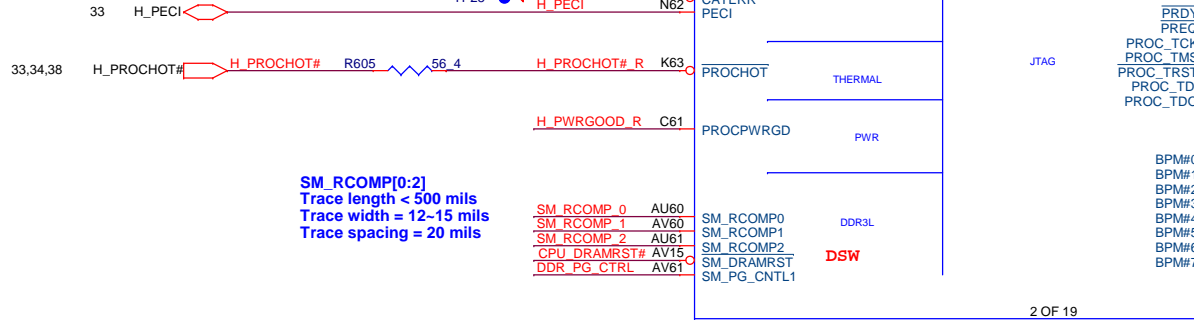
03

Haswell ULT (SIDE BAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4-6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1-11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10-17 inches

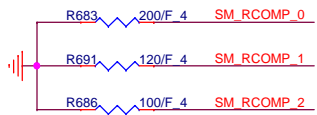


SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12-15 mils
Trace spacing = 20 mils

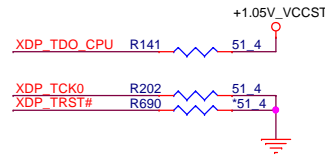
TCK,TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1-6 inches
Length match < 300 mils

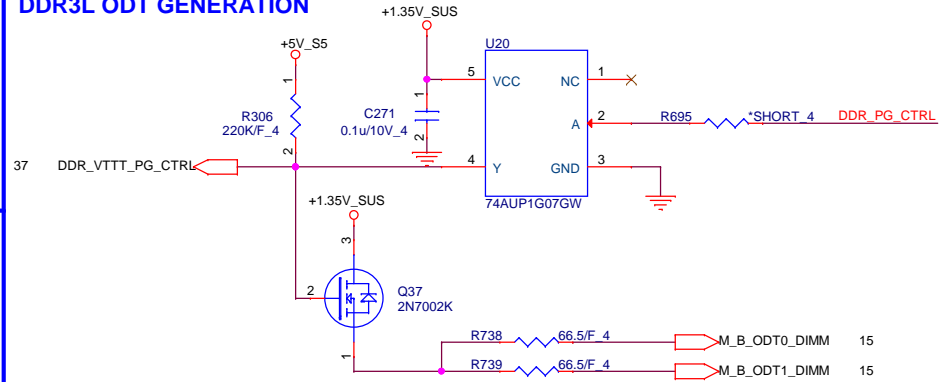
DRAM COMP



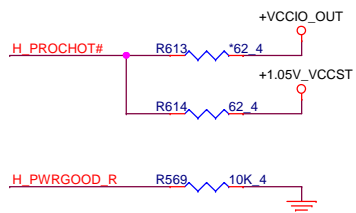
XDP PU/PD



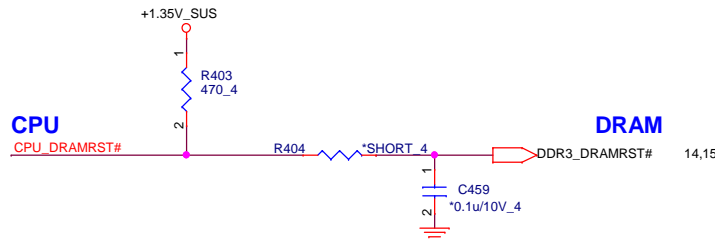
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST

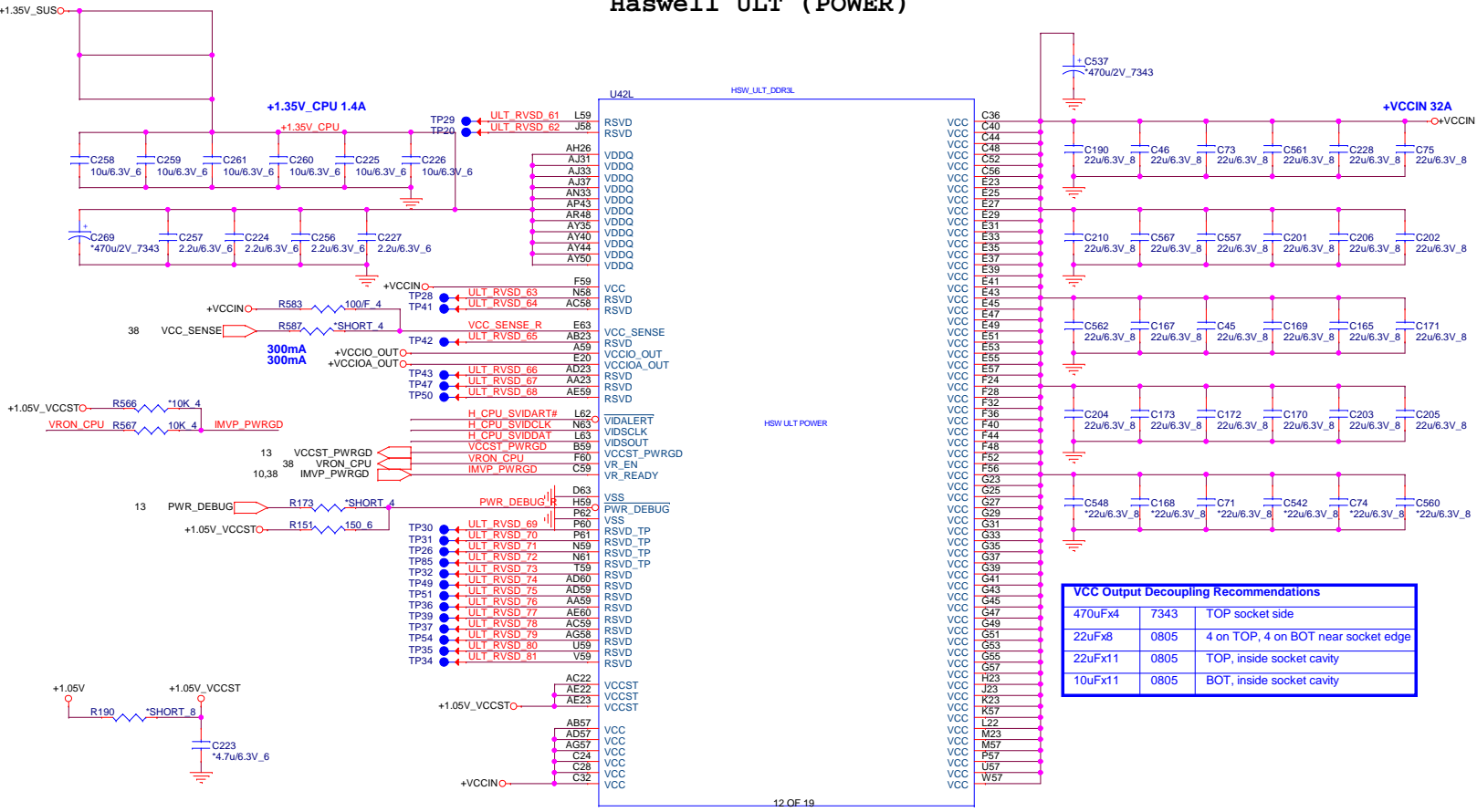


Quanta Computer Inc.

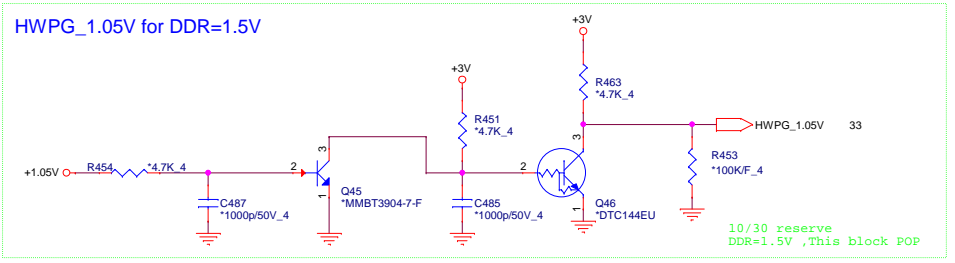
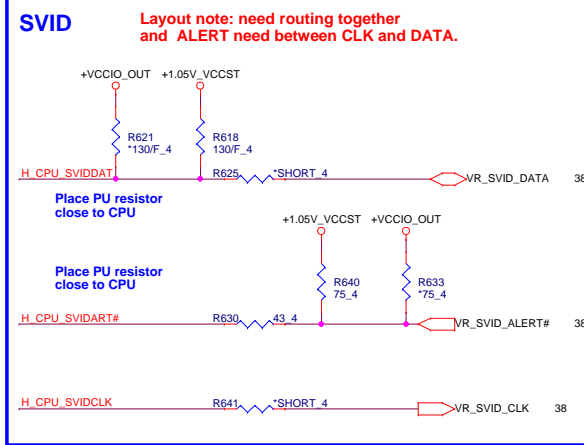
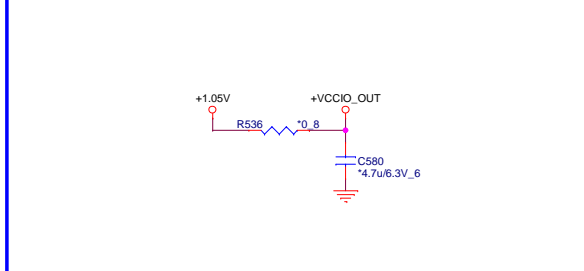
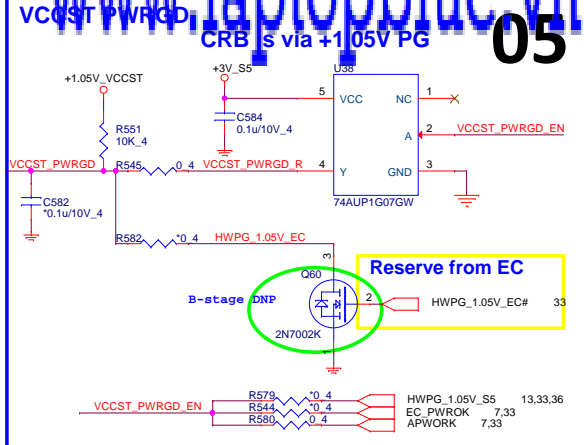
PROJECT : ZRQ

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity

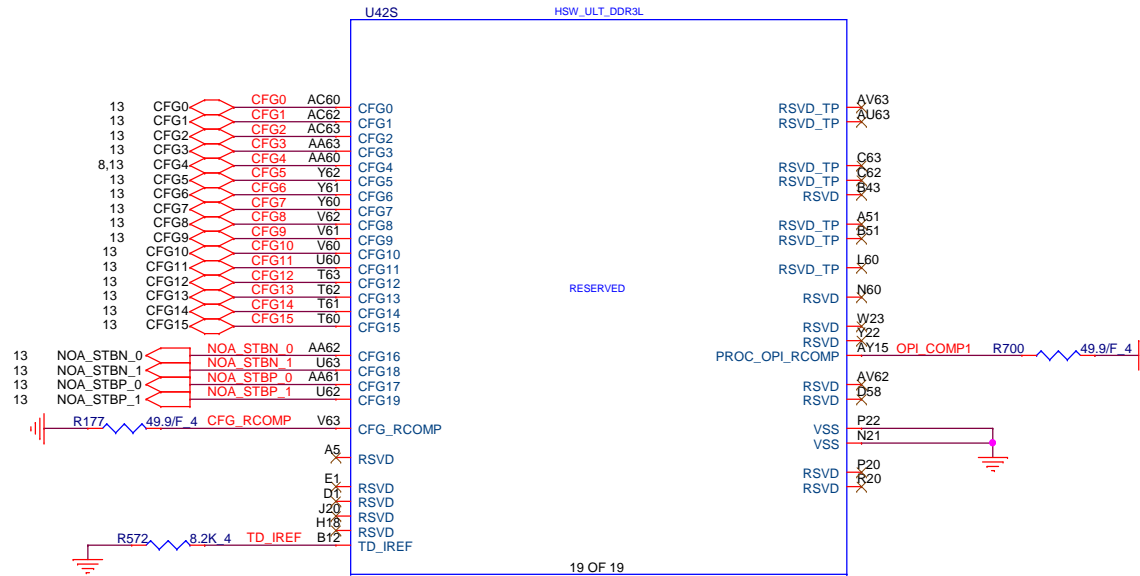
Haswell ULT (POWER)



VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity



Haswell ULT (CFG,RSVD)

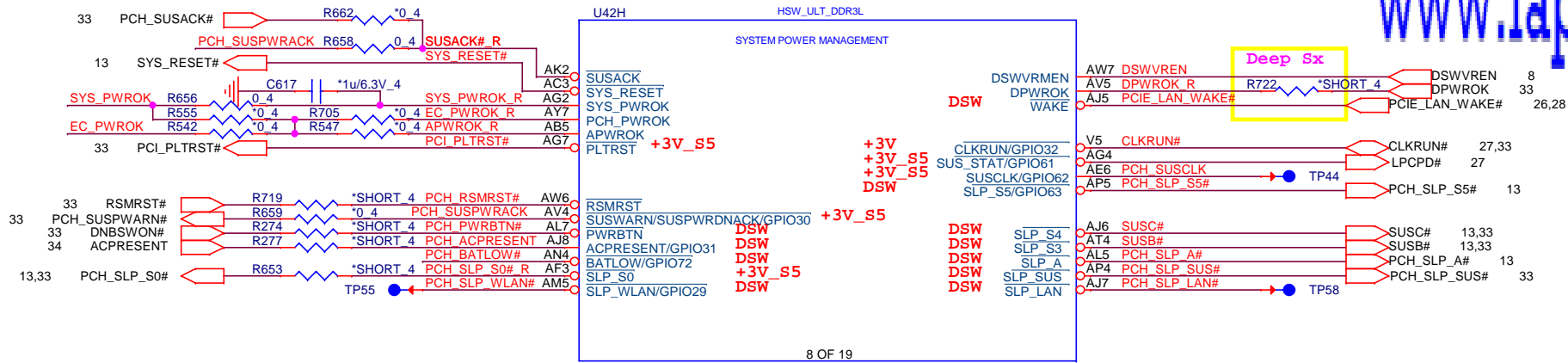


Processor Strapping

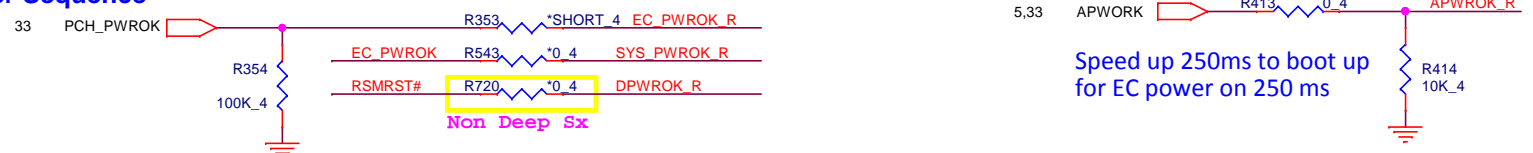
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R203 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R184 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R192 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R171 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R172 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R183 *1K 4



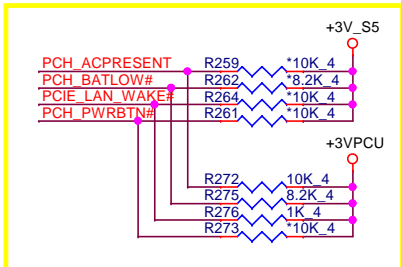
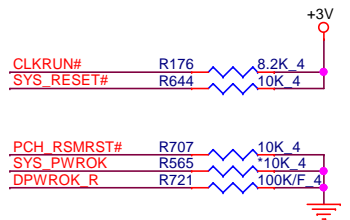
Haswell ULT PCH (PM)



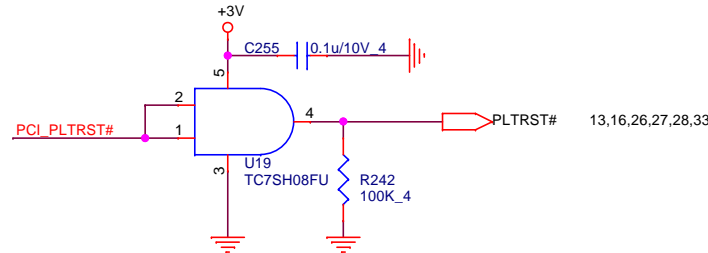
Power Sequence



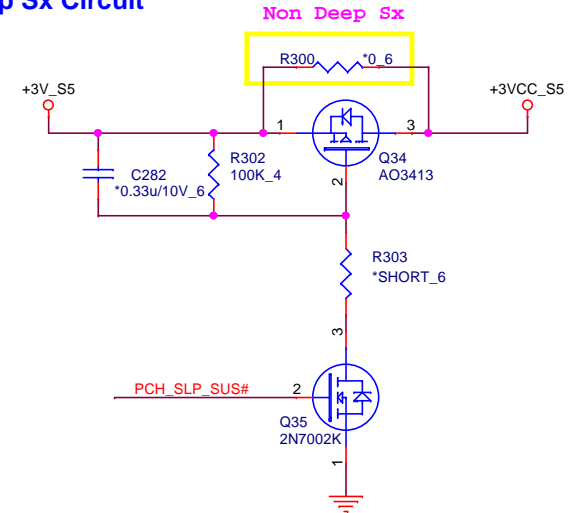
PCH PM PU/PD



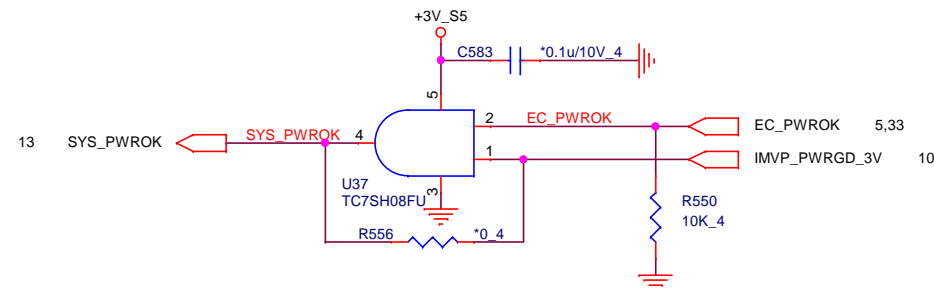
PLTRST# Buffer



Deep Sx Circuit

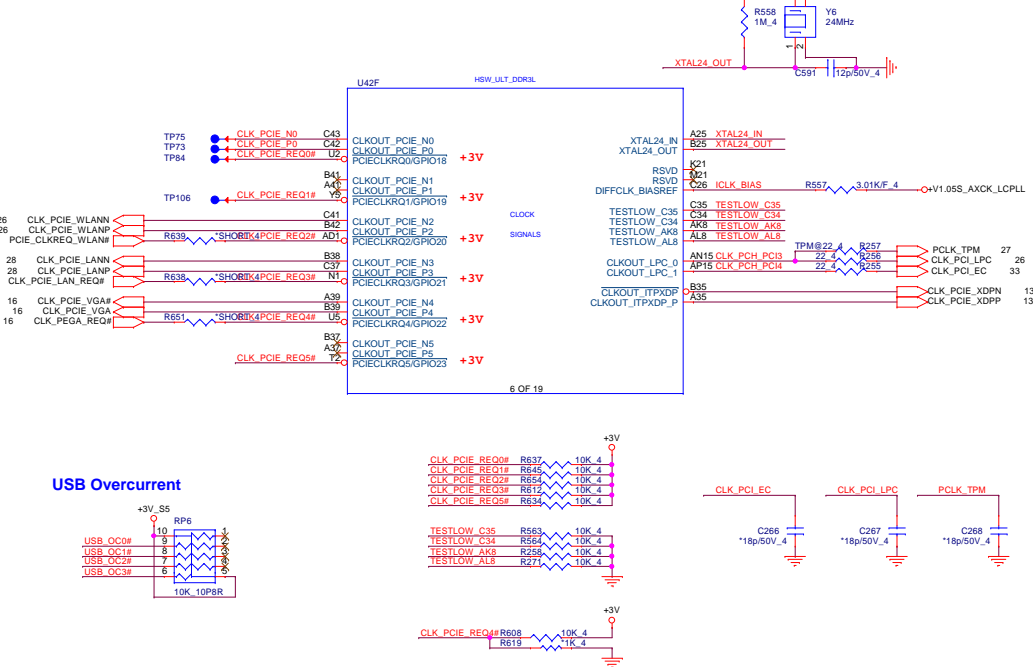
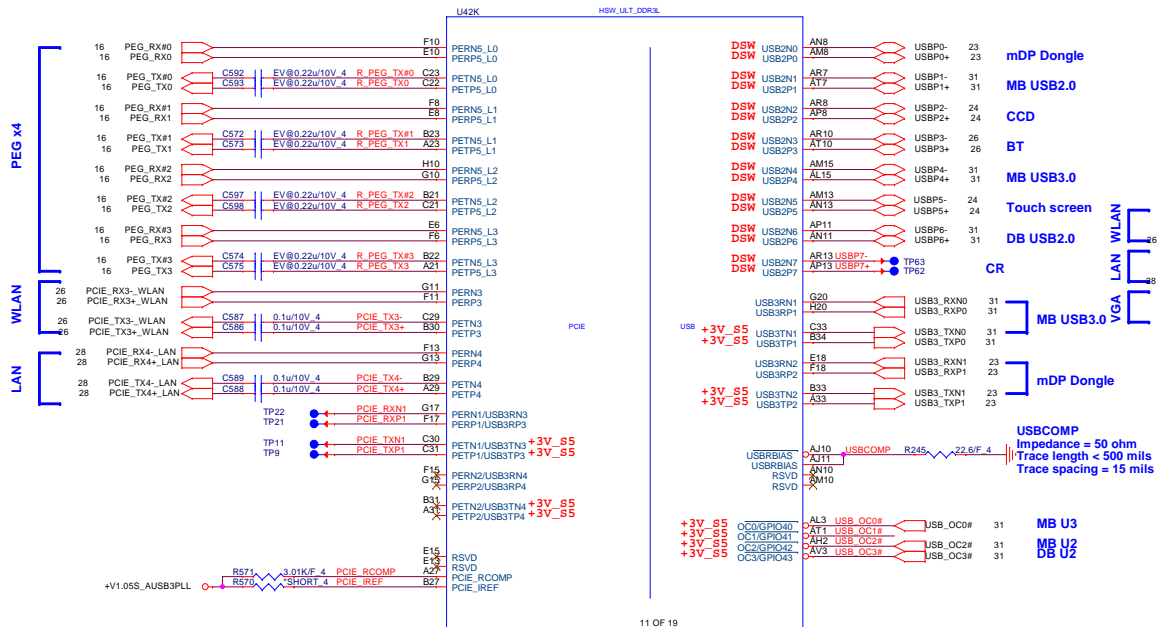


SYSPWOK

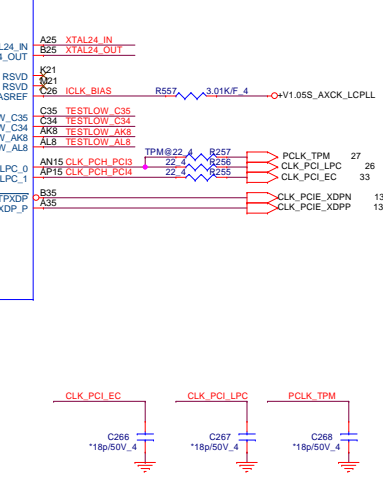
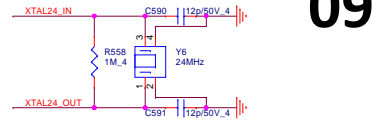
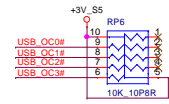


Haswell ULT PCH (PCIE,USB3.0,USB2.0)

Haswell ULT PCH (CLOCK)

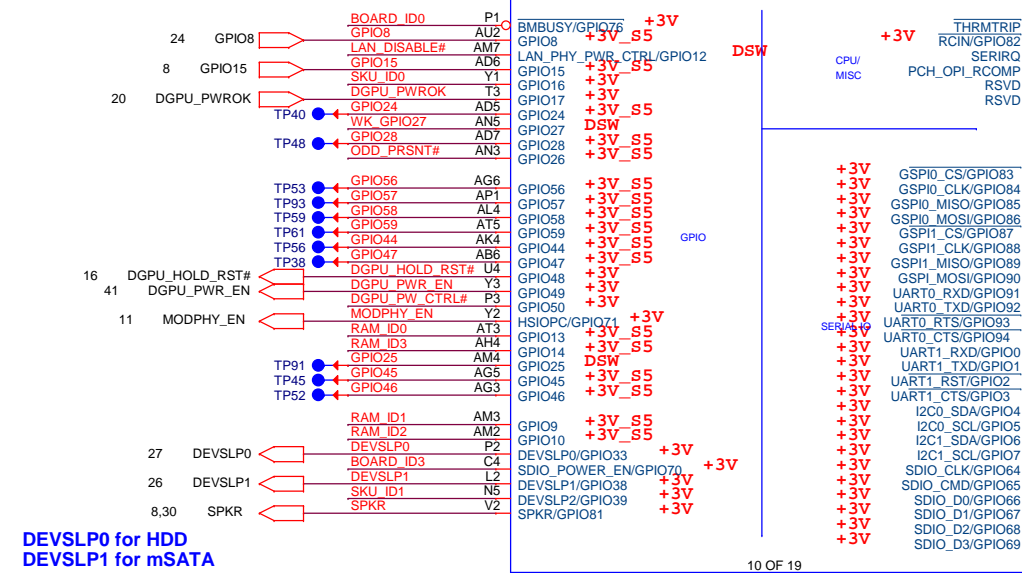


USB Overcurrent



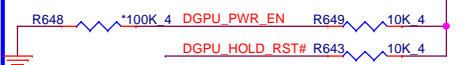
Haswell ULT PCH (GPIO, CPU/MISC, NCTF)

GPIO8	High	Low
	No touch panel	Touch panel

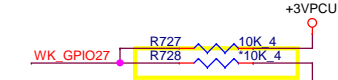
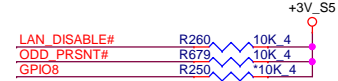
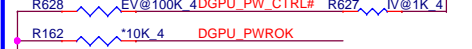


DEVSLP0 for HDD
DEVSLP1 for mSATA

IRQ_SERIRQ	R155	10K 4
DEVSLP0	R169	*10K 4
DEVSLP1	R611	*10K 4
SIO_RCIN#	R187	*10K 4
SIO_EXT_SMI#	R135	*10K 4
SIO_EXT_SCI#	R131	*10K 4
GPIO83	R206	*10K 4
GPIO84	R150	*10K 4
GPIO85	R207	*10K 4
GPIO87	R152	*10K 4
GPIO88	R208	*10K 4
GPIO89	R205	*10K 4
GPIO90	R597	*10K 4
GPIO91	R594	*10K 4
GPIO92	R209	*10K 4
GPIO93	R590	*10K 4
GPIO94	R588	*10K 4
GPIO0	R210	*10K 4
GPIO1	R589	*10K 4
GPIO2	R595	*10K 4
GPIO3	R592	*10K 4
GPIO4	R585	*10K 4
GPIO5	R586	*10K 4
GPIO64	R584	*10K 4
GPIO65	R134	*10K 4
GPIO67	R130	*10K 4
GPIO68	R128	*10K 4
GPIO69	R581	*10K 4

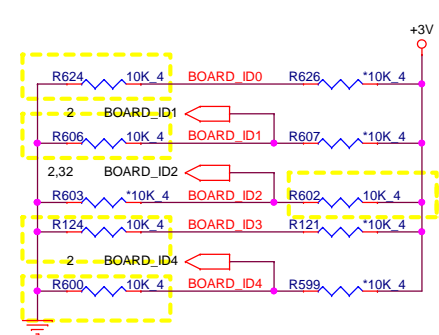


high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)



GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

Board ID



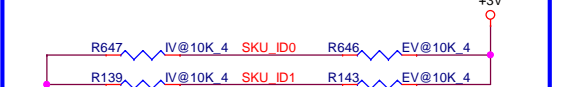
	Low	High
BOARD_ID0	DDR3	GDDR5
BOARD_ID1	Enable on board memory	Disable on board memory
BOARD_ID2	Pin8 of SYNAPTICS and ELAN are NC pin. BIOS maybe will use EEPROM detection. Default is pull high.	
BOARD_ID3	Reserved (Default)	Reserved
BOARD_ID4	Reserved (Default)	Reserved

RAM ID



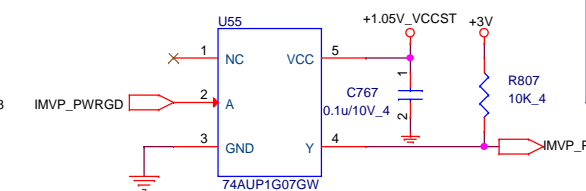
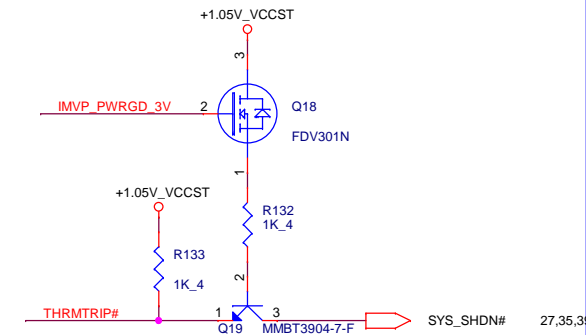
Vender	RAM_ID	Q PN	Mfr. PN	Freq.
Hynix	0000	AKD5JGETW04	H5TC4G63AFR-PRBA	1600MHz
Elpida	0001	AKD5JGST400	EDJ4216EBBG-DJ-F	1333MHz
Elpida	0010	AKD5JGST404	EDJ4216EFBG-GN-F	1600MHz

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip

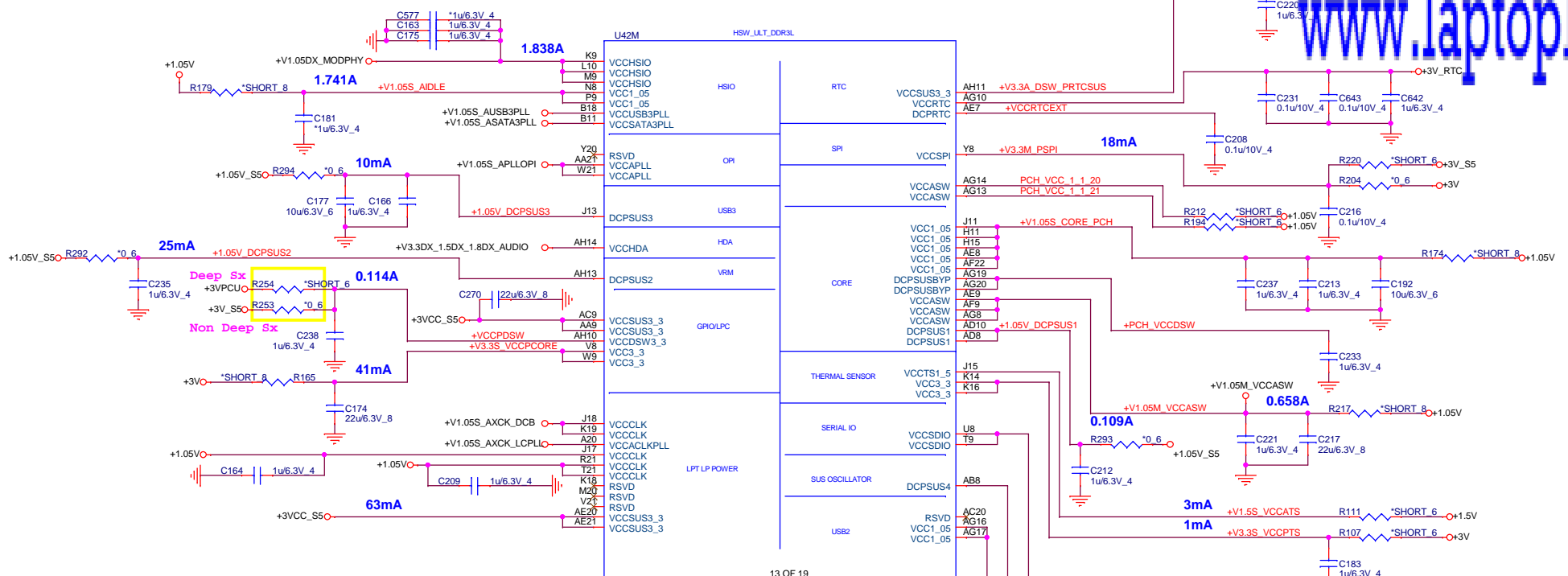


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PROJECT : ZRQ

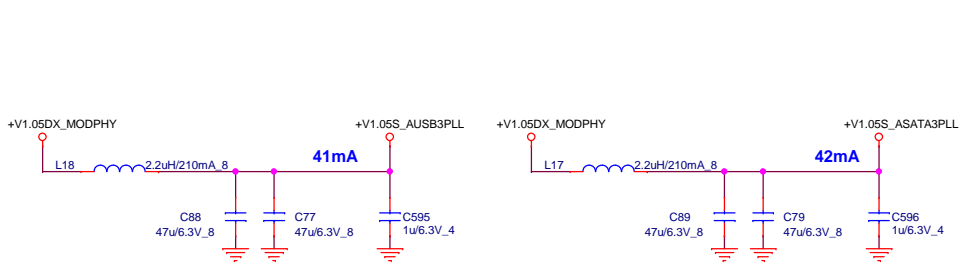
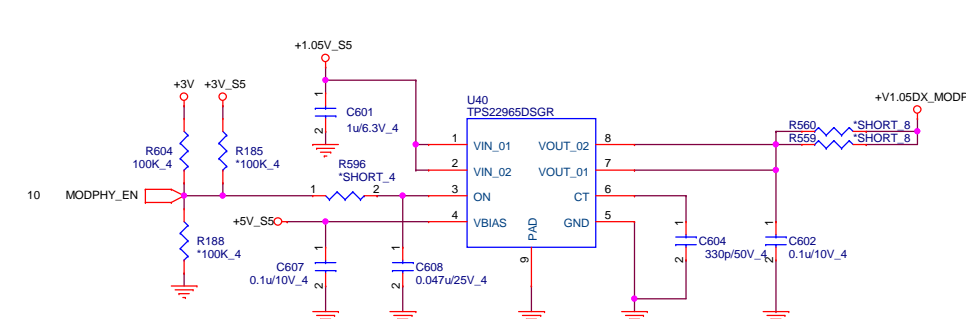
Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	3A
Date:	Monday, April 08, 2013	Sheet 10 of 47

Haswell ULT PCH (Power)

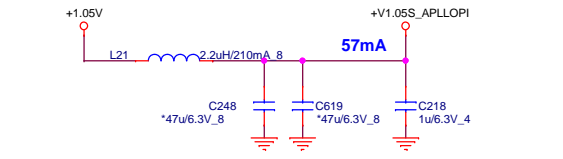
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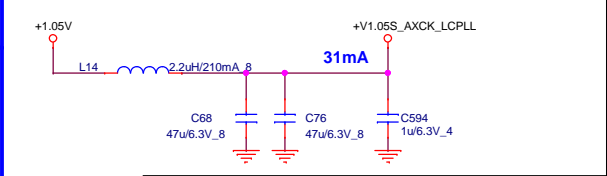
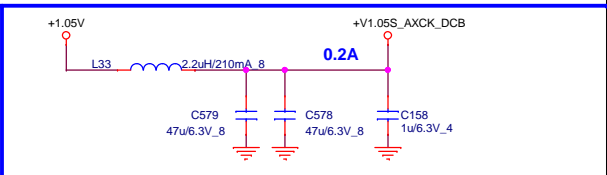
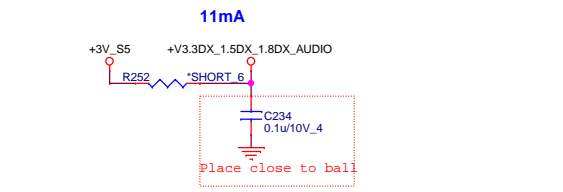
PCH VCCHSIO Power



VCCAPLL power



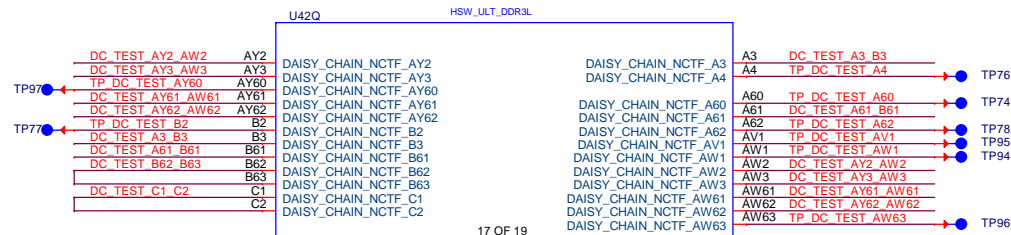
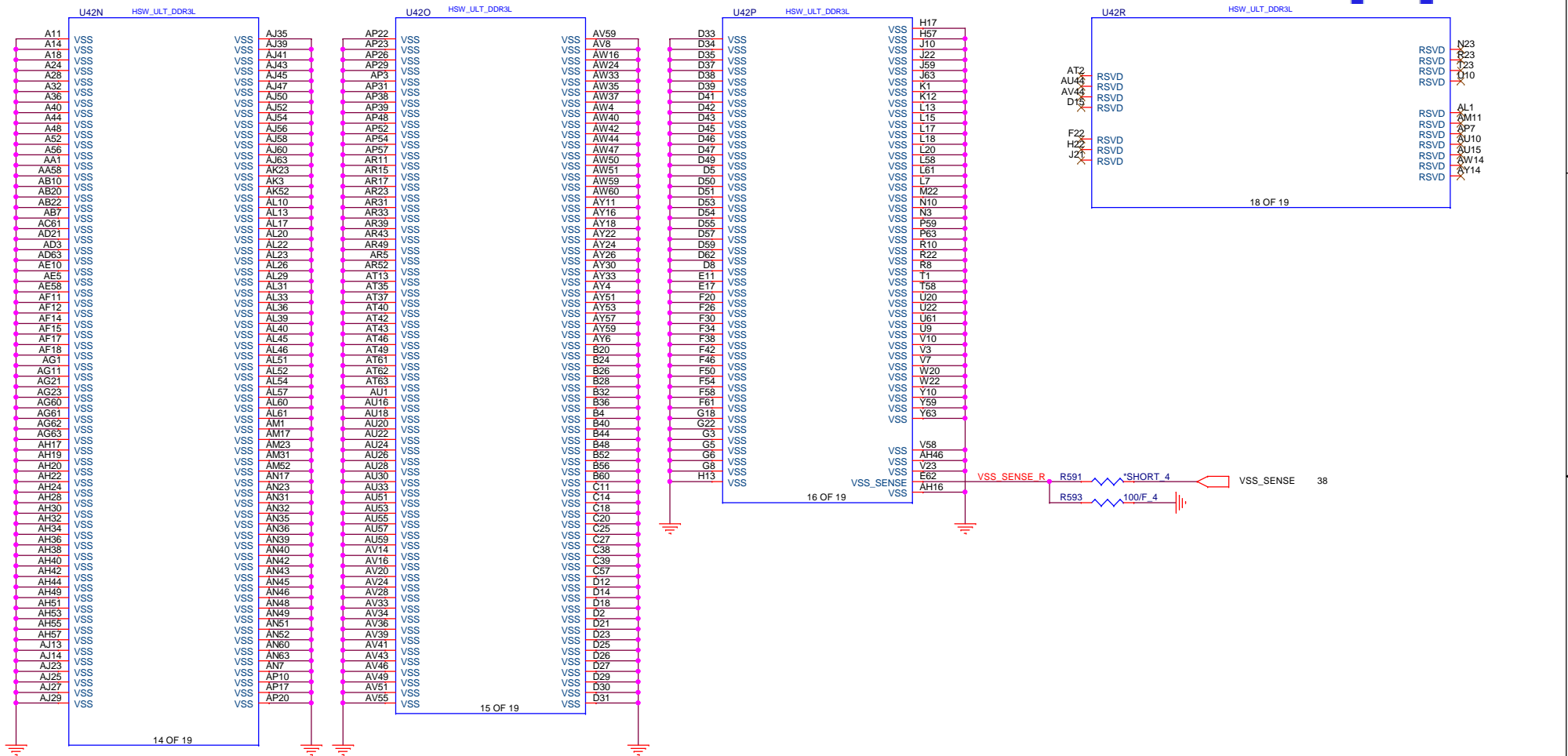
PCH HDA Power



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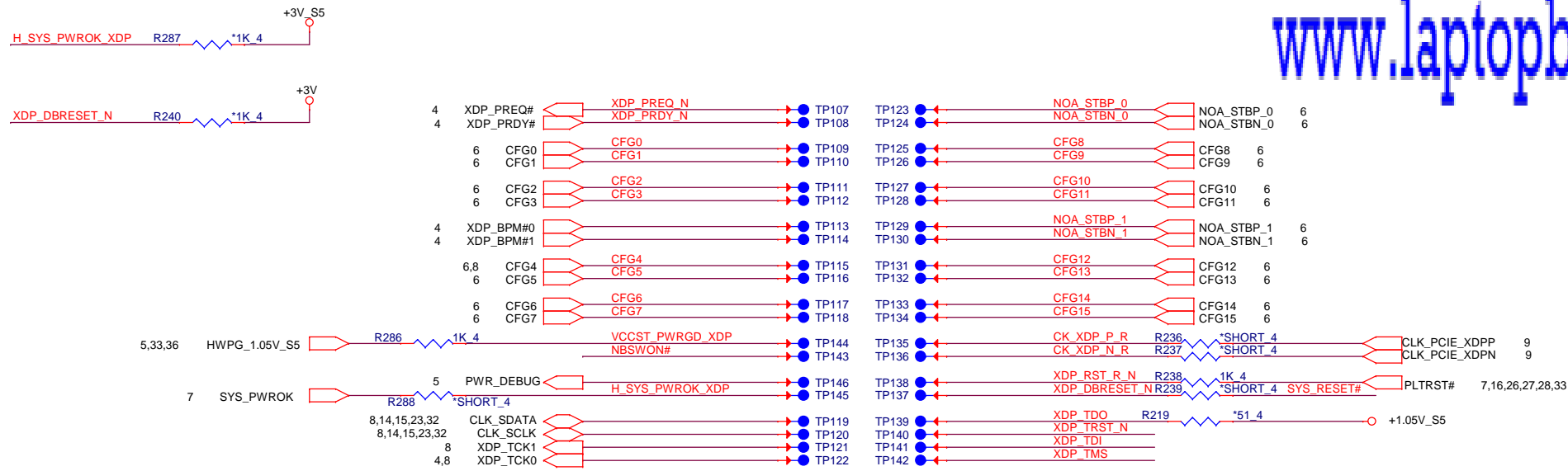
Size	Document Number	Rev
	LPT 5/6 (POWER)	3A
Date:	Monday, April 08, 2013	Sheet 11 of 47

Haswell ULT (GND)

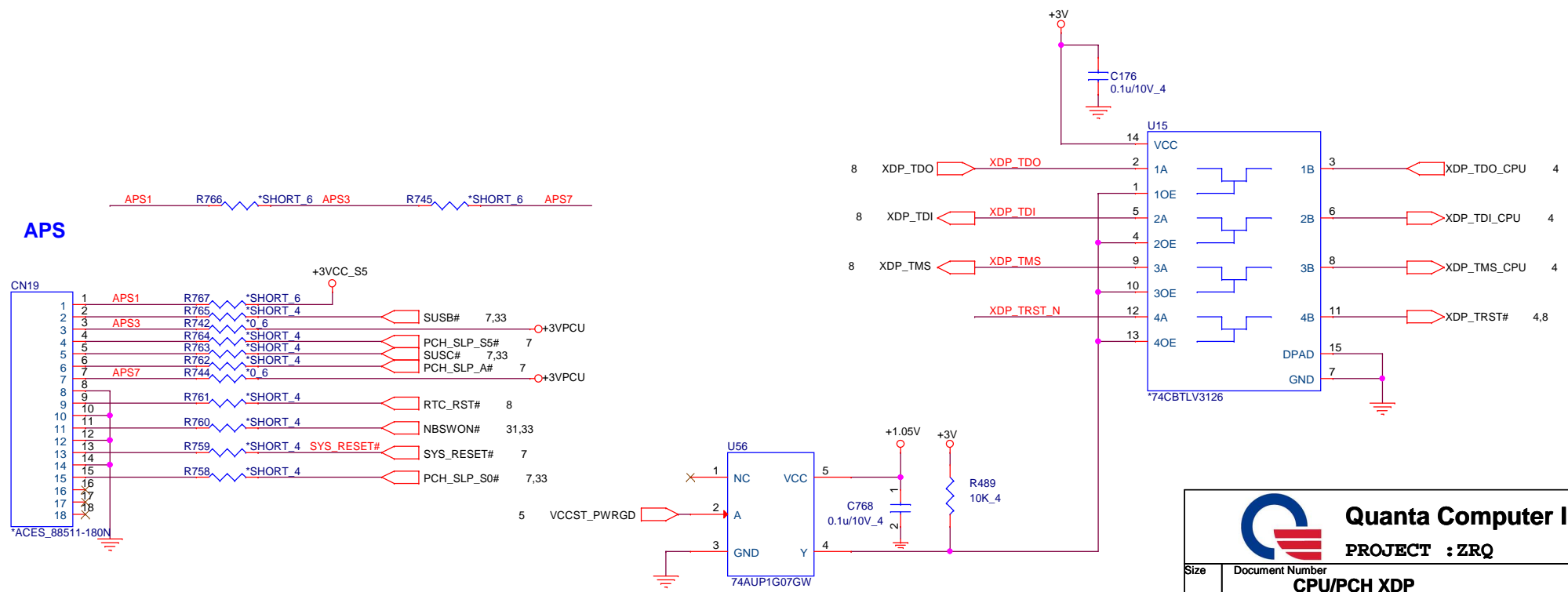


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PROJECT : ZRQ

Size	Document Number	Rev
	LPT 6/6 (GND)	3A
Date:	Monday, April 08, 2013	Sheet 12 of 47

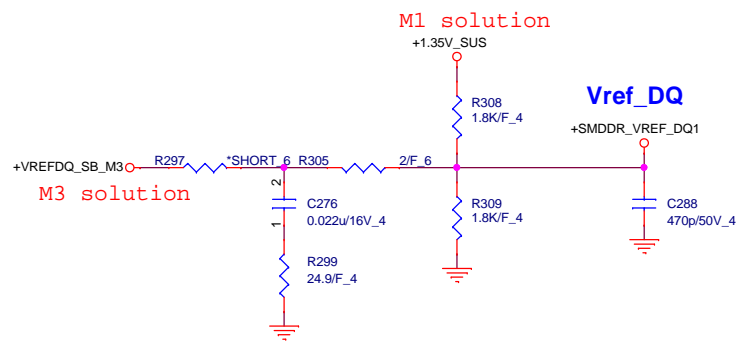
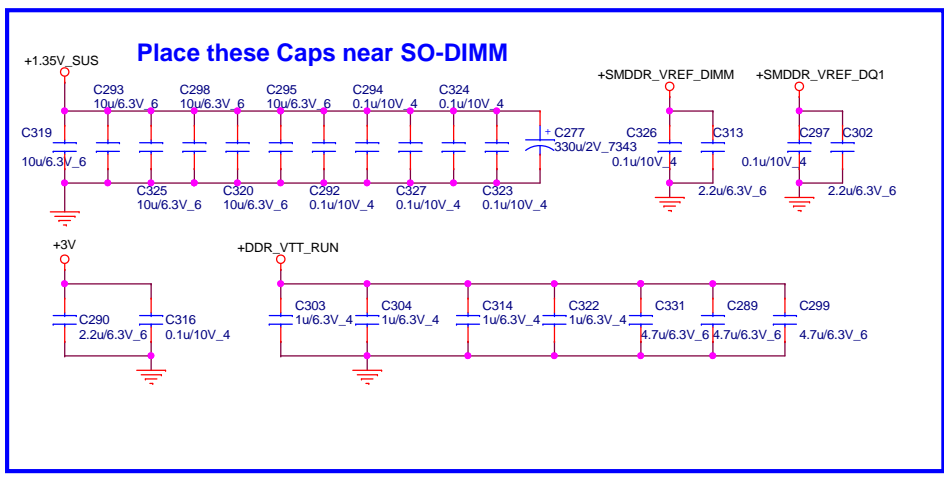
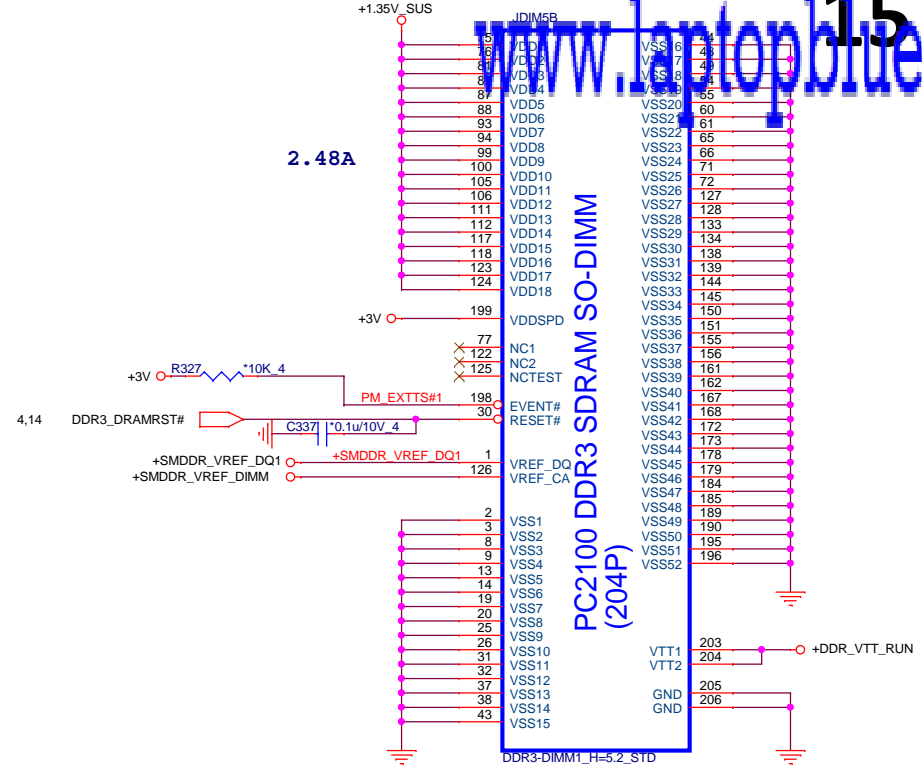
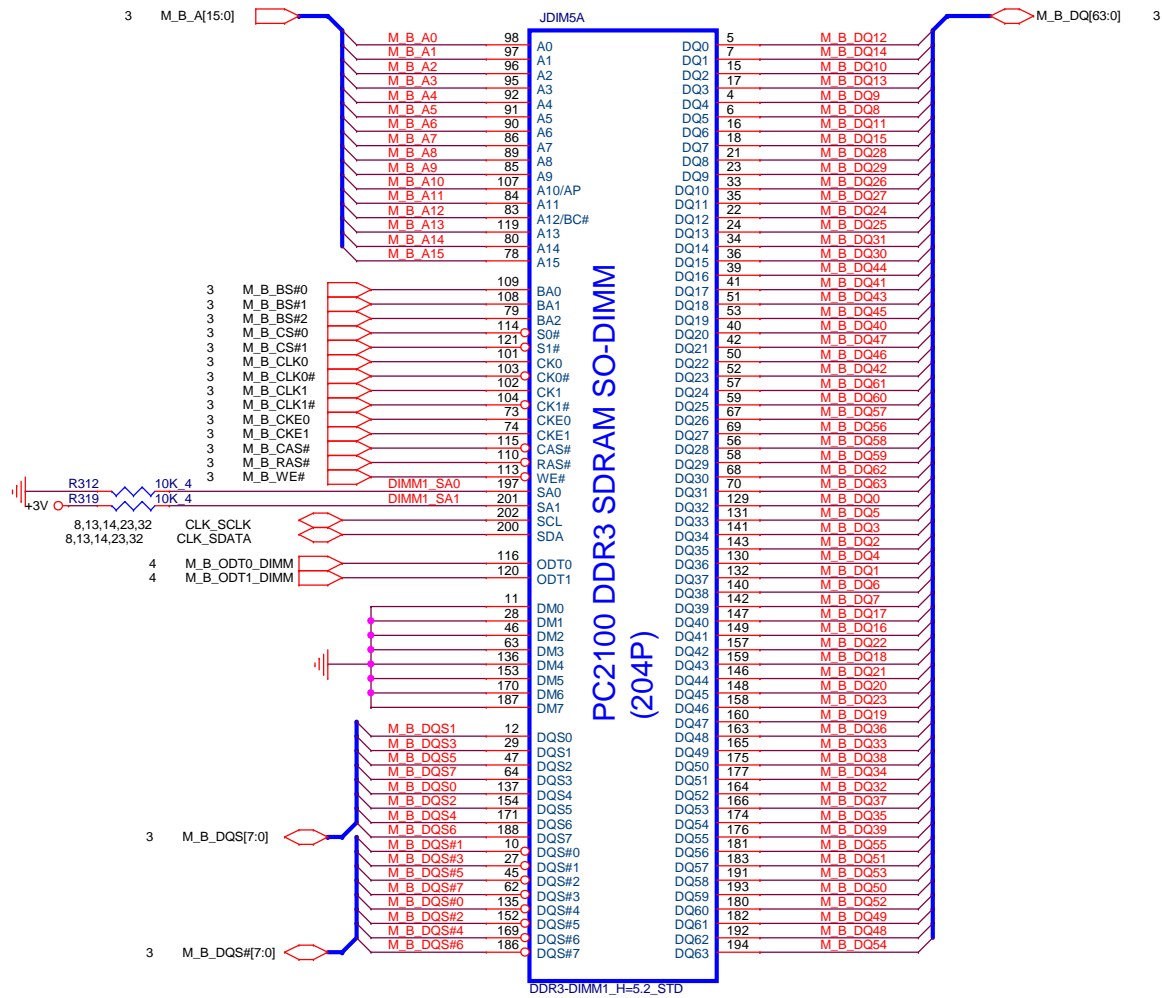


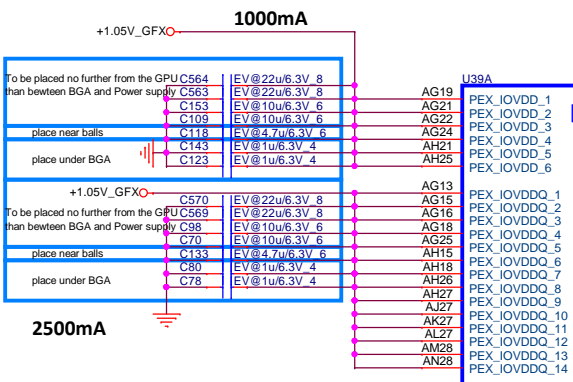
APS



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PROJECT : ZRQ

Size	Document Number	Rev
	CPU/PCH XDP	3A
Date:	Monday, April 08, 2013	Sheet 13 of 47





[PEG Interface]

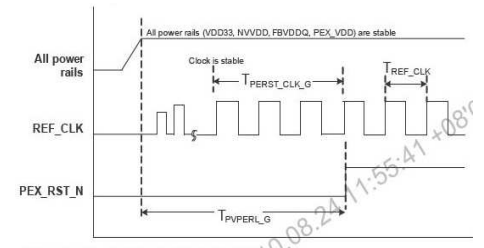
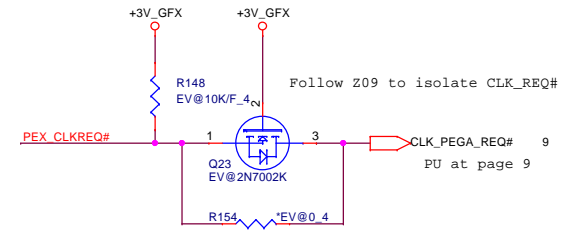
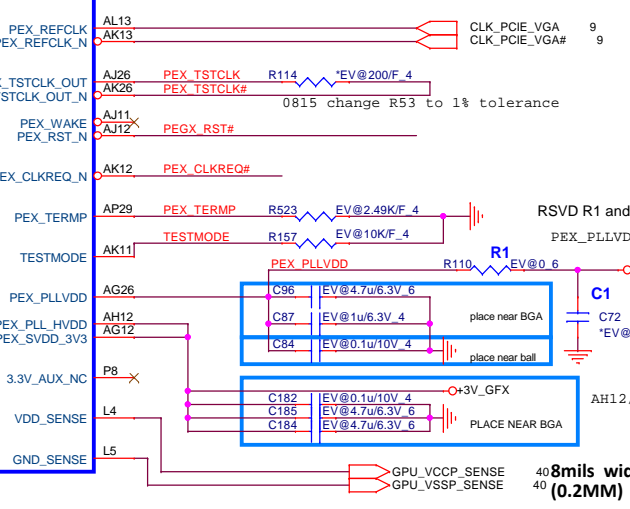
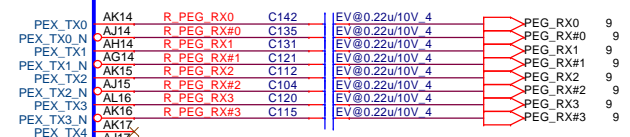
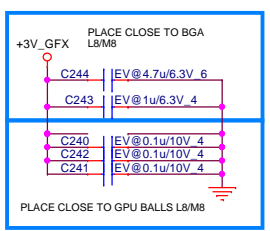
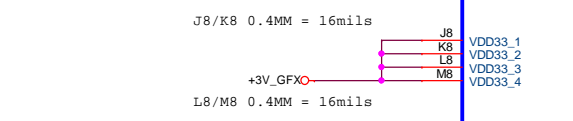
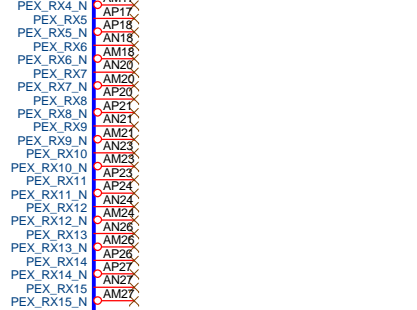
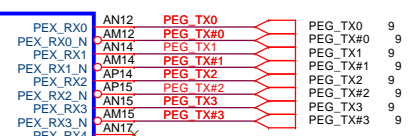
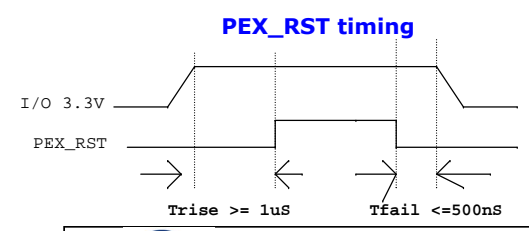
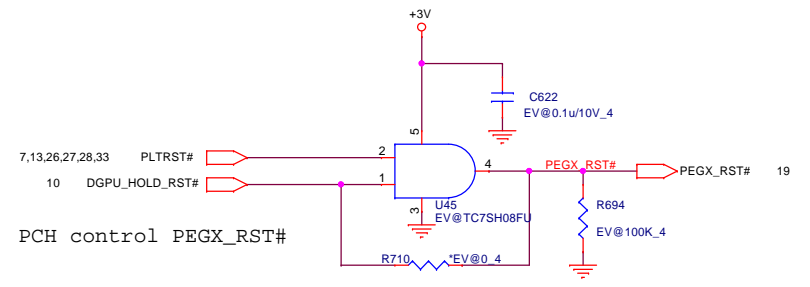
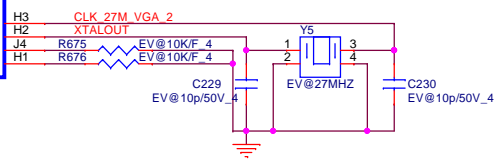
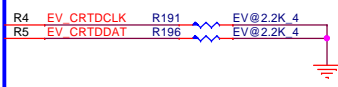
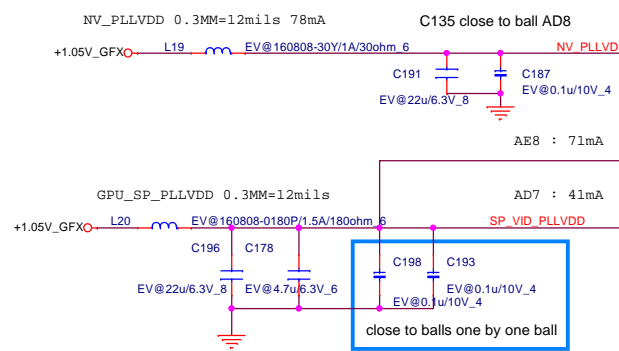
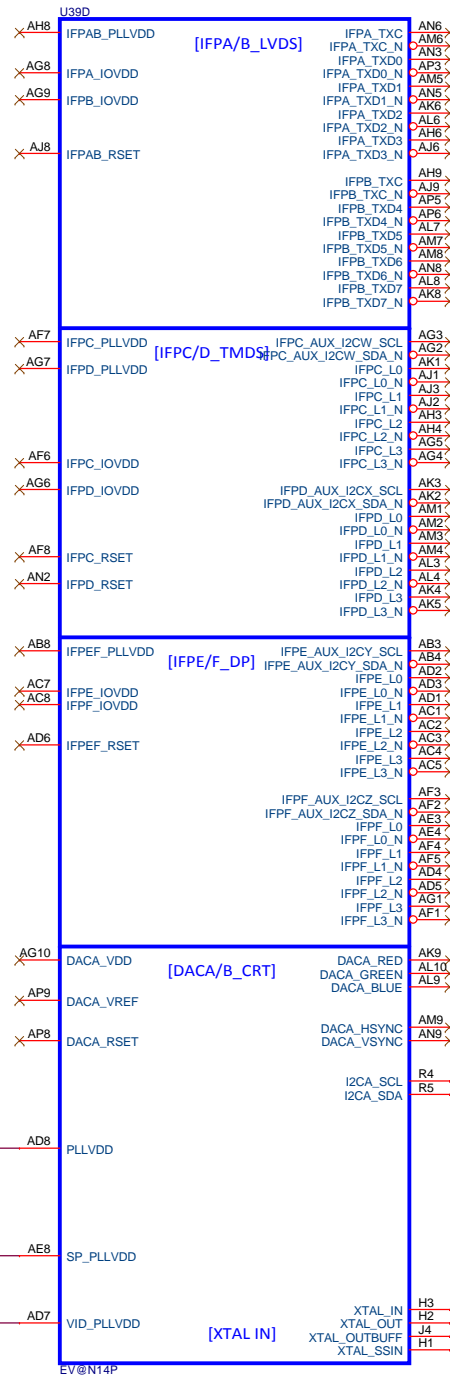


Figure 3-18. PEX_RST_N Timing for GPU
Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
$T_{FPVPERL_G}$	$T_{FPVPERL_G} \geq 103$	
$T_{PERST_CLK_G}$	$T_{PERST_CLK_G} \geq 1T_{REF_CLK}$	



N14P-GV2	
N14P-GT	



Quanta Computer Inc.
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Size	Document Number	Rev
	DGPU 3/5 (Display)	3A
Date:	Monday, April 08, 2013	Sheet 18 of 47

N14P-GV2	
N14P-GT	

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

STRAP3 Optimus --> 4.99k PD Discrete only --> 15K PD
Resistor P/N
4.99K --> CS24992FB26
10K --> CS31002FB26
15K --> CS31502FB24
20K --> CS32002FB29
24.9K --> CS32492FB16
30.1K --> CS33012FB18
34.8K --> CS33482FB22
45.3K --> CS34532FB18

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLN_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN#	PCIE_MAX_SPEED	DP_PLL_VDD33	0111

	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N14P_GV	L_10K	H_4.99K	H_4.99K	H_45.3K	L_45.3K	L_15K	L_4.99K	L_45.3K
N14P_GE	L_10K	L_10K	L_10K	H_10K	H_10K	L_10K	L_10K	L_10K
N14P_GT	L_10K	H_4.99K	L_15K	H_45.3K	L_4.99K	L_24.9K	L_4.99K	L_45.3K

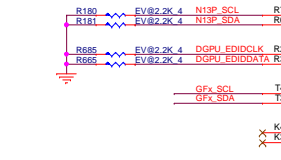
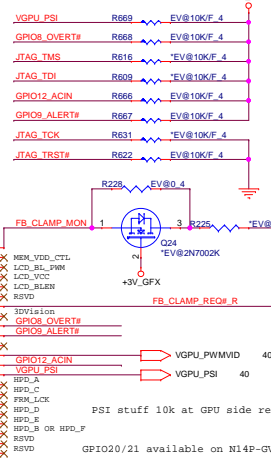
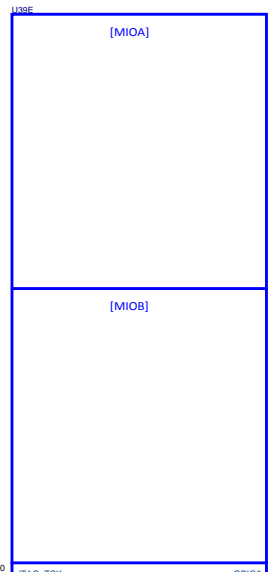
A.ROM_SI - MEMORY STRAP
B.ROM_SO - 5K pull high

D.STRAP 0 - 45k pull high
E.STRAP 1 - 5K pull down
F.STRAP 3 - 5k pull down

C1.For N14P-GT sku
N14P-GT device ID=0x0FE4
1.ROM_SCLK = 15K pull down
2.STRAP2 = 25K pull down
3.STRAP4 = 45k Pull down

C.For N14P-GV2 sku
N14P-GV2 QS device ID=0x1292
1.ROM_SCLK = 5K pull high
2.STRAP2 = 15k pull down
3.STRAP4=45 pull down
//For N14P-GV2 QS

N14P-GV2 ES device ID=0x12AD
1.ROM_SCLK = 15K pull down
2.STRAP2 = 30k pull high
3.STRAP4=10K pull down
//For N14P-GV2 ES



R3	
N14x others	40.2K
N14M-GE/GL	NC

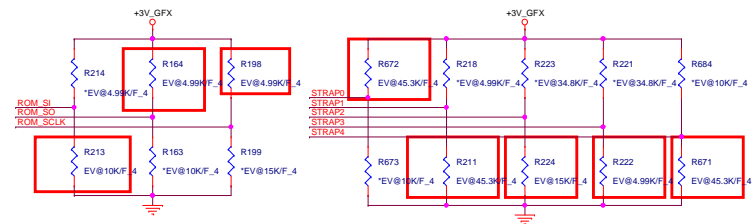
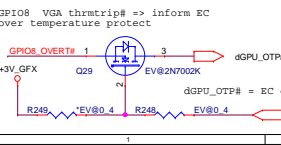
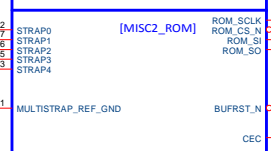
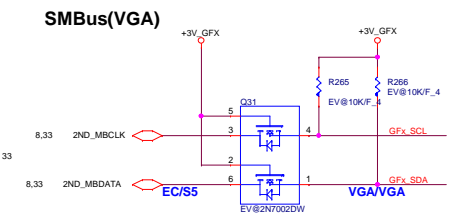
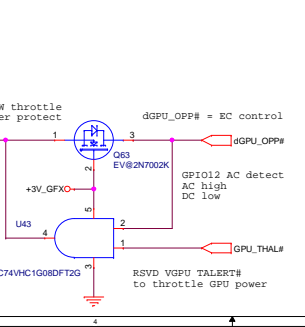


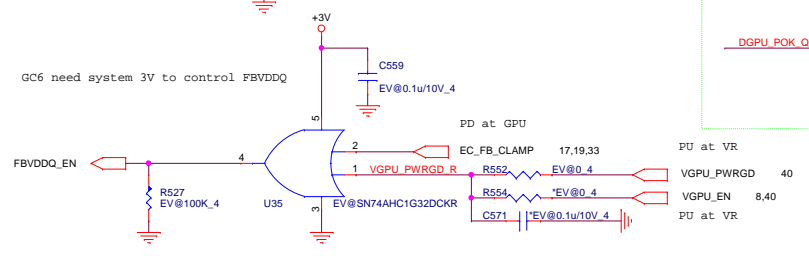
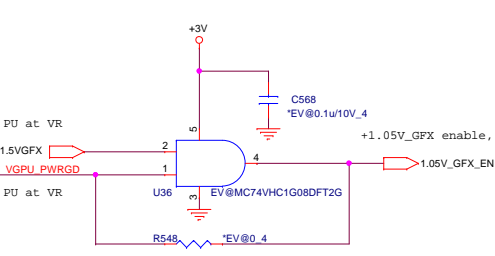
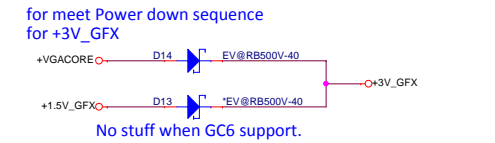
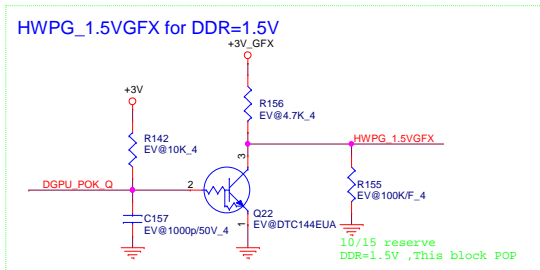
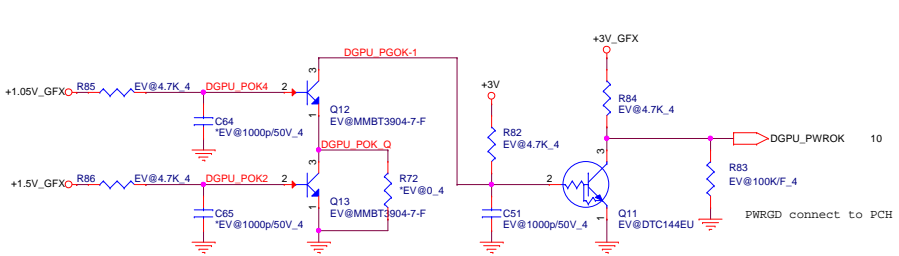
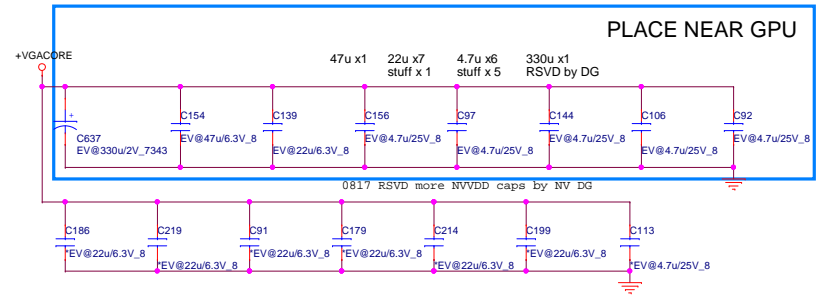
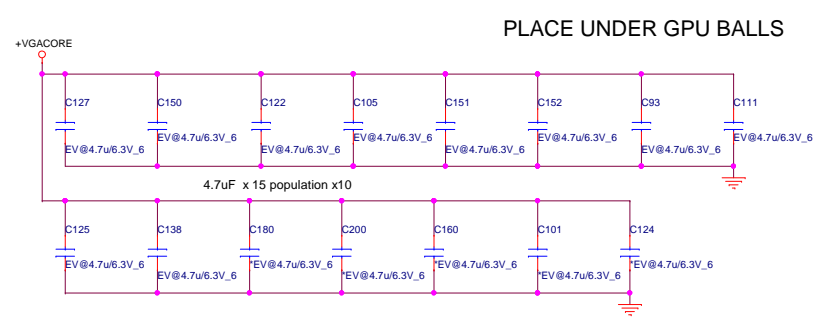
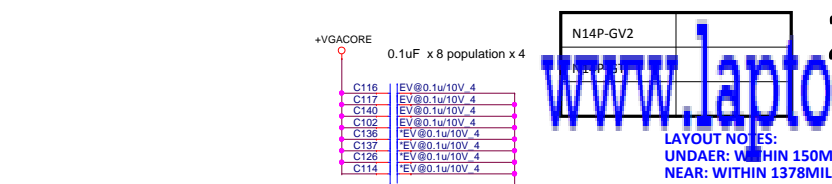
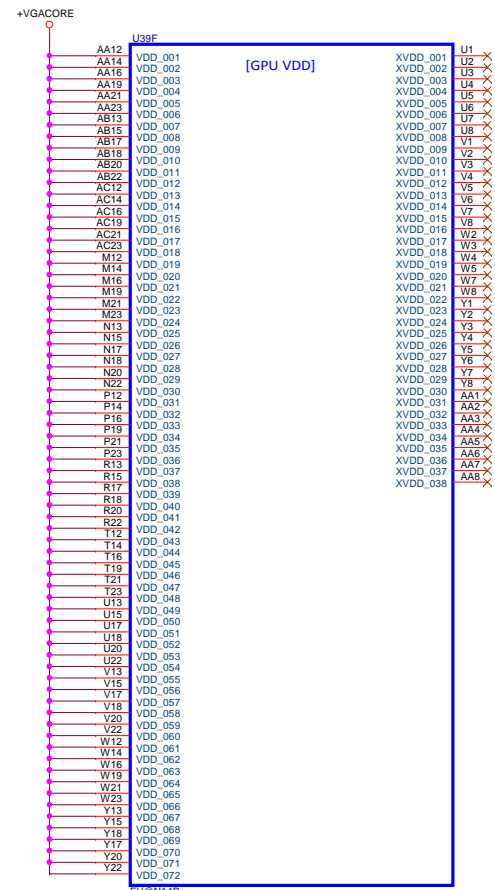
Table 9. N14P-GV/GT/GS/LP/GE GDDR5 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x4	1.5 V / 1.5 V	H5GQ2H24AFR-T2C	2500	N/A	Production Candidate
		0x6	1.35V / 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production Candidate
	Samsung	0x5	1.5 V / 1.5 V	K4G20325FD-FC04	2500	1219	Production Candidate
		0x7	1.35V / 1.35V	K4G20325FD-FC04	2000	1219	Production Candidate

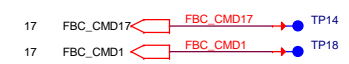
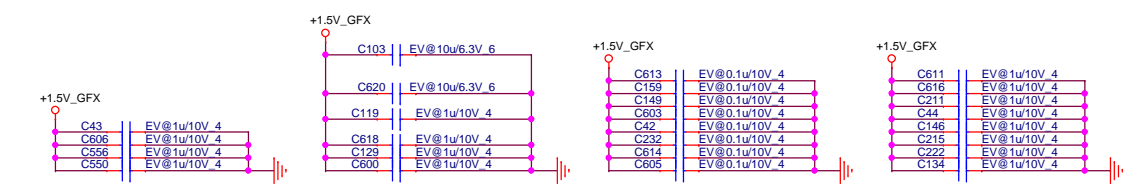
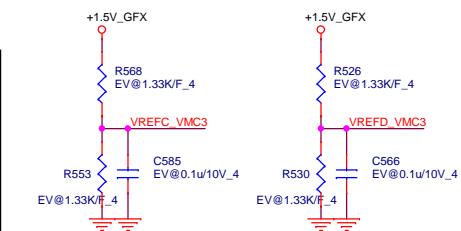
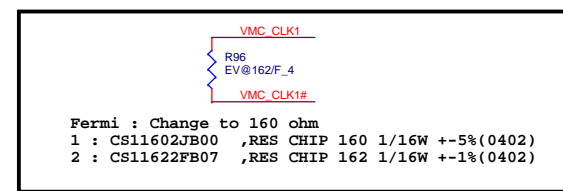
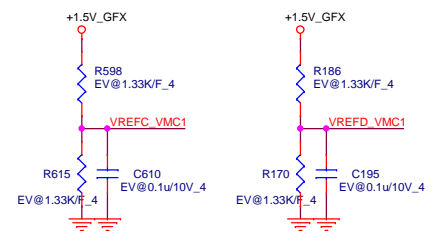
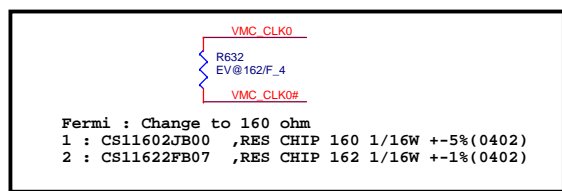
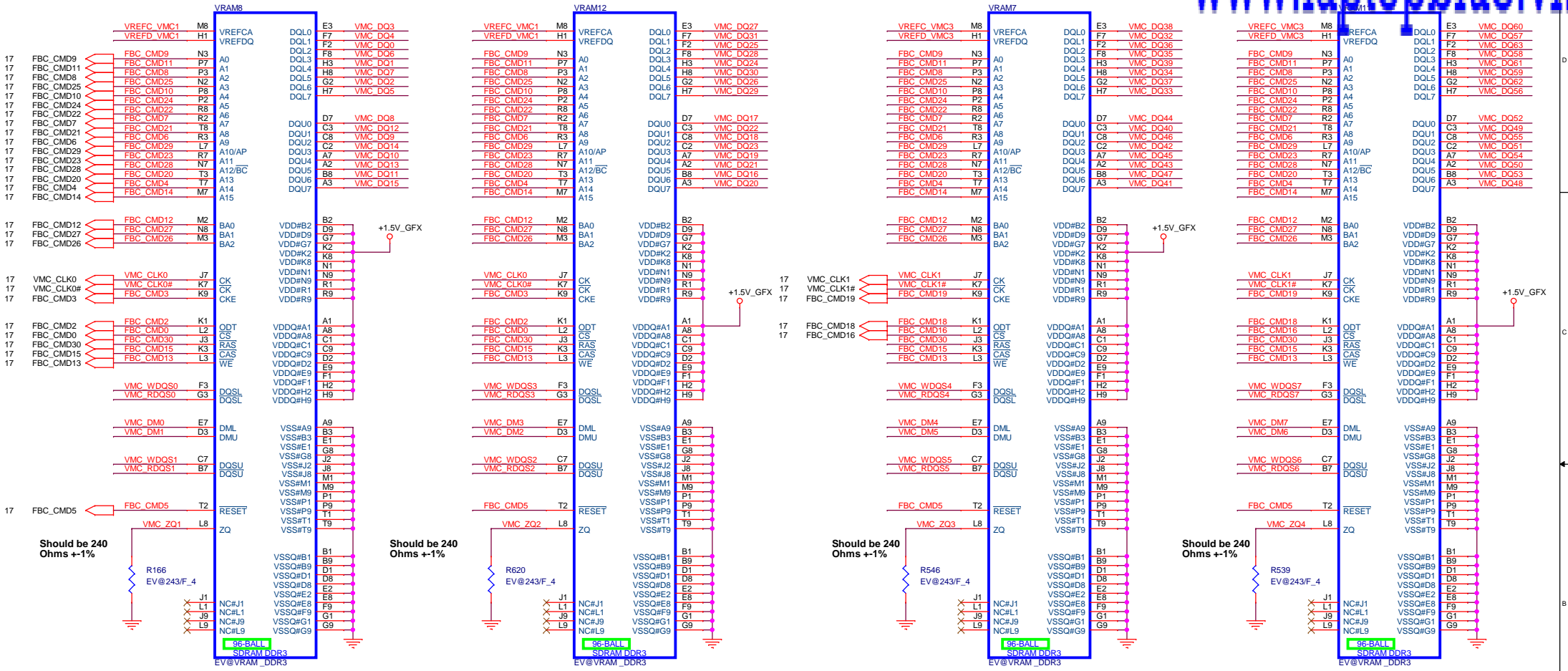
Vendor	P/N	Mfr. P/N	ROM_SI
Hynix	AKG5MUTW13	H5GQ2H24AFR-T2C	0100
Samsung		K4G20325FD-FC04	0101

PSI stuff 10k at GPU side ready, remove power page of pu 10k



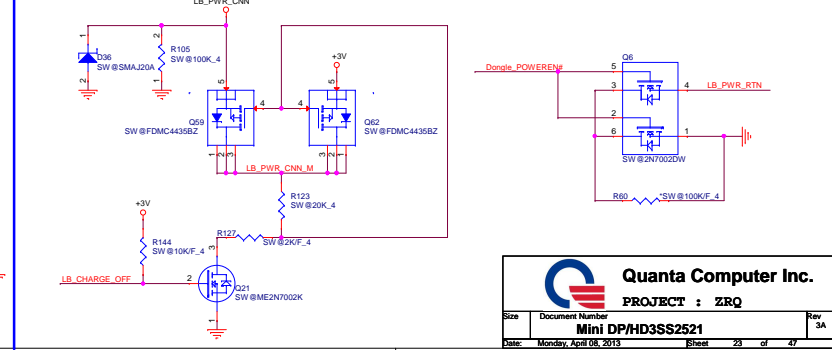
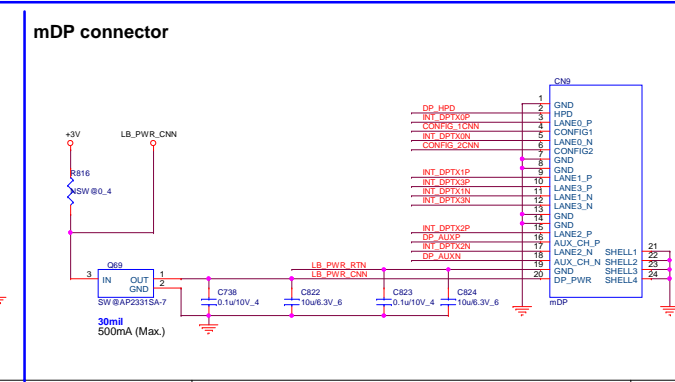
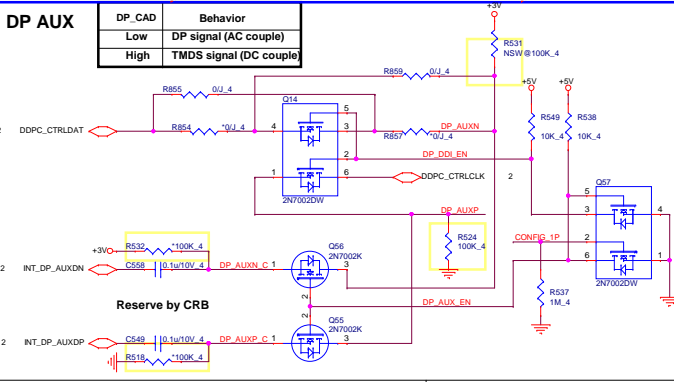
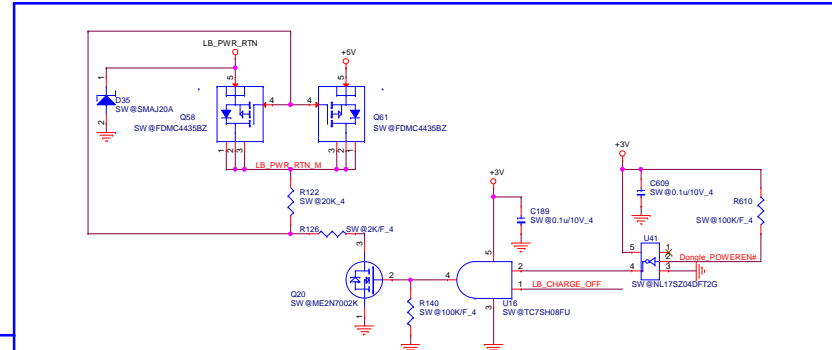
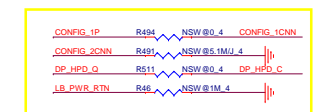
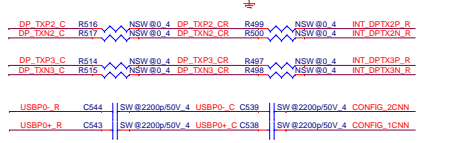
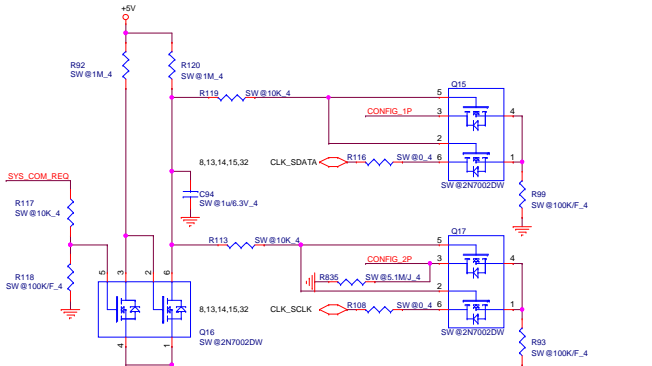
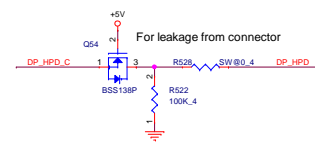
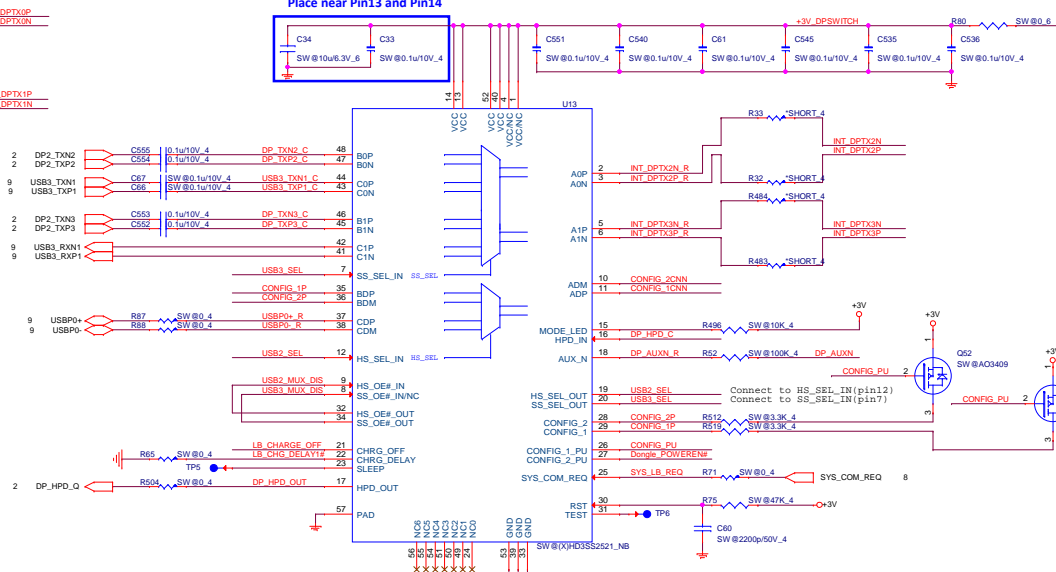
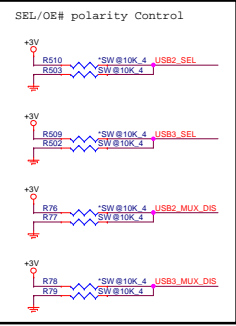
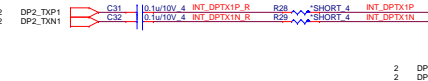
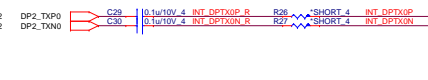


CHANNEL B: 1024MB DDR3X16

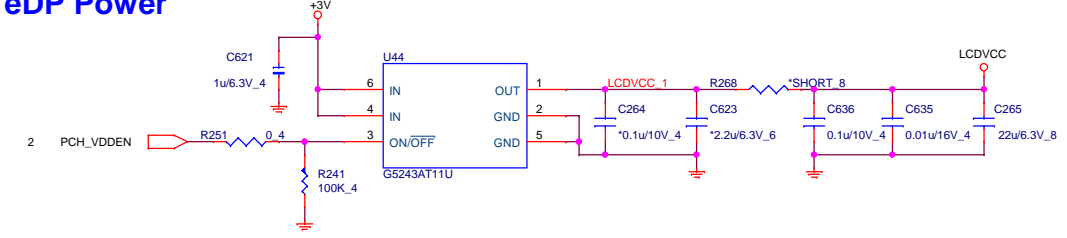


Mini DP ML (DPP)

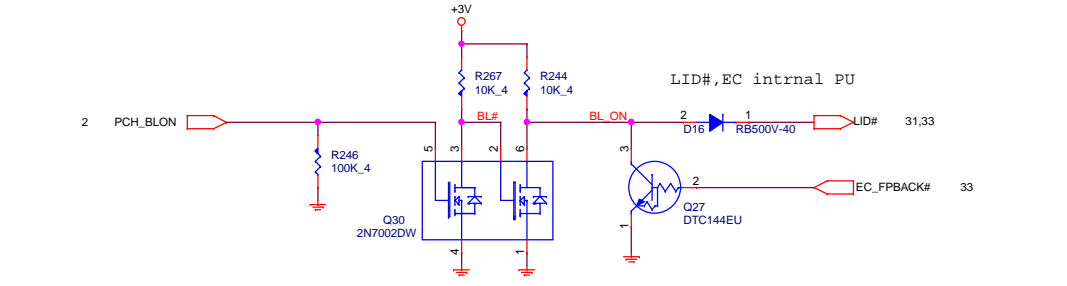
Layout Notes:
Place near Pin13 and Pin14



eDP Power



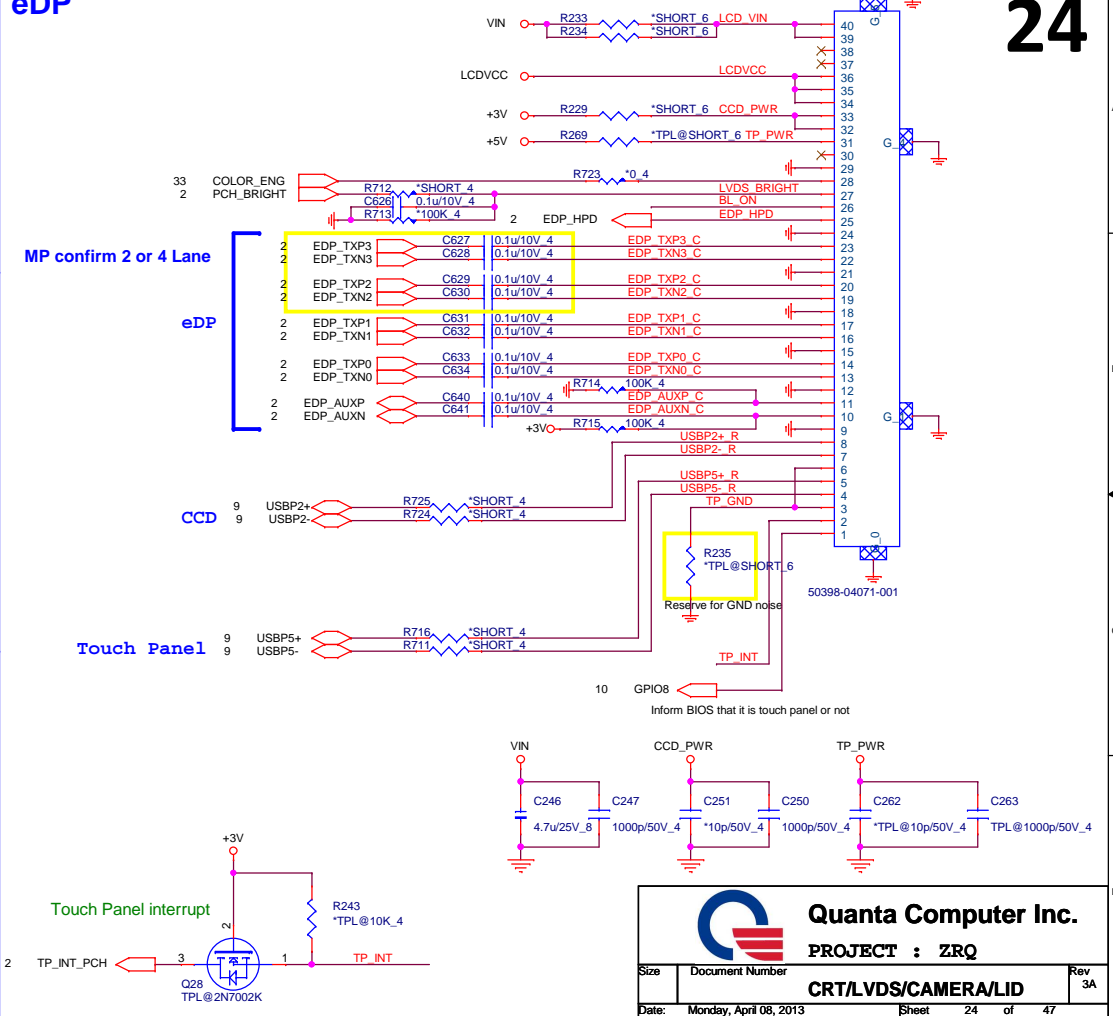
Backlight Control



Lid Switch (HSR)(move to USB/B)

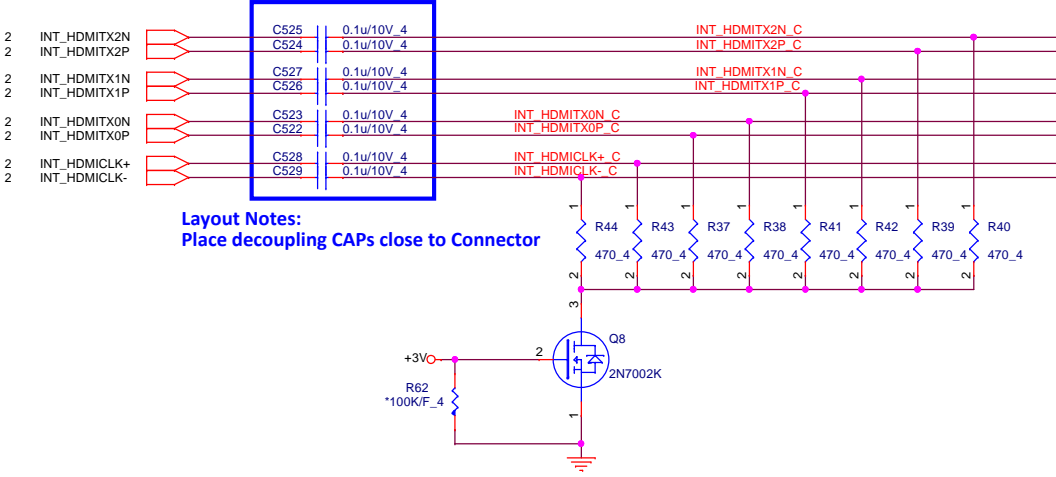


eDP

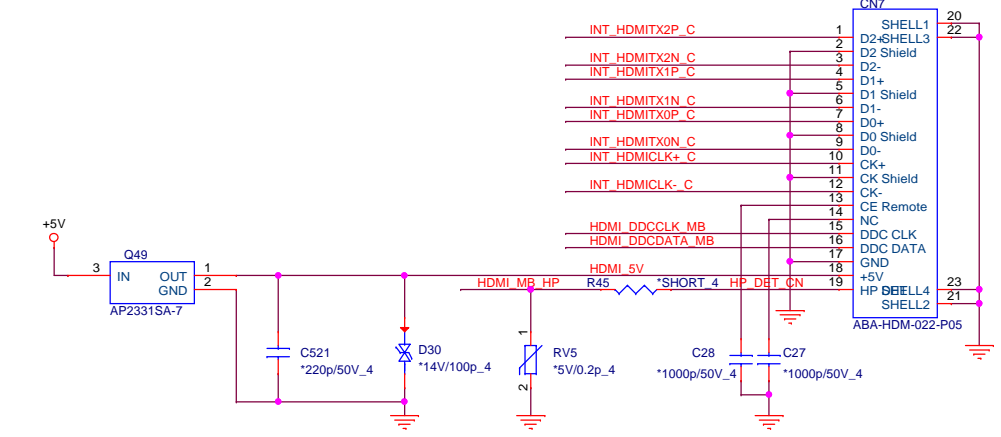


Quanta Computer Inc.
PROJECT : ZRQ
CRT/LVDS/CAMERA/LID
 Date: Monday, April 08, 2013 Sheet 24 of 47

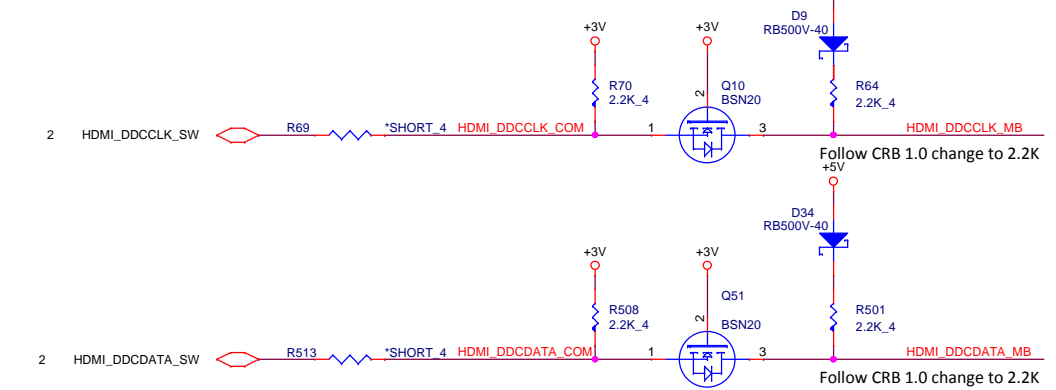
HDMI Cost Reduced level shift (HDM)



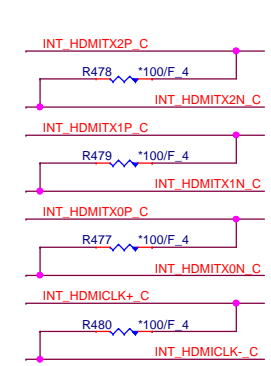
HDMI connector (HDM)



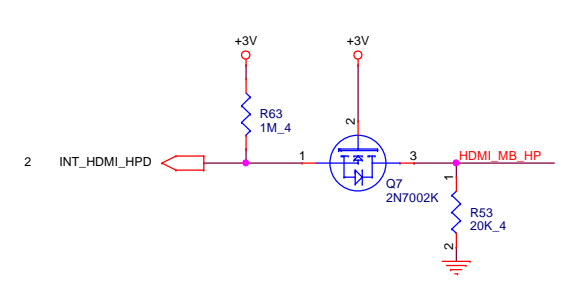
HDMI DDC (HDM)



EMI (EMC)



HDMI-detect (HDM)



Quanta Computer Inc.
PROJECT : ZRQ
HDMI (PS8101)

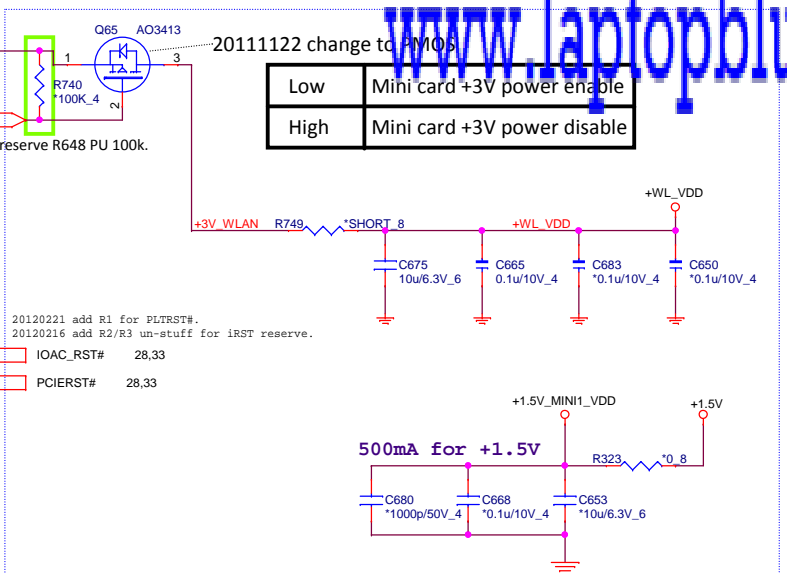
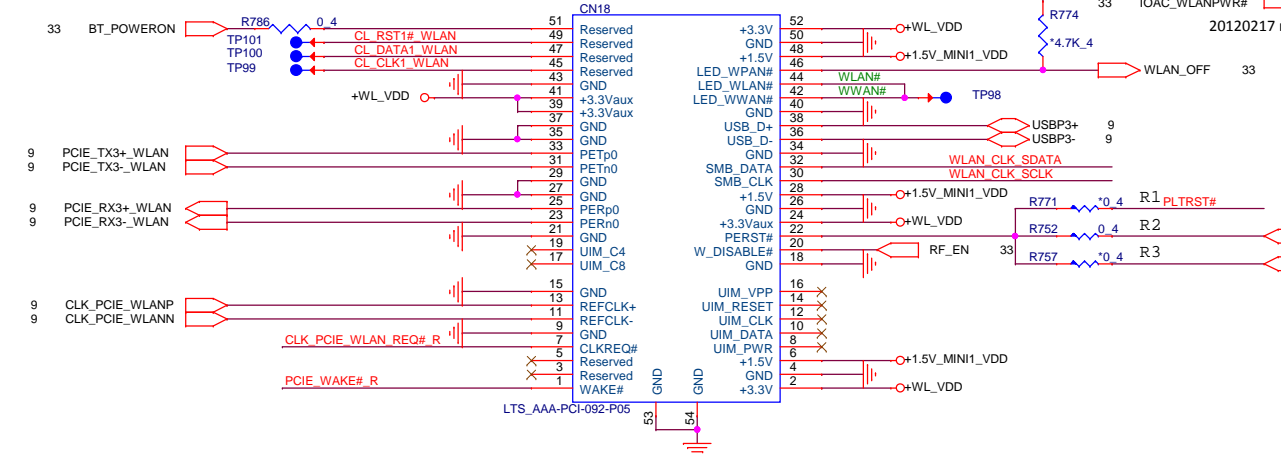
Size	Document Number	Rev
		3A
Date:	Monday, April 08, 2013	Sheet 25 of 47

MINI-CARD WLAN(MPC)

+3.3V: 1000mA
 +3.3Vaux:330mA
 +1.5V:500mA

Check LED signal. (active high or low)

H=5.2mm



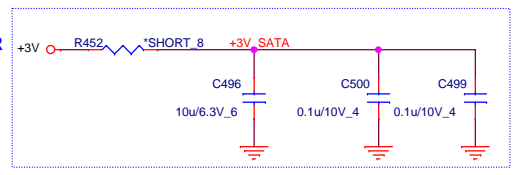
2011017 : stuff Q81 to enable wake function on WLAN for IOAC
 check IOAC power rail can reduce Q81

LAYOUT NOTE:
 CLOSE TO CONNECTOR

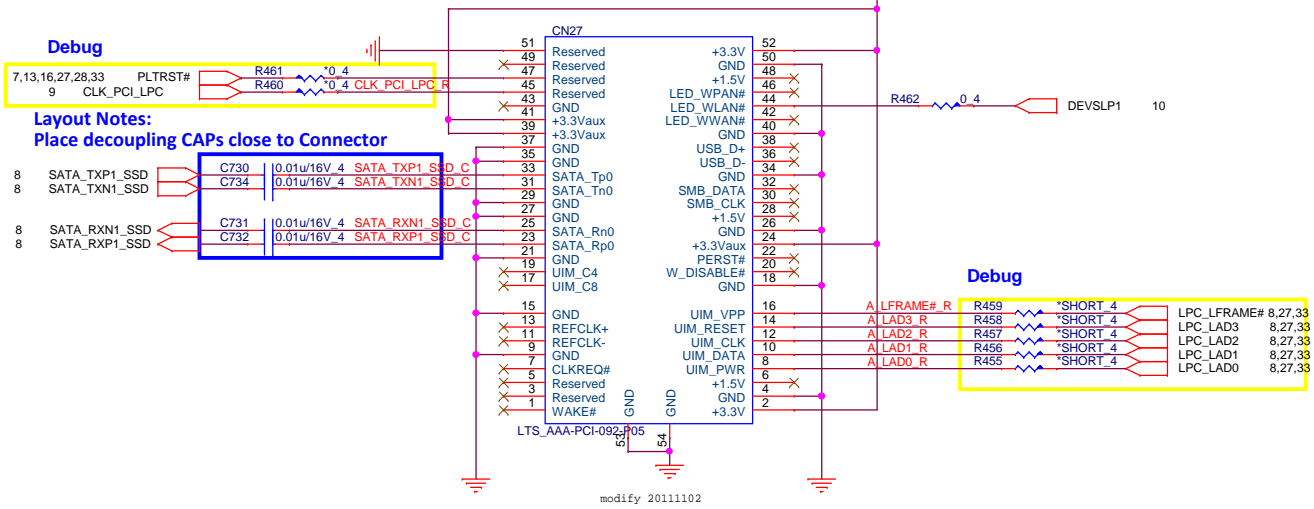
mSATA(MNC)

LAYOUT NOTE:
 CLOSE TO CONNECTOR

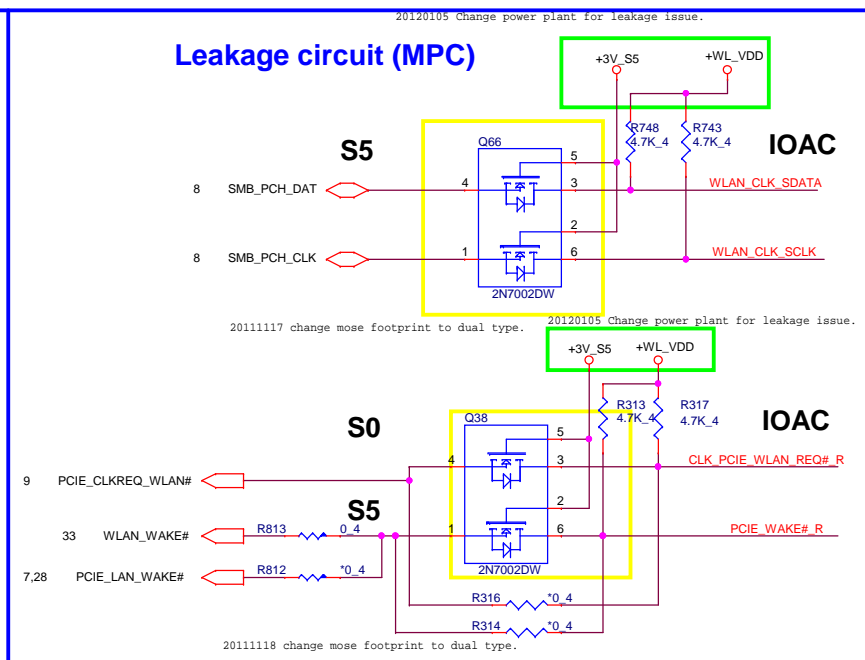
rating = 1000mA @ 128G



H=4.95mm



Leakage circuit (MPC)



2011015 Change power plant for leakage issue.

2011117 change mose footprint to dual type.

2012015 Change power plant for leakage issue.

2011118 change mose footprint to dual type.

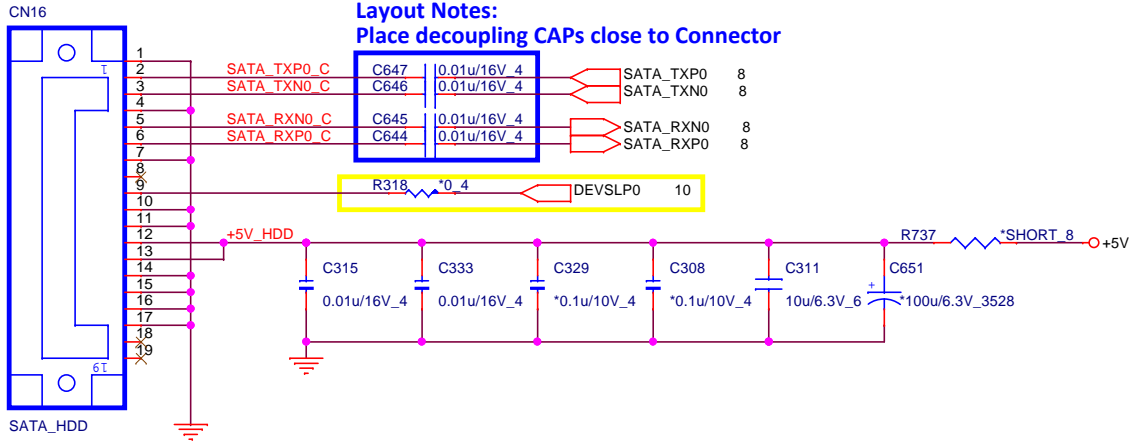
Quanta Computer Inc.
 PROJECT : ZRQ

Size	Document Number	Rev
		3A

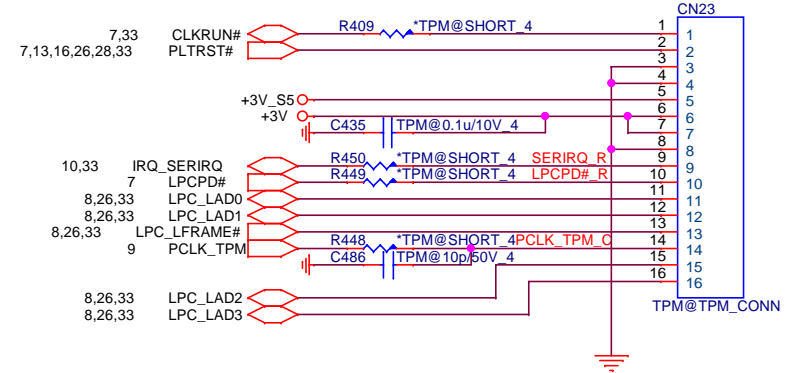
Mini Card/mSATA

Date: Monday, April 08, 2013 Sheet 26 of 47

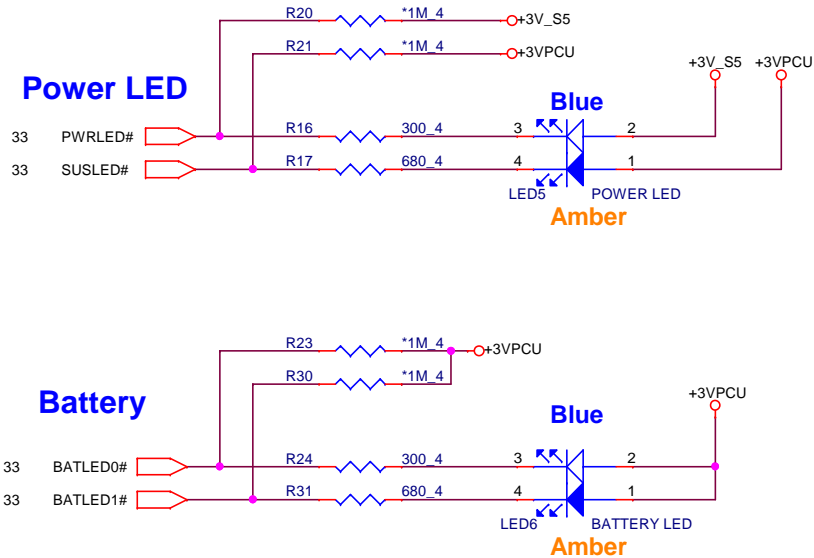
MAIN SATA HDD (HDD)



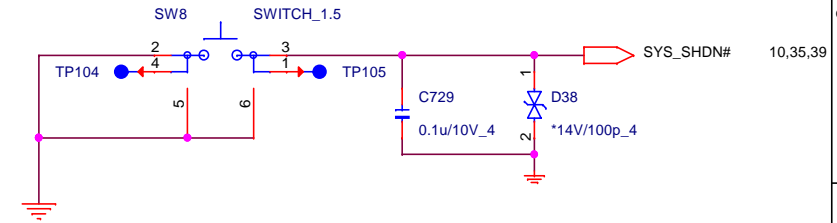
TPM (TPM)



LED(UIF)



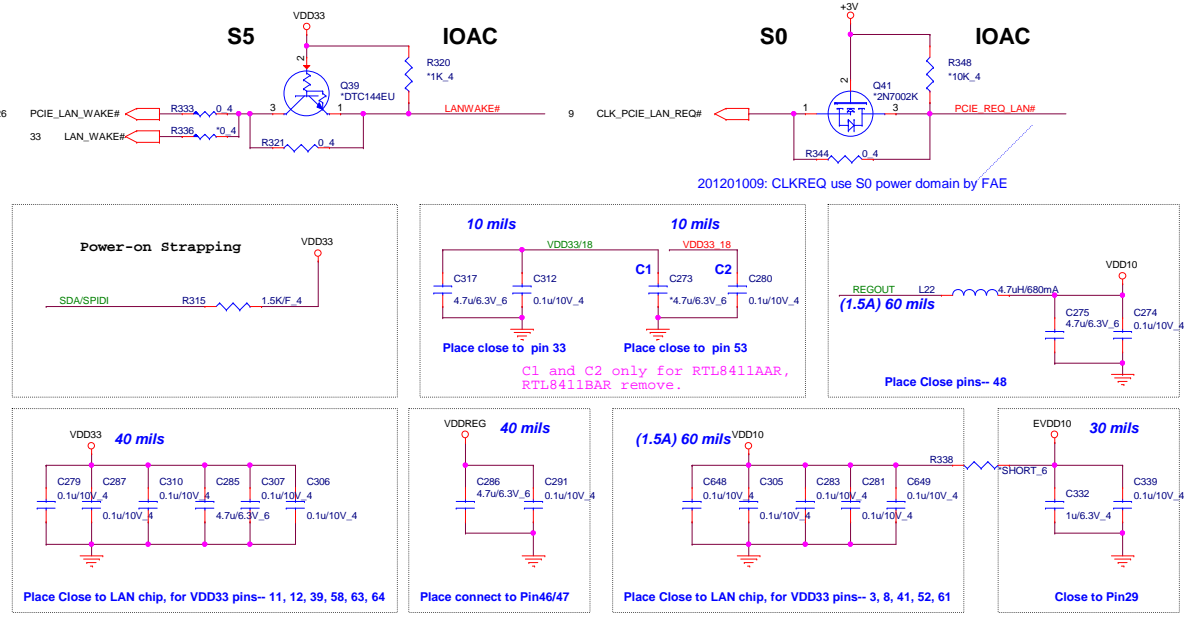
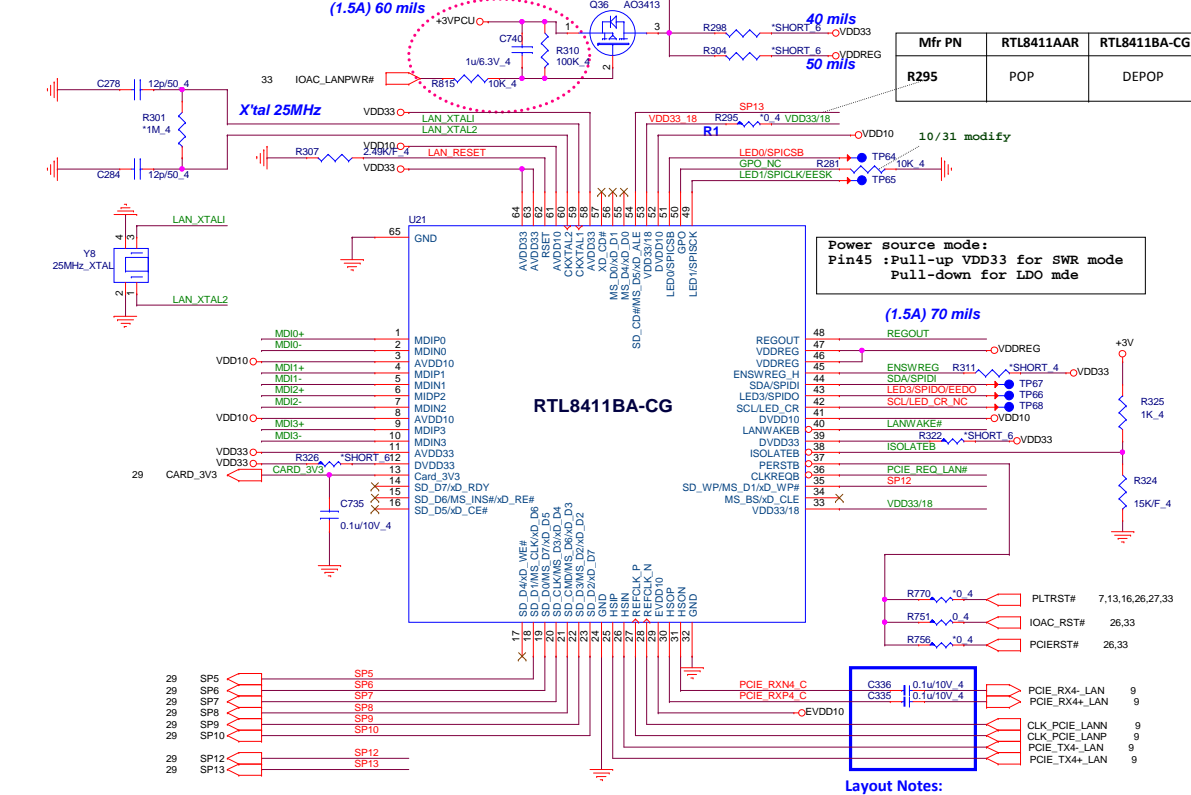
3/5VPCU reset switch (CLG)



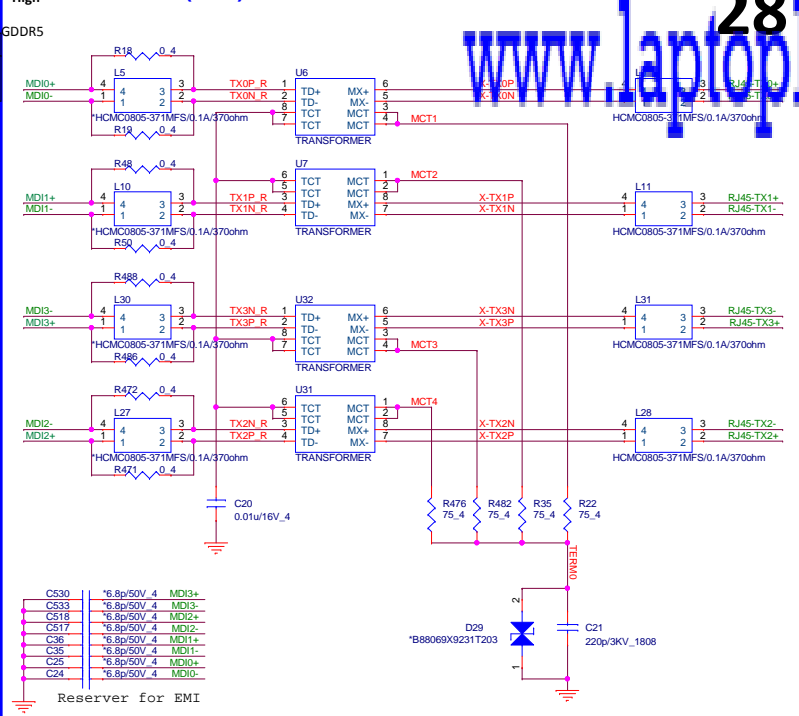
Quanta Computer Inc.
PROJECT : ZRQ

Size	Document Number	Rev
	SATA-HDD/ TPM	3A
Date:	Monday, April 08, 2013	Sheet 27 of 47

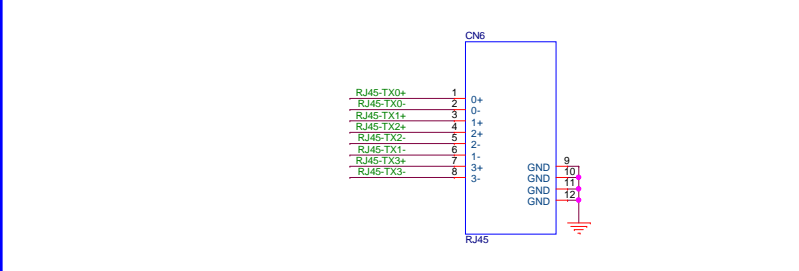
LAN/Card reader (LAN)



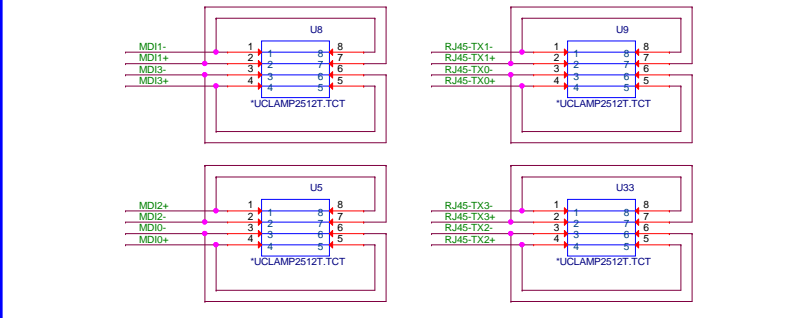
High Transformer (LAN)



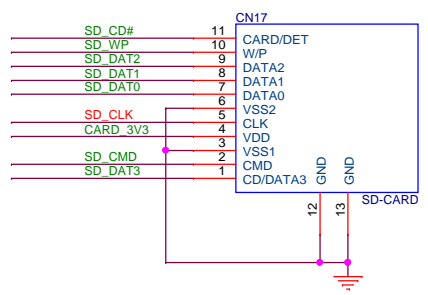
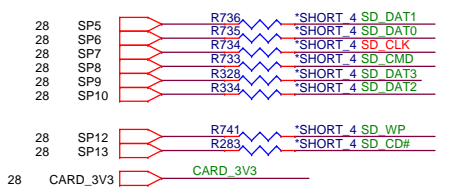
RJ45 CONNECTOR (LAN)



SURGE (LAN)



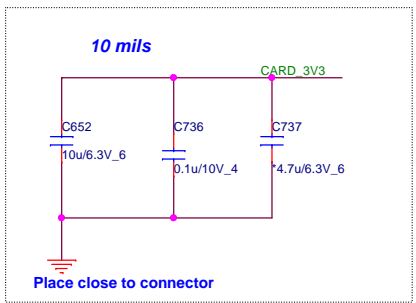
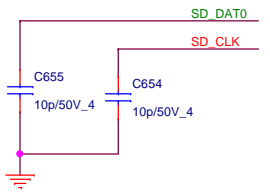
SD/MMC CARD READER CONNECTOR (MMC)



Share Pin

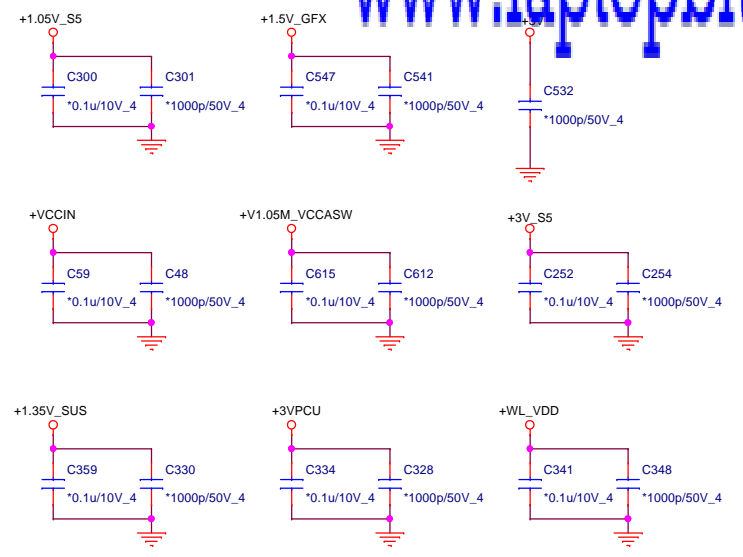
SP1	SD_D7	xD_RDY
SP2	SD_D6	MS_INS#
SP3	SD_D5	xD_RE#
SP4	SD_D4	xD_CE#
SP5	SD_D1	xD_D6
SP6	SD_D0	MS_CLK
SP7	SD_CLK	MS_D7
SP8	SD_CMD	MS_D3
SP9	SD_D3	xD_D4
SP10	SD_D2	MS_D6
SP11	MS_BS	xD_D2
SP12	SD_WP	xD_D7
SP13	SD_CD#	MS_D1
SP14	MS_D4	xD_WP#
SP15	MS_D0	xD_CE#
SP16		xD_D1
SP16		xD_CD#

EMI

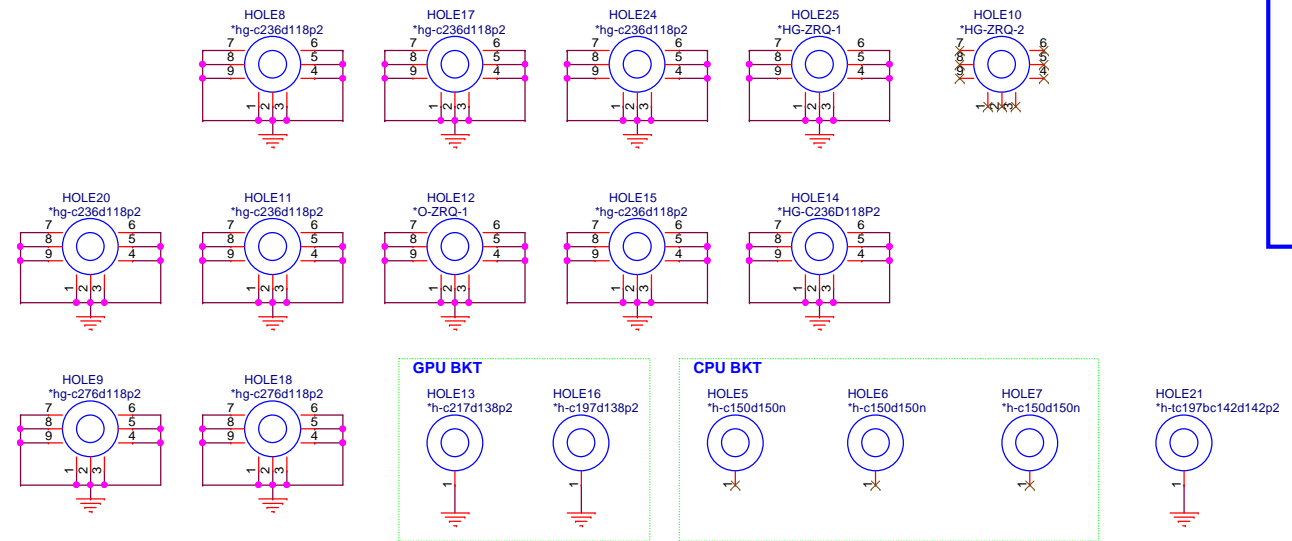


Stitching cap (EMC)

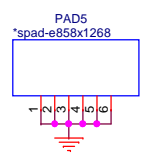
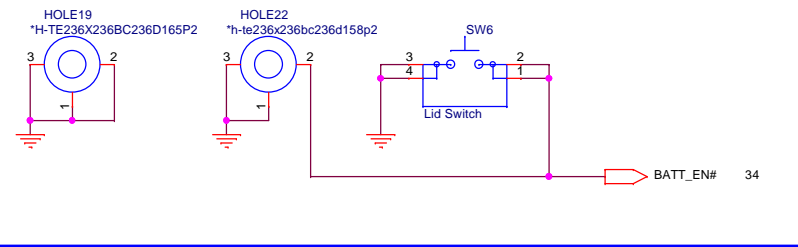
www.laptopblue.vn



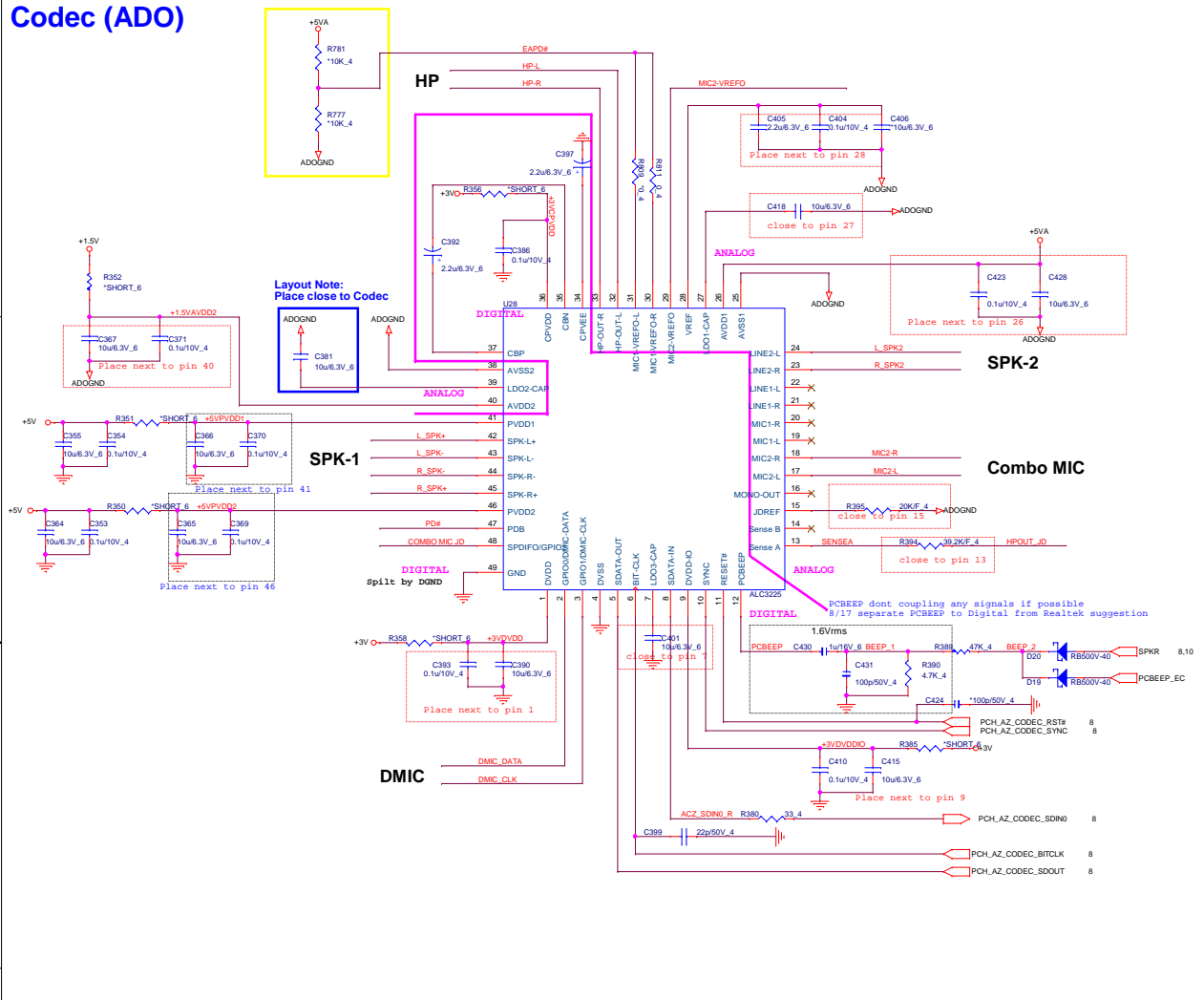
HOLE(OTH)



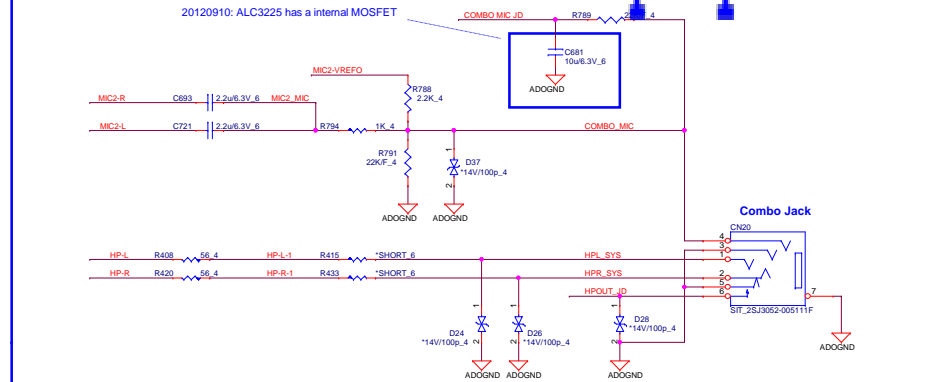
BATT Enable short pad



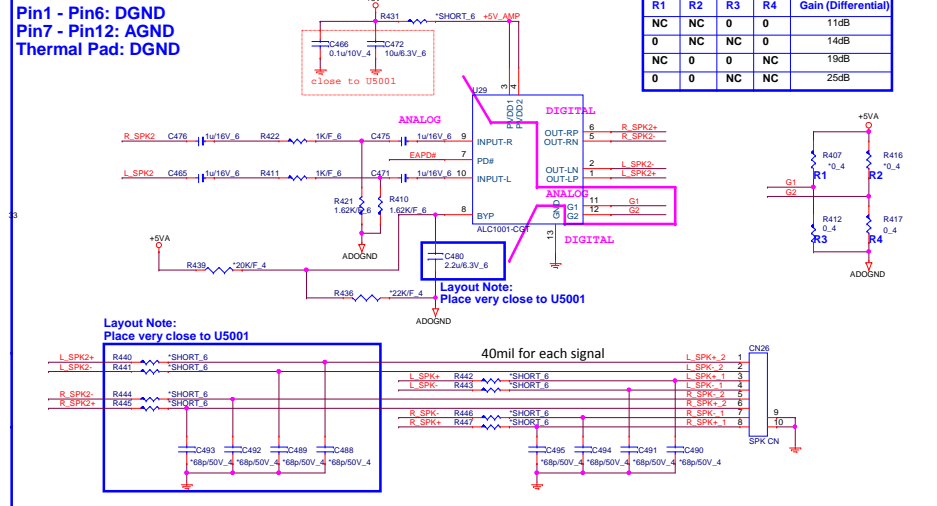
Codec (ADO)



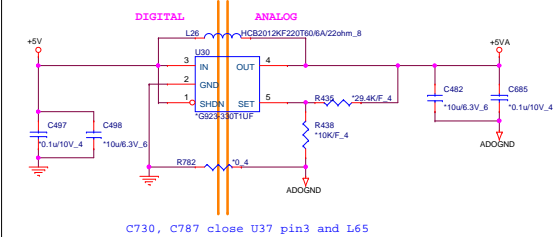
HEADPHONE/Mic combo (AMP)



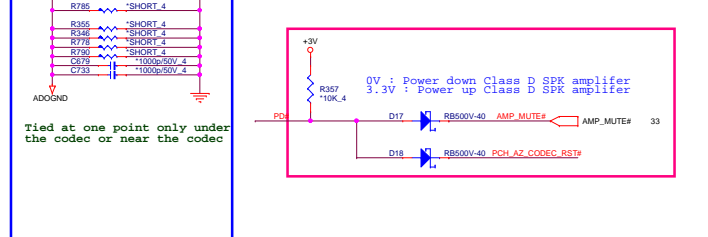
Internal Speaker (AMP)



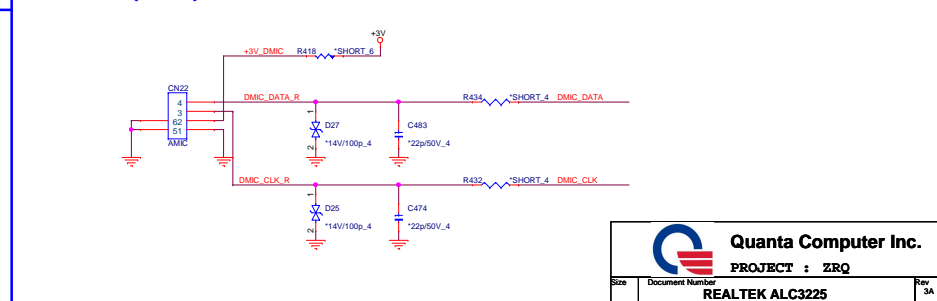
Power(ADO)



Mute(ADO)

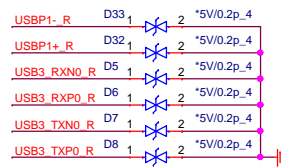
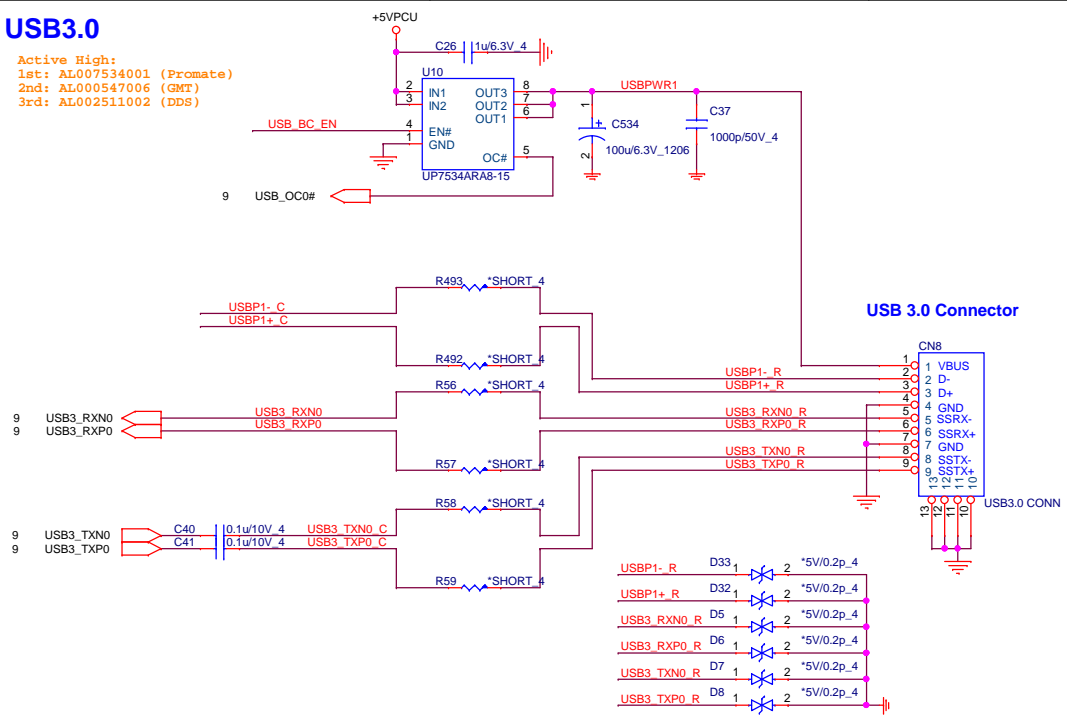


INT DMIC(AMP)



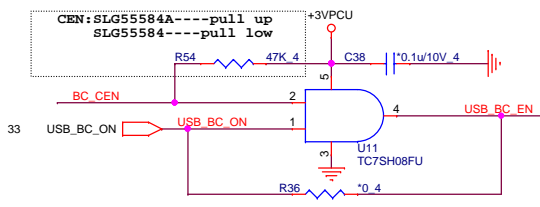
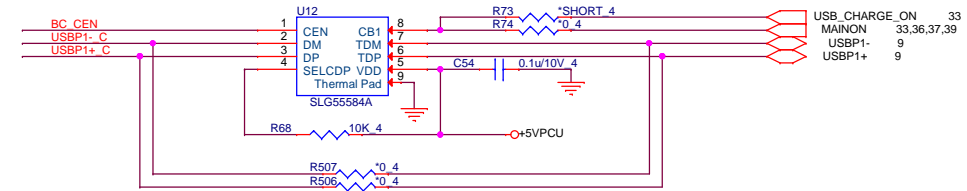
USB3.0

Active High:
 1st: AL007534001 (Promote)
 2nd: AL000547006 (GMT)
 3rd: AL002511002 (DDS)

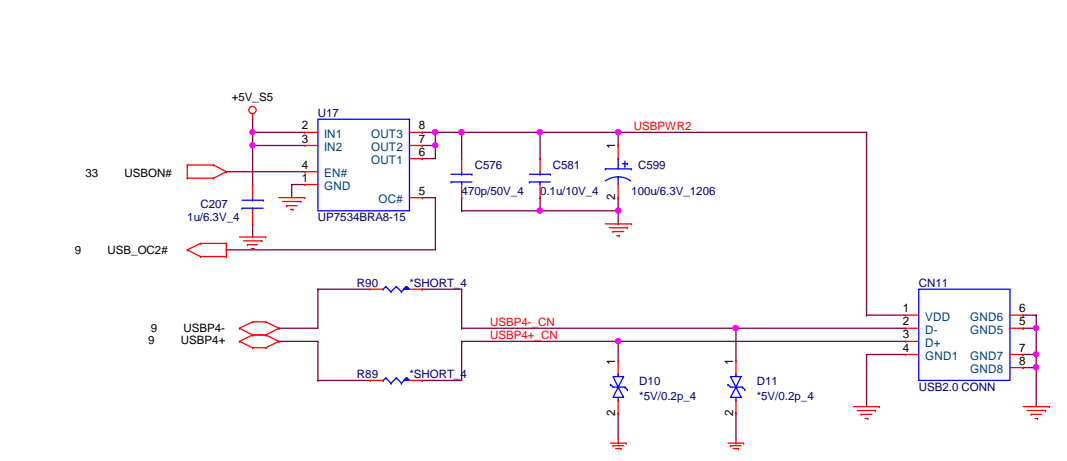


USB Charger to 3.0

CB	SELCDP	Function
0	X	DCP autotodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

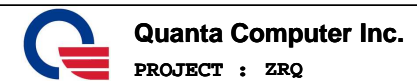
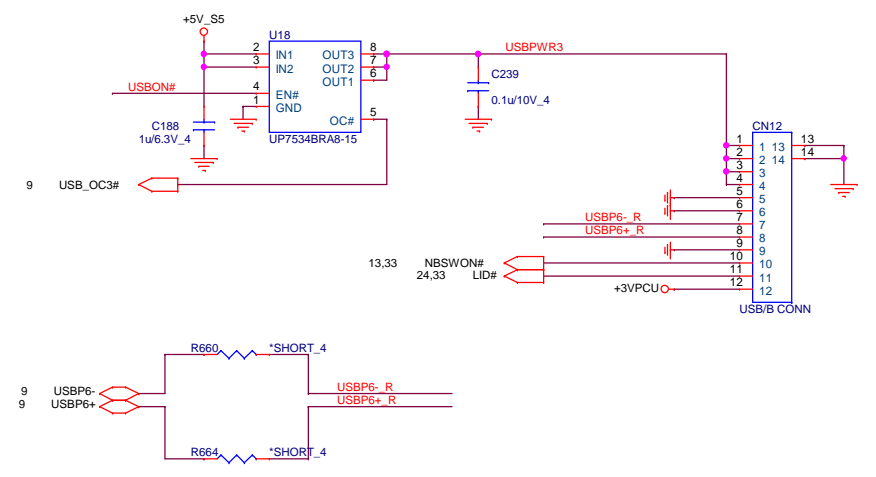


USB2.0

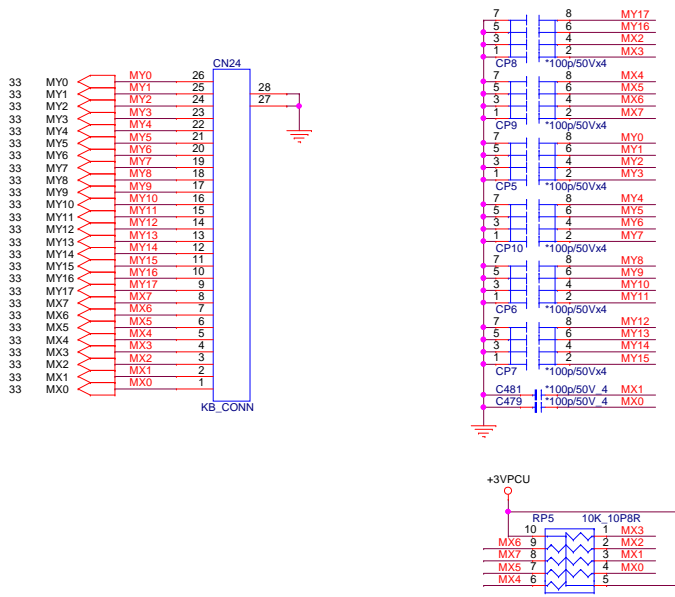


I/O board

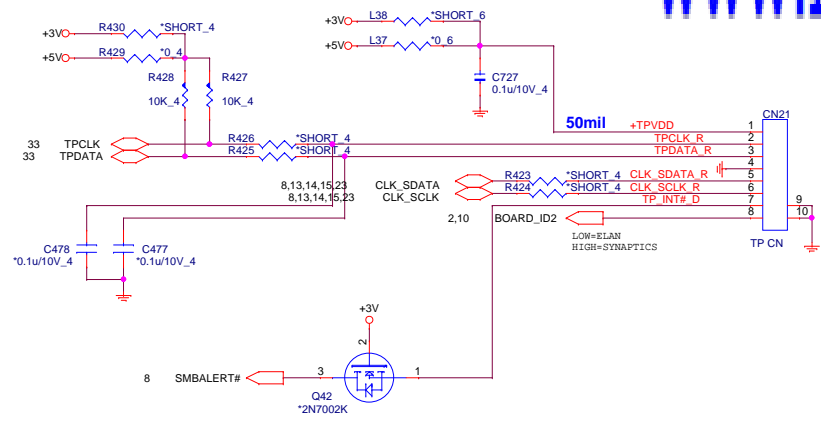
1st source: AL007534000
 2ns source: AL082025000



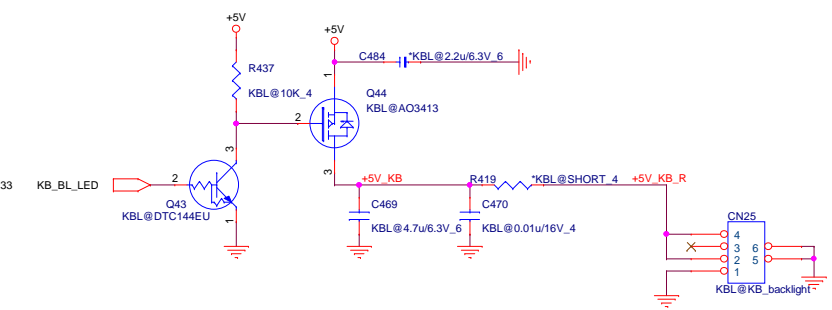
K/B (KBC)



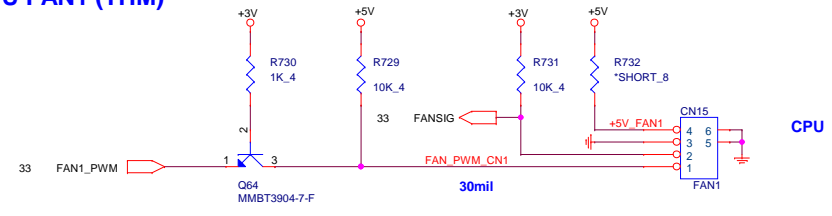
TOUCHPAD BOARD CONN (TPD)



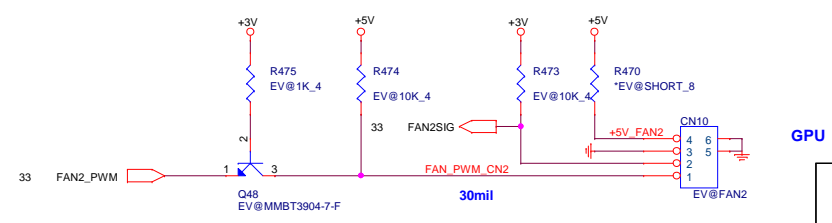
KB_BL LED (KBC)



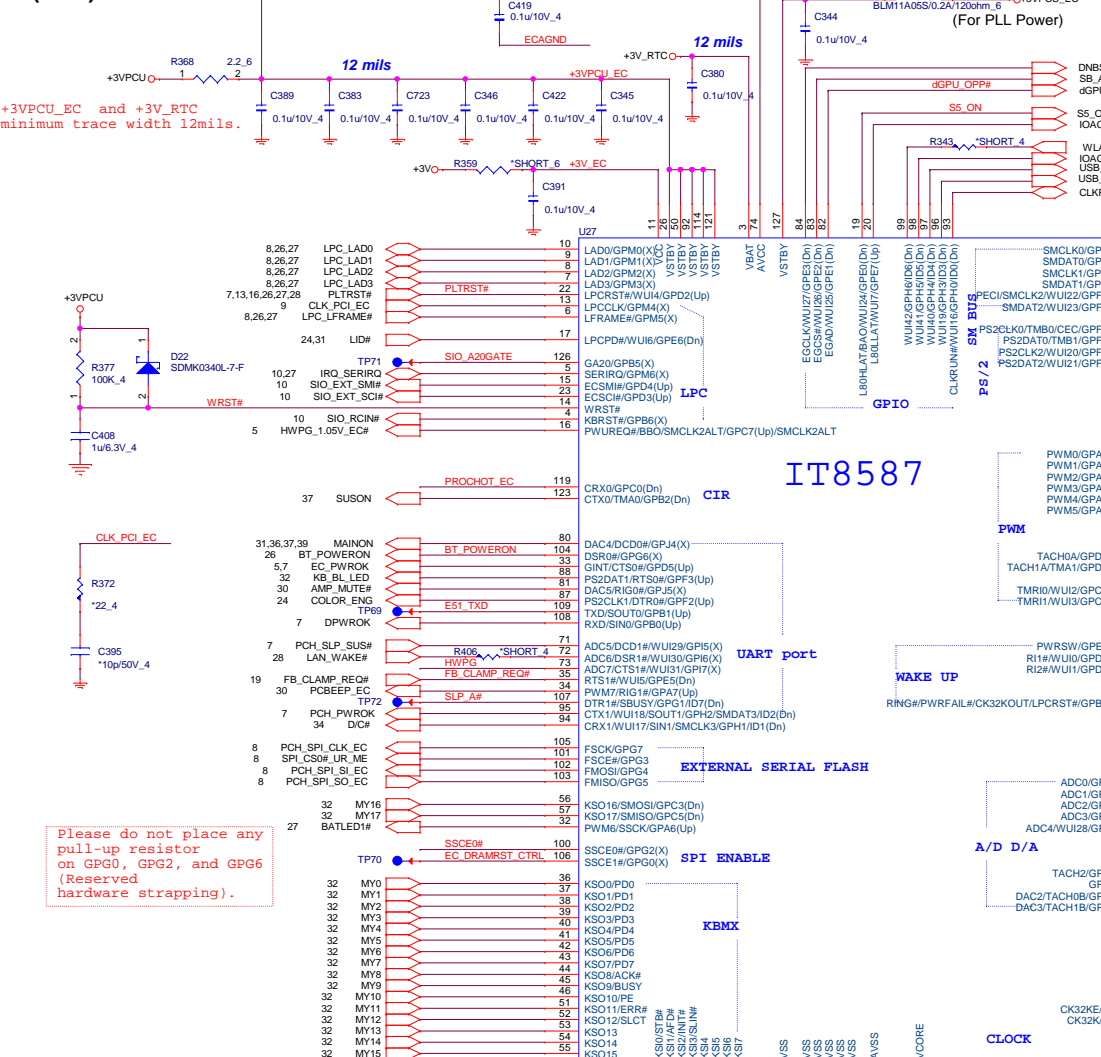
CPU FAN1 (THM)



CPU FAN2 (THM)



EC(KBC)

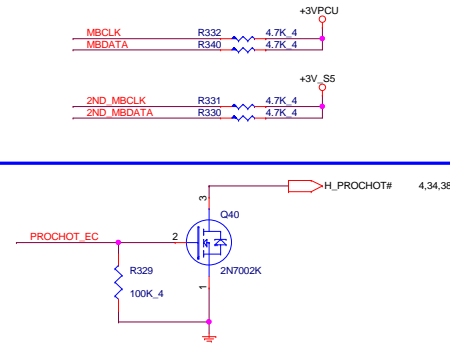


Please do not place any pull-up resistor on GPG0, GPG2, and GPG6 (Reserved hardware strapping).

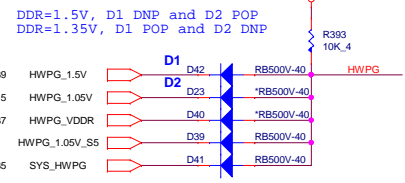
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	N/A
SM Bus 4	

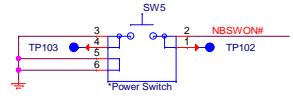
SM BUS PU(KBC)



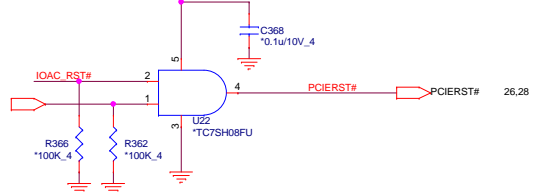
HWPG(KBC)

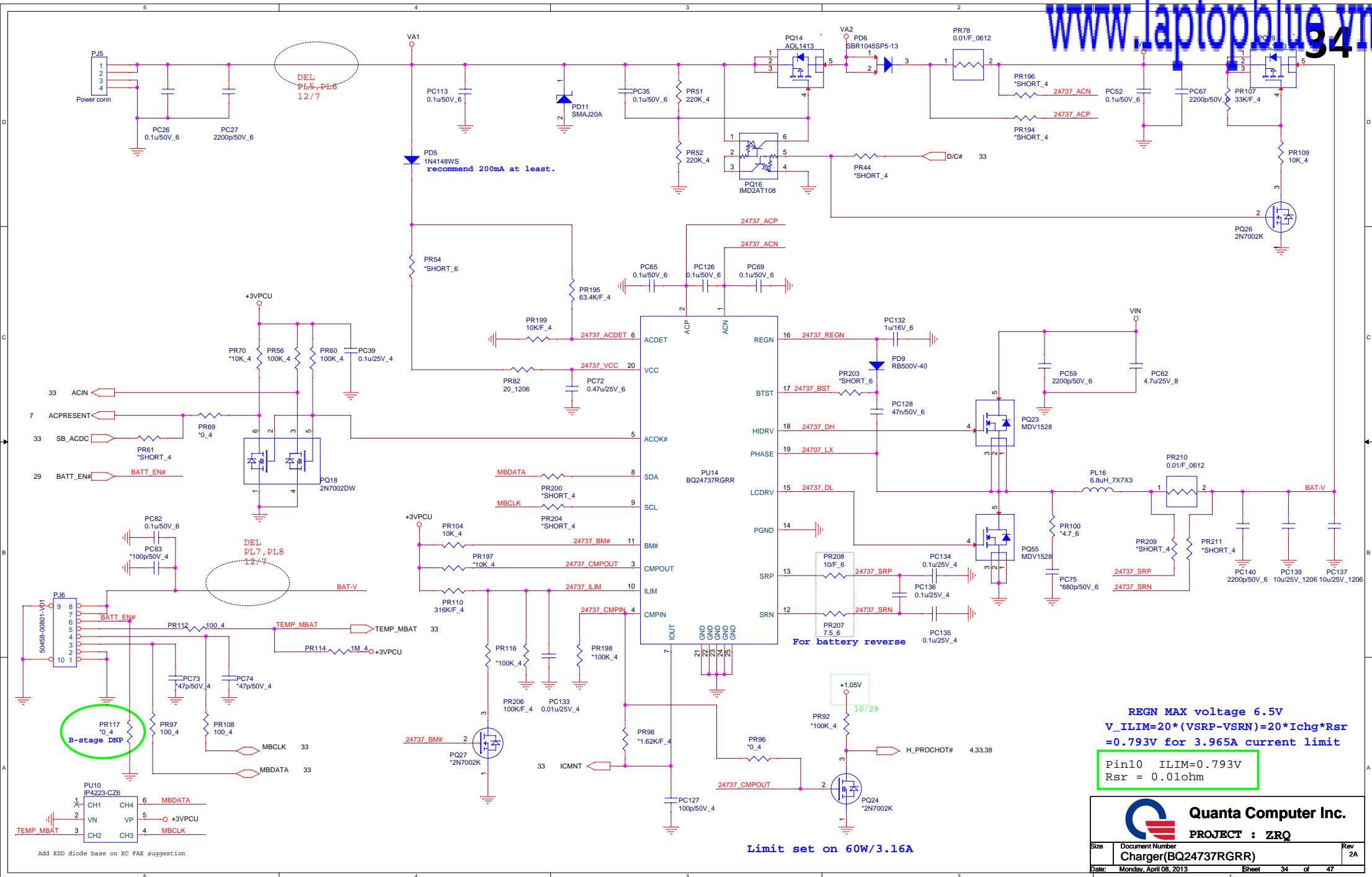


For test only



IRST



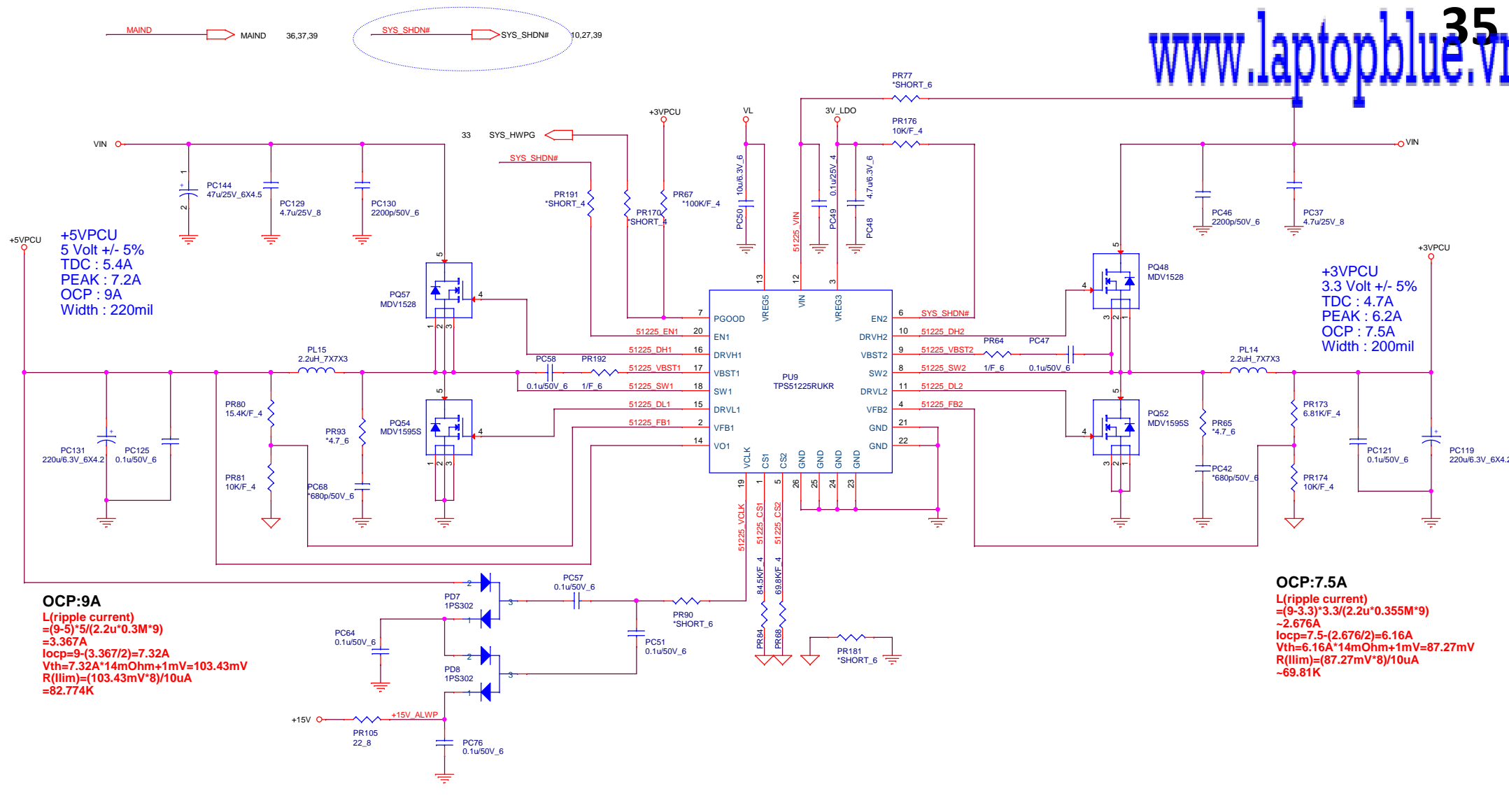


REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr}$
 $= 0.793V$ for 3.965A current limit
 Pin10 ILIM=0.793V
 $R_{sr} = 0.01ohm$

Limit set on 60W/3.16A

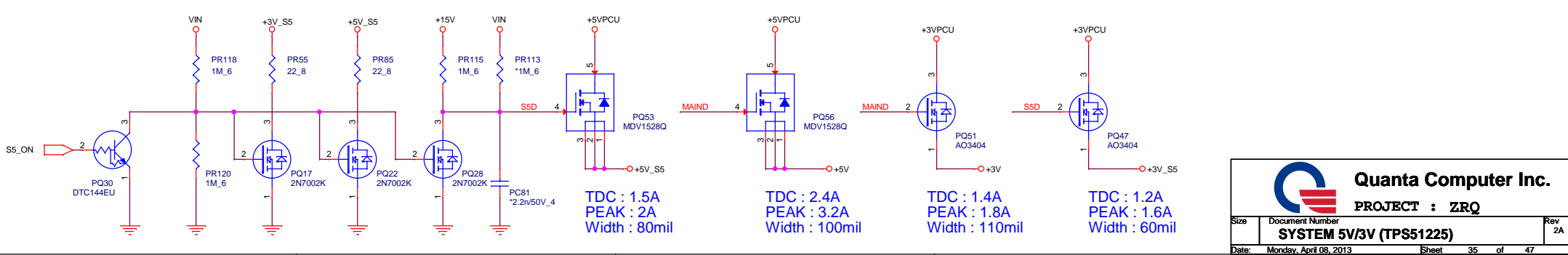
		Quanta Computer Inc. PROJECT : ZRQ	
		Size Document Number Charger(BQ24737RGR)	Rev 2A
Date: Monday, April 08, 2013		Sheet 34 of 47	

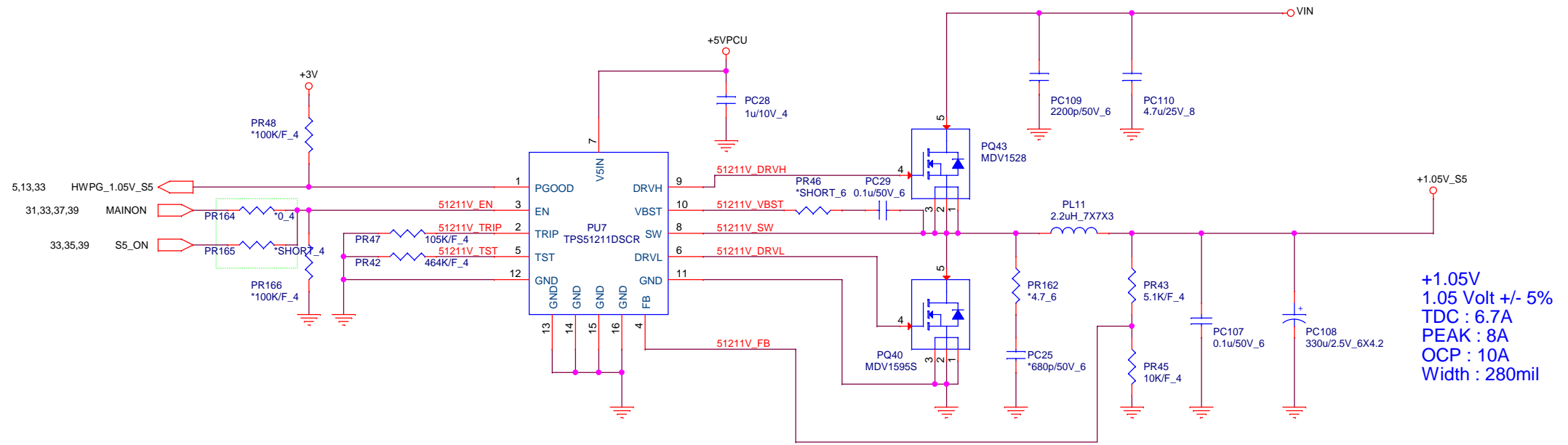
Add ESD diode base on EC FAR suggestion



OCP:9A
 $L(\text{ripple current}) = (9-5) \cdot 5 / (2.2 \cdot 0.3M \cdot 9) = 3.367A$
 $I_{ocp} = 9 - (3.367/2) = 7.32A$
 $V_{th} = 7.32A \cdot 14m\Omega + 1mV = 103.43mV$
 $R(I_{lim}) = (103.43mV \cdot 8) / 10\mu A = 82.774K$

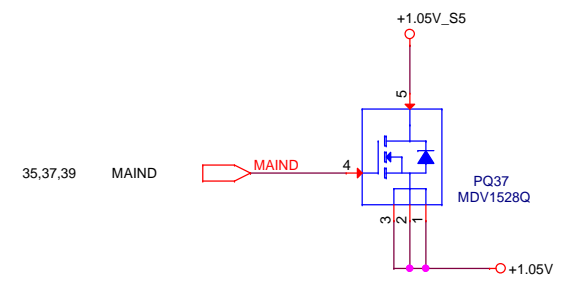
OCP:7.5A
 $L(\text{ripple current}) = (9-3.3) \cdot 3.3 / (2.2 \cdot 0.355M \cdot 9) = 2.676A$
 $I_{ocp} = 7.5 - (2.676/2) = 6.16A$
 $V_{th} = 6.16A \cdot 14m\Omega + 1mV = 87.27mV$
 $R(I_{lim}) = (87.27mV \cdot 8) / 10\mu A = 69.81K$






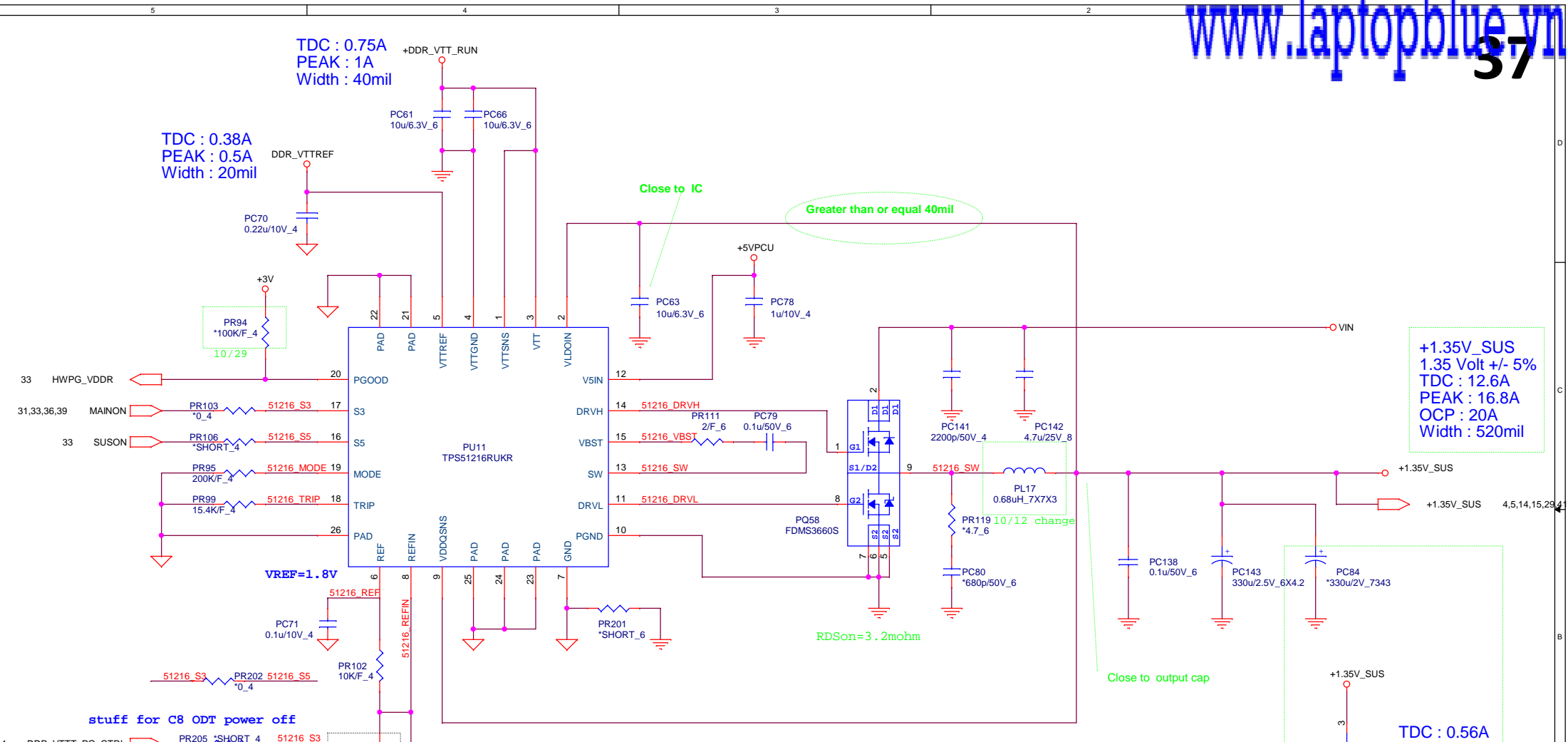
+1.05V
 1.05 Volt +/- 5%
 TDC : 6.7A
 PEAK : 8A
 OCP : 10A
 Width : 280mil

OCP=10A
 L ripple current
 $= (19-1.05) * 1.05 / (2.2u * 290k * 19)$
 $= 1.555A$
 $V_{trip} = 10 - (1.555 / 2) * 14mohm$
 $= 0.129V$
 $R_{limit} = 0.129 / 10uA * 8 = 103.293Kohm$



TDC : 2.4A
 PEAK : 3.2A
 Width : 100mil

 Quanta Computer Inc. PROJECT : ZRQ		Size	Document Number	Rev
			+1.05V(TPS51211)	2A
Date:	Monday, April 08, 2013	Sheet	36	of 47



TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

+1.35V_SUS
1.35 Volt +/- 5%
TDC : 12.6A
PEAK : 16.8A
OCP : 20A
Width : 520mil

TDC : 0.56A
PEAK : 0.75A
Width : 20mil

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=10A
L ripple current
= $(19-1.35) * 1.35 / (0.68u * 400k * 19)$
=4.611A
 $V_{trip} = 10 - (4.611/2) * 2.5mohm$
=0.01923V
 $R_{limit} = 0.01923 / 10uA * 8 = 15.389Kohm$

OCP=20A
L ripple current
= $(19-1.5) * 1.5 / (0.68u * 400k * 19)$
=5.079A
 $V_{trip} = 20 - (5.079/2) * 2.5mohm$
=0.04365V
 $R_{limit} = 0.04365 / 10uA * 8 = 34.92Kohm$

DDR=1.35V
OCP=10A
PR95=15.4K/F_4
PR97=30.1K/F_4

DDR=1.5V
OCP=20A
PR95=35.7K/F_4
PR97=51K/F_4

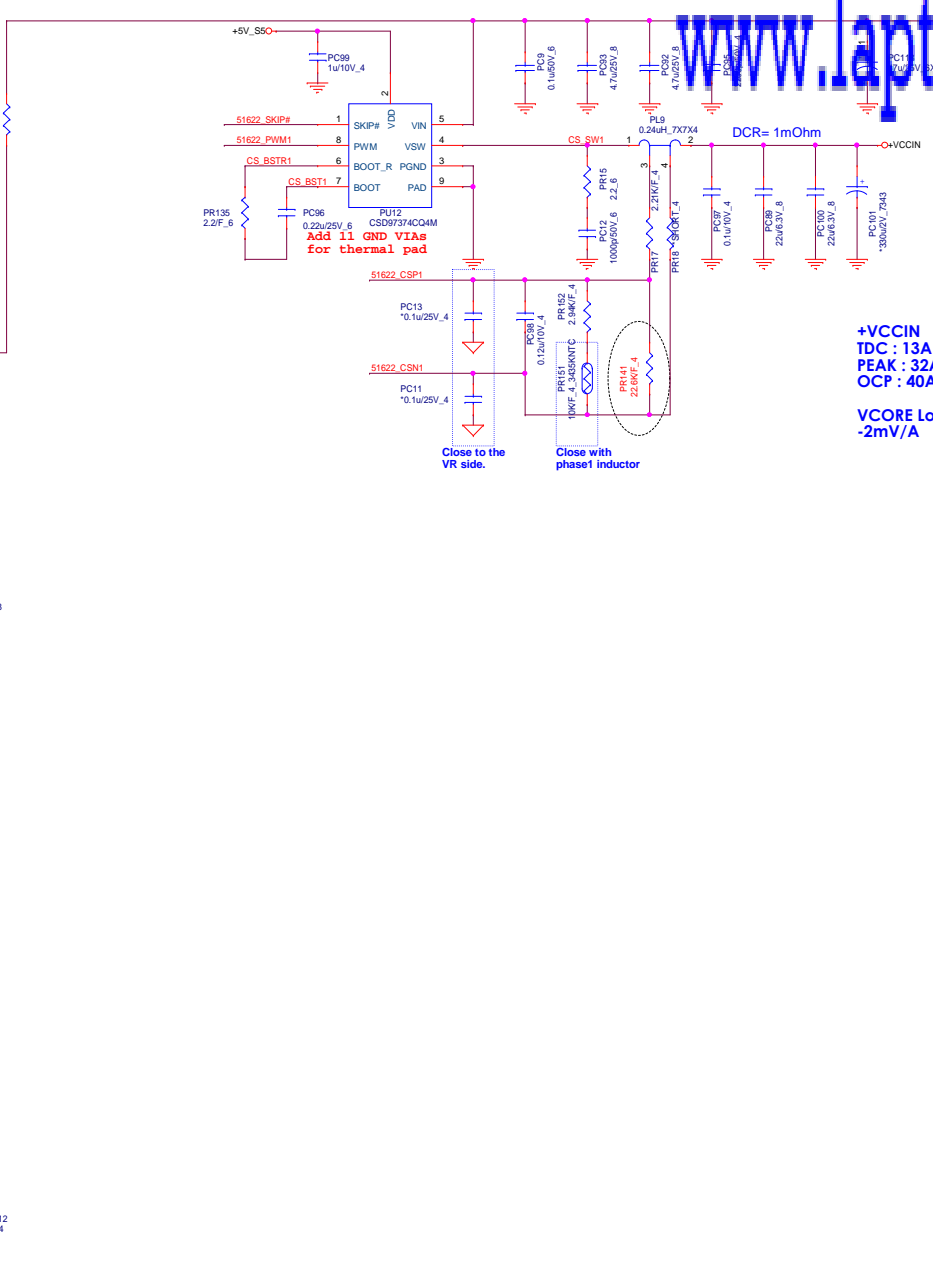
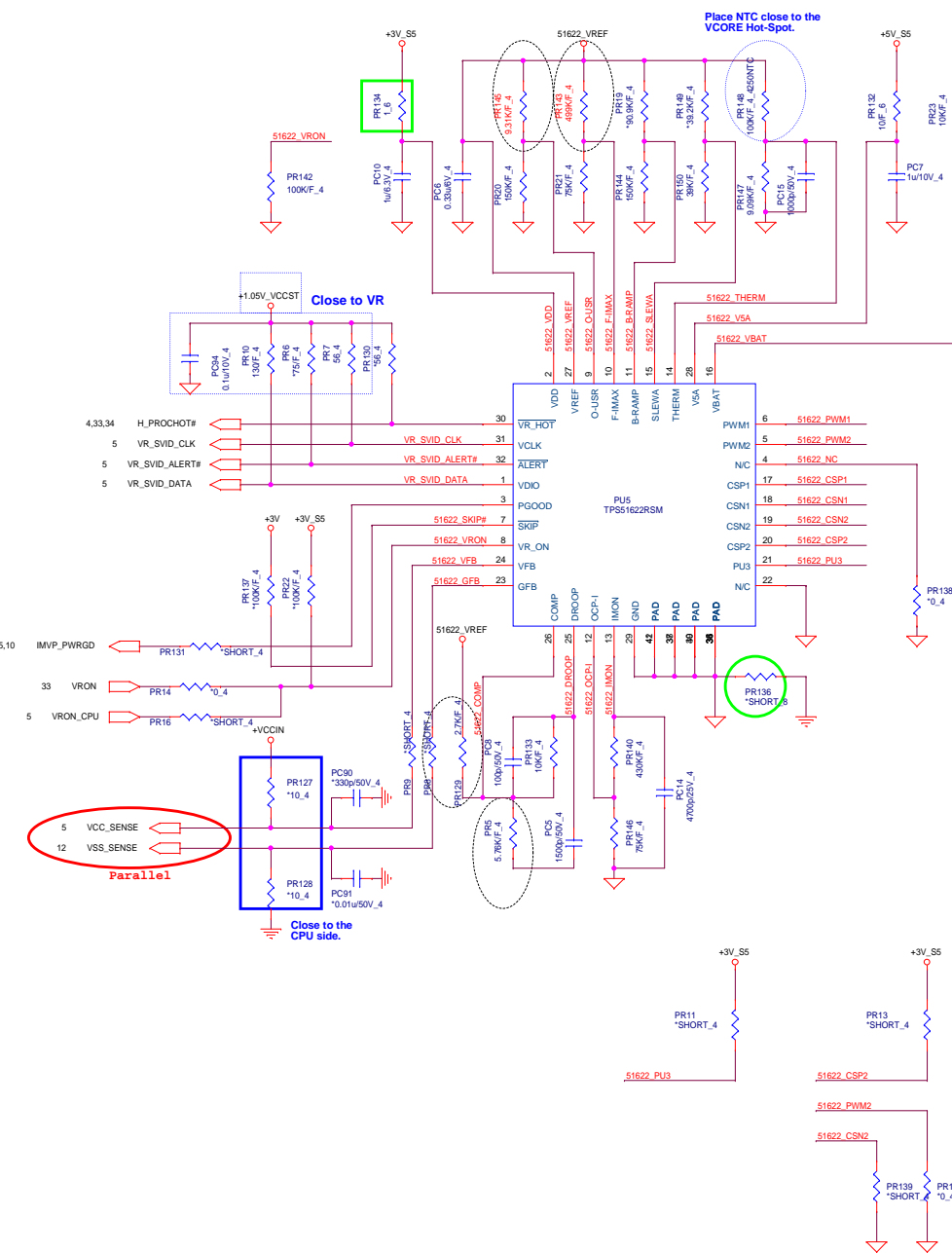
Quanta Computer Inc.
PROJECT : ZRQ

Size: Document Number
Date: Monday, April 08, 2013

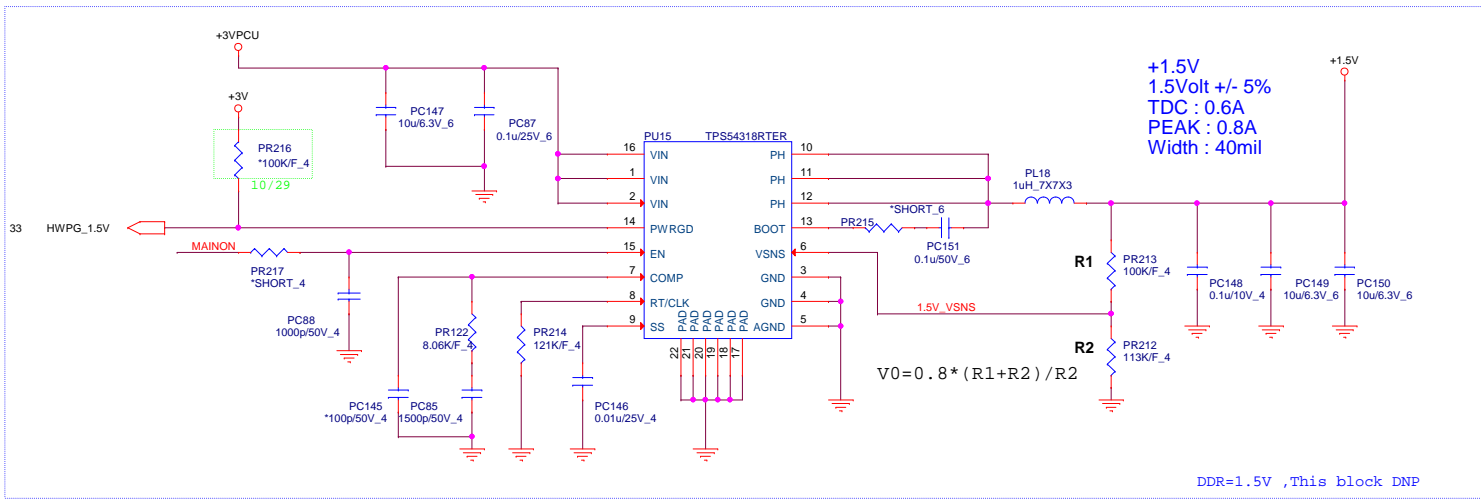
Sheet 37 of 47

Rev 2A

1

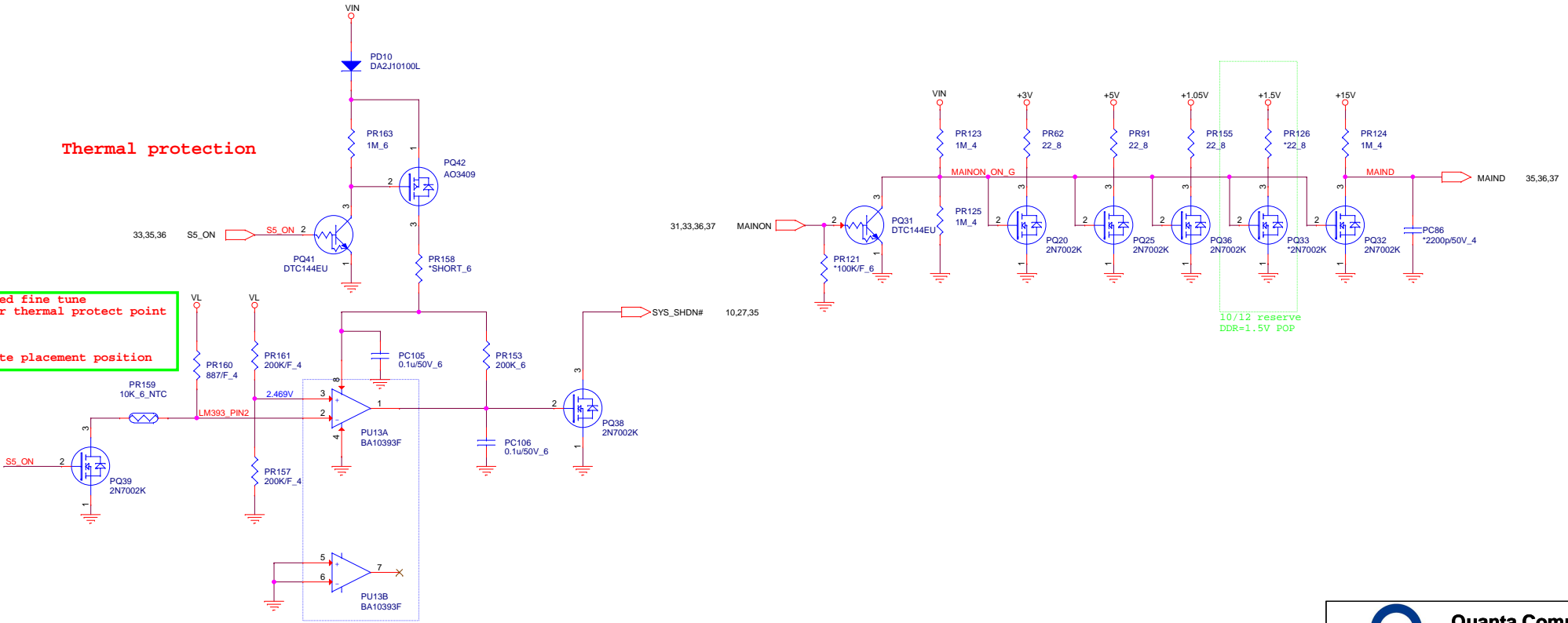


+VCCIN
 TDC : 13A
 PEAK : 32A
 OCP : 40A
VCORE Load Line :
 -2mV/A

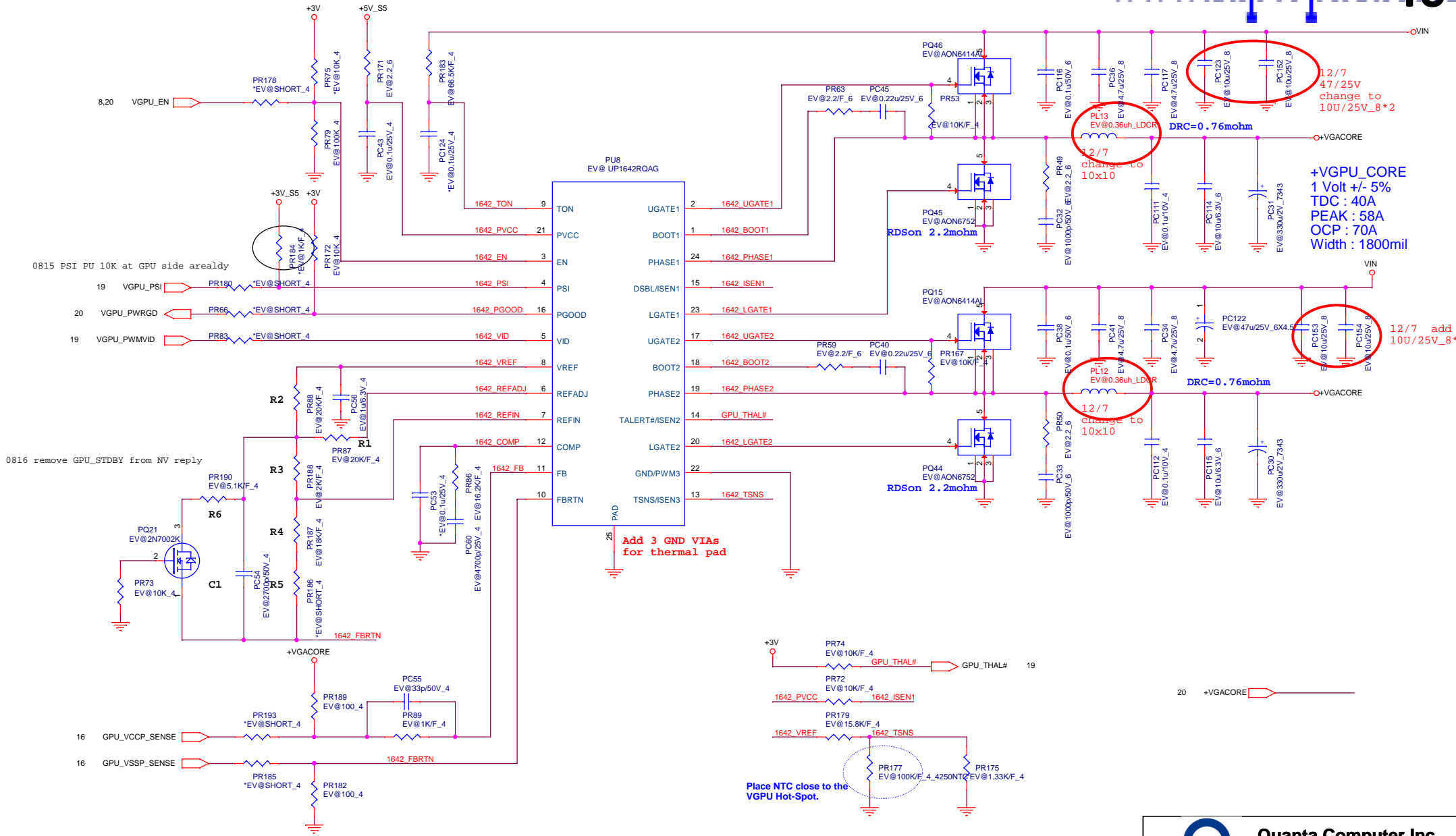


Thermal protection

Need fine tune for thermal protect point
Note placement position



For EC control thermal protection (output 3.3V)



8,20 VGPU_EN

0815 PSI PU 10K at GPU side already

19 VGPU_PSI

20 VGPU_PWRGD

19 VGPU_PWMVID

0816 remove GPU_STDBY from NV reply

Add 3 GND VIAs for thermal pad

Place NTC close to the VGPU Hot-Spot.

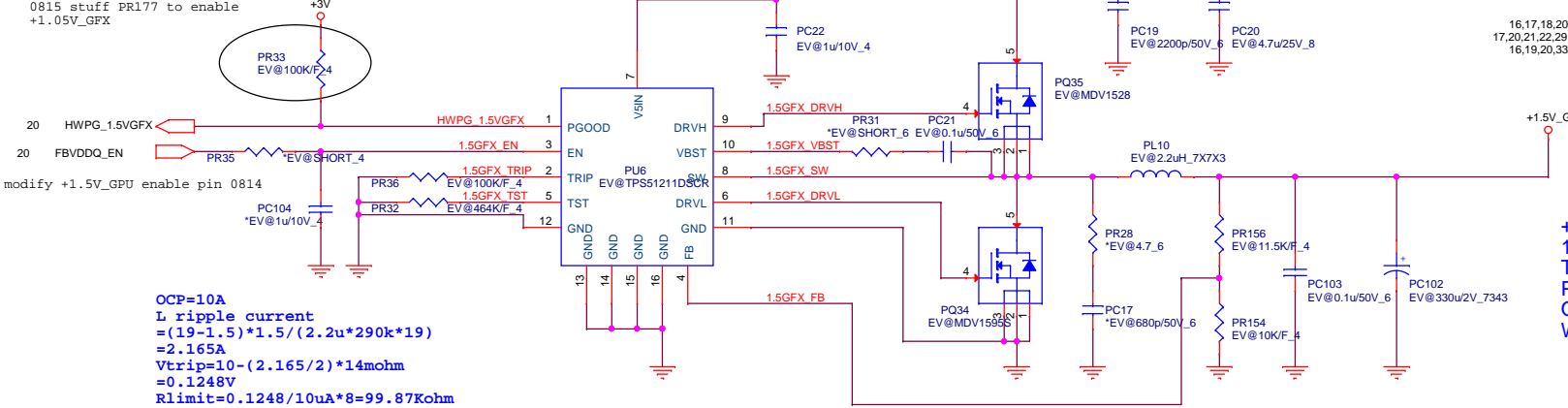
12/7
47/25V
change to
100u/25V_8*2

+VGPU_CORE
1 Volt +/- 5%
TDC : 40A
PEAK : 58A
OCP : 70A
Width : 1800mil

12/7 add
100u/25V_8*2



0815 stuff PR177 to enable
+1.05V_GFX



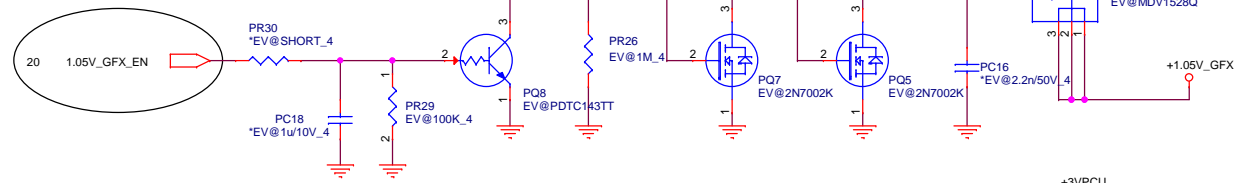
16,17,18,20 +1.05V_GFX
17,20,21,22,29 +1.5V_GFX
16,19,20,33 +3V_GFX

+1.5V_GFX
1.5 Volt +/- 5%
TDC : 6.3A
PEAK : 8.4A
OCP : 10A
Width : 250mil

DDR=1.5V ,This block DNP

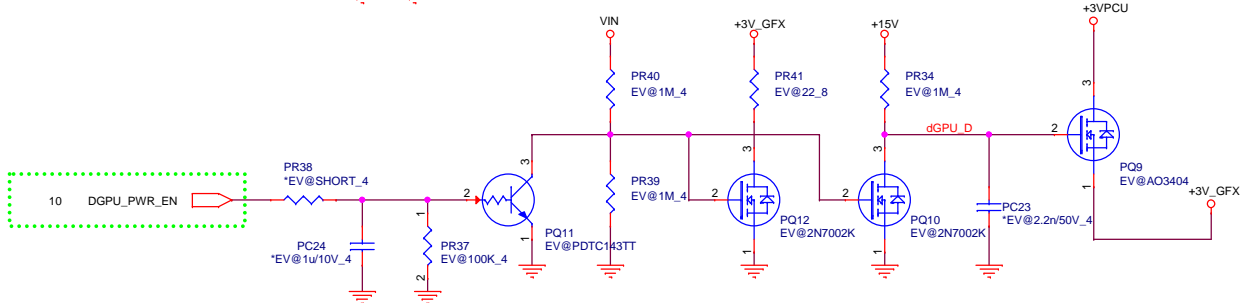
OCP=10A
L ripple current
= (19-1.5)*1.5/(2.2u*290k*19)
= 2.165A
Vtrip=10-(2.165/2)*14mohm
= 0.1248V
Rlimit=0.1248/10uA*8=99.87Kohm

modify +1.05V_GFX enable pin 0814

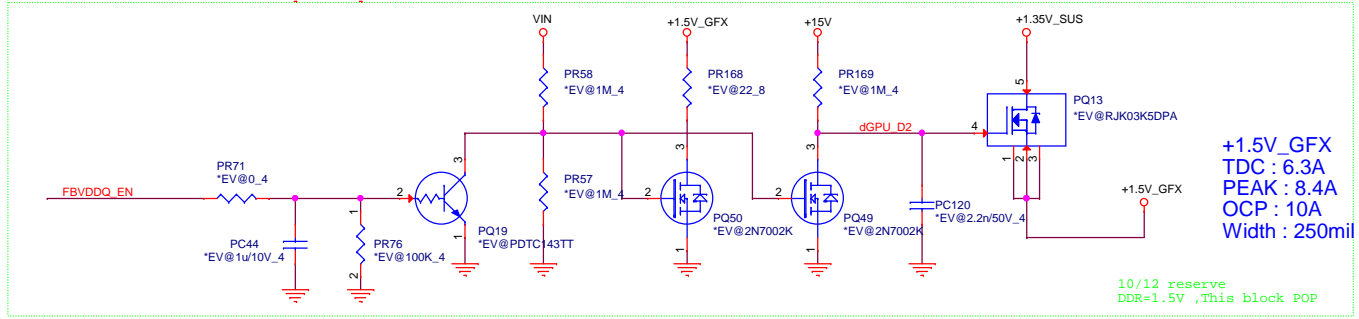


+1.05V_GFX
TDC : 2.3A
PEAK : 3A
Width : 100mil

10 DGPU_PWR_EN



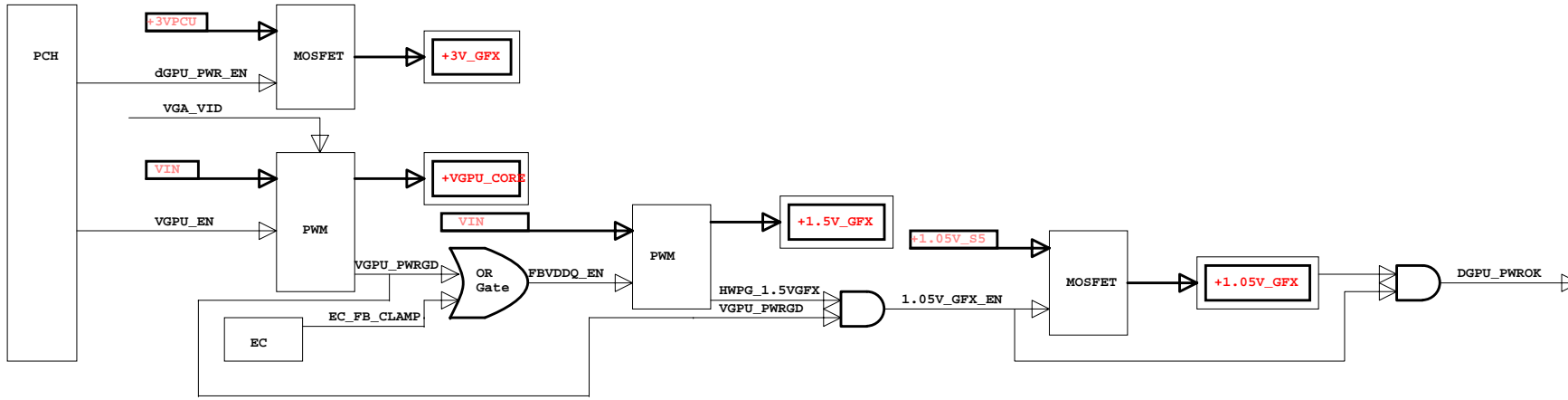
+3V_GFX
TDC : 0.76A
PEAK : 1A
Width : 40mil



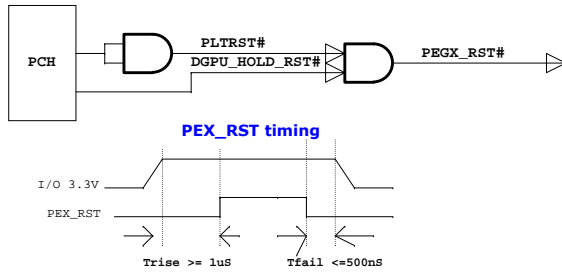
+1.5V_GFX
TDC : 6.3A
PEAK : 8.4A
OCP : 10A
Width : 250mil

10/12 reserve
DDR=1.5V ,This block POP

VGA power up sequence



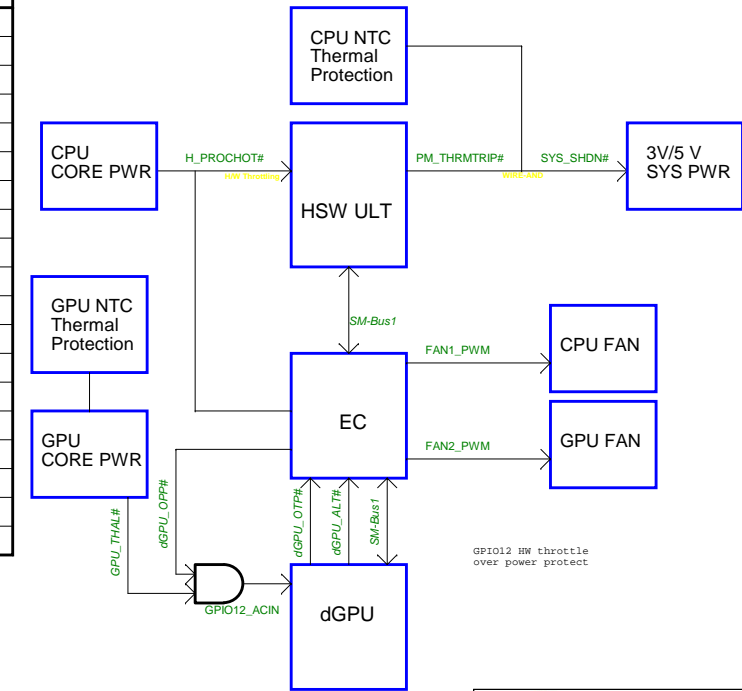
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.5V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

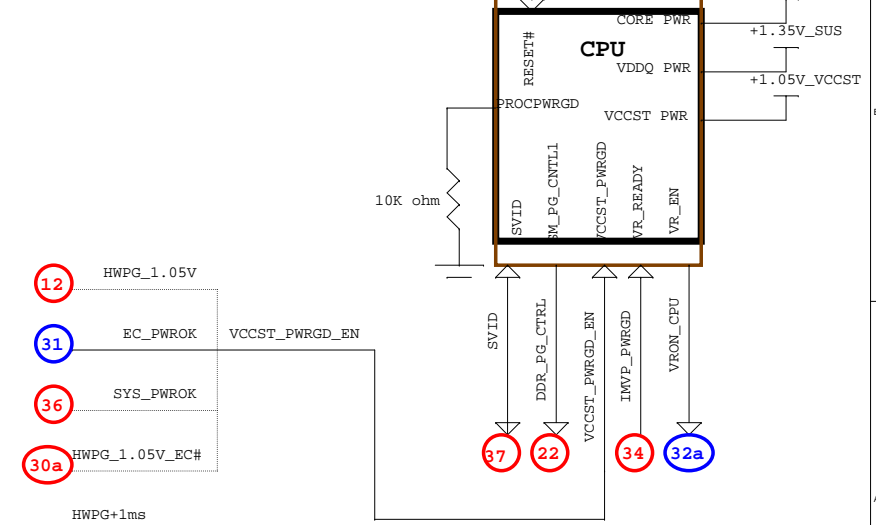
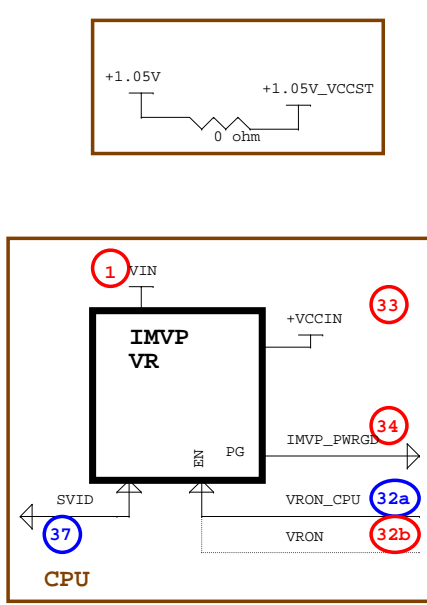
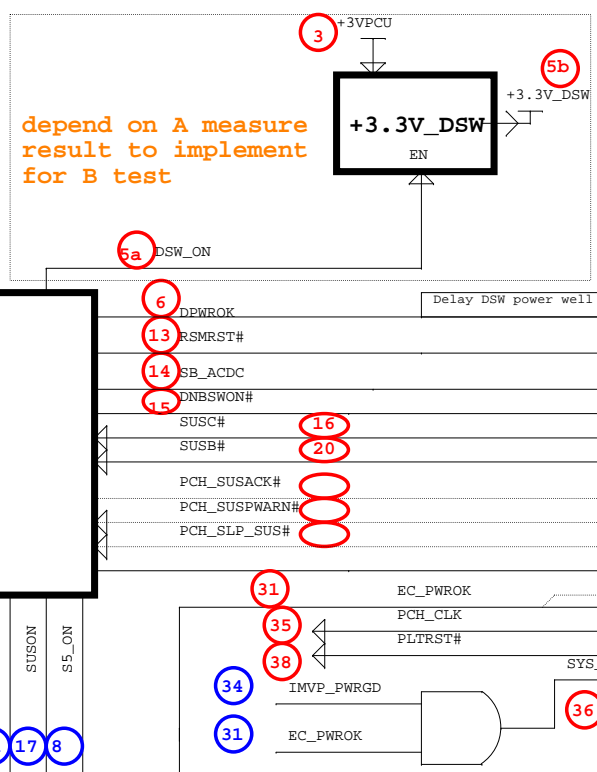
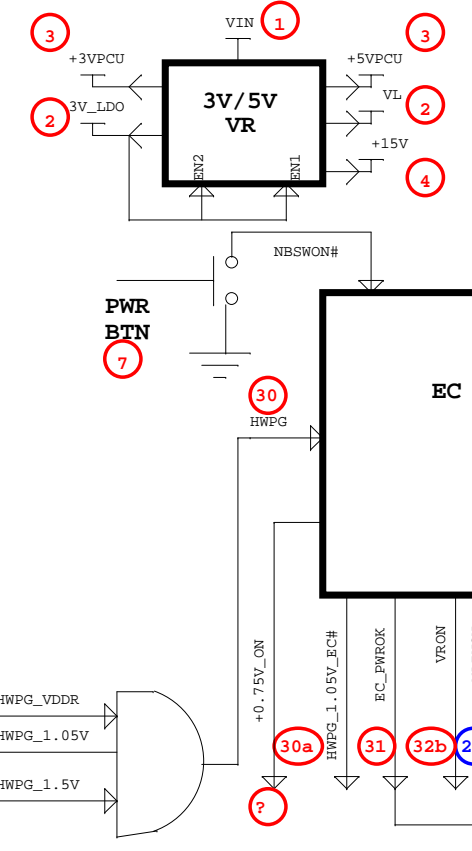
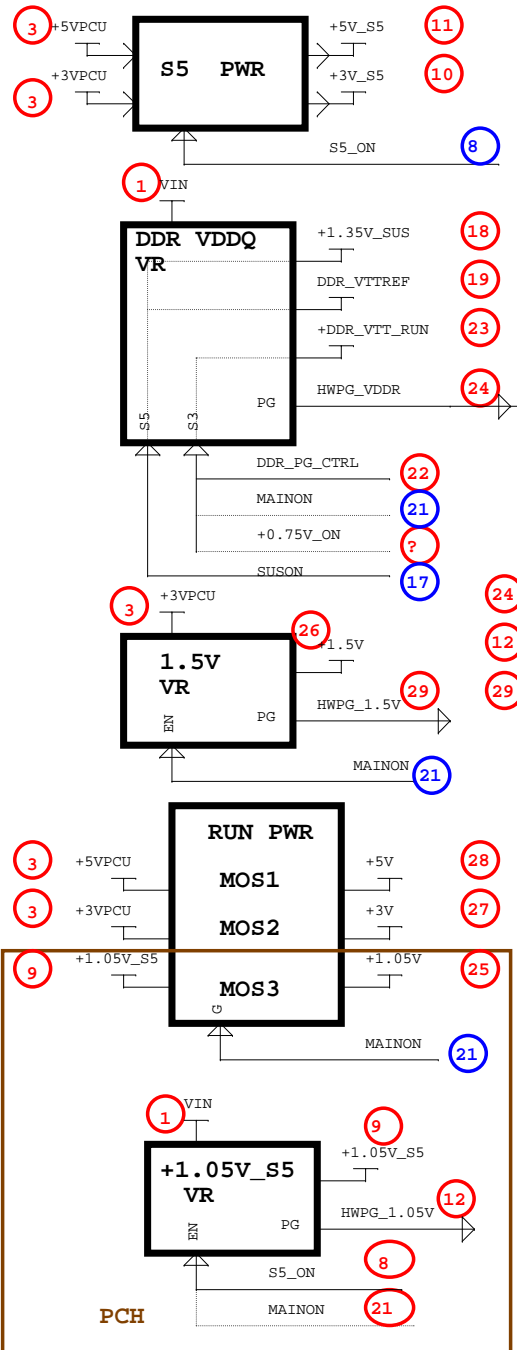
Thermal Follow Chart

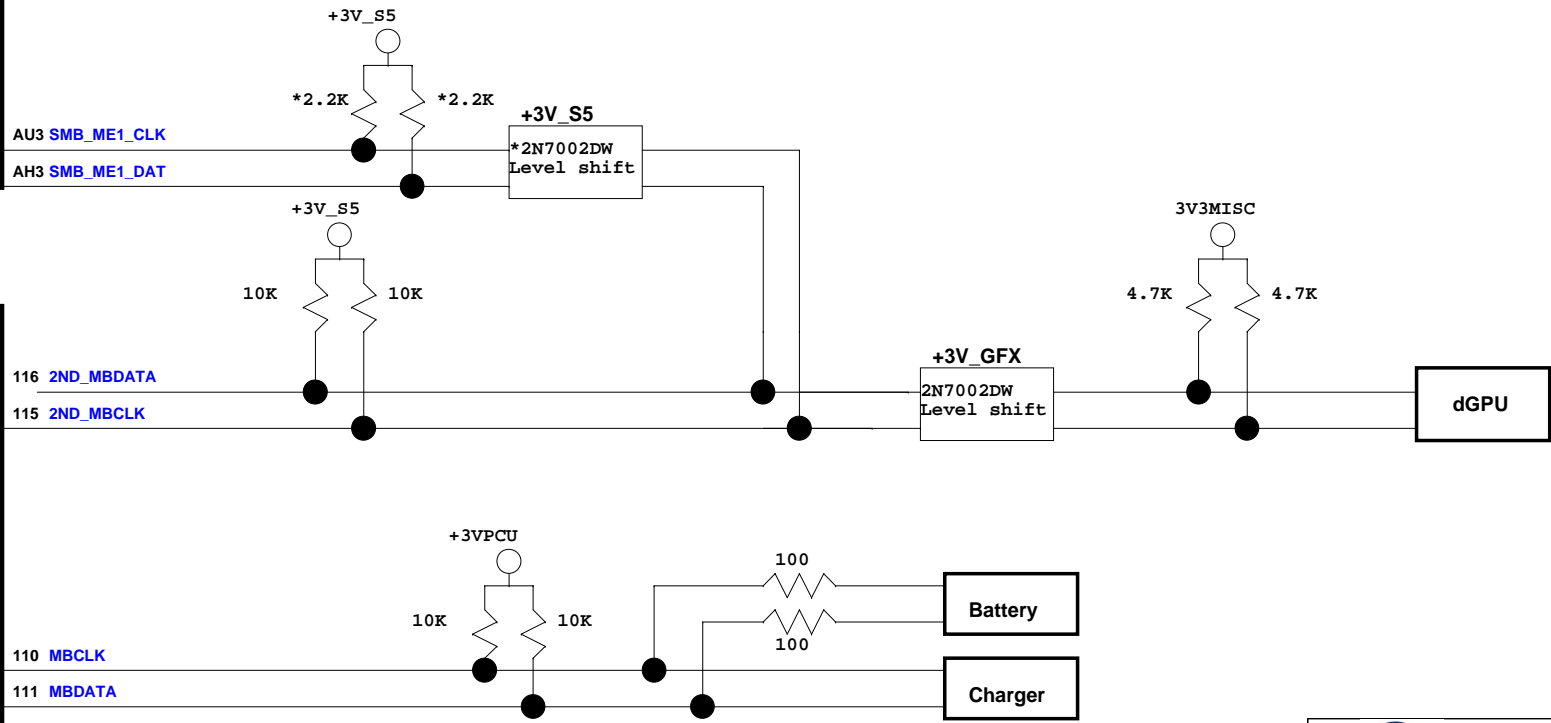
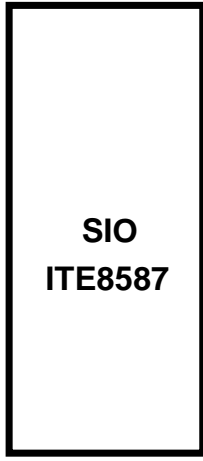
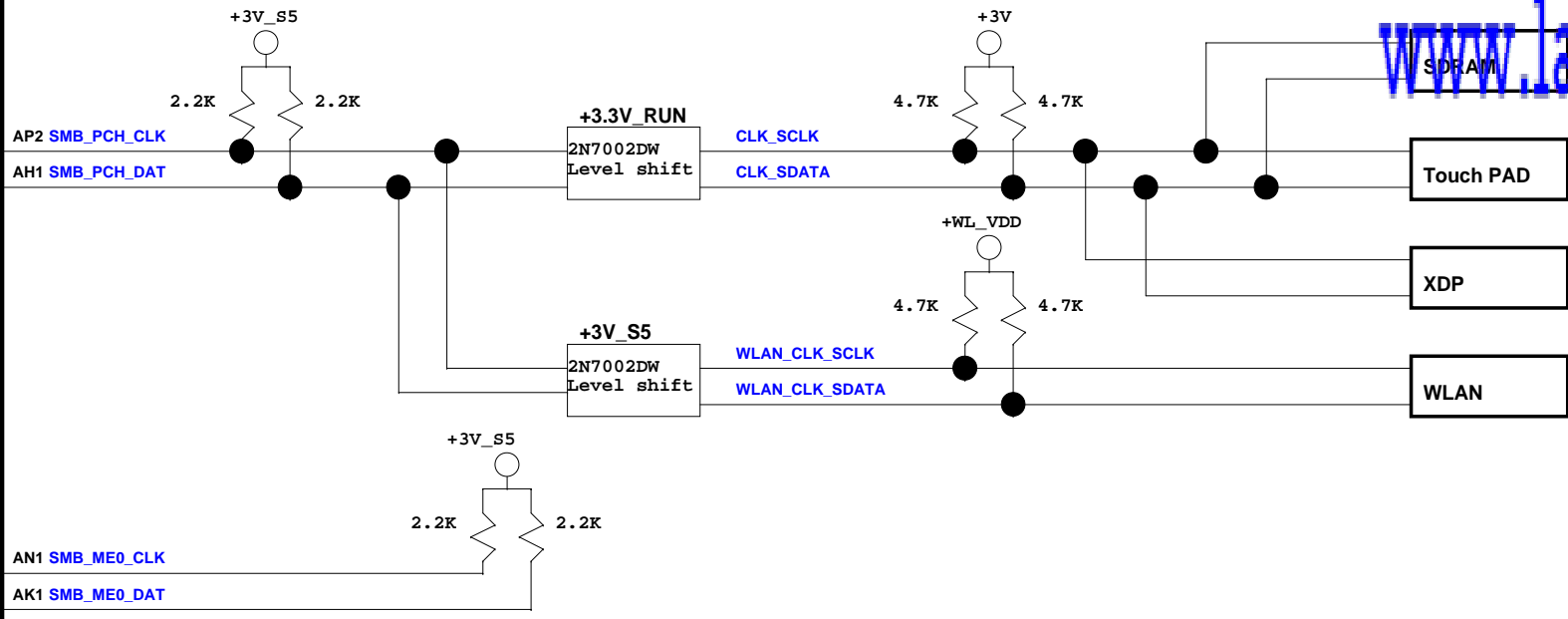
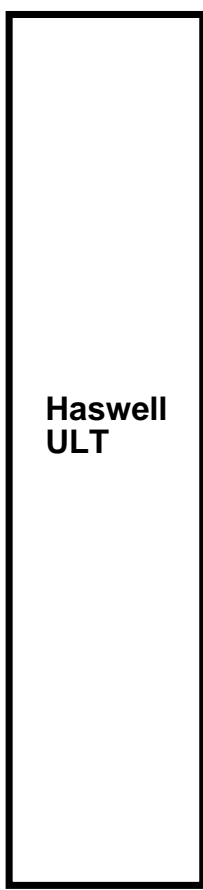


dGPU_OTPH# EC notify HW throttle over power protect
 dGPU_ALTH# for ADPS circuit to inform EC NV dGPU VPS Alert
 dGPU_OTPL# VGA thrmtrip# => Inform EC over temperature protect

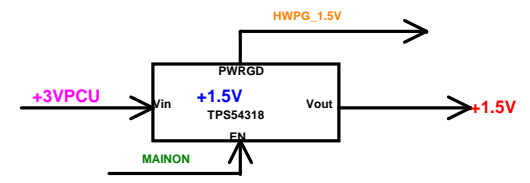
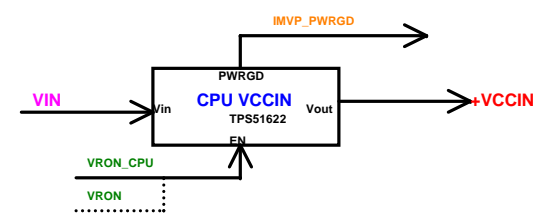
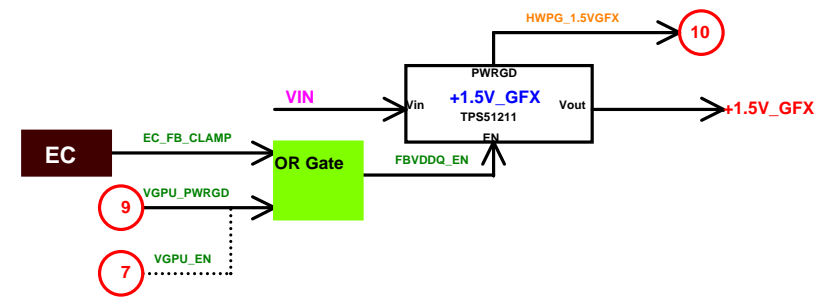
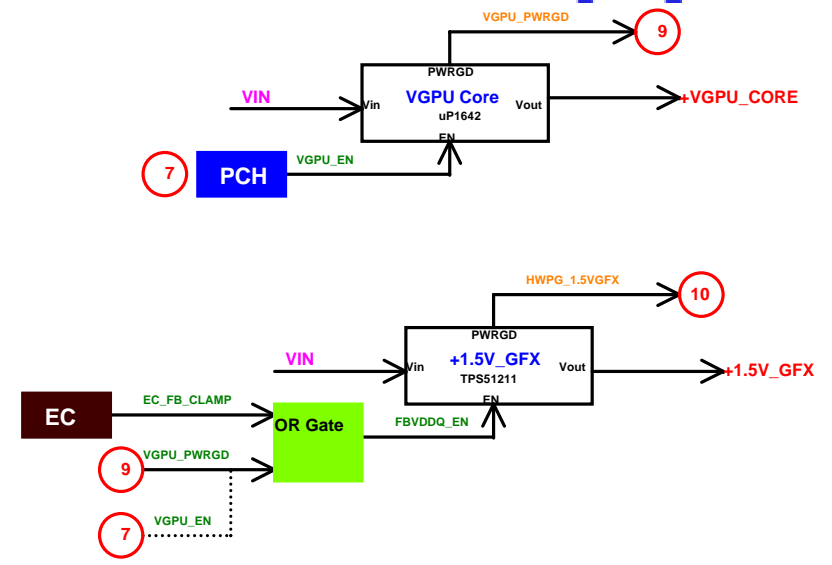
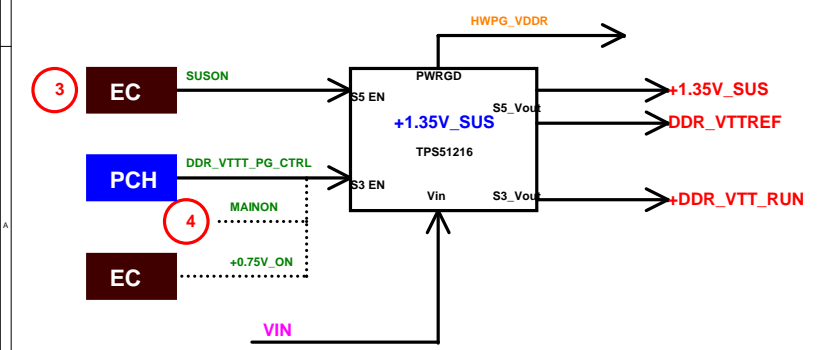
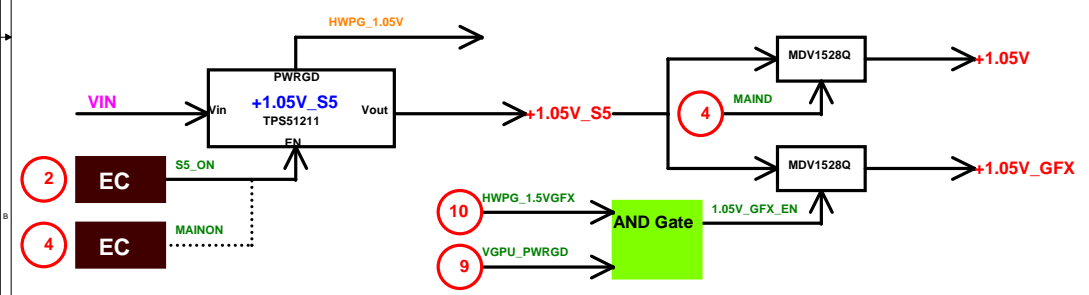
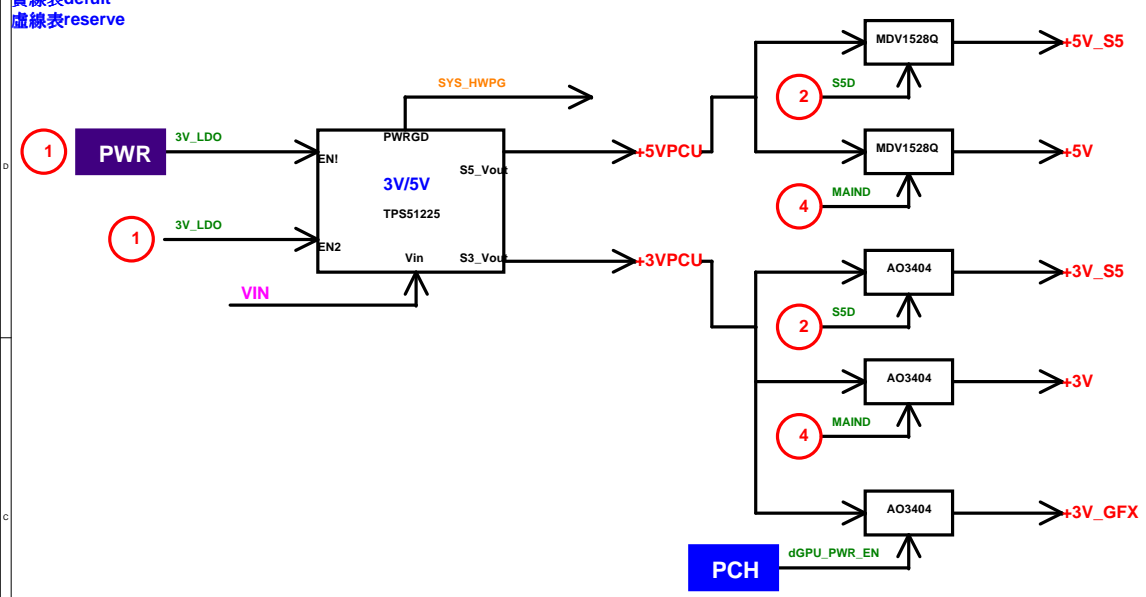
Battery Mode

Support Deep Sx





實線表default
虛線表reserve



Model	Version	CHANGE LIST			
ZRQ	1A				
	2A	1	Add R886 Pull down for EDP_HPD(Intel check List).(Page 02)		
		2	Add R811 and reserve R809 for Codes Vendor request.(Page 30)		
		3	Change R345 footprint from 0402 to 0603.(Page 14)		
		4	Change U10 to correct PN AL007534001.(Page 31)		
		5	Improve IMVP_PWIRGD voltage to low ,so del R66_Q9 ,R61_Q50,R495 and add U55 ,C767 ,R807 .(Page 10)		
		6	Change CN12 to 12 PIN connect_DFFC12FR034 .(Page 31)		
		7	Change SW6 from DHP08TEPV00 to DHPATE2CK03.(Page 29)		
		8	Move Hall sensor function to USB.B.(Page 24)		
		9	Add RS28 100K PD for MAINON, Upgrade U27 from AJ08SS70F02 to AJ08SS70F03 .(Page33)		
		10	Collect netname -v1.05S_VCCPCPU to -v1.3.S_VCCSDIO .(Page11)		
		11	Q7 change from PMF780SN to BAMB0020002 .(Page25)		
		12	Correct U41 footprint to s0055-p-a-to-shlha-b .(Page23)		
		13	Change LE5D6 PIN from BEB00024ZA0 to BEB00025ZA0 .(Page27)		
		14	Del Q5 ,Q47,R51,R25 , add U56,C768 .(Page13)		
		15	DEL_PL5,PLA,PL7,PL8 .(Page34 ,power)		
		16	Change PR145 from CS28872FB08 to CS2932FB13 .(Page38 ,Power)		
		17	Change PR143 from CS45362FB00 to CS4492FB11 .(Page38 ,Power)		
		18	Change PR129 from CS22672FB12 to CS22702FB14 .(Page38 ,power)		
		19	Change PR5 from CS1002FB26 to CS25762FB01 .(Page38 ,Power)		
		20	Change PR141 from CS32433FB19 to CS3262FB15 .(Page38 ,Power)		
		21	Change PC123 from CS64704MZ10 to CH6104KEA00 .(Page40 ,Power)		
		22	Add PC152,PC153,PC154 to CH6104KEA00 .(Page40 ,Power)		
		23	Change PL12,PL13 from CV-24P0MZ00 to CV-36T0MZ01 10X10 size .(Page40 ,Power)		
		24	SWAP USB0 and USB1 .(Page09)		
		25	Change CN27 to DFBIS2FR044 same as CN18 (Page 26)		
		26	add CN12 PIN4 for USBPWR3 .(Page 31)		
		27	CN9 change footprint to dp-adi0022-p001a-20p-smt .(Page 23)		
		28	Depop R728 and Pop R727 to save Deep S3 can't wake issue .(Page 10)		
		29	Del C429 .(Page20)		
		30	Add R826(VRON)_RS2780N) 100k to Gnd .(Page33)		
		31	Change CN9 FN to DFD20FR001 .(Page23)		
		32	Add C735 ,0.1u for Vendor request .(Page28)		
		33	Add C736 ,0.1u and reserve C727 ,4.7u for Vendor request .(Page29)		
		34	Change R348 Pull up to -3V .(Page28)		
		35	TEMP_MBAT from battery connect pin 5 to pin 6 (BATT_EN0) .(Page34)		
		36	Change R354(PCH_PWROK) from 10 k to 100K .(Page07)		
		37	Reverse R808 ,R810 ,0 Ohm .(Page30)		
		38	Change JP18 Packing and PN same as JP19 .(Page37)		
		39	Add R835 for Vendor request .(Page23)		
		40	Change R491 from 1M to 5.1M .(Page23)		
		41	Change R491 from 121 to 120ohm(Intel Check list) .(Page04)		
		42	Change S3SLEDPD power from -3V ,S3 to -3V_PCH .(Page27)		
		43	Change CN13 to DFBIS0F047 10-pin to PE request, Footprint is "ps12401-1011-40p-a-smt .(Page24)		
		44	VCPU_PSI Pull high from -3V to -3V_SS .(Page40)		
		45	B-SMT USE RT18411BA,CC need Depop R295 and change U21 PN to AL008411004 .(Page28)		
		46	C596,C591 change from 18P to 12P(V6) .(Page09)		
		47	C278,C284 change from 27P to 12P(V8) .(Page28)		
		48	Depop R147,R106,R04,R534 and Pop R91,R95,R146,R533 to support Qual Mode .(Page10)		
		49	Pop R9184.(Page40 ,Power) 内部行文		
		50	Change P18 from AL001642000 to AL001642001 .(Page40 ,Power) 内部行文		
		51	PCS EOD Part change to CH43118R006 .(Page38 ,Power)		
		52	PCS,PCS EOD Part change to CH21506B14 .(Page38,39 ,Power)		
		53	Change U27 from AJ08SS70F03 to AJ08SS70F04 .(Page33) 内部行文		
		54	Add level shift fuctions .(Page25)		
		55	Depop PR75 .(Page40 ,Power) 内部行文		
		56	Change PC15 to 1000p ,50V(CH21006B10) .(Page38 ,Power) 内部行文		
		57	Depop PR75 .(Page40 ,Power) 内部行文		
	3A	1	Depop R226 ,Pop Q26(BAM70020002)_R795 (CS1002FB26) for CG6 function.(Page19)		
		2	Swap Pin 25 and Pin 32.(Page33)		
		3	Del L01,C519 , and Add Q69,C738,C822,C823,C824 for SDA request.(Page23)		
		4	Add Test Pad on SWS_S08 for SMT request.(Page27,33)		
		5	Add C317 ,4.7u for Vendor request.(Page28)		
		6	SWAP CLKOUT_PCH .(Page09)		
		7	Pop R477 ,R478 ,R479 ,R480 _100ohm(CS11002FB22 for HDMI EMI Issue.(Page25)		
		8	Pop C655,C654 _10p(CB1006B008) for SD CLK EMI issue .(Page29)		
		9	Pop B10K C399 _22p(CB1206B008) for EMI issue .(Page30)		
		10	Del Pop PR117 .(Page34)		
		11	C285 change from 0402 to 0603 size .(Page28)		
		12	Del CN5,C272,C253 footprint .(Page13)		
		13	Depop R336 ,Pop R533 for Lan can't link to exlurer .(Page28)		
		14	Depop R548 .(Page28)		
		15	Reverse R512 for PCH_LAN_WAKE# .(Page26)		
		16	Add R815,R740 and pop R310 for software of Lan VCC.(Page20)		
		17	R608 connect to CLK_PCH_REQ04# .(Page09)		
		18	Depop SWS .(Page23)		
		19	Del JP Resistor 0.001F_3720 (CS-00187L00)_JP5,JP6,JP10,JP11,JP12,JP13,JP14,JP15,JP17,JP18,JP19,JP20,JP21,JP16		
		20	Del 0 ,4 (CS00002B30) to SHORT PAD ,4 : PR8,PR9,PR11,PR13,PR16,PR18,PR20,PR23,PR33,PR44,PR61,PR66,PR68,PR106,PR131,PR139,PR165,PR170,PR178,PR180,PR185,PR191,PR193,PR194,PR196,PR200,PR204,PR205,PR209,PR211,PR217,PR186		
		21	Del 0 ,6 (CS00003J95) to SHORT PAD ,6 : PR31,PR46,PR54,PR57,PR90,PR181,PR201,PR203,PR215,PR158		
		22	Del 0 ,8 (CS00004A40) to SHORT PAD ,8 : PR136		
		23	Add R813 ,0 OHM.(Page26)		
		24	Change C740 from 0603 to 0402 size.(Page28)		
		25	Depop Q39 ,R276,Pop R321 and change R320 to 1K to meet Lanwake signal spec.(Page28)		
		26	Depop U5A-11L-1JL28 ; and Pop R34,R47,R49,R55,R490,R487,R488,R489.(Page20)		
		27	Del JP7 ,JP8 ,JP9(CS-001AGM13).(Page05)		
		28	Change to 0402 shortpad:R45,R69,R173,R215,R236,R237,R239,R274,R277,R283,R288,R311,R320,R334,R353,R404,R409,R419,R423,R424,R425,R426,R430,R432,R434,R448,R449,R450, R513,R570,R573,R587,R591,R596,R625,R641,R652,R653,R678,R695,R712,R719,R722,R733,R734,R735,R736,R741,R758,R759,R760,R761,R762,R763,R764,R765		
		29	Change to 0603 shortpad:R107,R111,R158,R194,R197,R212,R229,R233,R234,R252,R269,R298,R303,R304,R338,R350,R351,R352,R356,R388,RR411,R15,R418,R422,R441,R433,R440,R441, R442,R443,R444,R445,R446,R447,R540,R745,R766,R767		
		30	Change to 0805 shortpad:R165,R174,R179,R190,R217,R228,R270,R452,R470,R559,R560,R732,R757,R749		
		31	Change R408,R420 from 47 ohm to 56 ohm.(Page30)		
		32	Change R411 ,R422 from shortpad to 0603 Footprint.(Page30)		
DOC NO.	PROJECT MODEL	ZRQ	APPROVED BY:	DATE:	
	PART NUMBER:		DRAWING BY:	REVISION:	

CHANGE LIST

Model

Version

ZRQ

3B

- 1 R276 change from 10K to 1K ,Depop R320. (PCIE_LAN_WAKE#), 内部行文
- 2 Change C24 KB Conn FN to DFPC26F8063 .(Page 32), 内部行文
- 3 Change I27 EC to E version A1088870F85 .(Page 33), 内部行文
- 4 Fine tune Amp Gain =>R422,R411 change from 0 ohm to 1k , and pop R421,R410 to 1.62K .(Page 30)
- 5 Change TEMP_MBAT from Pin 6 to Pin 5 of P.J1 .(Page 34)
- 6 Depop Q24 , and Add R228 to solve level abnormal issue for CG6 .(Page 19)
- 7 Add R816 and net "LE_PWR_CNN_Q" to stiff Q69 always for safety issue .(Page 19)
- 8 Reverse R855,R859 and add R854,R857 .(Page 23)
- 9 For WHQL Change USB Part1 and Part4
- 10 Add new on Board RAM HYNIX H5TC4G63AFR-PRBA RAM ID:0000
- 11 Del L35L36,L6,L7,L8,L29,L112,L131,L32,L116,L134

3C

- 12 Change to 0402 shortpad: R725,R724,R711,R716,R26,R27,R28,R29,R32,R33,R483,R484,R493,R492,R56,R57,R58,R59, R90,R89,R66,R664,R702,R638,R639,R651,R225,R246,R355,R779,R785,R790,R73 , R455,R456,R457,R458,R459,R443,R406,R596
- 13 For HDMI 7-2 issue change R37,R38,R39,R40,R41,R42,R43,R44 To 470 ohm and remove R478,R479,R477,R480 (Page 25)
- 14 For TI HDSS5251 issue R77,R79,R502,R503 need mount 10K, change R528 from 100 ohm to 0 ohm and remove R854,R857 , add R855,R859. (Page 23)
- 15 Change to 0603 shortpad: R373,R337,R382,R297,R235,R326,R322,L38,R385,R220,R254,R359