

H100 series

INTEGRATED CIRCUITS

INTERMEDIATE TEMPERATURE RANGE
-40°C TO 85°C

- WIDE RANGE OF SUPPLY VOLTAGE
10.8V TO 16V
- HIGH DC NOISE IMMUNITY 5V (TYP.) AT
 $V_{CC} = 15V$
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS IC'S

High level logic family

High Level Logic is a family of high threshold integrated circuits.

It offers the advantages of 5V DC noise immunity, high signal levels, large supply voltage tolerances and unusually high fan-out.

These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.

The H 100 series elements are available in the hermetically sealed ceramic dual in-line package.

ABSOLUTE MAXIMUM RATINGS

| | |
|--|----------------|
| Supply Voltage (V_{CC}) continuous | 18V |
| Input Voltage | -0.5V to 16V |
| Storage Temperature Range | -65°C to 150°C |

OPERATING CONDITIONS

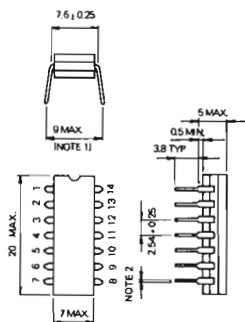
| | |
|-----------------------|---------------|
| Operating Temperature | -40°C to 85°C |
| Supply Voltage | 10.8V to 16V |

ORDERING NUMBER

H1XX D6

PHYSICAL DIMENSIONS

14 pin ceramic DIP

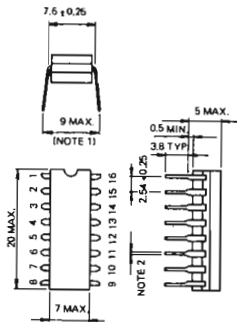


NOTES

- 1) Leads are intended for insertion in hole rows on 7.6 mm centres. They are purposely shipped with "positive" (9 mm.) misalignment to facilitate insertion.
- 2) Board-drilling dimensions should equal your practice for a conventional 0.51 mm. diameter lead.
- 3) All dimensions in mm.

PHYSICAL DIMENSIONS

16 pin ceramic DIP

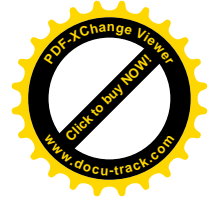


NOTES

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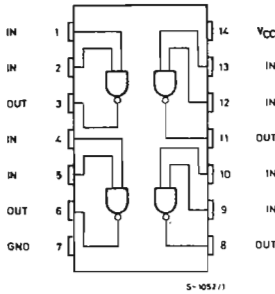
H100 series



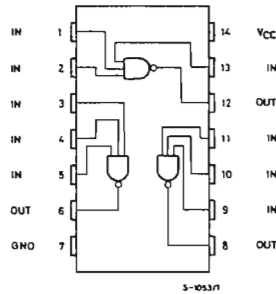
INTERMEDIATE TEMPERATURE RANGE

CONNECTION DIAGRAMS

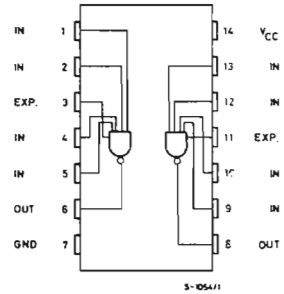
H 102/H 122



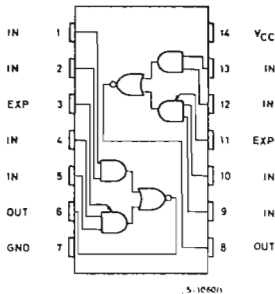
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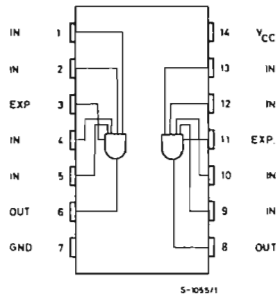
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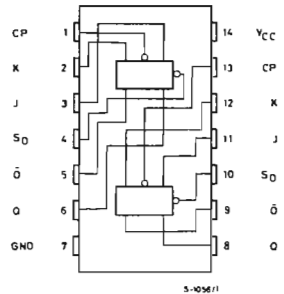
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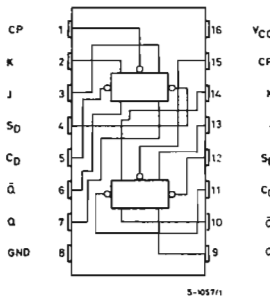
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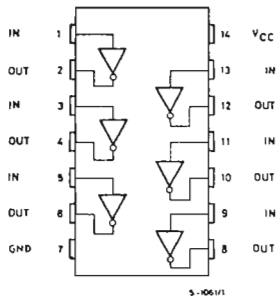
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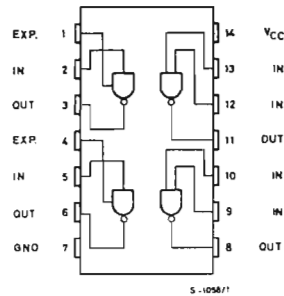
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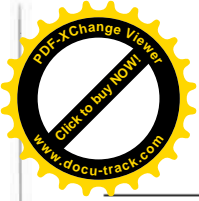


H 112/H 118



H 113

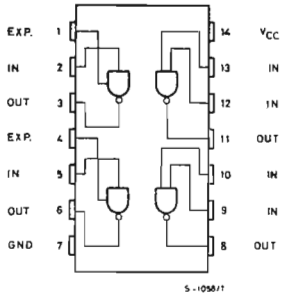




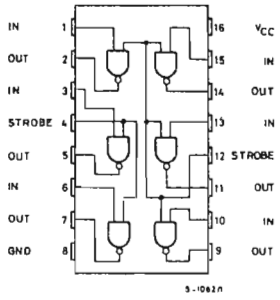
INTERMEDIATE TEMPERATURE RANGE

CONNECTION DIAGRAMS (continued)

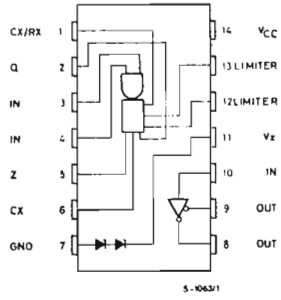
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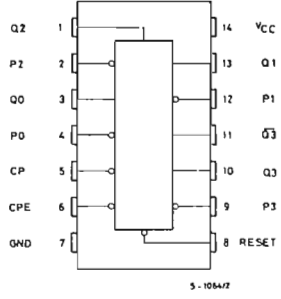
H 115/H119



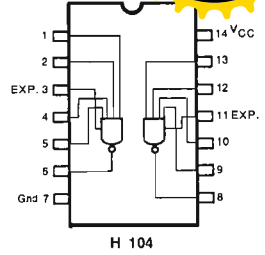
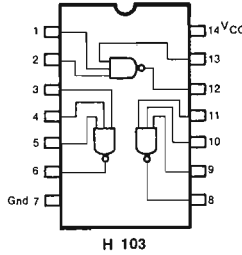
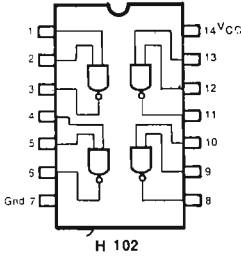
H 117



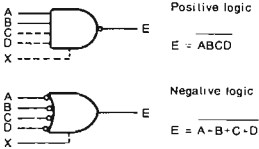
H 156



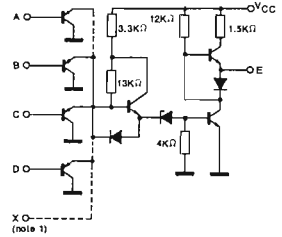
CONNECTION DIAGRAMS (Top view)



LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)



ELECTRICAL CHARACTERISTICS

| SYMBOL | CHARACTERISTIC | -40°C | | 25°C | | 85°C | | UNIT | CONDITIONS |
|-------------------|--|-------|-------|-------|-------|-------|-------|------|--|
| | | Min. | Max. | Min. | Typ. | Max. | Min. | | |
| V _{OH} | Output High Voltage | 14.5 | 9.3 | 14.5 | 15 | 9.3 | 9.8 | V | V _{CC} = 16V V _{CC} = 10.8V V _{IN} = V _{IL} I _{OH} = -200μA I _{OH} = -200μA (see below) |
| V _{OL} | Output Low Voltage | 1.5 | | 1 | | 1.5 | | V | V _{CC} = 16V V _{CC} = 10.8V V _{IN} = V _{IH} I _{OL} = 12.5mA I _{OL} = 9mA (see below) |
| V _{IL} | Input Low Voltage | 6 | | 6 | | 6 | | V | Guaranteed Input Low Threshold for All Inputs |
| V _{IH} | Input High Voltage | 8 | | 8 | | 8 | | V | Guaranteed Input High Threshold for All Inputs |
| I _F | Input Low Current | -0.5 | -0.36 | -0.08 | -0.5 | -0.06 | -0.36 | mA | V _{CC} = 16V } V _F = 1.5V V _{CC} = 10.8V } |
| I _{FEX} | Expander Input Low Current (Note 2) | -1.4 | -1 | -0.9 | -1.4 | -0.75 | -1 | mA | V _{CC} = 16V } V _{FEX} = 2V V _{CC} = 10.8V } |
| I _R | Reverse Input Current | 5 | | 0.1 | | 5 | | μA | V _{CC} = 16V V _R = 16V |
| I _{SC} | Output Short Circuit Current | -6.5 | -20 | -6.5 | -13.5 | -20 | -6.5 | mA | V _{CC} = 16V Inputs and Output Grounded |
| I _{PDH} | High Level Power Dissipation Current (Each Gate) | 6 | | 4.4 | | 6 | | mA | V _{CC} = 16V Inputs High |
| I _{PDFL} | Low Level Power Dissipation Current (Each Gate) | 2 | | 1.2 | | 2 | | mA | V _{CC} = 16V Inputs Low |
| TPD ₊ | Turn-Off Delay | | | 160 | | 250 | | nsec | V _{CC} = 15V See Test Circuit |
| TPD ₋ | Turn-On Delay | | | 50 | | 100 | | nsec | V _{CC} = 15V See Test Circuit |

NOTES: 1) The node can be expanded using EB383 or BAY72 diodes
2) For H104 only