FT6X36

Self-Capacitive Touch Panel Controller

INTRODUCTION

The FT6X36 Series ICs are single-chip capacitive touch panel controller IC with a built-in 16 bit enhanced Micro-controller unit (MCU).They adopt the self-capacitance technology, which supports single point and gesture touch or two points. In conjunction with a self-capacitive touch panel, The FT6X36 Series ICs implement the user-friendly input function and are widely used in various portable devices, such as smart phones, MIDs ad GPS.

The FT6X36 series ICs include FT6236/FT6336/FT6436L/FT6436, the difference of their specifications will be listed individually in this datasheet.

FEATURES

- Self-Capacitive Sensing Techniques support single point touch and gesture or two point touch
- Absolute X and Y coordinates or gesture
- 1 point and gestures / 2 points supported
- High immunity to RF and power Interferences
- Auto-calibration: Insensitive to Capacitance and Environmental Variations
- Built-in Enhanced MCU
- FT6236 supports up to 22 or 28 channels of sensors /drivers
- FT6336 supports up to 36 channels of sensors /drivers
- FT6436L supports up to 42 channels of sensors /drivers
- FT6436 supports up to 46 channels of sensors /drivers
- Report Rate: Up to 100Hz
- Support Interfaces :I2C
- Support single film material TP and triangle pattern without additional shield
- Internal accuracy ADC and smooth filters
- Support 2.8V to 3.6V Operating Voltage
- Support independent IOVCC
- Built-in LDO for Digital Circuits
- High efficient power management with 3 Operating Modes
  - Active Mode
  - Monitor Mode
  - Hibernation Mode
- Operating Temperature Range: -40℃ to +85℃
- ESD:HBM≥7000V,MM≥350V

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT6X36 accommodate a wide range of applications with a set of buttons up to a 2D touch sensing device, their typical applications are listed below.

- Mobile phones, smart phones
- GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras
- MIDs

FT6X36 series ICs support up to 5.5 inch Touch Panel; users may find out their target IC from the specs listed in the following table,

Model Name	Panel	Package			Touch Panel Size
	Channel	Type	Pin	Size	
FT6236HMg	22	QFN4*4	32	0.5-P0.4	≤3.0"
FT6236GMA	28	QFN5*5	40	0.6-P0.4	≤4.0"
FT6336DMB	36	QFN6*6	48	0.6-P0.4	≤4.5 inch
FT6436LDQb	42	QFN6*6	56	0.6-P0.35	≤5.0 inch
FT6436DQf	46	QFN6*6	56	0.6-P0.35	≤5.5 inch

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT6X36.

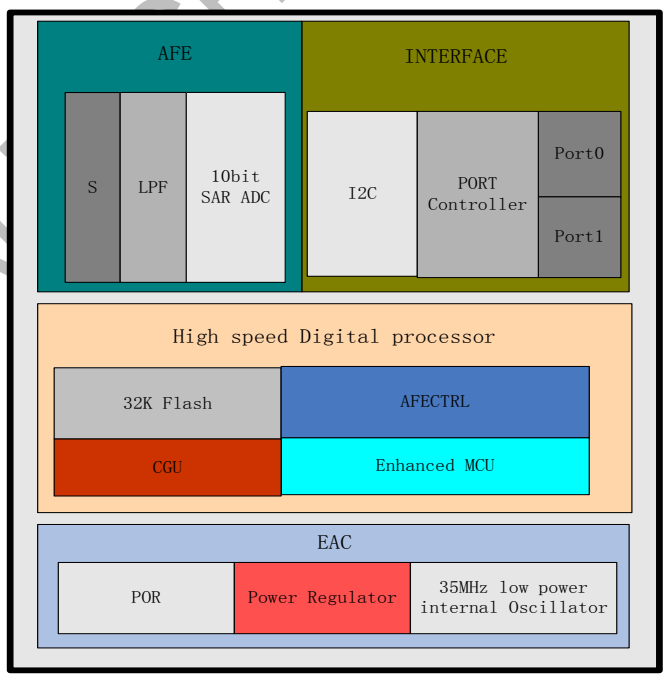


Figure 2-1 FT6X36 System Architecture Diagram

The FT6X36 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So it supports both driver and Sensor functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU

For the Enhanced MCU, larger program and data memories are supported. Furthermore, A Flash ROM is implemented to store programs and some key parameters.
Complex signal Processing algorithms are implemented by MCU to detect the touches reliably and efficiently.
Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDDA supply.

2.2 MCU

This section describes some critical features and operations supported by the Enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the Enhanced MCU core, we have added the following circuits,

- Memory:32KB Flash
- Data Memory: 4KB SRAM
- Timer: A number of timers are available to generate different clocks
- Master Clock:17.5MHz from a 35MHz RC Oscillator
- Clock Manager: To control various clocks under different operation conditions of the system

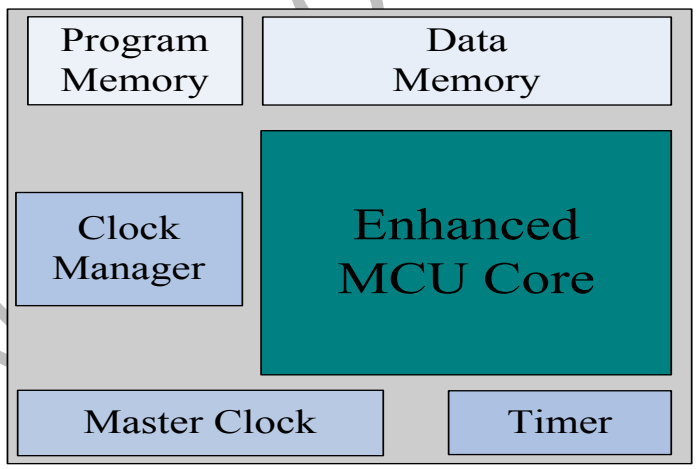


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT6X36 operates in the following three modes:

- Active Mode

In this mode, FT6X36 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT6X36 to speed up or to slow down.

- Monitor Mode

In this mode, FT6X36 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT6X36 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor

- Hibernation Mode

In this mode, the chip is set in a power down mode. It shall respond to the “RESET” or “Wakeup” signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

Host Interface Figure *2-3* shows the interface between a host processor and FT6X36. This interface consists of the following three sets of signals:

- Serial Interface
- Interrupt from FT6X36 to the Host
- Reset Signal from the Host to FT6X36

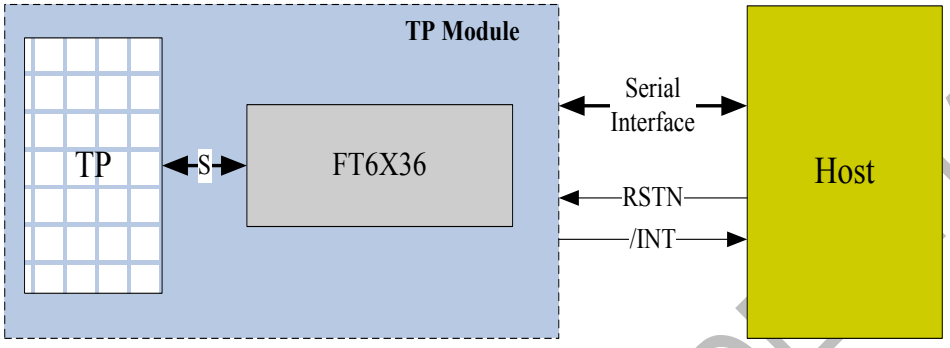


Figure 2-3 Host Interface Diagram

The serial interface of FT6X36 is I2C. The details of this interface are described in detail in Section 2.5. The interrupt signal (/INT) is used for FT6X36 to inform the host that data are ready for the host to receive. The RSTN signal is used for the host to reset FT6X36. After resetting, FT6X36 shall enter the Active mode.

2.4 Serial Interface

FT6X36 supports the I2C interfaces, which can be used by a host processor or other devices.

2.4.1 I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

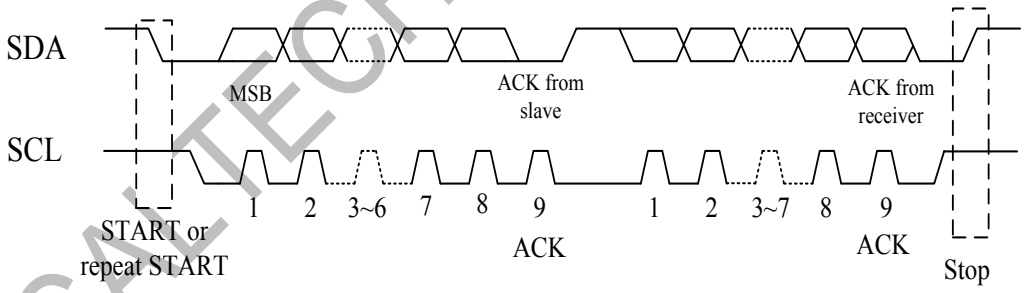


Figure 2-4 I2C Serial Data Transfer Format

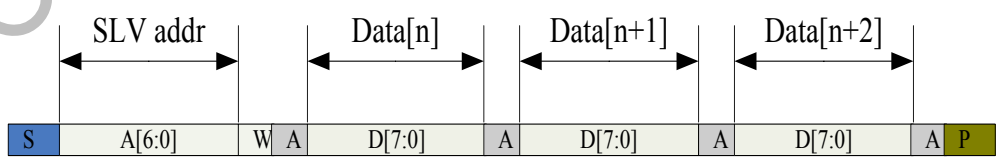


Figure 2-5 I2C master write, slave read

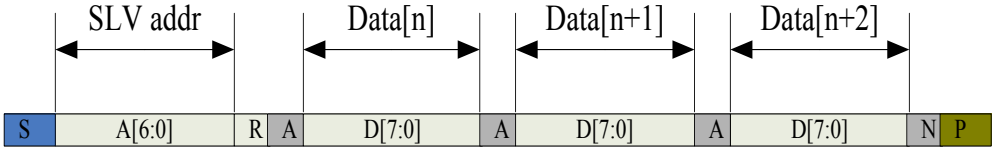


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDDA - VSSA	-0.3 ~ +3.6	V	1, 2
Power Supply Voltage2	VDD3 - VSS	-0.3 ~ +3.6	V	1, 3
I/O Digital Voltage	IOVCC	1.8~3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes

1. If used beyond the absolute maximum ratings, FT6X36 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VDDA (high) ≥VSSA (low).
3. Make sure VDD(high) ≥VSS(low).

3.2 DC Characteristics

Table 3-2 DC Characteristics (VDDA=2.8~3.6V, Ta=-40~85℃)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 x IOVCC	-	IOVCC	V	
Input low -level voltage	VIL		-0.3	-	0.3 x IOVCC	V	
Output high -level voltage	VOH	IOH=-0.1mA	0.7 x IOVCC	-	-	V	
Output low -level voltage	VOL	IOH=0.1mA	-	-	0.3 x IOVCC	V	
I/O leakage current	ILI	Vin=0~VDDA	-1	-	1	μA	
Current consumption （Normal operation mode）	Iopr	VDDA =VDD3= 2.8V Ta=25℃ MCLK=17.5MHz	-	4	-	mA	
Current consumption （Monitor mode）	Imon	VDDA =VDD3= 2.8V Ta=25℃ MCLK=17.5MHz	-	1.5	-	mA	
Current consumption （Sleep mode）	Islp	VDDA =VDD3= 2.8V Ta=25℃ MCLK=17.5MHz	-	50	-	uA	
Step-up output voltage	VDD5	VDDA = VDD3=2.8V	-	5	-	V	
Power Supply voltage	VDDA VDD3		2.8	-	3.3	V	

3.3 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V； Ta=25℃	34.65	35	35.35	MHz	

Table 3-4 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V； Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V； Ta=25℃	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V； Ta=25℃	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V； Ta=25℃	-	5	-	V	

3.4 I/O Ports Circuits

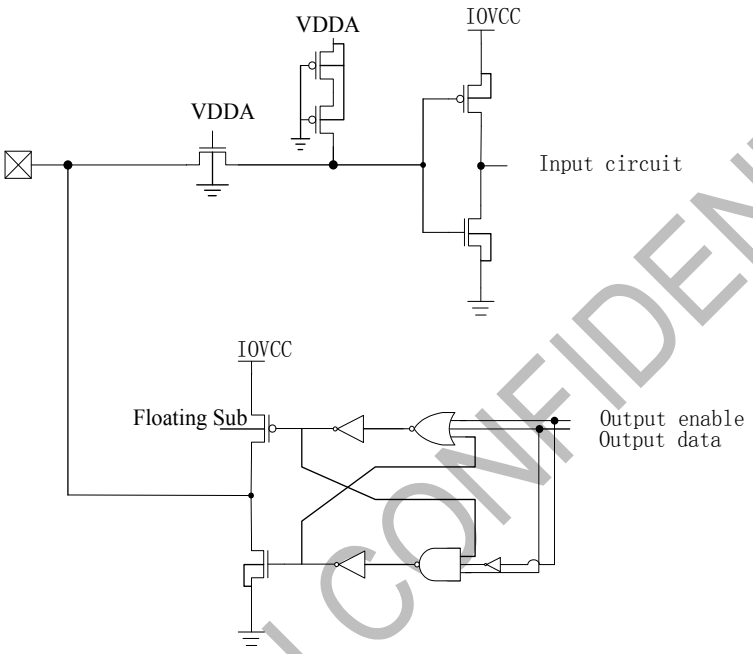


Figure 3-1 Digital In/Out Port Circuit

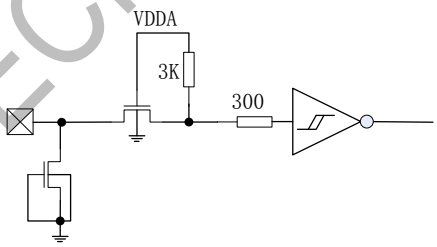


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset/Wake Sequence

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on. INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

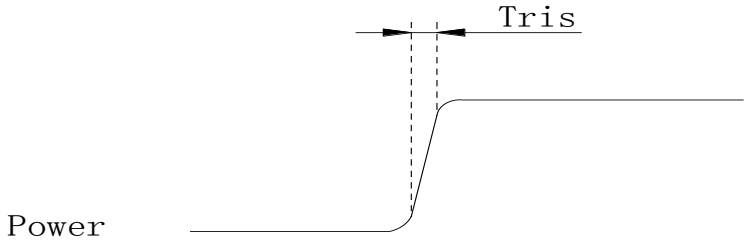


Figure 3-7 Power on time

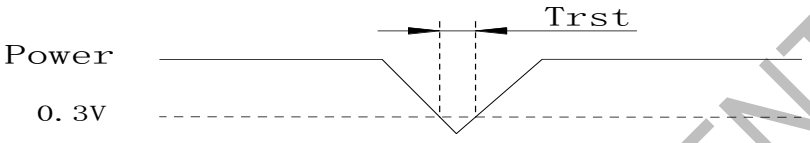


Figure 3-8 Power Cycle requirement

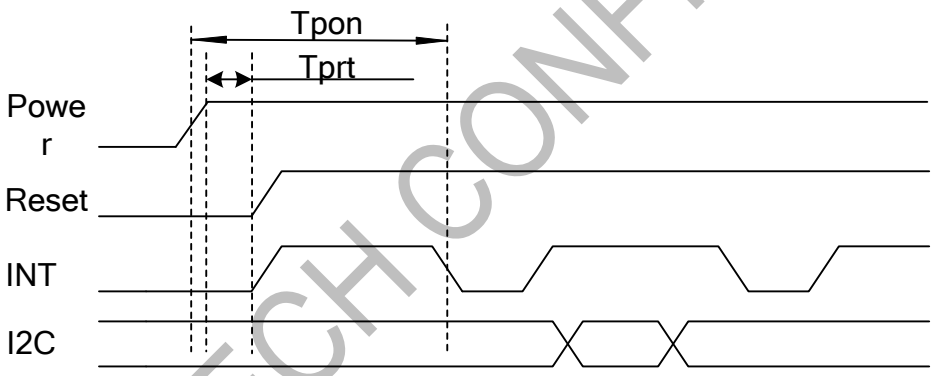


Figure 3-9 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

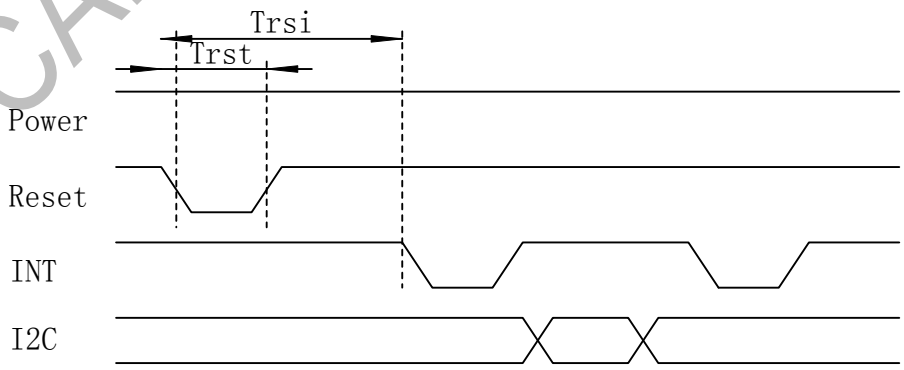


Figure 3-10 Reset Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units

Tris	Rise time from 0.1VDD to 0.9VDD	-	3	ms
Tpon	Time of starting to report point after powering on	300	-	ms
Tprt	Time of being low after powering on	1	-	ms
Trsi	Time of starting to report point after resetting	300	-	ms
Trst	Reset time	5	-	ms

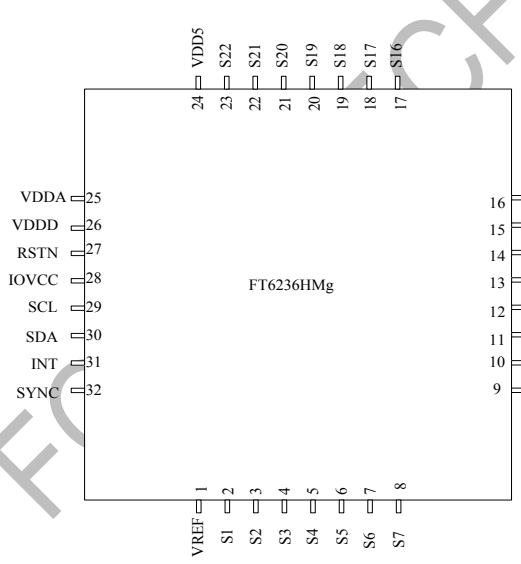
4 PIN CONFIGURATIONS

Pin List of FT6X36

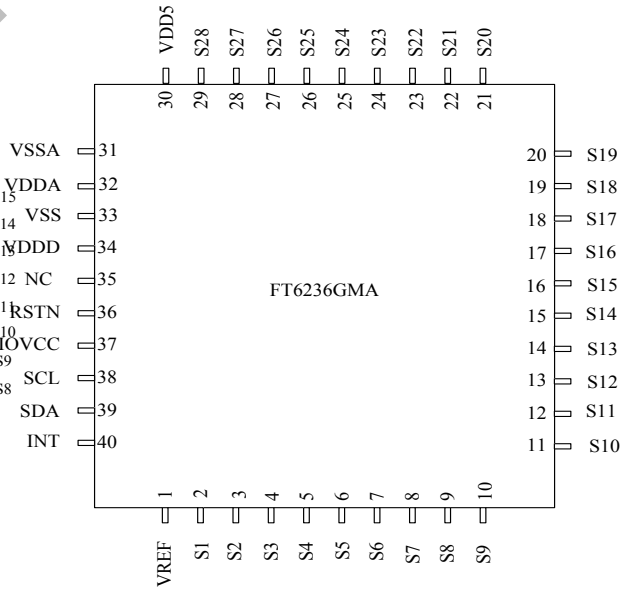
Table 4-1 Pin Definition of FT6X36

Name	Pin No.					Type	Description
	FT6236H Mg	FT6236G MA	FT6336D MB	FT6436D Qf	FT6436L DQb		
VREF	1	1	47	56	53	PWR	Generated internal reference voltage. A 1μF ceramic capacitor to ground is required.
S1	2	2	48	1	54	I/O	Capacitance sensor /driver channel
S2	3	3	1	2	55	I/O	Capacitance sensor /driver channel
S3	4	4	2	3	56	I/O	Capacitance sensor /driver channel
S4	5	5	3	4	1	I/O	Capacitance sensor /driver channel
S5	6	6	4	5	2	I/O	Capacitance sensor /driver channel
S6	7	7	5	6	3	I/O	Capacitance sensor /driver channel
S7	8	8	6	7	4	I/O	Capacitance sensor /driver channel
S8	9	9	7	8	5	I/O	Capacitance sensor /driver channel
S9	10	10	8	9	6	I/O	Capacitance sensor /driver channel
S10	11	11	9	10	7	I/O	Capacitance sensor /driver channel
S11	12	12	10	11	8	I/O	Capacitance sensor /driver channel
S12	13	13	11	12	9	I/O	Capacitance sensor /driver channel
S13	14	14	12	13	10	I/O	Capacitance sensor /driver channel
S14	15	15	13	14	11	I/O	Capacitance sensor /driver channel
S15	16	16	14	15	12	I/O	Capacitance sensor /driver channel
S16	17	17	15	16	13	I/O	Capacitance sensor /driver channel
S17	18	18	16	17	14	I/O	Capacitance sensor /driver channel
S18	19	19	17	18	15	I/O	Capacitance sensor /driver channel
S19	20	20	18	19	16	I/O	Capacitance sensor /driver channel
S20	21	21	19	20	17	I/O	Capacitance sensor /driver channel
S21	22	22	20	21	18	I/O	Capacitance sensor /driver channel
S22	23	23	21	22	19	I/O	Capacitance sensor /driver channel
S23		24	22	23	20	I/O	Capacitance sensor /driver channel
S24		25	23	24	21	I/O	Capacitance sensor /driver channel
S25		26	24	25	22	I/O	Capacitance sensor /driver channel
S26		27	25	26	23	I/O	Capacitance sensor /driver channel
S27		28	26	27	24	I/O	Capacitance sensor /driver channel
S28		29	27	28	25	I/O	Capacitance sensor /driver channel
S29			28	29	26	I/O	Capacitance sensor /driver channel
S30			29	30	27	I/O	Capacitance sensor /driver channel
S31			30	31	28	I/O	Capacitance sensor /driver channel
S32			31	32	29	I/O	Capacitance sensor /driver channel
S33			32	33	30	I/O	Capacitance sensor /driver channel
S34			33	34	31	I/O	Capacitance sensor /driver channel
S35			34	35	32	I/O	Capacitance sensor /driver channel
S36			35	36	33	I/O	Capacitance sensor /driver channel
S37				37	34	I/O	Capacitance sensor /driver channel

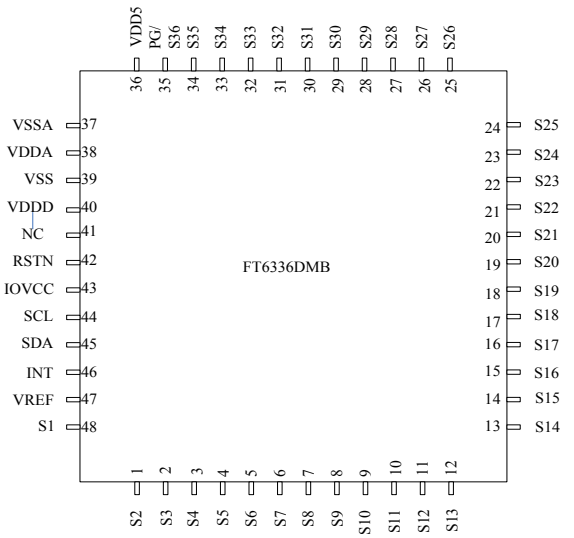
S38				38	35	I/O	Capacitance sensor /driver channel
S39				39	36	I/O	Capacitance sensor /driver channel
S40				40	37	I/O	Capacitance sensor /driver channel
S41				41	38	I/O	Capacitance sensor /driver channel
S42				42	39	I/O	Capacitance sensor /driver channel
S43					40	I/O	Capacitance sensor /driver channel
S44					41	I/O	Capacitance sensor /driver channel
S45					42	I/O	Capacitance sensor /driver channel
S46					43	I/O	Capacitance sensor /driver channel
VDD5	24	30	36	43	44	PWR	High voltage power supply from the charge pump LDO generated internally. A 1μF ceramic to ground is required.
VSSA		31	37			GND	Analog ground
VDDA	25	32	38	44	45	PWR	Analog power supply, A 1μF ceramic capacitor to ground is required.
VSS		33	39			GND	Analog ground
VDDD	26	34	40	45	46	PWR	Digital power supply. A 1μF ceramic capacitor to ground is required.
VSSD						GND	Analog ground
RSTN	27	36	42	46	47	I	External Reset, Low is active
IOVCC	28	37	43	47	48	PWR	I/O power supply
SCL	29	38	44	48	49	I/O	I2C clock input
SDA	30	39	45	49	50	I/O	I2C data input and output
INT	31	40	46	52	51	I/O	External interrupt to the host



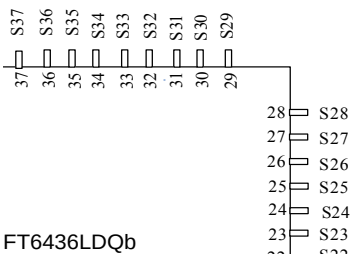
FT6236HMg Package Diagram



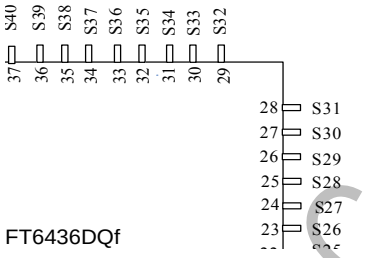
FT6236GMA Package Diagram



FT6336DMB Package Diagram



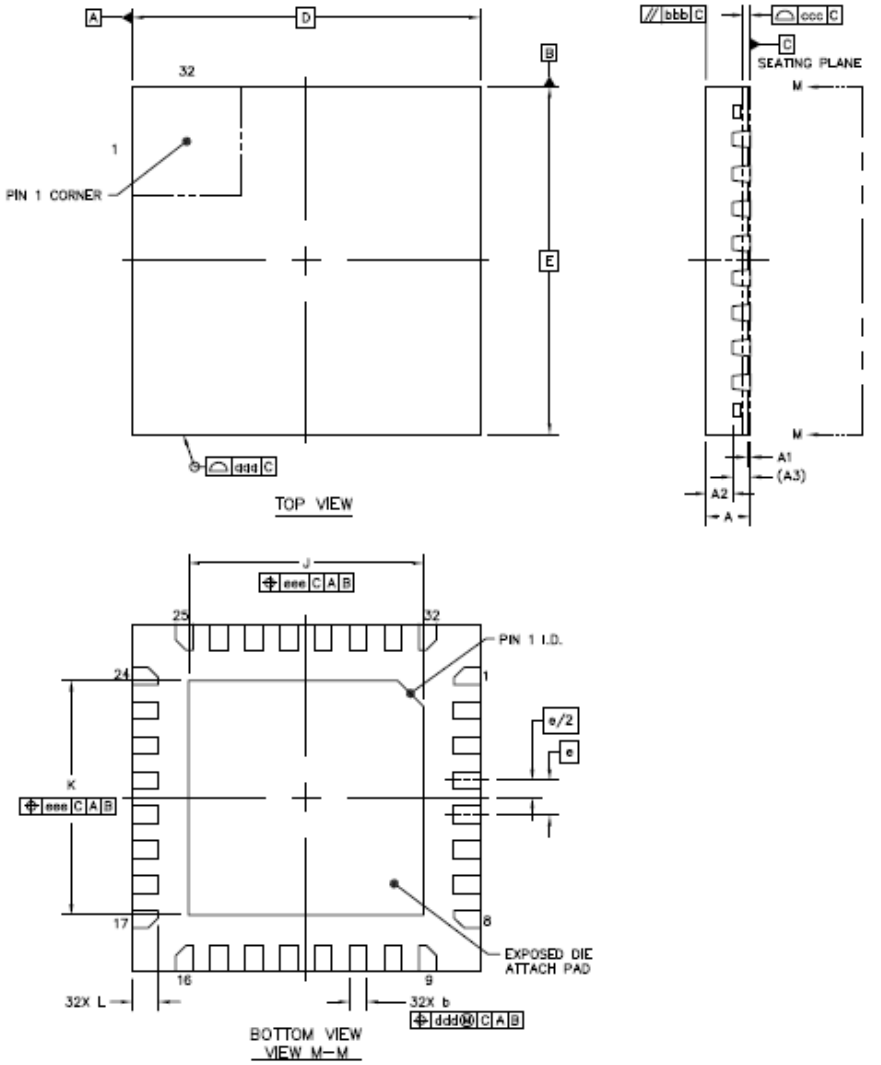
FT6436LDQb Package Diagram



FT6436DMf Package Diagram

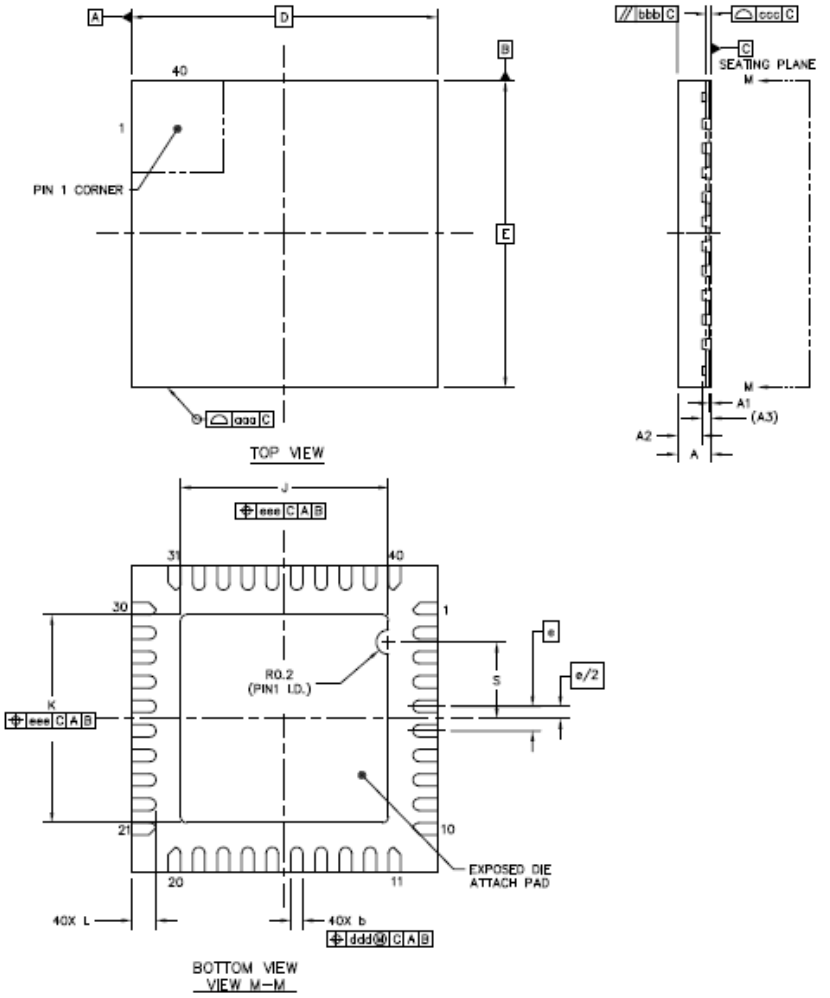
5 PACKAGE INFORMATION

5.1 Package Information of QFN-4x4-32L Package



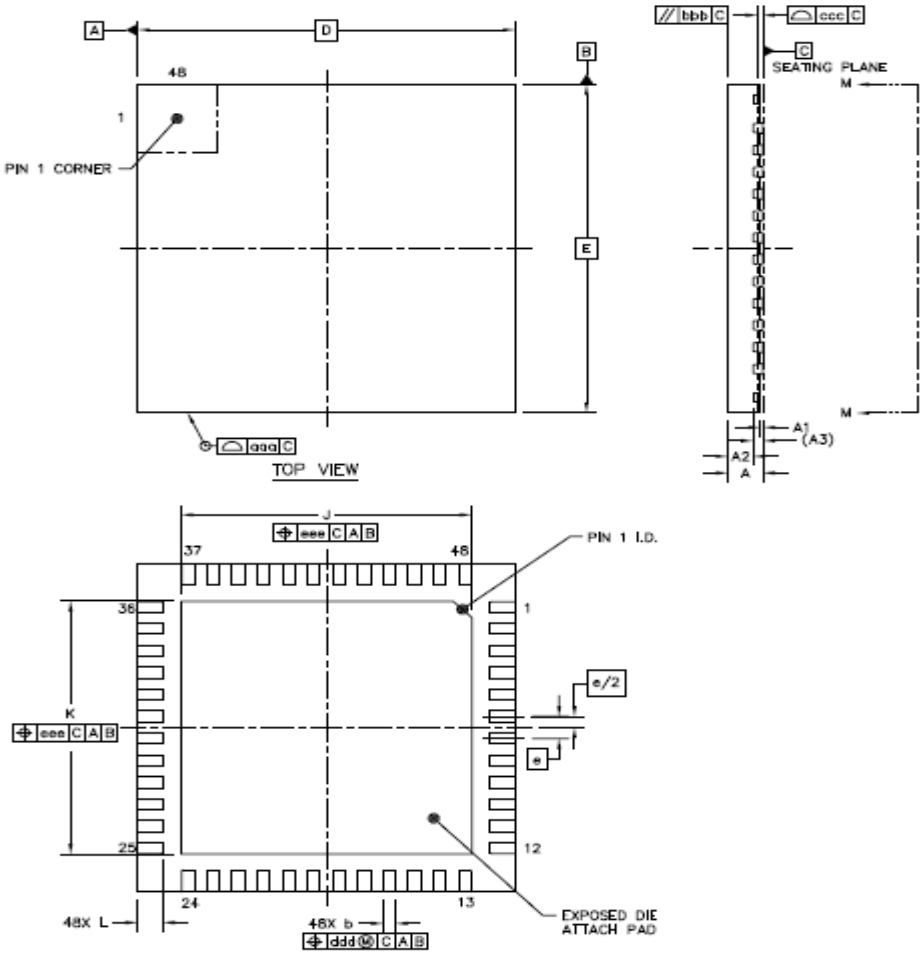
Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.45	0.5	0.55
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.3	----
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4 BSC	
	E		4 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	2.6	2.7	2.8
	K	2.6	2.7	2.8
Lead Length	L	0.25	0.3	0.35
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.2 Package Information of QFN-5x5-40L Package



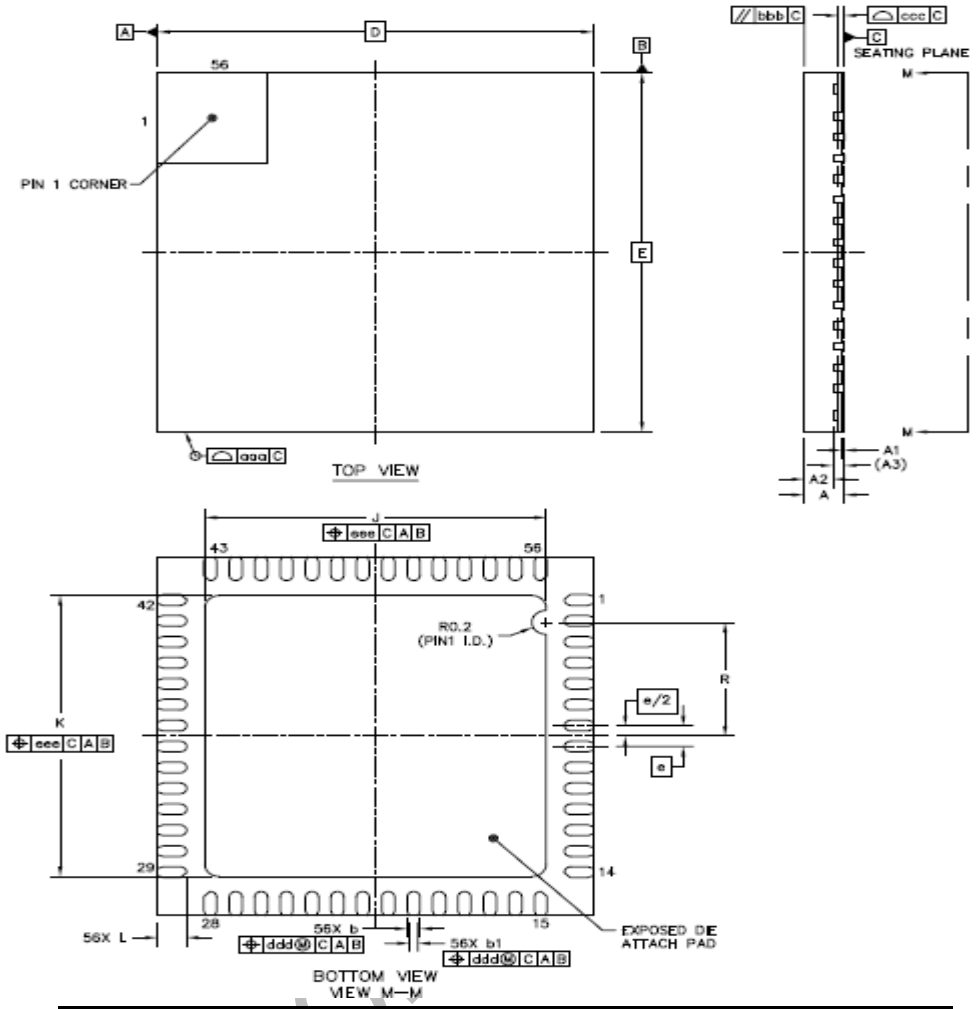
Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	0.425
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		5 BSC	
	E		5 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	3.3	3.4	3.5
	K	3.3	3.4	3.5
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.3 Package Information of QFN-6x6-48L Package



Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	0.425
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.15	0.20	0.25
Body Size	D		6 BSC	
	E		6 BSC	
Lead Pitch	e		0.4 BSC	
EP Size	J	4.52	4.62	4.72
	K	4.52	4.62	4.72
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.4 Package Information of QFN-6x6-56L Package



Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	----
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.13	0.18	0.23
	b1	0.07	0.12	0.17
Body Size	D		6 BSC	
	E		6 BSC	
Lead Pitch	e		0.35 BSC	
EP Size	J	4.6	4.7	4.8
	K	4.6	4.7	4.8
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.5 Order Information

Package Type	QFN
	32Pin(4*4)/40Pin(5*5)/48Pin(6*6)/56Pin(6*6)
	0.5-P0.4/0.6-P0.4/0.6-P0.4/0.6-P0.35
Product Name	FT6236HMg/FT6236GMA/FT6336DMB/FT6436LDQb/FT6436DQf

Note:

1). The last two letters in the product name indicate the package type and thickness and lead pitch.

2). The three last letter indicates the package type..

H : QFN-4*4 ; G : QFN-5*5 ; D : QFN-6*6

3). The second last letter indicates the thickness and lead pitch.

M : 0.6-P0.4 ; Q : 0.6-P0.35

4). The last letter indicates the numbers of sensors.

g : 22 ; A : 28 ; B： 36 ; b： 42 ; f： 46

T: Track Code

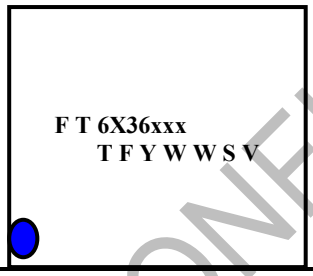
F/R:"F" for Lead Free process,

"R" for Halogen Free process

Y: Year Code

WW: Week Code

S: Lot Code



V：IC Version

Product Name	Package Type	Pannel Channels
FT6236HMg	**QFN-32L(4*4)**	**22**
FT6236GMA	**QFN-40L(5*5)**	**28**
FT6336DMB	**QFN-48L(6*6）**	**36**
FT6436LDQb	**QFN-56L(6*6)**	**42**
FT6436DQf	**QFN-56L(6*6)**	**46**

END OF DATASHEET

Application Note for FT6x06 CTPM

Application Note for FT6x06 CTPM	
Project name	Touch panel
Version	0.1
Release date	Jul 26,2012
Owner	J.H. Kuo
Classification	Confidential
Approval	

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Revision History

Date	Version	List of changes	Author + Signature
Jul 26,2012	1.0	Initial draft.	J.H. Kuo

Table of Contents

Terminology

CTP – Capacitive touch panel

CTPM – Capacitive touch panel module

1. CTPM interface to Host

Figure 1-1 shows how CTPM communicates with host device. I²C interface supported by FT6x06 that is two-wire serial bus consisting of data line SDA and SCL clock line, used for serial data transferring between host and slave device.

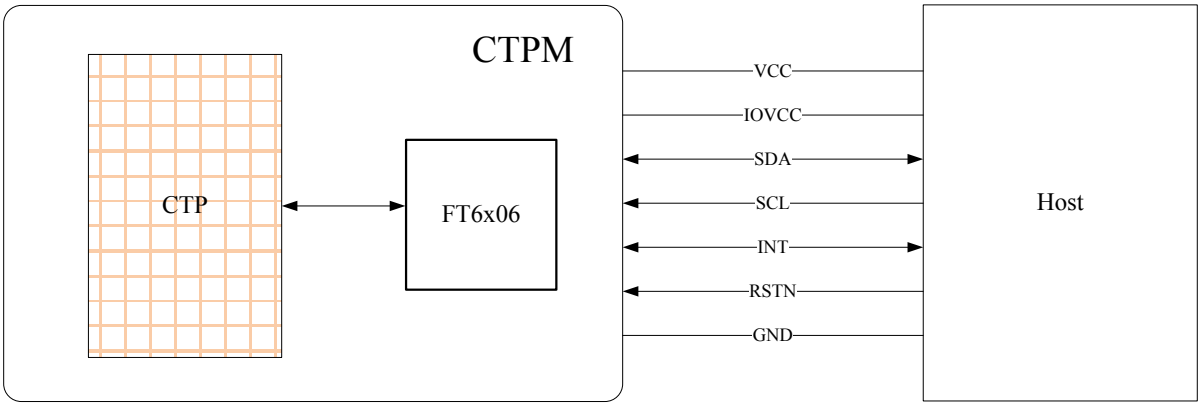


Figure 1-1 CTPM and Host connection

INT port and RSTN port form the control interface. The INT port controlled by FT6x06 will send out an interrupt request signal to the host when there is a valid touch on CTP. The INT port also has another input function that host can wake up FT6x06 from the Hibernate mode. Host can send the reset signal to CTPM via RSTN port to reset the FT6x06 if needed. The Power Supply voltage of CTPM ranges from 2.8V to 3.6V, and the interface supply voltage named IOVCC ranges from 1.8V to 3.6V. For details, please refer to Table 1-1.

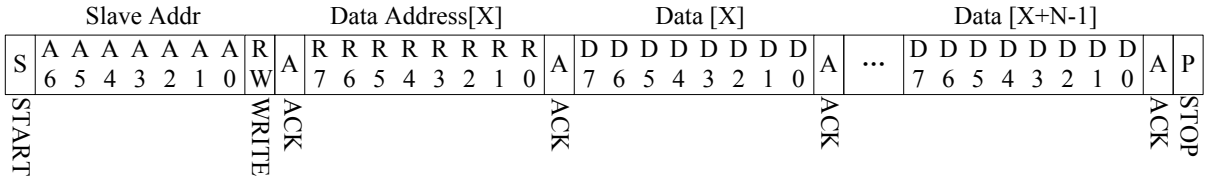
Table 1-1 Description for CTPM and Host interface

Port Name	Description
VCC	CTPM power supply, ranges from 2.8V to 3.6V.
IOVCC	CTPM interface power supply for GPIO, ranges from 1.8V to 3.6V. If GPIO supply voltage is equal to VCC (2.8V~3.6V), IOVCC pin can be connected to VCC. If GPIO supply voltage is 1.8V, IOVCC pin can be connected to VDDD pin or external 1.8V power supply.
SDA	I²C data input and output.
SCL	I²C clock input.
INT	The interrupt request signal from CTPM to Host. The wake up signal from host to CTPM, active low and the low pulse width ranges from 0.5ms to 1ms.
RSTN	The reset signal from host to CTPM, active low, and the low pulse width should be more than or equal to 1ms.
GND	Power ground.

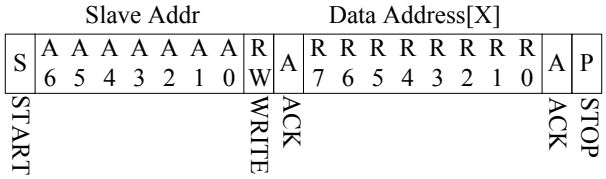
1.1 I²C Read/Write Interface description

It is important to note that the SDA and SCL must connect with a pull-high resistor respectively before you read/write I²C data.

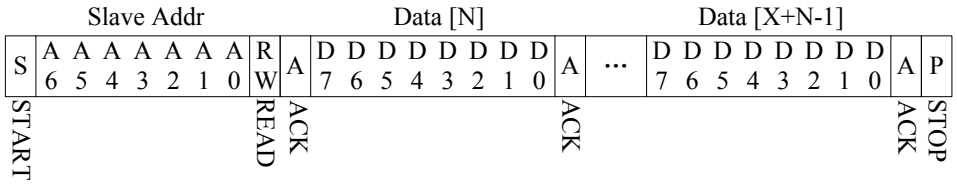
Write N bytes to I²C slave



Set Data Address



Read X bytes from I²C Slave



1.2 Interrupt/Wake-up signal from CTPM to Host

As for standard CTPM, host needs to use both interrupt signal and I²C interface to get the touch data. CTPM will output an interrupt request signal to the host when there is a valid touch. Then host can get the touch data via I²C interface. If there is no valid touch detected, the INT will output high level, and the host does not need to read the touch data. There are two kinds of method to use interrupt: interrupt trigger and interrupt polling.

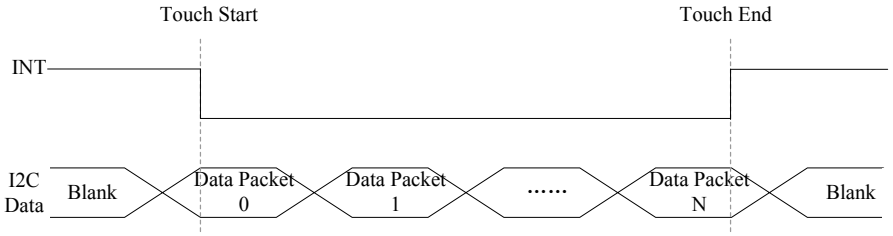


Figure 1-2 Interrupt polling mode

As for interrupt polling mode, INT will always be pulled to low level when there is a valid touch point, and be high level when a touch finished.

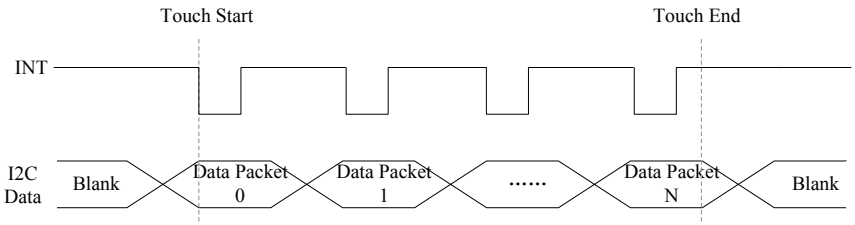


Figure 1-3 Interrupt trigger mode

While for interrupt trigger mode, INT signal will be set to low if there is a touch detected. But whenever an update of valid touch data, CTPM will produce a valid pulse on INT port for INT signal, and host can read the touch data periodically according to the frequency of this pulse. In this mode, the pulse frequency is the touch data updating rate.

When CTPM stays in hibernate mode, the INT port will act as a pull-high input port and wait for an external wake up signal. Host may send out a low pulse to wake up CTPM from the hibernate mode. The wake-up low pulse width ranges from 0.5 ms to 1 ms, the reason for this is that the INT port will act as an interrupt request signal output port after wake-up.

1.3 Reset signal from Host to CTPM

Host can send the reset signal via RSTN port to reset FT6x06. The reset signal should not be set to low while in normal running mode, but when programming flash, the RSTN port must be connected to GND. The RSTN port can also be used to active the CTPM in hibernate mode. Note that the reset pulse width should be more than 1ms.

2. Standard Application circuit of FT6x06

Table 2-1 is a brief summary of the FT6x06 application features. Figure2-1, Figure2-2, demonstrates the typical FT6x06 application schematic respectively. It consists of Capacitive Touch Panel (CTP), FT6x06 chip, and some peripheral components. According to the size of CTPM, you can choose the number of channels needed.

Table 2-1 Brief features of FT6X06

IC Type	**FT6206GMA**	**FT6306DMB**
Operating Voltage(V)	2.8 ~ 3.6	2.8 ~ 3.6
IOVCC(V)	1.8 ~ 3.6	1.8 ~ 3.6
Channel	28	36
Panel Size	2.8” ~ 4.3”	4.3” ~ 7.0”
Touch points	2	2
Interface	I^2C	I^2C
Report rate	>60Hz	>60Hz
Package (mm)	5*5 QFN40	6*6 QFN48

2.1 FT6206GMA typical application schematic for voltage of 2.8~3.6V

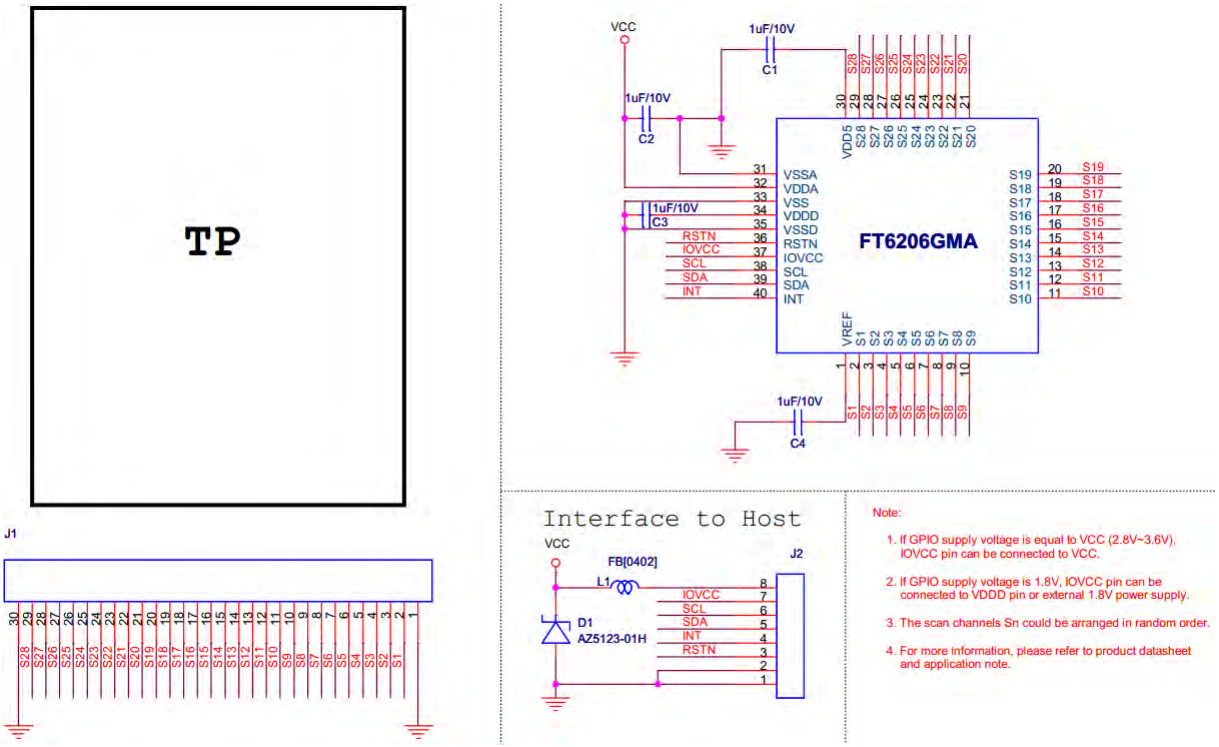


Figure 2-1 FT6206GMA typical application schematic for voltage of 2.8~3.6V

2.2 FT6306DMB typical application schematic for voltage of 2.8~3.6V

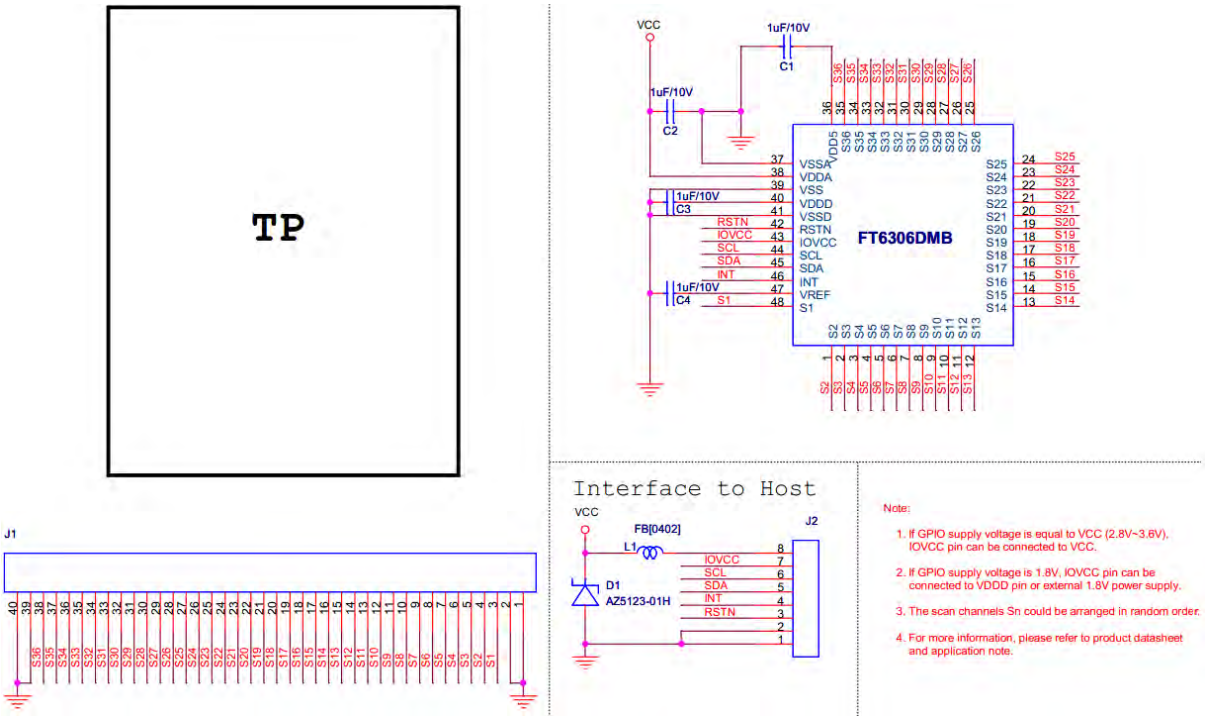


Figure 2-2 FT6306DMB typical application schematic for voltage of 2.8~3.6V

3. CTPM Register Mapping

This chapter describes the standard CTPM communication registers in address order for working mode. The most detailed descriptions of the standard products communication registers are in the register definitions section of each chapter.

3.1 Working Mode

The CTP is fully functional as a touch screen controller in working mode. The access address to read and write is just logical address which is not enforced by hardware or firmware. Here is the working mode register map.

Working Mode Register Map

Address	Name	Default Value	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Host Access
0x00	DEV_MODE	0x00		[2:0]Device Mode							R/W
0x01	GEST_ID	0x00	[7:0]Gesture ID								R
0x02	TD_STATUS	0x00					[3:0] Number of touch points				R
0x03	P1_XH	0xFF	[7:6]1st Event Flag				[3:0] 1st Touch X Position[11:8]				R
0x04	P1_XL	0xFF	[7:0] 1st Touch X Position								R
0x05	P1_YH	0xFF	[7:4] 1st Touch ID				[3:0] 1st Touch Y Position[11:8]				R
0x06	P1_YL	0xFF	[7:0] 1st Touch Y Position								R
0x07	P1_WEIGHT	0xFF	[7:0] 1st Touch Weight								R
0x08	P1_MISC	0xFF	[7:4] 1st Touch Area								R
0x09	P2_XH	0xFF	[7:6]2nd Event Flag				[3:0]2nd Touch X Position[11:8]				R
0x0A	P2_XL	0xFF	[7:0] 2nd Touch X Position								R
0x0B	P2_YH	0xFF	[7:4] 2ndTouch ID				[3:0] 2nd Touch Y Position[11:8]				R
0x0C	P2_YL	0xFF	[7:0] 2nd Touch Y Position								R
0x0D	P2_WEIGHT	0xFF	[7:0] 2nd Touch Weight								R
0x0E	P2_MISC	0xFF	[7:4] 2nd Touch Area								R
…											
0x80	TH_GROUP		[7:0] Threshold for touch detection								R/W
…											
0x85	TH_DIFF		Filter function coefficient[7:0]								R/W
0x86	CTRL	0x01	[7:0] 0: Will keep the Active mode when there is no touching. 1: Switching from Active mode to Monitor mode automatically when there is no touching.								R/W
0x87	TIMEENTERMONITOR	0x0A	[7:0] The time period of switching from Active mode to Monitor mode when there is no touching.								R/W
0x88	PERIODACTIVE		[7:0] Report rate in Active mode.								R/W
0x89	PERIODMONITOR	0x28	[7:0] Report rate in Monitor mode.								R/W
…											
0x91	RADIAN_VALUE	0x0A	[7:0] The value of the minimum allowed angle while Rotating gesture mode								R/W
0x92	OFFSET_LEFT_RIGHT	0x19	[7:0] Maximum offset while Moving Left and Moving Right gesture								R/W

0x93	OFFSET_UP_DOWN	0x19	[7:0] Maximum offset while Moving Up and Moving Down gesture	R/W
0x94	DISTANCE_LEFT_RIGHT	0x19	[7:0] Minimum distance while Moving Left and Moving Right gesture	R/W
0x95	DISTANCE_UP_DOWN	0x19	[7:0] Minimum distance while Moving Up and Moving Down gesture	R/W
0x96	DISTANCE_ZOOM	0x32	[7:0] Maximum distance while Zoom In and Zoom Out gesture	R/W
…				
0xA1	LIB_VER_H		[7:0] High 8-bit of LIB Version info	R
0xA2	LIB_VER_L		[7:0] Low 8-bit of LIB Version info	R
0xA3	CIPHER	0x06	[7:0] Chip Selecting	R
0xA4	G_MODE	0x01	[7:0] 0x00: Interrupt Polling mode 0x01: Interrupt Trigger mode	R/W
0xA5	PWR_MODE	0x00	[7:0] Current power mode which system is in	R/W
0xA6	FIRMID		[7:0] Firmware Version	R
0xA8	FOCALTECH_ID	0x11	[7:0] FocalTech's Panel ID	R
…				
0xAF	RELEASE_CODE_ID	0x01	[7:0] Release code version	R
…				
0xBC	STATE	0x01	[7:0] Current Operating mode	R/W

3.1.1 DEVICE_MODE

This is the device mode register, which is configured to determine the current mode of the chip.

Address	Bit Address	Register Name	Description
0x00	6:4	[2:0]Device Mode	000b WORKING Mode 100b FACTORY Mode

3.1.2 GEST_ID

This register describes the gesture of a valid touch.

Address	Bit Address	Register Name	Description
0x01	7:0	Gesture ID[7:0]	Gesture ID 0x10 Move Up 0x14 Move Right 0x18 Move Down 0x1C Move Left 0x48 Zoom In 0x49 Zoom Out 0x00 No Gesture

3.1.3 TD_STATUS

This register is the Touch Data status register.

Address	Bit Address	Register Name	Description
0x02	3:0	Number of touch points [3:0]	The detected point number, 1-2 is valid.
	7:4	Reserved	

3.1.4 Pn_XH (n:1-2)

This register describes MSB of the X coordinate of the nth touch point and the corresponding event flag.

Address	Bit Address	Register Name	Description
0x03 ~	7:6	Event Flag	00b: Press Down 01b: Lift Up

0x09			10b: Contact 11b: No event
	5:4		Reserved
	3:0	Touch X Position [11:8]	MSB of Touch X Position in pixels

3.1.5 Pn_XL (n:1-2)

This register describes LSB of the X coordinate of the nth touch point.

Address	Bit Address	Register Name	Description
0x04 ~ 0x0A	7:0	Touch X Position [7:0]	LSB of the Touch X Position in pixels

3.1.6 Pn_YH (n:1-2)

This register describes MSB of the Y coordinate of the nth touch point and corresponding touch ID.

Address	Bit Address	Register Name	Description
0x05 ~ 0x0B	7:4	Touch ID[3:0]	Touch ID of Touch Point, this value is 0x0F when the ID is invalid
	3:0	Touch Y Position [11:8]	MSB of Touch Y Position in pixels

3.1.7 Pn_YL (n:1-2)

This register describes LSB of the Y coordinate of the nth touch point.

Address	Bit Address	Register Name	Description
0x06 ~ 0x0C	7:0	Touch Y Position [7:0]	LSB of the Touch Y Position in pixels

3.1.8 Pn_WEIGHT (n:1-2)

This register describes weight of the nth touch point.

Address	Bit Address	Register Name	Description
0x07 ~ 0x0D	7:0	Touch Weight[7:0]	Touch pressure value

3.1.9 Pn_MISC (n:1-2)

This register describes the miscellaneous information of the nth touch point.

Address	Bit Address	Register Name	Description
0x08 ~ 0x0E	7:4	Touch Area[3:0]	Touch area value

4. Communication between host and CTPM

4.1 Communication Contents

The data Host received from the CTPM through I^2C interface are different depend on the configuration in Device Mode Register of the CTPM. Please refer to Section 3---CTPM Register Mapping.

4.2 I^2C Example Code

The code is only for reference, if you want to learn more, please contact our FAE staff.

```
//////////////////////////////////////////////////////////////////
// I2C write bytes to device.
// Arguments: ucSlaveAdr - slave address
//                ucSubAdr - sub address
```

```
//                  pBuf - pointer of buffer
//                  ucBufLen - length of buffer
//////////////////////////////////////////////////////////////////
void i2cBurstWriteBytes(BYTE ucSlaveAdr, BYTE ucSubAdr, BYTE *pBuf, BYTE ucBufLen)
{
    BYTE ucDummy; // loop dummy
    ucDummy = I2C_ACCESS_DUMMY_TIME;
    while(ucDummy--)
    {
        if (i2c_AccessStart(ucSlaveAdr, I2C_WRITE) == FALSE)
            continue;
        if (i2c_SendByte(ucSubAdr) == I2C_NON_ACKNOWLEDGE) // check non-acknowledge
            continue;
        while(ucBufLen--) // loop of writting data
        {
            i2c_SendByte(*pBuf); // send byte
            pBuf++; // next byte pointer
        } // while
        break;
    } // while
    i2c_Stop();
}

//////////////////////////////////////////////////////////////////
// I2C read bytes from device.
//
// Arguments: ucSlaveAdr - slave address
//                  ucSubAdr - sub address
//                  pBuf - pointer of buffer
//                  ucBufLen - length of buffer
//////////////////////////////////////////////////////////////////
void i2cBurstReadBytes(BYTE ucSlaveAdr, BYTE ucSubAdr, BYTE *pBuf, BYTE ucBufLen)
{
    BYTE ucDummy; // loop dummy

    ucDummy = I2C_ACCESS_DUMMY_TIME;
    while(ucDummy--)
    {
        if (i2c_AccessStart(ucSlaveAdr, I2C_WRITE) == FALSE)
            continue;
        if (i2c_SendByte(ucSubAdr) == I2C_NON_ACKNOWLEDGE) // check non-acknowledge
            continue;
        if (i2c_AccessStart(ucSlaveAdr, I2C_READ) == FALSE)
            continue;
```

```
            while(ucBufLen--) // loop to burst read
            {
                *pBuf = i2c_ReceiveByte(ucBufLen); // receive byte
                pBuf++; // next byte pointer
            } // while
            break;
        } // while
        i2c_Stop();
}

//////////////////////////////////////////////////////////////////
// I2C read current bytes from device.
//
// Arguments: ucSlaveAdr - slave address
//                pBuf - pointer of buffer
//                ucBufLen - length of buffer
//////////////////////////////////////////////////////////////////
void i2cBurstCurrentBytes(BYTE ucSlaveAdr, BYTE *pBuf, BYTE ucBufLen)
{
    BYTE ucDummy; // loop dummy

    ucDummy = I2C_ACCESS_DUMMY_TIME;
    while(ucDummy--)
    {
        if (i2c_AccessStart(ucSlaveAdr, I2C_READ) == FALSE)
            continue;
        while(ucBufLen--) // loop to burst read
        {
            *pBuf = i2c_ReceiveByte(ucBufLen); // receive byte
            pBuf++; // next byte pointer
        } // while
        break;
    } // while
    i2c_Stop();
}
```