Universal Serial Bus Type-C Cable and Connector Specification

Release 2.1
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Specification Work Group Chairs / Specification Editors

Intel Corporation (USB Promoter company)	Yun Ling – Mechanical WG co-chair, Mechanical Chapter Co-editor Brad Saunders – Plenary/Functional WG chair, Specification Co-author
Specwerkz	Bob Dunstan – Functional WG co-chair, Specification Co-author
Seagate	Alvin Cox, Mechanical WG co-chair, Mechanical Chapter Co-editor

Specification Work Group Contributors

Note: For historical reasons, the following list also includes individual contributors that were members of the work group and associated with their company affiliations at the time of the original Release 1.0 through to the latest release.

Advanced-Connectek, Inc. (ACON)	Victory Chen	Conrad Choy	Alan Tsai
	Glen Chandler	Vicky Chuang	Wayne Wang
	Dennis Cheung	Jessica Feng	Stephen Yang
	Jeff Chien	Aven Kao	Sunney Yang
	Lee (Dick Lee) Ching	Danny Liao	
Advanced Micro Devices	Steve Capezza	Jason Hawken	Joseph Scanlon
	Walter Fry	Gerald Merits	Peter Teng
	Will Harris	Tim Perley	Sujan Thomas
Allion Labs, Inc.	Howard Chang	Yan Ken	Chester Tsai
	Alex Chuang	Stan Lin	Chou Tsungbo
	Maroco Fan	Minoru Ohara	
	Terry Kao	Brian Shih	
Amphenol Corporation	Louis Chan	Terry Ke	Shawn Wei
	Zhinenng Fan	Martin Li	Alan Yang
	Jesse Jaramillo	Lino Liu	
Agilent Technologies, Inc.	James Choate		
Analogix Semiconductor, Inc.	Mehran Badii	Haijian Sui	Yueke Tang
	Greg Stewart		
Apple Inc. (USB Promoter company)	Colin Abraham	Brian Follis	Matthew Mora
	Mahmoud Amini	Zheng Gao	Nathan Ng
	Sree Anantharaman	Derek Iwamoto	James Orr
	Brian Baek	Scott Jackson	Keith Porthouse
	Paul Baker	Girault Jones	Breton Saunders
	Michael Bonham	Keong Kam	Reese Schreiber
	Carlos Calderon	Kevin Keeler	Sascha Tietz
	Jason Chung	Min Kim	Jennifer Tsai
	David Conroy	Woopoung Kim	Colin Whitby-Strevens
	Bill Cornelius	Alan Kobayashi	Jeff Wilcox
	Christophe Daniel	Alexei Kosut	Eric Wiles
	Raju Desai	Christine Krause	Dan Wilson
	William Ferry	Chris Ligtenberg	Dennis Yarak
ASMedia Technology Inc.	Kuo Lung Li		
Bizlink Technology, Inc.	Alex Chou	Morphy Hsieh	Kevin Tsai

Cadence Design Systems, Inc.	Marcin Behrendt	Dariusz Kaczmarczyk	Neelabh Singh
	Huzaifa Dalal	Tomasz Klimek	Michal Staworko
	Pawel Eichler	Jie Min	Fred Stivers
	Sathish Kumar Ganesan	Asila Nahas	Mark Summers
		Uyen Nguyen	Claire Ying
Canova Tech	Piergiorgio Beruto	Michael Marioli	Paola Pilla
	Andrea Maniero	Antonio Orzelli	Nicola Scantamburlo
Cirrus Logic Inc.	Sean Davis	Darren Holding	Brad Lambert
Corning Optical Communication LLC	Wojciech Giziewicz	Ian McKay	Jamie Silva
Cosemi Technologies Inc.	Samir Desai	Devang Parekh	
Cypress Semiconductor	Chia Hua Chang	Rushil Kadakia	Jagadeesan Raj
	Mark Fu	Benjamin Kropf	Sanjay Sancheti
	Naman Jain	Venkat Mandagulathur	Subu Sankaran
	Savan Javia	Anup Nayak	Anita Thimma Govarthanarajan
Dell	Mohammed Hijazi	Ken Nicholas	Thomas Voor
	David Meyers	Ernesto Ramirez	Merle Wood
	Sean O'Neal	Siddhartha Reddy	
Dialog Semiconductor (UK) Ltd.	Yimin Chen		
Diodes Incorporated	Kay Annamalai	Bob Lo	Jin-sheng Wang
	Justin Lee	Jaya Shukla	Ada Yip
	Paul Li	Qun Song	
DisplayLink (UK) Ltd.	Pete Burgers		
DJI Technology Co., Ltd.	Steve Huang		
Electronics Testing Center, Taiwan	Sophia Liu		
Elka International Ltd.	Roy Ting		
Ellisys	Abel Astley	Mario Pasquali	Tim Wei
	Rick Bogart	Chuck Trefts	
Etron Technology, Inc.	Chien-Cheng Kuo		
Feature Integration Technologies Inc.	Jacky Chan	KungAn Lin	Paul Yang
	Chen Kris	Yuchi Tsao	Amanda Ying
	Yulin Lan		
Foxconn / Hon Hai	Patrick Casher	Chris Goralka	Pei Tsao
	Asroc Chen	Bob Hall	AJ Yang
	Brandon Chen	Chien-Ping Kao	Yuan Zhang
	Joe Chen	Ji Li	Jessica Zheng
	Allen Cheng	Ann Liu	Jie Zheng
	Jason Chou	Terry Little	Andy Yao
	Edmond Choy	Steve Sedio	
	Fred Fons	Christine Tran	
Foxlink/Cheng Uei Precision Industry Co., Ltd.	Robert Chen	Armando Lee	Steve Tsai
	Sunny Chou	Dennis Lee	Wen Yang
	Carrie Chuang	Justin Lin	Wiley Yang
	Wen-Chuan Hsu	Robert Lu	Junjie Yu
	Alex Hsue	Tse Wu Ting	

Fresco Logic Inc.	Brian Collins	Bob McVay	Christopher Meyers
Google	Naga Viswanadha Udaya Kiran Ammu	Eric Herrmann	Vincent Palatin
	Alec Berg	Nithya Jagannathan	Dylan Reid
	Joshua Boilard	Nathan Kolluru	Adam Rodriguez
	Alec Berg	Lawrence Lam	David Schneider
	Todd Broch	Adam Langley	Stephan Schooley
	Chao Fei	Benson Leung	Toshak Singhal
	Jim Guerin	Abraham Levkoy	Ken Wu
	Jeffrey Hayashida	Ingrid Lin	Songping Wu
	Mark Hayter	Richard Palatin	
Granite River Labs	Yung Han Ang	Alan Chuang	Prasannakumar Marikunte Nagaraju
	Velmurugan Ayyakkannu	Mike Engbretson	Krishna Murthy
	Hariprasad Bhat	Vishal Kakade	Amy Peng
	Sandy Chang	Jesson Li	Johnson Tan
	Allen Chen	Caspar Lin	Annie Tao
	Swee Guan Chua	Bala M	Chin Hun Yaep
Honor Device Co., Ltd.	Wang Feng		
Hirose Electric Co., Ltd.	Jeremy Buan	William MacKillop	Eungsoo Shin
	William Kysiak	Gourgen Oganessyan	Sid Tono
	Sang-Muk Lim		
Hosiden Corporation	Takahisa Otsuji	Fumitake Tamaki	
HP Inc. (USB Promoter company)	Lee Atkinson	Robin Castell	Jim Mann
	Srinath Balaraman	Steve Chen	Linden McClure
	Rami Bathaniah	Michael Krause	Mike Pescetto
	Roger Benson	Rahul Lakdawala	Asjad Shamim
	Alan Berkema		
I-PEX (Dai-ichi Seiko)	Alan Kinningham	Ro Richard	
Indie Semiconductor	Ian Board	Jim Wilshire	
Infineon Technologies	Tue Fatt David Wee		
Intel Corporation (USB Promoter company)	Dave Ackelson	Vijaykumar Kadgi	Rajaram Regupathy
	Mike Bell	Luke Johnson	Oren Salomon
	Dmitriy Berchanskiy	Jerzy Kolinski	Brad Saunders
	Brad Berlin	Rolf Kuhnis	Tomer Savariego
	Pierre Bossart	Henrik Leegaard	Ehud Shoor
	Kuan-Yu Chen	Edmond Lau	Amit Srivastava
	Hengju Cheng	Xiang Li	Einat Surijan
	Oded David	Yun Ling	Ron Swartz
	Jhuda Dayan	Guobin Liu	David Thompson
	Paul Durley	Steve McGowan	Karthi Vadivelu
	Saranya Gopal	Sankaran Menon	Tsion Vidal
	Yaniv Hayat	Udaya Natarajan	Stephanie Wallick
	Howard Heck	Aruni Nelson	Rafal Wielicki
	Hao-Han Hsu	Chee Lim Nge	Devon Worrell
	Seppo Ingalsuo	Sagar Pawar	Li Yuan
	Abdul (Rahman) Ismail	Duane Quiet	Reza M. Zamani
	James Jaussi	Kannappan Rajaraman	Vitaly Zhivov
	Ziv Kabiry	Sridharan Ranganathan	

Japan Aviation Electronics Industry Ltd. (JAE)	Kenji Hagiwara Hiroaki Ikeda Masaki Kimura Toshio Masumoto Kenta Minejima Toshiyuki Moritake Joe Motojima Ron Muir	Tadashi Okubo Kazuhiro Saito Kimiaki Saito Yuichi Saito Mark Saubert Toshio Shimoyama Tatsuya Shioda Atsuo Tago	Masaaki Takaku Jussi Takaneva Junichi Takeuchi Tomohiko Tamada Kentaro Toda Kouhei Ueda Takakazu Usami Masahide Watanabe Youhei Yokoyama
JPC/Main Super Inc.	Sam Tseng	Ray Yang	
Kandou Bus SA	Hitaish Sharma	David Stauffer	Paul Wilson
Keysight Technologies Inc.	Pedro Merlo		
Kinetic Technologies, Inc.	Ramesh Dandapani	Jay Slivkoff	Sireesha Vemulapalli
Leadtrend	Yao-Wei Hsieh		
LeCroy Corporation	Mike Engbretson Daniel H. Jacobs	Tyler Joe	Giuseppe Leccia
Lenovo	Rob Bowser Tomoki Harada	Jianye Li Wei Liu	Howard Locker
LG Electronics Inc.	Do Kyun Kim	Yoon Jong Lee	
Lintes Technology Co., Ltd.	Tammy Huang Charles Kaun RD Lintes	Max Lo CT Pien	JinYi Tu Jason Yang
Lotes Co., Ltd.	Ariel Delos Reyes Ernest Han Mark Ho Regina Liu-Hwang	Charles Kaun Chi-Chang Lin James Lin Max Lo	John Lynch JinYi Tu Jason Yang
LSI Corporation	Dave Thompson		
Luxshare-ICT	Josue Castillo Daniel Chen Kenny Chen Lisen Chen Sally Chiu CY Hsu Blue Ho	Alan Kinningham Antony Lin Gorden Lin John Lin Stone Lin Alan Liu Sean O'Neal	Scott Shuey James Stevens Carr Wang Yangli Wang Eric Wen Pat Young
Maxim Integrated Products	Forrest Christo Ken Helfrich	Sang Kim Jeff Lo	Michael Miskho Jacob Scott
MCCI Corporation	Terry Moore		
MediaTek Inc.	Alex YC Lin		
MegaChips Corporation	Alan Kobayashi	Satoru Kumashiro	
Mercedes-Benz Research & Development, North America, Inc.	Hans Wickler		

Microchip (SMSC)	Josh Averyt Mark Bohm Shannon Cash Thomas Farkas Fernando Gonzalez	Matthew Kalibat Donald Perkins Richard Petrie Mohammed Rahman Andrew Rogers	John Sisto Anthony Tarascio Kiet Tran Christopher Twigg Prasanna Vengateshan
Microsoft Corporation (USB Promoter company)	Randy Aull Jim Belesiu Michelle Bergeron Fred Bhesania Anthony Chen Philip Froese Vivek Gupta David Hargrove Robbie Harris Teemu Helenius Robert Hollyer Lily Huang	Dan Iatco Kai Inha Jayson Kastens Andrea Keating Shoaib Khan Patrick Law Eric Lee Ivan McCracken Arvind Murching Gene Obie Toby Nixon Arjun Padmanabhan	Praveen Kumar Palacharla Rahul Ramadas Srivatsan Ravindran Nathan Sherman Bala Sivakumar Timo Toivola Vahid Vassey David Voth Andrew Yang Panu Ylihaavisto
Molex LLC	Adib Al Abaji	Alan MacDougall	
Monolithic Power Systems	Junyong Gong Di Han Yuncong Jiang	Istvan Nagy Chris Sporck	Ao Sun Vincent Wu
MQP Electronics Ltd.	Sten Carlsen	Pat Crowe	
Multilane Inc.	Fadi Daou	Rita Khawaja	Elias Khoury
NEC Corporation	Kenji Oguma		
Newnex Technology Corp.	Sam Liu	Nimrod Peled	
Nokia Corporation	Daniel Gratiot Pekka Leinonen	Samuli Makinen Pekka Talmola	Timo Toivola Panu Ylihaavisto
Nuvoton Technology Corp.	Nimrod Peled		
NVIDIA	Jamie Aitken		
NXP Semiconductors	Mahmoud EL Sabbagh Dennis Ha	Ken Jaramillo Vijendra Kuroodi	Guru Prasad Krishnan TN
Oculus VR LLC	Amish Babu	Marty Evans	Joaquin Fierro
ON Semiconductor	Edward Berrios Rod Comer Eduardo De Reza	Oscar Freitas Christian Klein Amir Lahooti	Eric Maier Rick Pierce Michael Smith
Parade Technologies, Inc.	Jian Chen Brian Collins Robert McVay	Craig Wiley Paul Xu	Alan Yuen Jingfan Zhang
Power Integrations	Shruti Anand Rahul Joshi	Aditya Kulkarni Akshay Nayaknur	Amruta Patra
Qualcomm, Inc.	Lior Amarilio Vara Prasad Arikatla Aris Balatsos Nicholas Cadieux David Chang Tomer Ben Chen Richard Burrows Amit Gil	James Goel Amit Gupta Philip Hardy Will Kun Jonathan Luty Lalan Mishra George Paparrizos Vatsal Patel	Jack Pham Vamsi Samavedam Matthew Sienko Dmitrii Vasilchenko Joshua Warner Chris Wiesner

Realtek Semiconductor Corp.	Marco Chiu Tsung-Peng Chuang Charlie Hsu Fan-Hau Hsu	Ty Kingsmore Ray Lee Jay Lin Ryan Lin	Terry Lin Chuting Su Changhung Wu
Renesas Electronics Corp. (USB Promoter company)	Kai Bao Yen-Mo Chen Nobuo Furuya	Philip Leung Kiichi Muto Ziba Nami	Hajime Nozaki Yosuke Sasaki Toshifumi Yamaoka
Richtek Technology Corp.	Ben Chiang Max Huang	Leo Kang Roger Lo	Ken Shih Alex Yang
Rohde & Schwarz GmbH & Co. KG	Kai Uwe Schmidt	Martin Stumpf	Randy White
Rohm Co., Ltd.	Mark Aaldering Kris Bahar Ruben Balbuena Nobutaka Itakura	Yusuke Kondo Arun Kumar Chris Lin Kazuomi Nagai	Yoshinori Ohwaki Takashi Sato Hiroshi Yoshimura
Samsung Electronics Co., Ltd.	Jaedeok Cha KangSeok Cho Junhwa Choi Wooin Choi Yeongbok Choi Cheolyoon Chung Ilhyung Chung JaeRyong Han Jaehyeok Jang Wonseok Jang	Sung Geun Joo Koyoungwon Kim Sangju Kim Soondo Kim Woonki Kim Jagoun Koo Termi Kwon Cheolho Lee Edward Lee	Jun Bum Lee Jinyoung Oh Chahoon Park Chulwoo Park Youngjin Park Jung Waneui Sunggeun Yoon
SB C&S Corp.	Toshinari Nakamura Morito Ogikubo	Eiji Sakai	Kenji Watanabe
Seagate	Alvin Cox Emmanuel Lemay	Tony Priborsky Tom Skaar	Dan Smith
Shenzhen Deren Electronic Co., Ltd.	Smark (Zhudong) Huo Wen Fa Lei	Yang Lirong	Lucy Zhang
Silicon Line Gmbh	Ian Jackson	Boleslaw Wojtowicz	Zhiying Zhang
SiliConch Systems Private Limited	Jaswanth Ammineni Pavitra Balasubramanian Kaustubh Kumar Aniket Mathad	Shubham Paliwal Jinisha Patel Vinay Patel Rakesh Polasa	Vishnu Pusuluri Ranjith S Abhishek Sardeshpande Satish Anand Verkila
Simula Technology Inc.	John Chang Voss Cheng Thomas Li	Jung Lin Jyunming Lin Doris Liu	Richard Liu CK Wang Alice Yu
Softnautics LLP	Bhavesh Desai Hetal Jariwala	Dipakkumar Modi Ishita Shah	Ujjwal Talati
Sony Corporation	Shinichi Hirata	Shigenori Tagami	
Spectra7 Microsystems Corp.	Andrew Kim	James McGrath	John Mitchell
Specwerkz	Robert Dunstan	Amanda Hosler	Diane Lenox

STMicroelectronics (USB Promoter company)	Jerome Bach Nathalie Ballot Filippo Bonaccorso Guenael Cadier Dominique Chaillot Christophe Cochard Nicolas Florenchie	Cedric Force Gregory Gosciniak Chekib Hammami Joel Huloux Christophe Lorin Yohann Martiniault Patrizia Milazzo	Federico Musarra Pascal Legrand Richard O'Connor Massimo Panzica Nicolas Perrin
Sumitomo Electric Ind., Ltd.	Takeshi Inoue Yasuhiro Maeda	Wataru Sakurai Sainer Siagian	Masaki Suzuki Mitsuaki Tamura
Synaptics Inc.	Daniel Bogard Dan Ellis	Jeff Lukanc	Prashant Shamarao
Synopsys, Inc.	Subramaniam Aravindhan	Morten Christiansen Nivin George	Satya Patnala John Stonick
Taiwan Testing and Certification Center	Sophia Liu		
Tektronix, Inc.	Sourabh Das Mark Guenther	Abhijeet Shinde	Randy White
Texas Instruments (USB Promoter company)	Jawaid Ahmad Mike Campbell Greg Collins Gary Cooper Anant Gole GP Gopalakrishnan Craig Greenberg Richard Hubbard Nate Johnson Michael Koltun IV Yoon Lee Grant Ley	Win Maung Shafiuddin Mohammed Lauren Moore Jacob Ontiveros Brian Parten Martin Patoka Jason Peck John Perry Louis Peryea Brian Quach	Sai Karthik Rajaraman Wes Ray Dafydd Roche Anwar Sadat Cory Stewart Sue Vining Bill Waters Deric Waters Gregory Watkins Roy Wojciechowski
Thine Electronica, Inc.	Yuseke Fujita	Shuhei Yamamoto	
Total Phase	Chris Yokum		
Tyco Electronics Corp. (TE Connectivity Ltd.)	Max Chao Robert E. Cid Calvin Feng Kengo Ijiro Eiji Ikematsu Joan Leu Clark Li	Mike Lockyer Jeff Mason Takeshi Nakashima Luis A. Navarro Masako Saito Yoshiaki Sakuma Gavin Shih	Hiroshi Shirai Hidenori Taguchi Nathan Tracy Bernard Vetten Ryan Yu Noah Zhang Sjoerd Zwartkruis
UL LLC	Leo Chung Michael Hu Dylan Su	Henry Tsou Paul Vanderlaan Eric Wall	Lance Yang Chien-Wei Yeh
Unigraf OY	Steven Chen	Sergey Grushin	
Varjo Technologies	Kai Inha		
Ventev Mobile	Brad Cox	Colin Vose	
VIA Technologies Inc.	Terrance Shih	Jay Tseng	Fong-Jim Wang
Weltrend Semiconductor	Hung Chiang Jeng Cheng Liu	Wayne Lo Ho Wen Tsai	Eric Wu
Western Digital, HGST	Larry McMillan		

Xiaomi Communications Co., Ltd.	Xiaoxing Yang	Juejia Zhou

Pre-Release Draft Industry Reviewing Companies That Provided Feedback

Aces
Fairchild Semiconductor
Fujitsu Ltd.
Industrial Technology Research Institute (ITRI)
Joinsoon Electronics Mfg. Co. Ltd.
JST Mfg. Co., Ltd.
Korea Electric Terminal
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Motorola Mobility LLC
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Revision History

Revision	Date	Description
1.0	August 11, 2014	Initial Release
1.1	April 3, 2015	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.2	March 25, 2016	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.3	July 14, 2017	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
1.4	March 29, 2019	Reprint release including incorporation of all approved ECNs as of the revision date plus editorial clean-up.
2.0	August 2019	New release primarily for enabling *USB4* over USB Type-C connectors and cables. Also includes incorporation of all approved ECNs as of the revision date plus editorial clean-up.
2.1	May 2021	New release primarily for enabling Extended Power Range (EPR) and defining EPR cables aligning with *USB Power Delivery* Specification R3.1 V1.0. Also includes incorporation of all approved ECNs as the revision date plus editorial clean-up.

1 Introduction

With the continued success of the USB interface, there exists a need to adapt USB technology to serve newer computing platforms and devices as they trend toward smaller, thinner and lighter form-factors. Many of these newer platforms and devices are reaching a point where existing USB receptacles and plugs are inhibiting innovation, especially given the relatively large size and internal volume constraints of the Standard-A and Standard-B versions of USB connectors. Additionally, as platform usage models have evolved, usability and robustness requirements have advanced and the existing set of USB connectors were not originally designed for some of these newer requirements. This specification is to establish a new USB connector ecosystem that addresses the evolving needs of platforms and devices while retaining all of the functional benefits of USB that form the basis for this most popular of computing device interconnects.

1.1 Purpose

This specification defines the USB Type-C® receptacles, plug and cables.

The USB Type-C Cable and Connector Specification is guided by the following principles:

- Enable new and exciting host and device form-factors where size, industrial design and style are important parameters
- Work seamlessly with existing USB host and device silicon solutions
- Enhance ease of use for connecting USB devices with a focus on minimizing user confusion for plug and cable orientation

The USB Type-C Cable and Connector Specification defines a new receptacle, plug, cable and detection mechanisms that are compatible with existing USB interface electrical and functional specifications. This specification covers the following aspects that are needed to produce and use this new USB cable/connector solution in newer platforms and devices, and that interoperate with existing platforms and devices:

- USB Type-C receptacles, including electro-mechanical definition and performance requirements
- USB Type-C plugs and cable assemblies, including electro-mechanical definition and performance requirements
- USB Type-C to legacy cable assemblies and adapters
- USB Type-C-based device detection and interface configuration, including support for legacy connections
- USB Power Delivery optimized for the USB Type-C connector

The USB Type-C Cable and Connector Specification defines a standardized mechanism that supports Alternate Modes, such as repurposing the connector for docking-specific applications.

1.2 Scope

This specification is intended as a supplement to the existing *USB 2.0*, *USB 3.2*, *USB4™* and *USB Power Delivery* specifications. It addresses only the elements required to implement and support the USB Type-C receptacles, plugs and cables.

Normative information is provided to allow interoperability of components designed to this specification. Informative information, when provided, may illustrate possible design implementations.

1.3 Related Documents

USB 2.0 *Universal Serial Bus Revision 2.0 Specification*
This includes the entire document release package.

USB 3.2 *Universal Serial Bus Revision 3.2 Specification*
This includes the entire document release package.
USB 3.1 Legacy Cable and Connector Specification, Revision 1.0

USB4 *USB4™ Specification, Version 1.0, August 2019*
(including posted errata and ECNs)

TBT3 Chapter 13 of *USB4 Specification, Version 1.0, August 2019*

USB PD *USB Power Delivery Specification, Revision 2.0, Version 1.3, January 12, 2017*
USB Power Delivery Specification, Revision 3.1, Version 1.0, May 2021 (including posted errata and ECNs)

USB BB *USB Billboard Device Class Specification, Revision 1.2.2, January 29, 2021*

USB BC *Battery Charging Specification, Revision 1.2 (including errata and ECNs through March 15, 2012), March 15, 2012*

DP AM *DisplayPort™ Alt Mode on USB Type-C Standard, Version 2.0, 12 March 2020*

All USB-specific documents are available for download at http://www.usb.org/documents. The DisplayPort Alt Mode specification is available from VESA (http://www.vesa.org).

1.4 Conventions

1.4.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, and then text.

1.4.2 Keywords

The following keywords differentiate between the levels of requirements and options.

1.4.2.1 Informative

Informative is a keyword that describes information with this specification that intends to discuss and clarify requirements and features as opposed to mandating them.

1.4.2.2 May

May is a keyword that indicates a choice with no implied preference.

1.4.2.3 N/A

N/A is a keyword that indicates that a field or value is not applicable and has no defined value and shall not be checked or used by the recipient.

1.4.2.4 Normative

Normative is a keyword that describes features that are mandated by this specification.

1.4.2.5 Optional

Optional is a keyword that describes features not mandated by this specification. However, if an optional feature is implemented, the feature shall be implemented as defined by this specification (optional normative).

1.4.2.6 Reserved

Reserved is a keyword indicating reserved bits, bytes, words, fields, and code values that are set-aside for future standardization. Their use and interpretation may be specified by future extensions to this specification and, unless otherwise stated, shall not be utilized or adapted by vendor implementation. A reserved bit, byte, word, or field shall be set to zero by the sender and shall be ignored by the receiver. Reserved field values shall not be sent by the sender and, if received, shall be ignored by the receiver.

1.4.2.7 Shall

Shall is a keyword indicating a mandatory (normative) requirement. Designers are mandated to implement all such requirements to ensure interoperability with other compliant Devices.

1.4.2.8 Should

Should is a keyword indicating flexibility of choice with a preferred alternative. Equivalent to the phrase “it is recommended that”.

1.4.3 Numbering

Numbers that are immediately followed by a lowercase “b” (e.g., 01b) are binary values. Numbers that are immediately followed by an uppercase “B” are byte values. Numbers that are immediately followed by a lowercase “h” (e.g., 3Ah) are hexadecimal values. Numbers not immediately followed by either a “b”, “B”, or “h” are decimal values.

1.5 Terms and Abbreviations

Term	Description
Accessory Mode	A reconfiguration of the connector based on the presence of Rd/Rd or Ra/Ra on CC1/CC2, respectively.
Active cable	Active cables are USB Full-Featured Type-C Cables that incorporate repeaters in the *USB 3.2* data path. All active cables, regardless of length, are expected to comply with this specification, the *USB 3.2* Appendix E, and the *USB 3.2* active cable CTS. Active cables may incorporate repeaters in both ends of the cable, one end, or anywhere in the cable.
Alternate Mode	Operation defined by a vendor or standards organization that is associated with a SVID assigned by the USB-IF. Entry and exit into and from an Alternate Mode is controlled by the *USB PD* Structured VDM Enter Mode and Exit Mode commands.
Alternate Mode Adapter (AMA)	A *USB PD* Device which supports Alternate Modes and acts as a UFP.
Audio Adapter Accessory Mode	The Accessory Mode defined by the presence of Ra/Ra on CC1/CC2, respectively. See Appendix A.
BMC	Biphase Mark Coding used for *USB PD* communication over the CC wire.
Cable Port Partner	The USB Type-C DRP, Source, or Sink connected to the cable plug.
Captive cable	A cable that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end.

Term	Description
CC	Configuration Channel (CC) used in the discovery, configuration and management of connections across a USB Type-C cable.
Charge-Through VPD (CTVPD)	A VCONN-Powered USB Device that has the mechanism to pass power and CC communication from one port to the other without any reregulation.
Configuration Lane	The USB 3.2 Configuration Lane is used to establish and manage dual-lane SuperSpeed USB operation. The Configuration Lane is specifically the SuperSpeed USB TX1/RX1 differential signal set in the cable/plug.
Debug Accessory Mode (DAM)	The Accessory Mode defined by the presence of Rd/Rd or Rp/Rp on CC1/CC2, respectively. See Appendix B.
Debug and Test System (DTS)	The combined hardware and software system that provides a system developer debug visibility and control when connected to a Target System in Debug Accessory Mode.
Default VBUS	VBUS voltage as defined by the *USB 2.0* and *USB 3.2* specifications. Note: where used, 5 V connotes the same meaning.
DFP	Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a host or the ports on a hub to which devices are connected. In its initial state, the DFP sources VBUS and VCONN, and supports data. A charge-only DFP port only sources VBUS.
Direct connect device	A device with either a captive cable or just a USB Type-C plug (e.g., thumb drive).
DRD (Dual-Role-Data)	The acronym used in this specification to refer to a USB port that can operate as either a DFP (Host) or UFP (Device). The role that the port initially takes is determined by the port's power role at attach. A Source port takes on the data role of a DFP and a Sink port takes on the data role of a UFP. The port's data role may be changed dynamically using *USB PD* Data Role Swap.
DRP (Dual-Role-Power)	The acronym used in this specification to refer to a USB port that can operate as either a Source or a Sink. The role that the port offers may be fixed to either a Source or Sink or may alternate between the two port states. Initially when operating as a Source, the port will also take on the data role of a DFP and when operating as a Sink, the port will also take on the data role of a UFP. The port's power role may be changed dynamically using *USB PD* Power Role Swap.
DR_Swap	*USB PD* Data Role Swap.
Dual-lane (x2)	USB 3.2 dual-lane operation is defined as simultaneously signaling on both sets of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 and TX2/RX2 in the cable/plug).
Electronically Marked Cable	A USB Type-C cable that uses *USB PD* to provide the cable's characteristics.

Term	Description
eMarker	The element in an Electronically Marked Cable that returns information about the cable in response to a *USB PD* Discover Identity command.
Initiator	The port initiating a Vendor Defined Message. It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Initiator will be a host.
Internal Temperature	In reference to an active cable, the temperature measured inside a plug. It is not the skin temperature. There is a relationship between the plug's internal temperature and the skin temperature, but that relationship is design dependent.
Local Plug	The cable plug being referred to.
Optically Isolated Active Cable (OIAC)	A cable with a USB Type-C Plug on each end with one Cable Plug supporting SOP' and the other supporting SOP". This cable is electrically isolated between the two plugs.
Passive cable	A cable that does not incorporate any electronics to condition the data path signals. A passive cable may or may not be electronically marked.
Port Partner	Refers to the port (device or host) a port is attached to.
Power Bank	A device with a battery whose primary function is to charge or otherwise extend the runtime of other USB Type-C devices.
Power Delivery Mode	A mode where the port partners are in a *USB PD* power contract (either Explicit or Implicit).
Power Sinking Devices (PSD)	Sink which draws power but has no other USB or Alternate Mode communication function, e.g. a USB-powered light.
Powered cable	A cable with electronics in the plug that requires VCONN indicated by the presence of Ra between the VCONN pin and ground.
PR_Swap	*USB PD* Power Role Swap.
Re-driver	Re-driver refers to an analog component that operates on the signal without re-timing it. This may include equalization, amplification, and transmitter. The re-driver does not include a clock-data recovery (CDR) circuit. Re-drivers are beyond the scope of this document.
Remote Plug	A remote cable plug in the context of OIAC plugs is the plug at the other end of the Optically Isolated Active Cable.
Repeater	Repeater refers to any active component that acts on a signal in order to increase the physical lengths and/or interconnect loss over which the signal can be transmitted successfully. The category of repeaters includes both re-timers and re-drivers.
Responder	The port responding to the Initiator of a Vendor Defined Message (VDM). It is independent of the port's PD role (e.g., Provider, Consumer, Provider/Consumer, or Consumer/Provider). In most cases, the Responder will be a device.

Term	Description
Re-timer	Re-timer refers to a component that contains a clock-data recovery (CDR) circuit that "retimes" the signal. The re-timer latches the signal into a synchronous memory element before re-transmitting it. It is used to extend the physical length of the system without accumulating high frequency jitter by creating separate clock domains on either side of the re-timer. Re-timers are defined in *USB 3.2* Appendix E and *USB4*.
SBU	Sideband Use.
Short Active Cable (SAC)	A cable with a USB Type-C Plug on each end at least one of which is a Cable Plug supporting SOP'. Cable length up to 5 meters.
SID	A Standard ID (SID) is a unique 16-bit value assigned by the USB-IF to identify an industry standard.
Single-lane (x1)	USB 3.2 single-lane operation is defined as signaling on only one set of SuperSpeed USB transmit and receive differential pairs (TX1/RX1 in the cable/plug).
Sink	Port asserting Rd on CC and when attached is consuming power from VBUS; most commonly a Device.
Skin Temperature	In reference to an active cable, the temperature of a plug's over-mold.
Source	Port asserting Rp on CC and when attached is providing power over VBUS; most commonly a Host or Hub DFP.
SVID	General reference to either a SID or a VID. Used by *USB PD* Structured VDMs when requesting SIDs and VIDs from a device.
Target System (TS)	The system being debugged in Debug Accessory Mode.
Type-A	A general reference to all versions of USB "A" plugs and receptacles.
Type-B	A general reference to all versions of USB "B" plugs and receptacles.
Type-C Plug	A USB plug conforming to the mechanical and electrical requirements in this specification.
Type-C Port	The USB port associated to a USB Type-C receptacle. This includes the USB signaling, CC logic, multiplexers and other associated logic.
Type-C Receptacle	A USB receptacle conforming to the mechanical and electrical requirements of this specification.
UFP	Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks VBUS and supports data.
USB 2.0 Type-C Cable	A USB Type-C to Type-C cable that only supports *USB 2.0* data operation. This cable does not include *USB 3.2* or SBU wires.
USB 2.0 Type-C Plug	A USB Type-C plug specifically designed to implement the *USB 2.0* Type-C cable.
USB Full-Featured Type-C Cable	A USB Type-C to Type-C cable that supports *USB 2.0*, *USB 3.2* and *USB4* data operation. This cable includes SBU wires and is an Electronically Marked Cable.

Term	Description
USB Full-Featured Type-C Plug	A USB Type-C plug specifically designed to implement the USB Full-Featured Type-C cable.
USB4 Hub	A USB4 hub product is used for USB port expansion, includes only USB upstream and downstream ports, and does not include any additional capability that exposes other connector types or functions except as defined in Section 5.2.3 (Alternate Modes).
USB4-based Dock	A USB4-based dock product combines a USB4 hub (including at least one exposed USB Type-C downstream port) with additional capabilities that either exposes other connector types and/or includes other user-visible functions, e.g. storage, networking, etc. Examples of functions that are not considered user-visible include firmware update and device authentication.
USB Safe State	The USB Safe State as defined by the *USB PD* specification.
VCONN-Powered Accessory (VPA)	An accessory that is powered from VCONN to operate in an Alternate Mode. VPAs cannot implement the charge-through mechanism described for VPDs, and instead must intermediate by negotiating USB Power Delivery with both the connected host and source in order to enable similar functionality.
VCONN-Powered USB Device (VPD)	A USB direct-connect or captive-cable device that can be powered solely from either VCONN or VBUS. VPDs may optionally support the VPD charge-through capability.
VCONN_Swap	*USB PD* VCONN Swap.
VDM	Vendor Defined Message as defined by the *USB PD* specification.
VID	A Vendor ID (VID) is a unique 16-bit value assigned by the USB-IF to identify a vendor.
vSafe0V	VBUS “0 volts” as defined by the *USB PD* specification.
vSafe5V	VBUS “5 volts” as defined by the *USB PD* specification.
x1	See Single-lane.
x2	See Dual-lane.

2 Overview

2.1 Introduction

The USB Type-C® receptacle, plug and cable provide a smaller, thinner and more robust alternative to legacy USB interconnect (Standard and Micro USB cables and connectors). This solution targets use in very thin platforms, ranging from ultra-thin notebook PCs down to smart phones where existing Standard-A and Micro-AB receptacles are deemed too large, difficult to use, or inadequately robust. Some key specific enhancements include:

- The USB Type-C receptacle may be used in very thin platforms as its total system height for the mounted receptacle is under 3 mm
- The USB Type-C plug enhances ease of use by being plug-able in either upside-up or upside-down directions
- The USB Type-C cable enhances ease of use by being plug-able in either direction between host and devices

While the USB Type-C interconnect no longer physically differentiates plugs on a cable by being an A-type or B-type, the USB interface still maintains such a host-to-device logical relationship. Determination of this host-to-device relationship is accomplished through a Configuration Channel (CC) that is connected through the cable. In addition, the Configuration Channel is used to set up and manage power and Alternate/Accessory Modes.

Using the Configuration Channel, the USB Type-C interconnect defines a simplified 5 volt VBUS-based power delivery and charging solution that supplements what is already defined in the *USB 3.2 Specification*. More advanced power delivery and battery charging features over the USB Type-C interconnect are based on the *USB Power Delivery Specification*. As a product implementation improvement, the USB Type-C interconnect shifts the *USB PD* communication protocol from being communicated over VBUS to being delivered across the USB Type-C Configuration Channel.

The USB Type-C receptacle, plug and cable designs are intended to support future USB functional extensions. As such, consideration was given to frequency scaling performance, pin-out arrangement and the configuration mechanisms when developing this solution. The definition of future USB functional extensions is not in the scope of this specification but rather will be provided in future releases of the base USB Specification, i.e., beyond the existing *USB4™ Specification*.

Figure 2-1 illustrates the comprehensive functional signal plan for the USB Full-Featured Type-C receptacle, not all signals shown are required in all platforms or devices. As shown, the receptacle signal list functionally delivers both *USB 2.0* (D+ and D−) and either *USB 3.2* or *USB4* (TX and RX pairs) data buses, USB power (VBUS) and ground (GND), Configuration Channel signals (CC1 and CC2), and two Sideband Use (SBU) signal pins. Multiple sets of USB data bus signal locations in this layout facilitate being able to functionally map the USB signals independent of plug orientation in the receptacle. For reference, the signal pins are labeled. For the *USB 2.0* Type-C receptacle, neither the *USB 3.2* nor *USB4* signals are implemented.

Figure 2-1 USB Type-C Receptacle Interface (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 2-2 illustrates the comprehensive functional signal plan for the USB Type-C plug. Only one CC pin is connected through the cable to establish signal orientation and the other CC pin is repurposed as VCONN for powering electronics in the USB Type-C plug. Also, only one set of *USB 2.0* D+/D− wires are implemented in a USB Type-C cable. For USB Type-C cables that only intend to support *USB 2.0* functionality, the TX/RX and SBU signals are not implemented. For the USB Type-C Power-Only plug (intended only for USB Type-C Sink applications), only nine contacts are implemented to support CC, VBUS, and GND.

Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View)

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

2.2 USB Type-C Receptacles, Plugs and Cables

Cables and connectors, including USB Type-C to USB legacy cables and adapters, are explicitly defined within this specification. These are the only connectors and cables that are authorized by the licensing terms of this specification. All licensed cables and connectors are required to comply with the compliance and certification requirements that are developed and maintained by the USB-IF.

The following USB Type-C receptacles and plugs are defined.

- USB Full-Featured Type-C receptacle for *USB 2.0*, *USB 3.2*, *USB4* and full-featured platforms and devices
- *USB 2.0* Type-C receptacle for *USB 2.0* platforms and devices
- USB Full-Featured Type-C plug
- *USB 2.0* Type-C plug
- USB Type-C Power-Only plug

The following USB Type-C cables are defined.

- USB Full-Featured Type-C cable with a USB Full-Featured Type-C plug at both ends for *USB 3.2*, *USB4* and full-featured applications
- *USB 2.0* Type-C cable with a *USB 2.0* Type-C plug at both ends for *USB 2.0* applications
- Captive cable with either a USB Full-Featured Type-C plug or *USB 2.0* Type-C plug at one end
- Active cables as defined in Chapter 6

All of the defined USB Type-C receptacles, plugs and cables (except OIAC) support USB charging applications, including support for the optional USB Type-C-specific implementation of the *USB Power Delivery Specification* (See Section 4.6.2.4).

All USB Full-Featured Type-C cables are electronically marked. *USB 2.0* Type-C cables may be electronically marked. See Section 4.9 for the requirements of Electronically Marked Cables.

The following USB Type-C to USB legacy cables and adapters are defined.

- USB 3.2 Type-C to Legacy Host cable with a USB Full-Featured Type-C plug at one end and a USB 3.1 Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy USB host*
- USB 2.0 Type-C to Legacy Host cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Standard-A plug at the other end – *this cable supports use of a USB Type-C-based device with a legacy USB 2.0 host (primarily for mobile charging and sync applications)*
- USB 3.2 Type-C to Legacy Device cable with a USB Full-Featured Type-C plug at one end and a USB 3.1 Standard-B plug at the other end – *this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host*
- USB 2.0 Type-C to Legacy Device cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Standard-B plug at the other end – *this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host*
- USB 2.0 Type-C to Legacy Mini Device cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Mini-B plug at the other end – *this cable supports use of legacy devices with a USB 2.0 Type-C-based host*
- USB 3.2 Type-C to Legacy Micro Device cable with a USB Full-Featured Type-C plug at one end and a USB 3.1 Micro-B plug at the other end – *this cable supports use of legacy USB 3.1 hubs and devices with a USB Type-C-based host*
- USB 2.0 Type-C to Legacy Micro Device cable with a USB 2.0 Type-C plug at one end and a USB 2.0 Micro-B plug at the other end – *this cable supports use of legacy USB 2.0 hubs and devices with a USB Type-C-based host*
- USB 3.2 Type-C to Legacy Standard-A adapter with a USB Full-Featured Type-C plug at one end and a USB 3.1 Standard-A receptacle at the other end – *this adapter supports use of a legacy USB "thumb drive" style device or a legacy USB ThinCard device with a USB 3.2 Type-C-based host*
- USB 2.0 Type-C to Legacy Micro-B adapter with a USB 2.0 Type-C plug at one end and a USB 2.0 Micro-B receptacle at the other end – *this adapter supports charging a USB Type-C-based mobile device using a legacy USB Micro-B-based chargers, either captive cable-based or used in conjunction with a legacy USB 2.0 Standard-A to Micro-B cable*

USB Type-C receptacle to USB legacy adapters are explicitly not defined or allowed. Such adapters would allow many invalid and potentially unsafe cable connections to be constructed by users.

2.3 Configuration Process

The USB Type-C receptacle, plug and cable solution incorporates a configuration process to detect a downstream facing port to upstream facing port (Source-to-Sink) connection for VBUS management and host-to-device connected relationship determination.

The USB Type-C port configuration process is used for the following:

- Source-to-Sink attach/detach detection
- Plug orientation/cable twist detection
- Initial power (Source-to-Sink) detection and establishing the data (Host-to-Device) relationship
- Detect if cable requires VCONN
- USB Type-C VBUS current detection and usage

- *USB PD* communication
- Discovery and configuration of functional extensions

Two pins on the USB Type-C receptacle, CC1 and CC2, are used for this purpose. Within a standard USB Type-C cable, only a single CC pin position within each plug of the cable is connected through the cable.

2.3.1 Source-to-Sink Attach/Detach Detection

Initially, Source-to-Sink attach is detected by a host or hub port (Source) when one of the CC pins at its USB Type-C receptacle senses a specified resistance to GND. Subsequently, Source-to-Sink detach is detected when the CC pin that was terminated at its USB Type-C receptacle is no longer terminated to GND.

Power is not applied to the USB Type-C host or hub receptacle (VBUS or VCONN) until the Source detects the presence of an attached device (Sink) port. When a Source-to-Sink attach is detected, the Source is expected to enable power to the receptacle and proceed to normal USB operation with the attached device. When a Source-to-Sink detach is detected, the port sourcing VBUS removes power.

2.3.2 Plug Orientation/Cable Twist Detection

The USB Type-C plug can be inserted into a receptacle in either one of two orientations, therefore the CC pins enable a method for detecting plug orientation in order to determine the lane ordering of the SuperSpeed USB data signal pairs functionally connected through the cable and identify the Configuration Lane for dual-lane operation when supported. This allows for signal routing, if needed, within a host or device to be established for a successful connection.

2.3.3 Initial Power (Source-to-Sink) Detection and Establishing the Data (Host-to-Device) Relationship

Unlike existing USB Type-A and USB Type-B receptacles and plugs, the mechanical characteristics of the USB Type-C receptacle and plug do not inherently establish the relationship of USB host and device ports. The CC pins on the receptacle also serve to establish an initial power (Source-to-Sink) and data (Host-to-Device) relationships prior to the normal USB enumeration process.

For the purpose of defining how the CC pins are used to establish the initial power relationship, the following port power behavior modes are defined.

1. Source-only – for this mode, the port exclusively behaves as a Source
2. Sink-only – for this mode, the port exclusively behaves as a Sink
3. Dual-Role-Power (DRP) – for this mode, the port can behave either as a Source or Sink

Additionally, when a port supports USB data operation, a port's data behavior modes are defined.

1. DFP-only – for this mode, the port exclusively behaves as a DFP
2. UFP-only – for this mode, the port exclusively behaves as a UFP
3. Dual-Role-Data (DRD) – for this mode, the port can behave either as a DFP or UFP

The DFP-only and UFP-only ports behaviorally map to traditional USB host ports and USB device ports, respectively but may not necessarily do USB data communication. When a host-only port is attached to a device-only port, the behavior from the user's perspective follows the traditional USB host-to-device port model. However, the USB Type-C connector solution does not physically prevent host-to-host or device-to-device connections. In this case, the resulting host-to-host or device-to-device connection results in a safe but non-functional situation.

Once initially established, the Source supplies VBUS and behaves as a DFP, and the Sink consumes VBUS and behaves as a UFP. *USB PD*, when supported by both ports, may then be used to independently swap both the power and data roles of the ports.

A port that supports dual-role operation by being able to shift to the appropriate connected mode when attached to either a Source-only or Sink-only port is a DRP. In the special case of a DRP being attached to another DRP, an initialization protocol across the CC pins is used to establish the initial host-to-device relationship. Given no role-swapping intervention, the determination of which is DFP or UFP is random from the user's perspective.

Two independent set of mechanisms are defined to allow a USB Type-C DRP to functionally swap power and data roles. When *USB PD* is supported, power and data role swapping is performed as a subsequent step following the initial connection process. For non-PD implementations, power/data role swapping can optionally be dealt with as part of the initial connection process. To improve the user's experience when connecting devices that are of categorically different types, products may be implemented to strongly prefer being a DFP or a UFP, such that the DFP/UFP determination becomes predictable when connecting two DRPs of differing categories. See Section 4.5.1.4 for more on available swapping mechanisms.

As an alternative to role swapping, a USB Type-C DRP may provide useful functionality by when operating as a host, exposing a CDC/network (preferably TCP/IP) stack or when operating as a device, exposing a CDC/network interface.

USB hubs have two types of ports, a UFP that is connected to a DFP (host or another hub) that initially functions as a Sink, and one or more DFPs for connecting other devices that initially function as Sources.

2.3.4 USB Type-C VBUS Current Detection and Usage

With the USB Type-C connector solution, a Source (host or downstream hub port) may implement higher source current over VBUS to enable faster charging of mobile devices or higher-power devices. All USB host and hub ports advertise via the CC pins the level of current that is presently available. The USB device port is required to manage its load to stay within the current level offered by the host or hub, including dynamically scaling back the load if the host or hub port changes its advertisement to a lower level as indicated over the CC pins.

Three current level advertisements at 5V VBUS are defined by USB Type-C Current:

- Default is the as-configured for high-power operation current value as defined by a USB Specification (500 mA for USB 2.0 ports; 900 mA or 1,500 mA for USB 3.2 ports operating in single-lane or dual-lane, respectively)
- USB Type-C Current @ 1.5 A
- USB Type-C Current @ 3.0 A

There is a clear functional distinction between advertising Default versus the USB Type-C Current at either 1.5 A or 3.0 A.

- Default is intended for host operation in providing bus power to a connected device where the host manages the device's current consumption for the low-power, high-power and suspend states as defined in the USB base specifications.

- USB Type-C Current at either 1.5 A or 3.0 A is primarily intended for charging applications. The Sink can vary its current draw up to the advertised limit. Offering USB Type-C Current at either 1.5 A or 3.0 A is allowed for a host providing bus power to a device. The host needs to assume that the device will continuously draw up to the offered limit.

The higher USB Type-C Current levels that can be advertised allows hosts and devices that do not implement *USB PD* to take advantage of higher charging current.

2.3.5 USB PD Communication

USB Power Delivery is a feature on products (hosts, hubs and devices). *USB PD* communications is used to:

- Establish power contracts that allow voltage and current beyond existing USB data bus specifications.
- Change the port sourcing VBUS.
- Change the port sourcing VCONN.
- Swap DFP and UFP roles.
- Communicate with cables.

The *USB PD* Bi-phase Mark Coded (BMC) communications are carried on the CC wire of the USB Type-C cable.

2.3.6 Functional Extensions

Functional extensions (see Chapter E) are enabled via a communications channel across CC using methods defined by the *USB Power Delivery Specification*.

2.4 VBUS

VBUS provides a path to deliver power between a host and a device, and between a USB power charger and a host/device. A simplified high-current supply capability is defined for hosts and chargers that optionally support current levels beyond the *USB 2.0*, *USB 3.2*, and *USB4* specifications. The *USB Power Delivery Specification* is supported.

Table 2-1 summarizes the power supply options available from the perspective of a device with the USB Type-C connector. Not all options will be available to the device from all host or hub ports – only the first two listed options are mandated by the base USB specifications and form the basis of USB Type-C Current at the Default USB Power level.

Table 2-1 Summary of power supply options

Mode of Operation	Voltage	Current	Notes
USB 2.0	5 V	See *USB 2.0*	
USB 3.2	5 V	See *USB 3.2*	
USB4	5 V	1.5 A	See Section 5.3.
USB BC 1.2	5 V	1.5 A[1]	Legacy charging
USB Type-C Current @ 1.5 A	5 V	1.5 A	Supports higher power devices
USB Type-C Current @ 3.0 A	5 V	3 A	Supports higher power devices
USB PD	Configurable up to 48 V	Configurable up to 5 A	Directional control and power level management

Notes:

1. Whereas *USB BC 1.2* specification permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A, the USB Type-C specification requires that a Source port that supports *USB BC 1.2* be at a minimum capable of supplying 1.5 A and advertise USB Type-C Current @ 1.5 A in addition to supporting the *USB BC 1.2* power provider termination.

The USB Type-C receptacle is specified for current capability of 5 A whereas standard USB Type-C cable assemblies are rated for 3 A. The higher rating of the receptacle enables systems to deliver more power over directly attached docking solutions or using appropriately designed chargers with captive cables when implementing *USB PD*. Also, USB Type-C cable assemblies designed for *USB PD* and appropriately identified via electronic marking are allowed to support up to 5 A.

USB Type-C cable assemblies designed for *USB PD* Extended Power Range (EPR) operation are required to have an electronic marking indicating EPR compatibility. These cables are required to be electronically marked for 5 A and 50 V and include the EPR Mode Capable bit set.

2.5 VCONN

Once the connection between host and device is established, the CC pin (CC1 or CC2) in the receptacle that is not connected via the CC wire through the standard cable is repurposed to source VCONN to power circuits in the plug needed to implement Electronically Marked Cables (see Section 4.9), VCONN-Powered Accessories and VCONN-Powered USB Devices. Initially, the source supplies VCONN and the source of VCONN may be swapped using *USB PD* VCONN_Swap.

Once VCONN is available, all electronically marked cables use it as the only power source. If VCONN is applied after VBUS, then until VCONN is available, the cable may remain unpowered or may draw power from VBUS.

VCONN functionally differs from VBUS in that it is isolated from the other end of the cable. VCONN is independent of VBUS and, unlike VBUS which can use *USB PD* to support higher voltages, VCONN voltage stays within the range of 3.0 to 5.5 V (vVCONNValid).

2.6 Hubs

USB hubs implemented with USB Type-C receptacles are required to clearly identify the upstream facing port. This requirement is needed because a user can no longer know which port on a hub is the upstream facing port and which ports are the downstream facing ports by the type of receptacles that are exposed, i.e., USB Type-B is the upstream facing port and USB Type-A is a downstream facing port.

3 Mechanical

3.1 Overview

This chapter defines the USB Type-C® connectors and wired cable assemblies. Cables which include active elements in the data path are defined in Chapter 6 (Active Cables).

3.1.1 Compliant Connectors

The USB Type-C specification defines the following standard connectors:

- USB Full-Featured Type-C receptacle
- *USB 2.0* Type-C receptacle
- USB Full-Featured Type-C plug
- *USB 2.0* Type-C plug
- USB Type-C Power-Only plug

3.1.2 Compliant Cable Assemblies

Table 3-1 summarizes the USB Type-C standard cable assemblies along with the primary differentiating characteristics. All USB Full-Featured Type-C cables shall support simultaneous, independent signal transmission on both *USB 3.2* and *USB4™* (TX and RX pairs) data buses. For USB Power Delivery, each cable assembly is identified as being either only usable for Standard Power Range (SPR) operation or usable for both SPR and Extended Power Range (EPR) operation. Existing SPR 5 A cables are being deprecated and replaced by EPR cables. All cables that are either full-featured and/or are rated at more than 3 A current are Electronically Marked Cables.

Table 3-1 USB Type-C Standard Cable Assemblies

Cable Ref	Plug 1	Plug 2	USB Version	Nominal Cable Length[2]	Current Rating	USB Power Delivery	USB Type-C Electronically Marked
CC2-3	C	C	USB 2.0	≤ 4 m	3 A	Supported (SPR only)	Optional
CC2-5[1]					5 A		Required
CC2-5E					5 A	Supported (SPR & EPR)	Required
CC3G1-3	C	C	USB 3.2 Gen1 and USB4 Gen2	≤ 2 m	3 A	Supported (SPR only)	Required
CC3G1-5[1]					5 A		
CC3G1-5E					5 A	Supported (SPR & EPR)	Required
CC3G2-3	C	C	USB 3.2 Gen2 and USB4 Gen2	≤ 1 m	3 A	Supported (SPR only)	Required
CC3G2-5[1]					5 A		
CC3G2-5E					5 A	Supported (SPR & EPR)	Required
CC4G3-3	C	C	USB4 Gen3	≤ 0.8 m	3 A	Supported (SPR only)	Required
CC4G3-5[1]					5 A		
CC4G3-5E					5 A	Supported (SPR & EPR)	Required

Note 1: These cables are deprecated in favor of having all 5 A cables be EPR-capable versions.

Note 2: The cable lengths listed in the table are informative and represent the practical lengths based on cable performance requirements.

USB Type-C products are also allowed to have a captive cable. See Section 3.4.3.

3.1.3 Compliant USB Type-C to Legacy Cable Assemblies

Table 3-2 summarizes the USB Type-C legacy cable assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. *USB 3.2* Type-C legacy cables assemblies that only offer performance up to *USB 3.1* Gen1 are not allowed by this specification. All USB Type-C to legacy cable assemblies are only defined specific to *USB 2.0* and *USB 3.2* as there are no USB Type-C to legacy cables that are uniquely applicable to *USB4*.

For USB Type-C legacy cable assemblies that incorporate Rp termination, the value of this termination is required to be specified to the Default setting of USB Type-C Current even though the cable assemblies are rated for 3 A. The Rp termination in these cables is intended to represent the maximum current of a compliant legacy USB host port, not the current rating of the cable itself. The cable current rating is intentionally set to a higher level given that there are numerous non-standard power chargers that offer more than the Default levels established by the *USB 2.0* and *USB 3.1* specifications.

Table 3-2 USB Type-C Legacy Cable Assemblies

Cable Ref	Plug 1[3]	Plug 2[3]	USB Version	Cable Length	Current Rating
AC2-3	USB 2.0 Standard-A	USB 2.0 Type-C[1]	USB 2.0	≤ 4 m	3 A
AC3G2-3	USB 3.1 Standard-A	USB Full-Featured Type-C[1]	USB 3.1 Gen2	≤ 1 m	3 A
CB2-3	USB 2.0 Type-C[2]	USB 2.0 Standard-B	USB 2.0	≤ 4 m	3 A
CB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-B	USB 3.1 Gen2	≤ 1 m	3 A
CmB2	USB 2.0 Type-C[2]	USB 2.0 Mini-B	USB 2.0	≤ 4 m	500 mA
CμB2-3	USB 2.0 Type-C[2]	USB 2.0 Micro-B	USB 2.0	≤ 2 m	3 A
CμB3G2-3	USB Full-Featured Type-C[2]	USB 3.1 Micro-B	USB 3.1 Gen2	≤ 1 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter cable are required to have Rp (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter cable are required to have Rd (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.5.3 for the mated resistance and temperature rise required for the legacy plugs.

3.1.4 Compliant USB Type-C to Legacy Adapter Assemblies

Table 3-3 summarizes the USB Type-C legacy adapter assemblies along with the primary differentiating characteristics. The cable lengths listed in the table are informative and represents the practical length based on cable performance requirements. All USB Type-C to legacy adapter assemblies are only defined specific to *USB 2.0* and *USB 3.2* as there are no USB Type-C to legacy adapters that are uniquely applicable to *USB4*.

Table 3-3 USB Type-C Legacy Adapter Assemblies

Adapter Ref	Plug	Receptacle[3]	USB Version	Cable Length	Current Rating
CμBR2-3	USB 2.0 Type-C[1]	USB 2.0 Micro-B	USB 2.0	≤ 0.15 m	3 A
CAR3G1-3	USB Full-Featured Type-C[2]	USB 3.1 Standard-A	USB 3.1 Gen1	≤ 0.15 m	3 A

Notes:

1. USB Type-C plugs associated with the "B" end of a legacy adapter are required to have Rp (56 kΩ ± 5%) termination incorporated into the plug assembly – see Section 4.5.3.2.2.
2. USB Type-C plugs associated with the "A" end of a legacy adapter are required to have Rd (5.1 kΩ ± 20%) termination incorporated into the plug assembly – see Section 4.5.3.2.1.
3. Refer to Section 3.7.6.3 for the mated resistance and temperature rise required for the legacy receptacles.

3.2 USB Type-C Connector Mating Interfaces

This section defines the connector mating interfaces, including the connector interface drawings, pin assignments, and descriptions. All dimensions in figures are in millimeters

3.2.1 Interface Definition

Figure 3-1 and Figure 3-3 show, respectively, the USB Type-C receptacle and USB Full-Featured Type-C plug interface dimensions.

Figure 3-11 shows the *USB 2.0* Type-C plug interface dimensions. The dimensions that govern the mating interoperability are specified. All the REF dimensions are provided for reference only, not hard requirements.

Key features, configuration options, and design areas that need attention:

1. Figure 3-1 shows a vertical-mount receptacle. Other PCB mounting types such as right-angle mount and mid-mount are allowed.
2. A mid-plate is required between the top and bottom signals inside the receptacle tongue to manage crosstalk in full-featured applications. The mid-plate shall be connected to the PCB ground with at least two grounding points. The mid-plate shall be designed such that plug pins A4, A5, A6, A7, A8, A9, and B4, B5, B6, B7, B8, B9 do not short to ground during the connector mating process with an effective 6.2 mm receptacle shell implementation. If the receptacle connector has a short shell or no shell, the connector manufacturer shall provide an effective length shell fixture for compliance testing. A reference design of the mid-plate is provided in Section 3.2.2.1.
3. Retention of the cable assembly in the receptacle is achieved by the side-latches in the plug and features on the sides of the receptacle tongue. Side latches are required for all plugs except plugs used for docking with no cable attached. Side latches shall be connected to ground inside the plug. A reference design of the side latches is provided in Section 3.2.2.2 along with its grounding scheme. Docking applications may not have side latches, requiring special consideration regarding EMC (Electromagnetic Compatibility).
4. The EMC shielding springs are required inside the cable plug. The shielding spring shall be connected to the plug shell. No EMC shielding spring finger tip of the USB Full-Featured Type-C plug or *USB 2.0* Type-C plug shall be exposed in the plug housing opening of the unmated USB Type-C plug (see Figure 3-12). Section 3.2.2.3 shows reference designs of the EMC spring.
5. Shorting of any signal or power contact spring to the plug metal shell is not allowed. The spring in the deflected state should not touch the plug shell. An isolation layer (e.g., Kapton tape placed on the plug shell) is recommended to prevent accidental shorting due to plug shell deformation.
6. The USB Type-C receptacle shall provide an EMC ground return path through one of the following options:
    - a system of specific points of contact on the receptacle outer shell (e.g., spring fingers or spring fingers and formed solid bumps),
    - internal EMC pads, or
    - a combination of both points of contact on the receptacle outer shell and internal EMC pads.

    If points of contacts are used on the receptacle, then the receptacle points of contact shall make connection with the mated plug within the contact zones defined in Figure 3-2. A minimum of four separate points of contact are required. Additional points of contact are allowed. See Section 3.2.2.4 for a reference design of receptacle outer shell. The reference design includes four spring fingers as points of contact. Alternate configurations may include spring fingers on the A contact side or B contact side and formed solid bumps (e.g., dimples) on the B contact side or A contact side, respectively. Spring fingers are required on a minimum of one side to provide a pressure fit on opposing sides of the plug shell. Additional bumps may be used, but if bumps are on opposing sides of the receptacle shell, the minimum distance between the bumps shall be greater than the maximum plug shell defined dimension.

If internal EMC pads are present in the receptacle, then they shall comply with the requirements defined in Figure 3-1. The shielding pads shall be connected to the receptacle shell. If no receptacle shell is present, then the receptacle shall provide a means to connect the shielding pad to ground. See Section 3.2.2.3 for a reference design of the shielding pad and ground connection.

7. This specification defines the USB Type-C receptacle shell length of 6.20 mm as a reference dimension. The USB Type-C receptacle is designed to have shell length of 6.20 ± 0.20 mm to provide proper mechanical and electrical mating of the plug to the receptacle (e.g., full seating of the plug in the receptacle and protection of the receptacle tongue during insertion/withdrawal). The USB Type-C receptacle at the system level should be implemented such that the USB Type-C receptacle connector mounted in the associated system hardware has an effective shell length equal to 6.20 ± 0.20 mm.

8. The USB Type-C connector mating interface is defined so that the electrical connection may be established without the receptacle shell. To prevent excessive misalignment of the plug when it enters or exits the receptacle, the enclosure should have features to guide the plug for insertion and withdrawal when a modified receptacle shell is present. If the USB Type-C receptacle shell is modified from the specified dimension, then the recommended lead in from the receptacle tongue to the plug point of entry is 1.5 mm minimum when mounted in the system.

   This specification allows receptacle configurations with a conductive shell, a non-conductive shell, or no shell. The following requirements apply to the receptacle contact dimensions shown in SECTION A-A and ALTERNATE SECTION A-A shown in Figure 3-1:

   - If the receptacle shell is conductive, then the receptacle contact dimensions of SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 shall be used.
   - If the receptacle shell is non-conductive, then the receptacle contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 shall be used. The contact dimensions of SECTION A-A are not allowed.
   - If there is no receptacle shell, then the receptacle contact dimensions of either SECTION A-A or ALTERNATE SECTION A-A shown in Figure 3-1 shall be used. If there is no receptacle shell and the receptacle is used in an implementation that does not effectively provide a conductive shell, then a receptacle with the contact dimensions of ALTERNATE SECTION A-A shown in Figure 3-1 should be used.

   Note: If the product that incorporates a USB Type-C receptacle supports Extended Power Range (EPR) operation, consideration should be given to the choice between the contact dimensions shown in SECTION A-A versus ALTERNATE SECTION A-A. EPR-compatible Sources and Sinks have to be designed to withstand potential electrical arcing during unplug events when power is being supplied across the connector and having a larger difference in length between the CC and VBUS pins may be beneficial when implementing detection circuitry intended to help mitigate the damage due to potential arcing. See Section H.3.2 for more information.

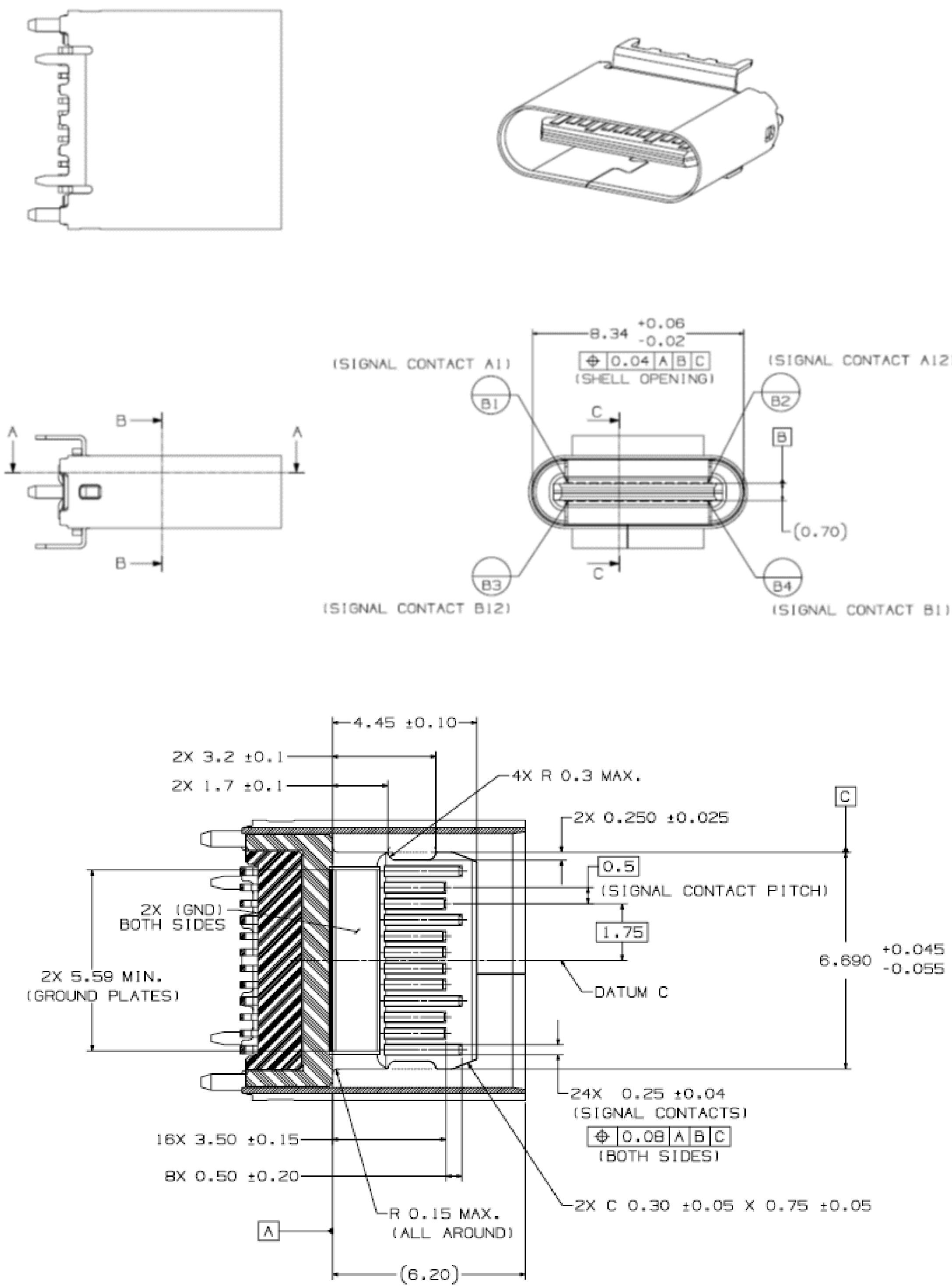
9. A paddle card (e.g., PCB) may be used in the USB Type-C plug to manage wire termination and electrical performance. Section 3.2.2.5 includes the guidelines and a design example for a paddle card.

10. This specification does not define standard footprints. Figure 3-4 shows an example SMT (surface mount) footprint for the vertical receptacle shown in Figure 3-1.

Additional reference footprints and mounting configurations are shown in Figure 3-5, Figure 3-6, Figure 3-7, Figure 3-8, Figure 3-9 and Figure 3-10.

11. The receptacle shell shall be connected to the PCB ground plane.
12. All VBUS pins shall be connected together in the USB Type-C plug.
13. All Ground return pins shall be connected together in the USB Type-C plug.
14. All VBUS pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all VBUS pins bussed together in the PCB).
15. All Ground return pins shall be connected together at the USB Type-C receptacle when it is in its mounted condition (e.g., all Ground return pins bussed together in the PCB).
16. The USB Type-C Power-Only plug is a depopulated version of the USB Full-Featured Type-C plug or the *USB 2.0* Type-C plug. The interface dimensions shall conform to Figure 3-3 or Figure 3-11. Contacts for CC, VBUS, and GND (i.e., A1, A4, A5, A9, A12, B1, B4, B9, and B12) shall be present. Physical presence of contacts in the other 15 contact locations is optional. The USB Type-C Power-Only plug shall only be used on a non-charger captive cable application. Implementation of Rd or CC communication on pin A5 is required in the application.

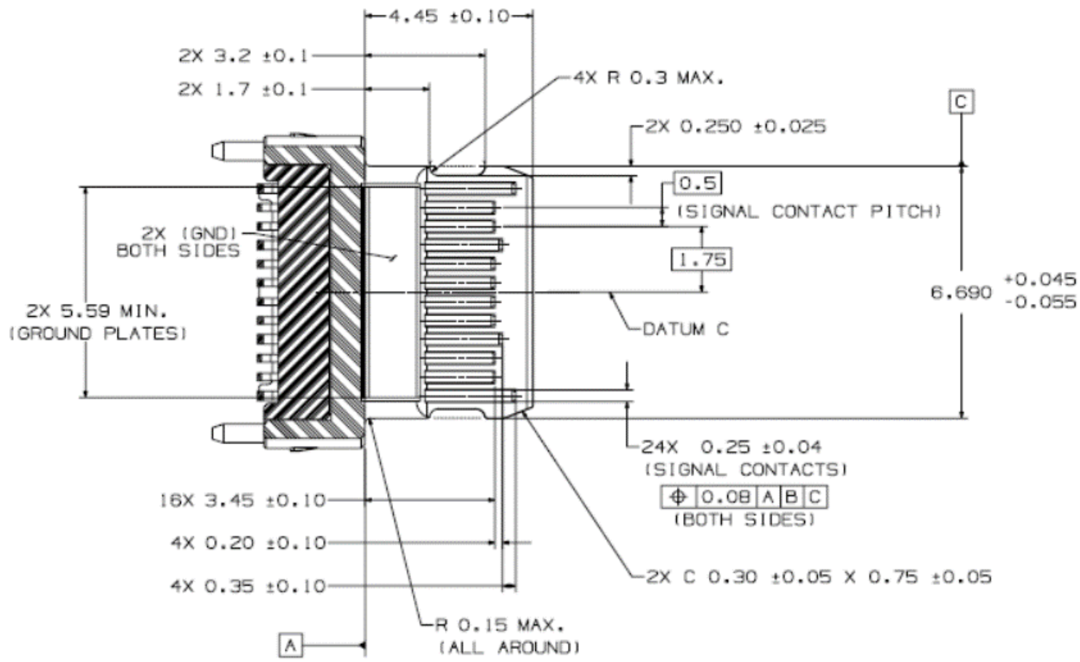
Figure 3-1 USB Type-C Receptacle Interface Dimensions



REFERENCE LENGTH – SEE NOTE 7.

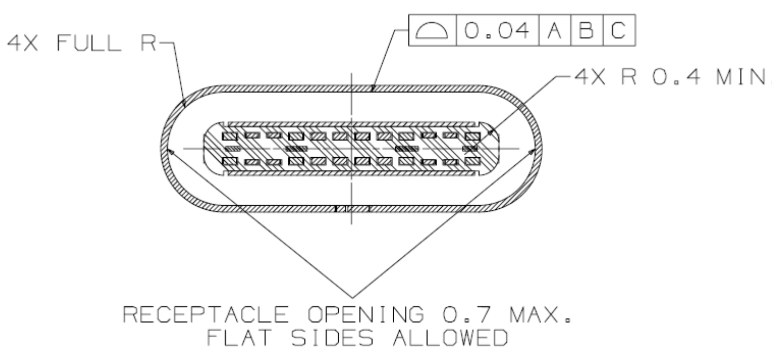
SECTION A-A

Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.



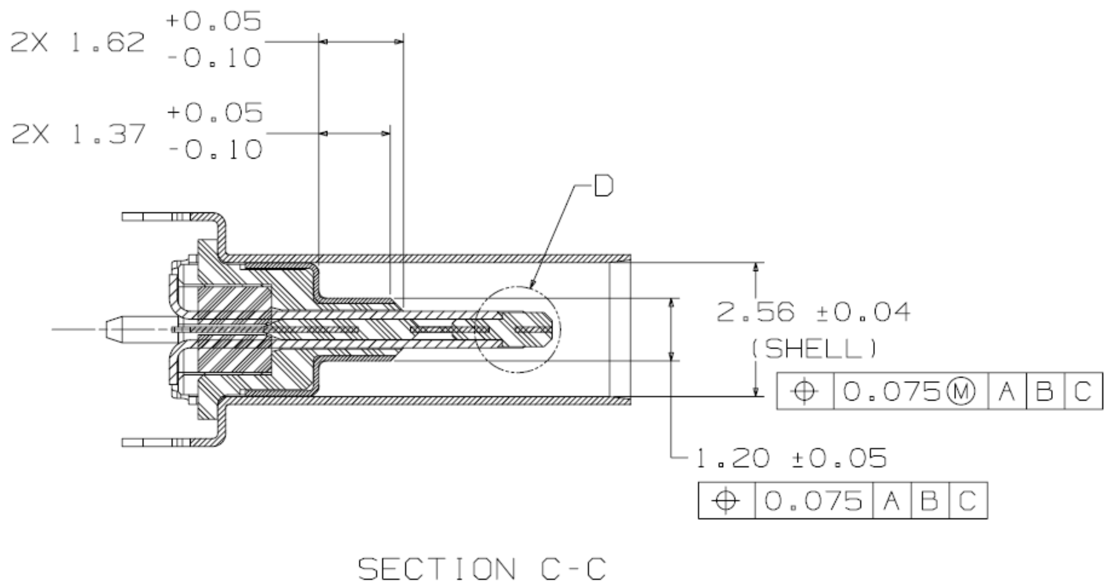
ALTERNATE SECTION A-A dimensions for use if the receptacle shell is non-conductive or there is no receptacle shell. This configuration is also allowed for receptacles with a conductive shell. See text for full requirements.

ALTERNATE SECTION A-A



SECTION B-B

Figure 3-1 USB Type-C Receptacle Interface Dimensions, cont.



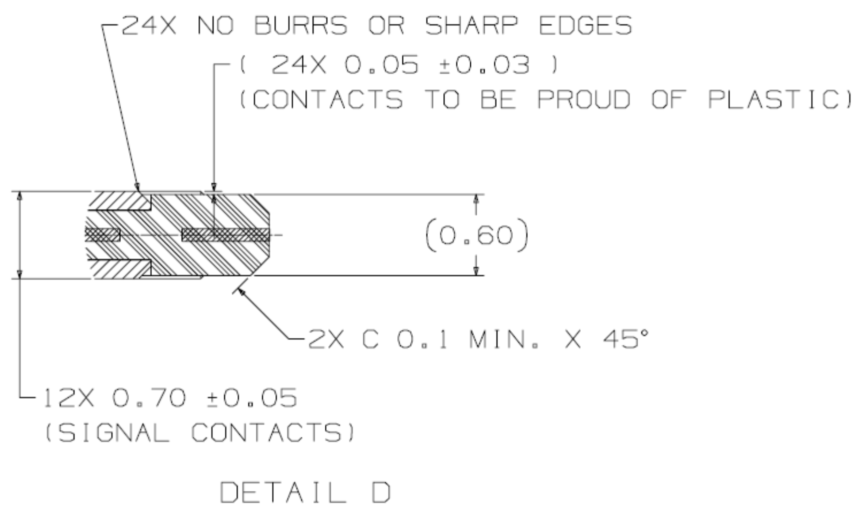


Figure 3-2 Reference Design USB Type-C Plug External EMC Spring Contact Zones

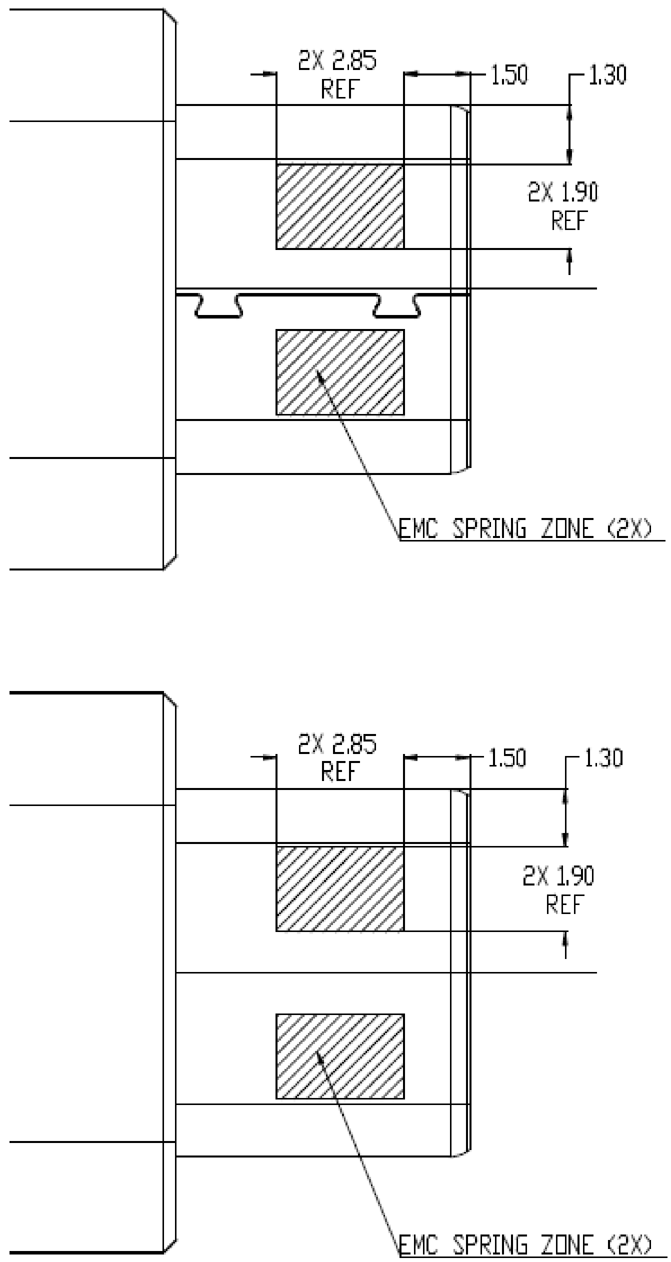


Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions

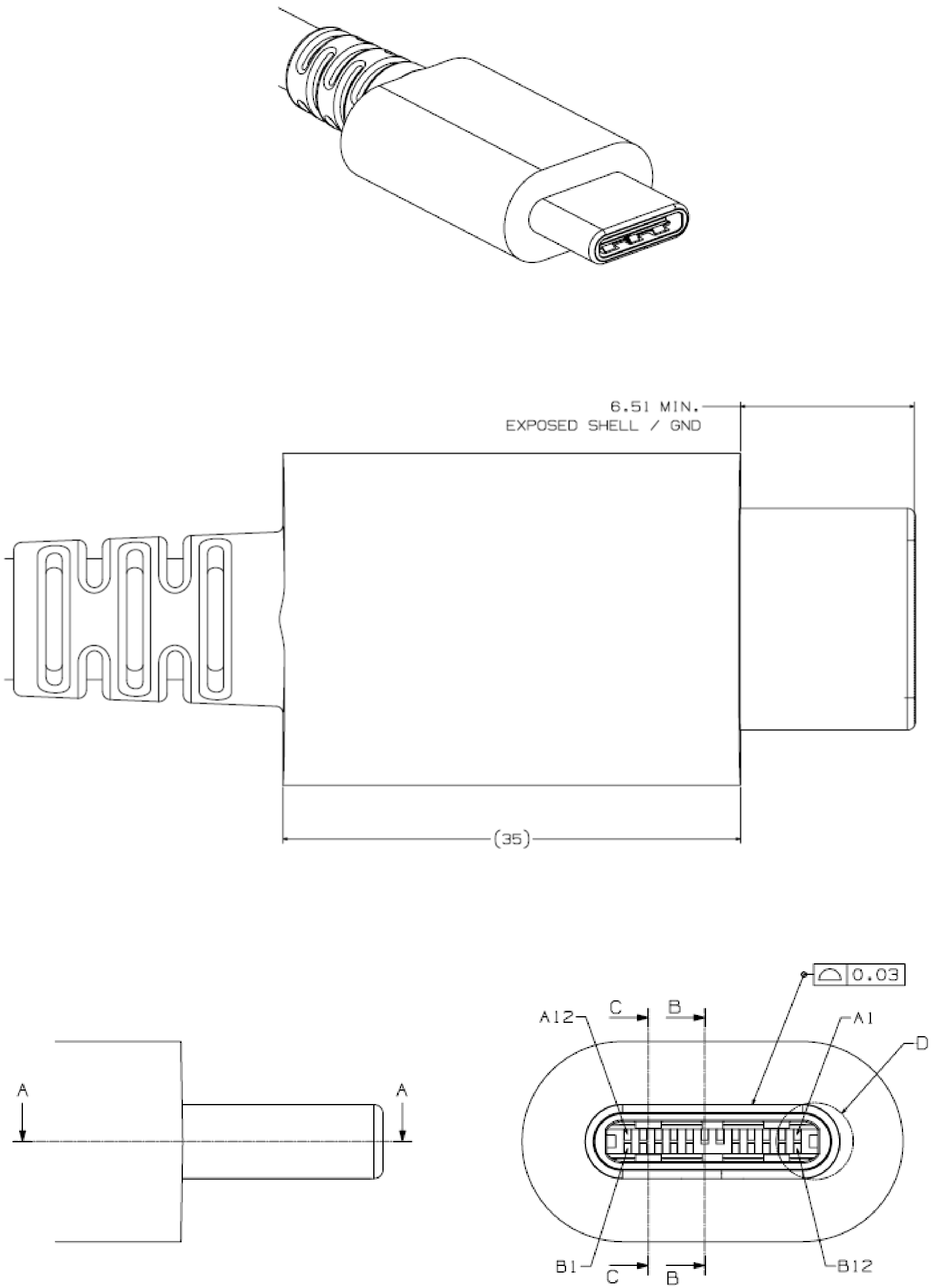
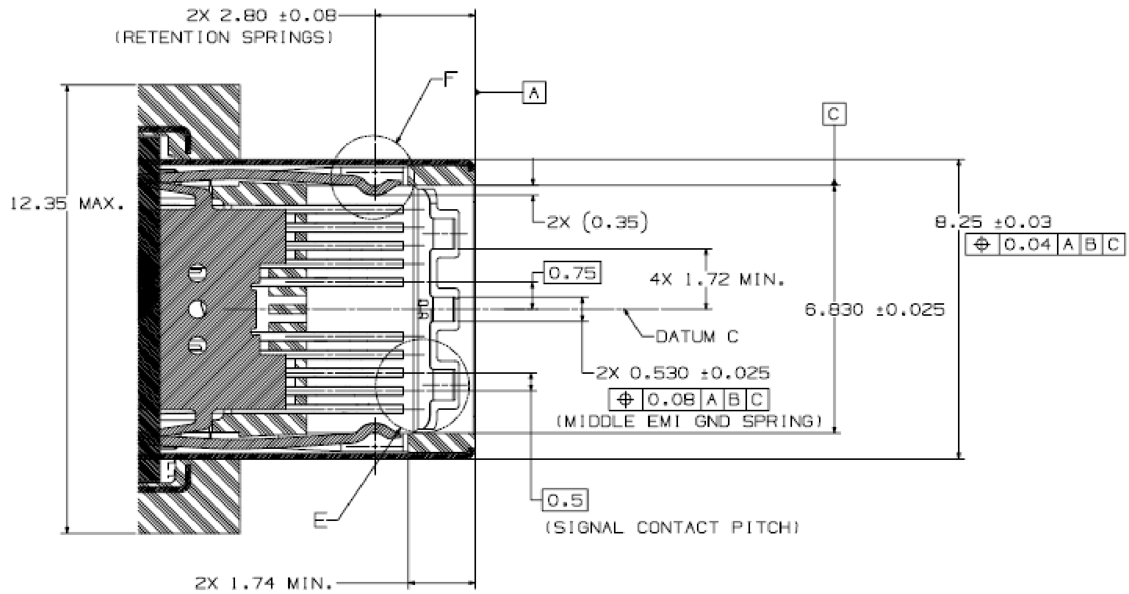
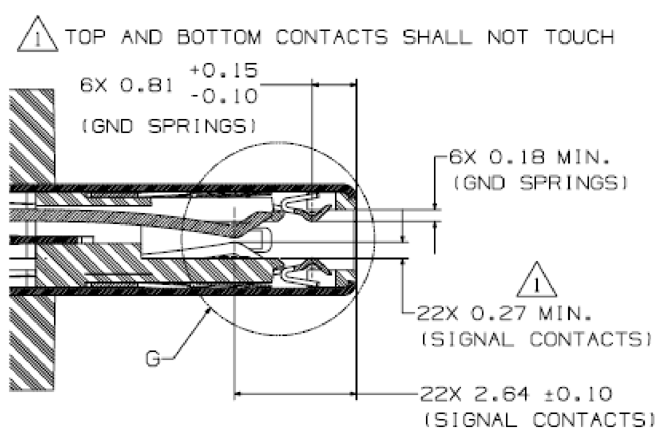


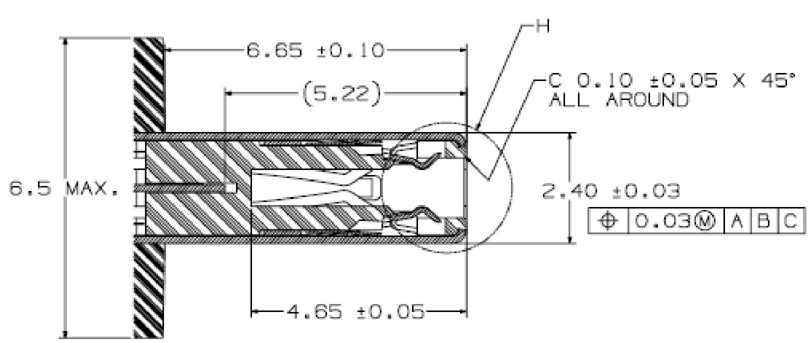
Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.



SECTION A-A



SECTION B-B



SECTION C-C

Figure 3-3 USB Full-Featured Type-C Plug Interface Dimensions, cont.

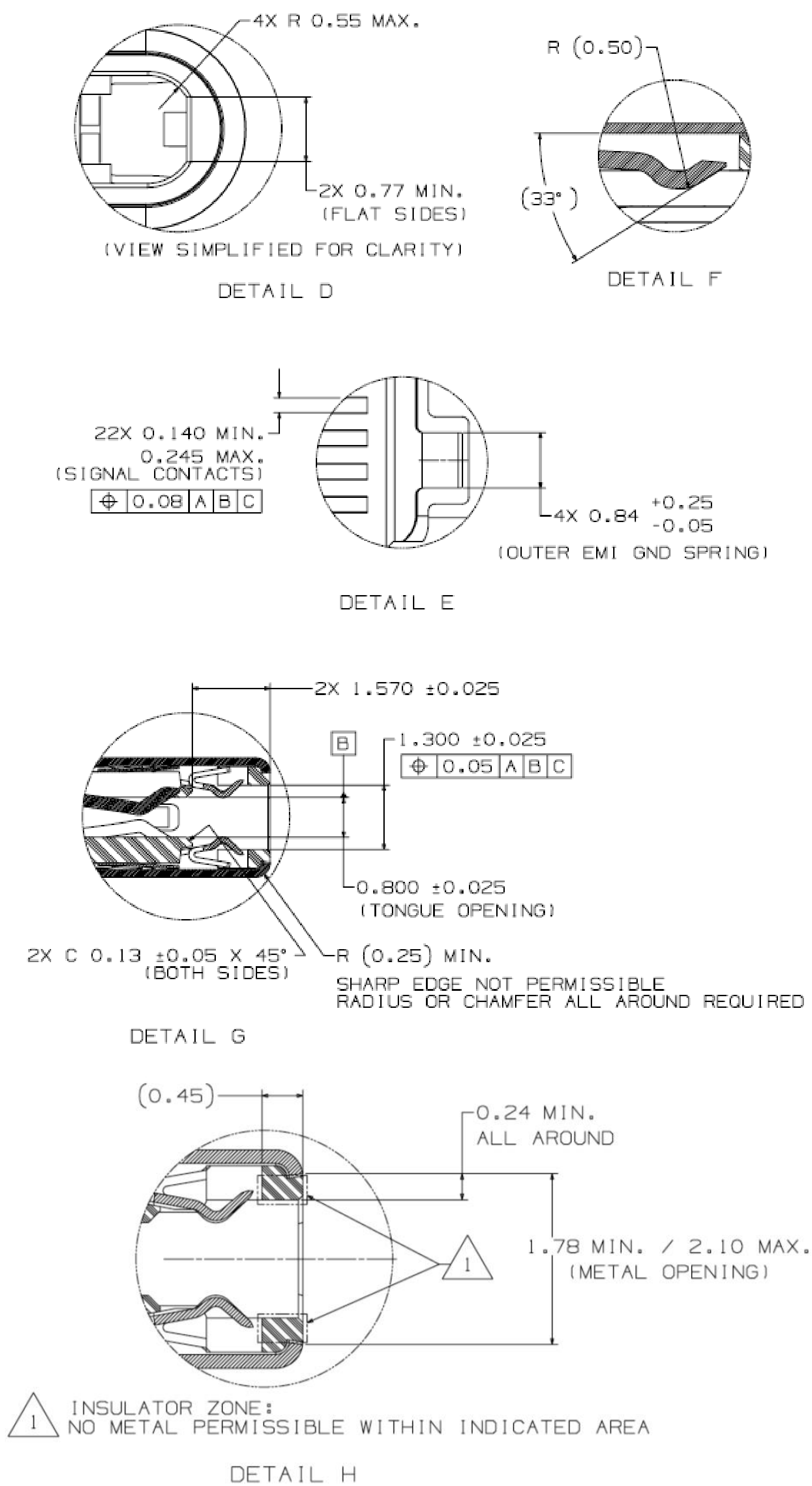


Figure 3-4 Reference Footprint for a USB Type-C Vertical Mount Receptacle (Informative)

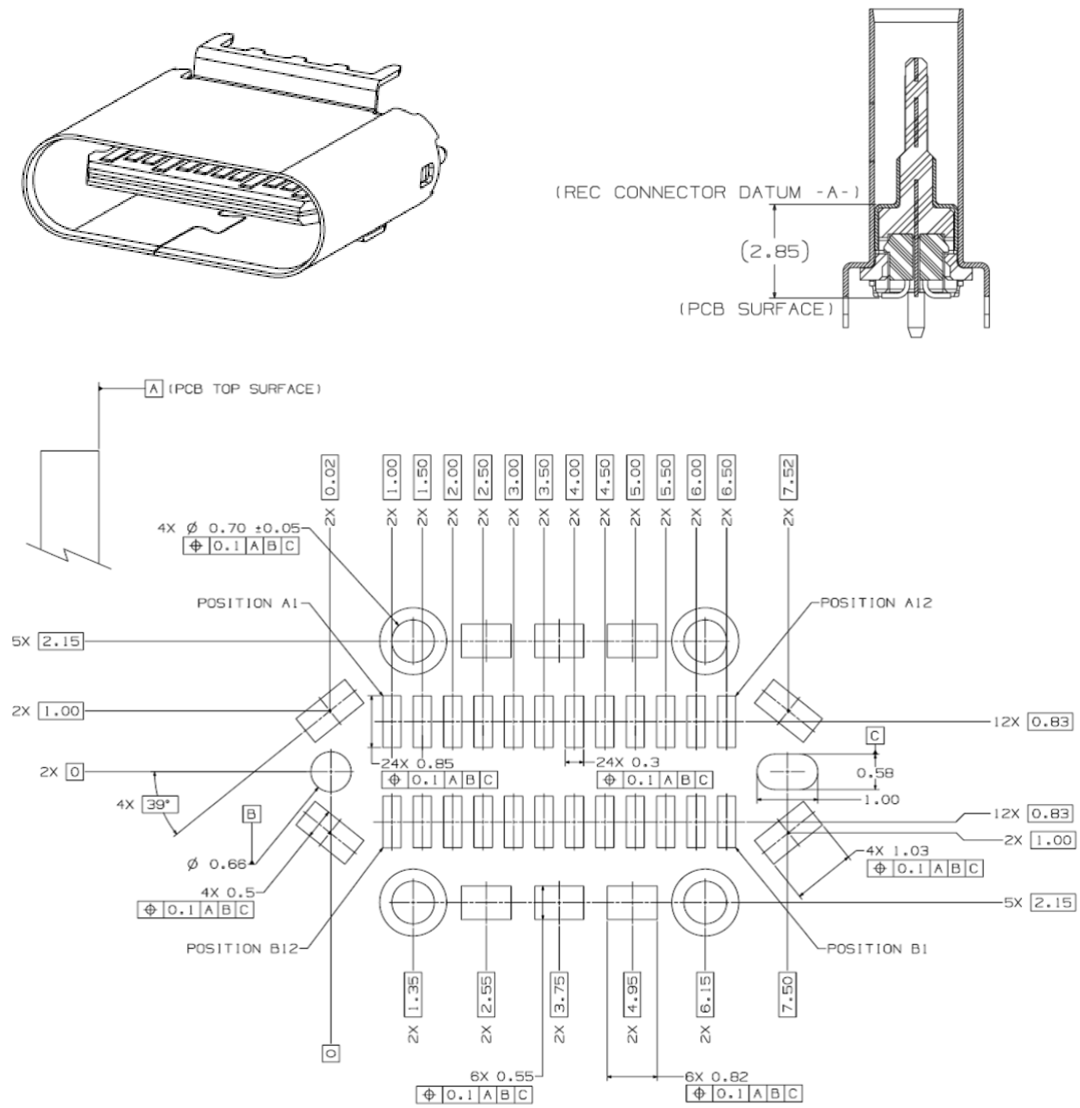


Figure 3-5 Reference Footprint for a USB Type-C Dual-Row SMT Right Angle Receptacle (Informative)

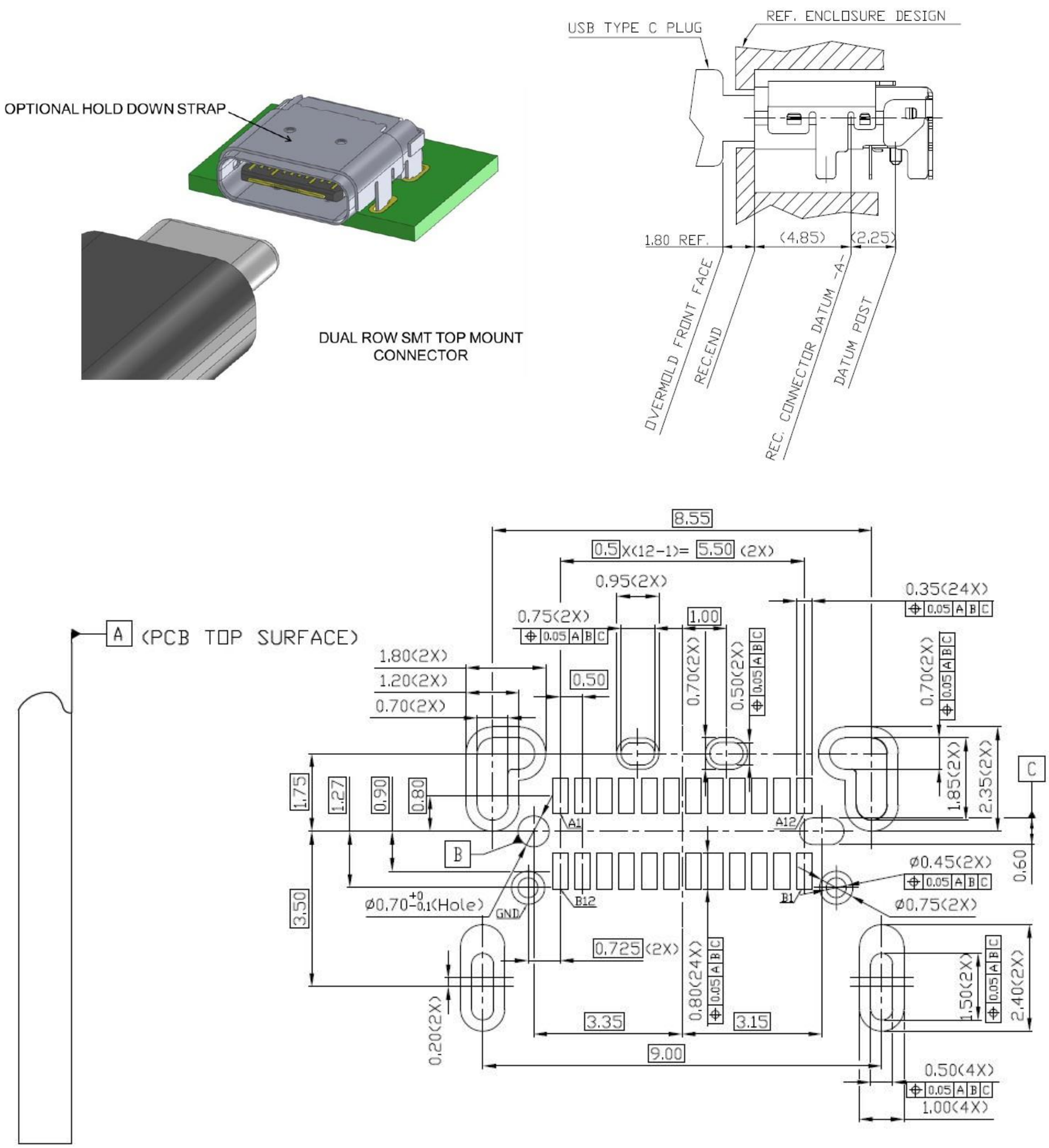


Figure 3-6 Reference Footprint for a USB Type-C Hybrid Right-Angle Receptacle (Informative)

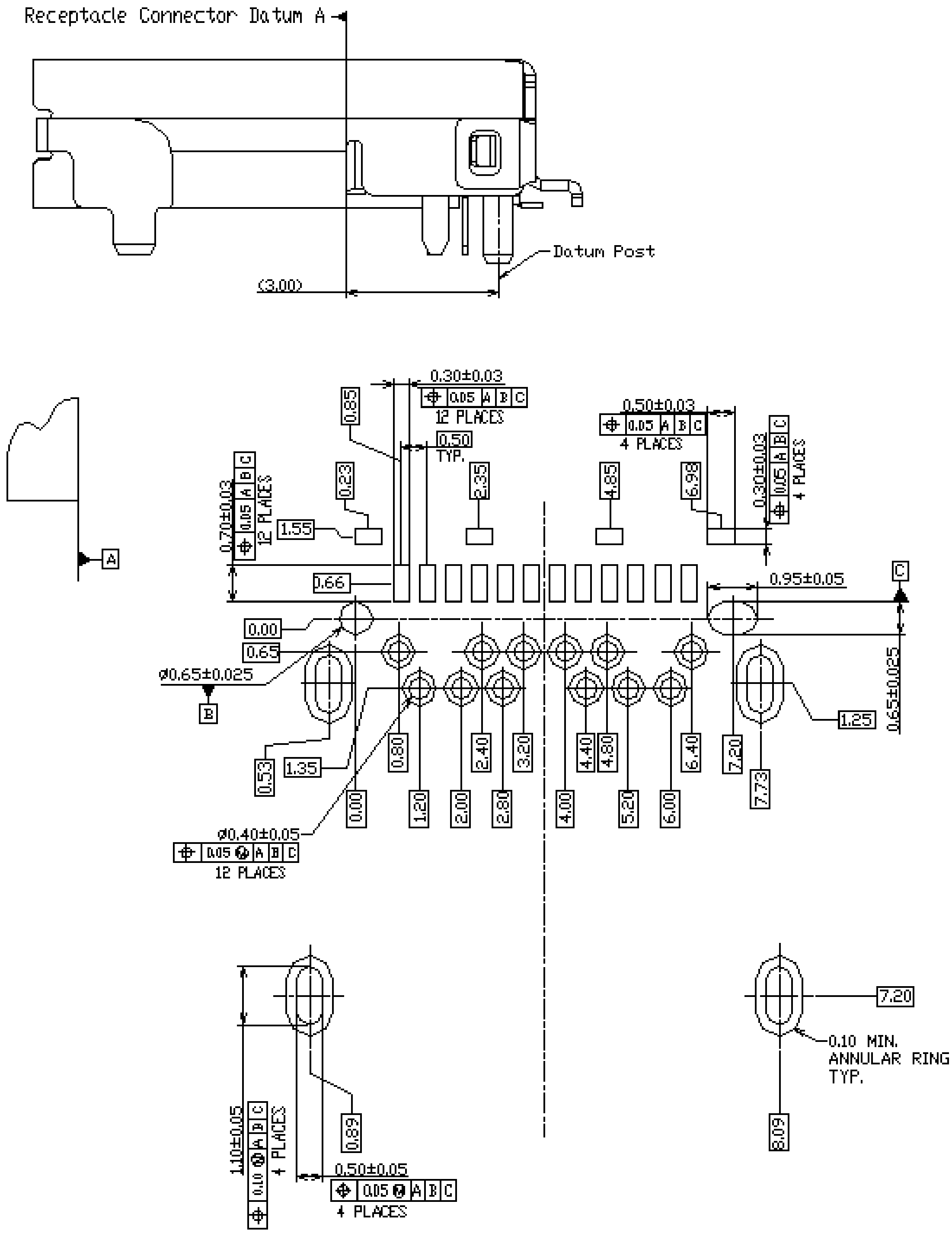
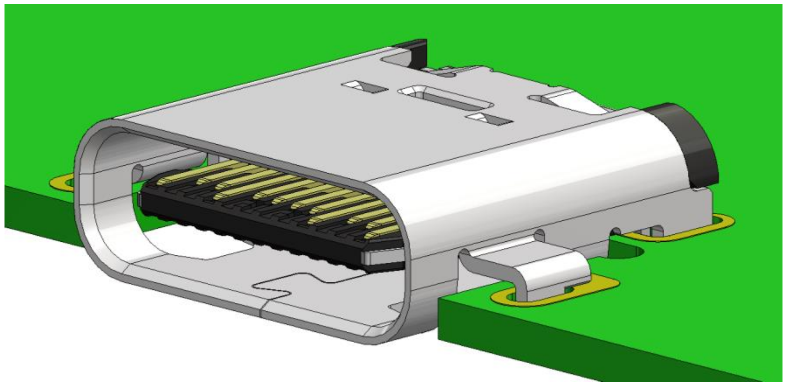


Figure 3-7 Reference Footprint for a USB Type-C Mid-Mount Dual-Row SMT Receptacle (Informative)



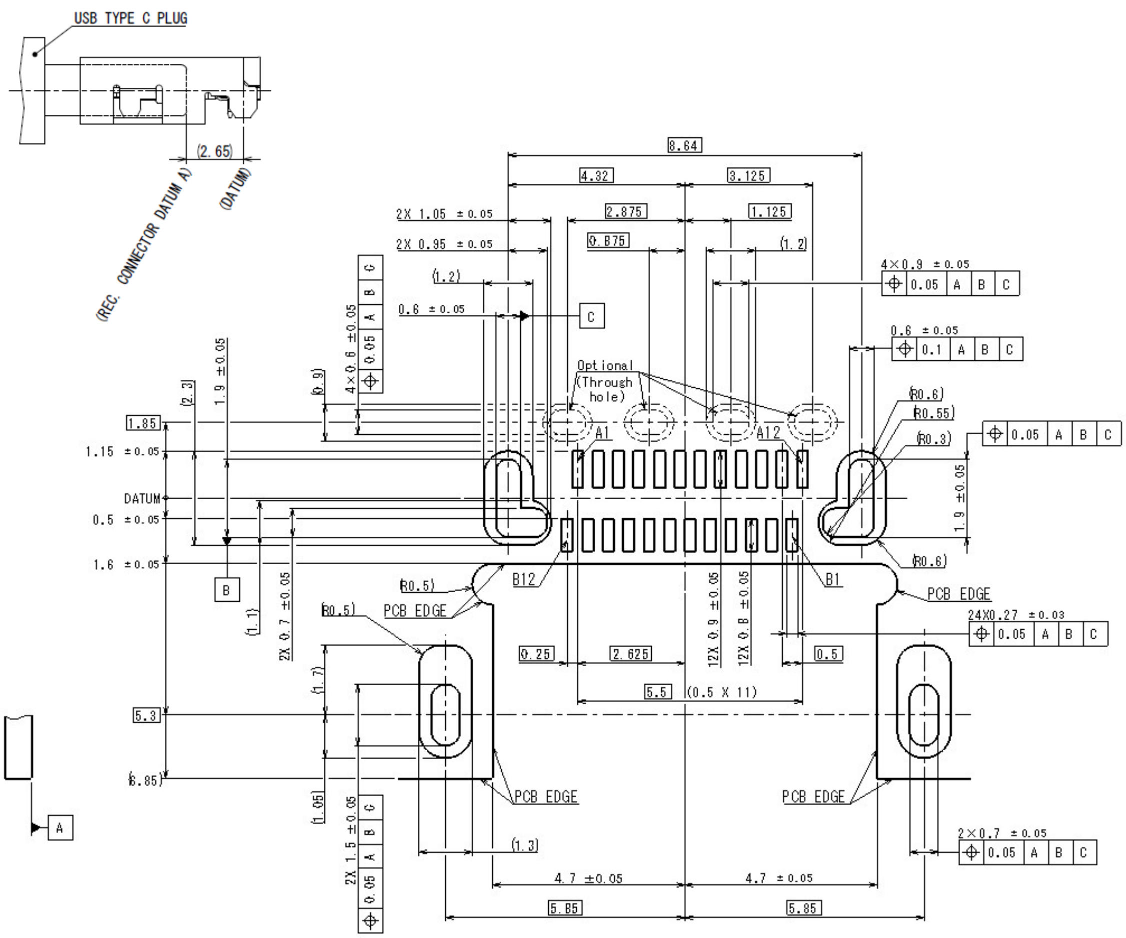


Figure 3-8 Reference Footprint for a USB Type-C Mid-Mount Hybrid Receptacle (Informative)

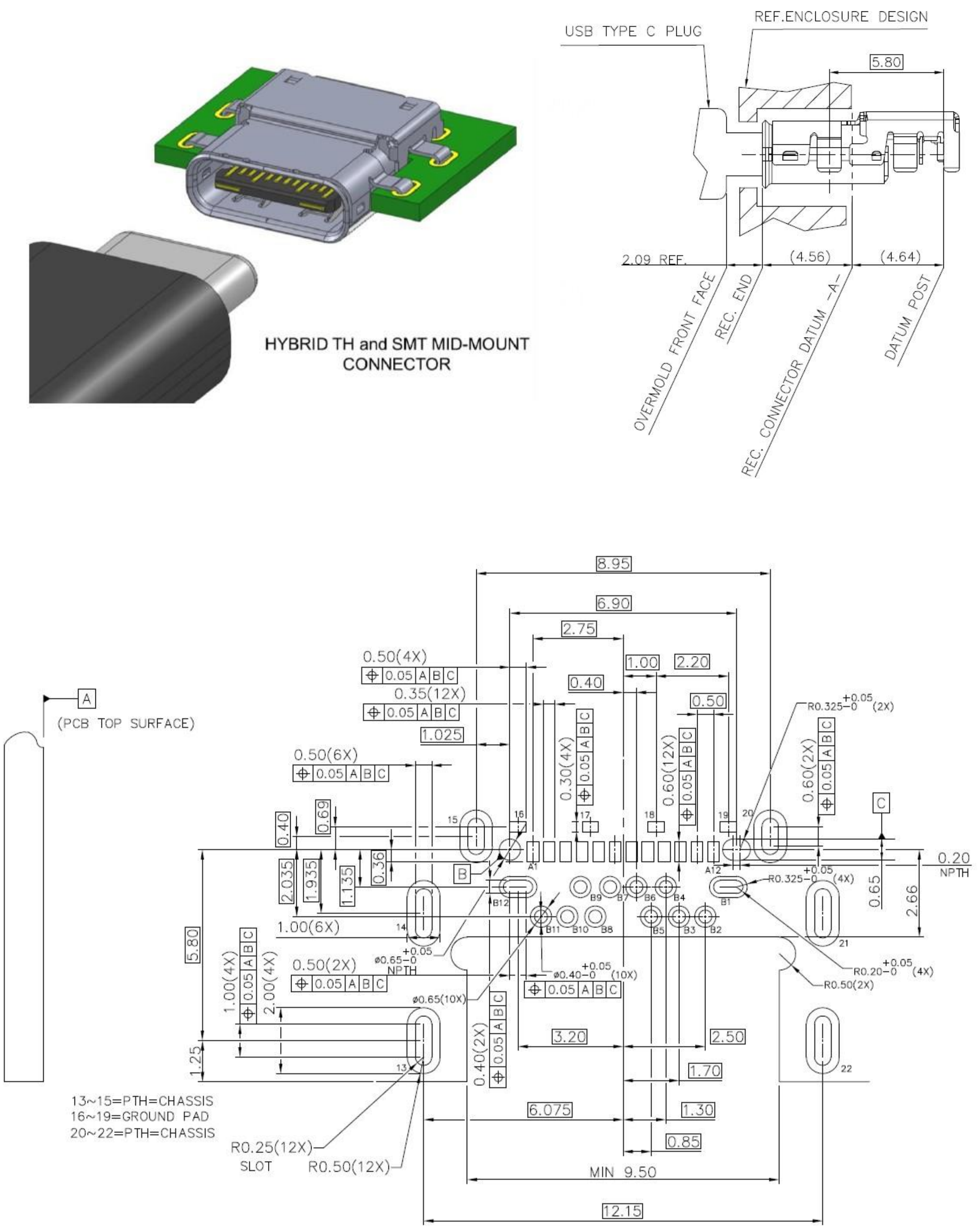


Figure 3-9 Reference Footprint for a USB 2.0 Type-C Through Hole Right Angle Receptacle (Informative)

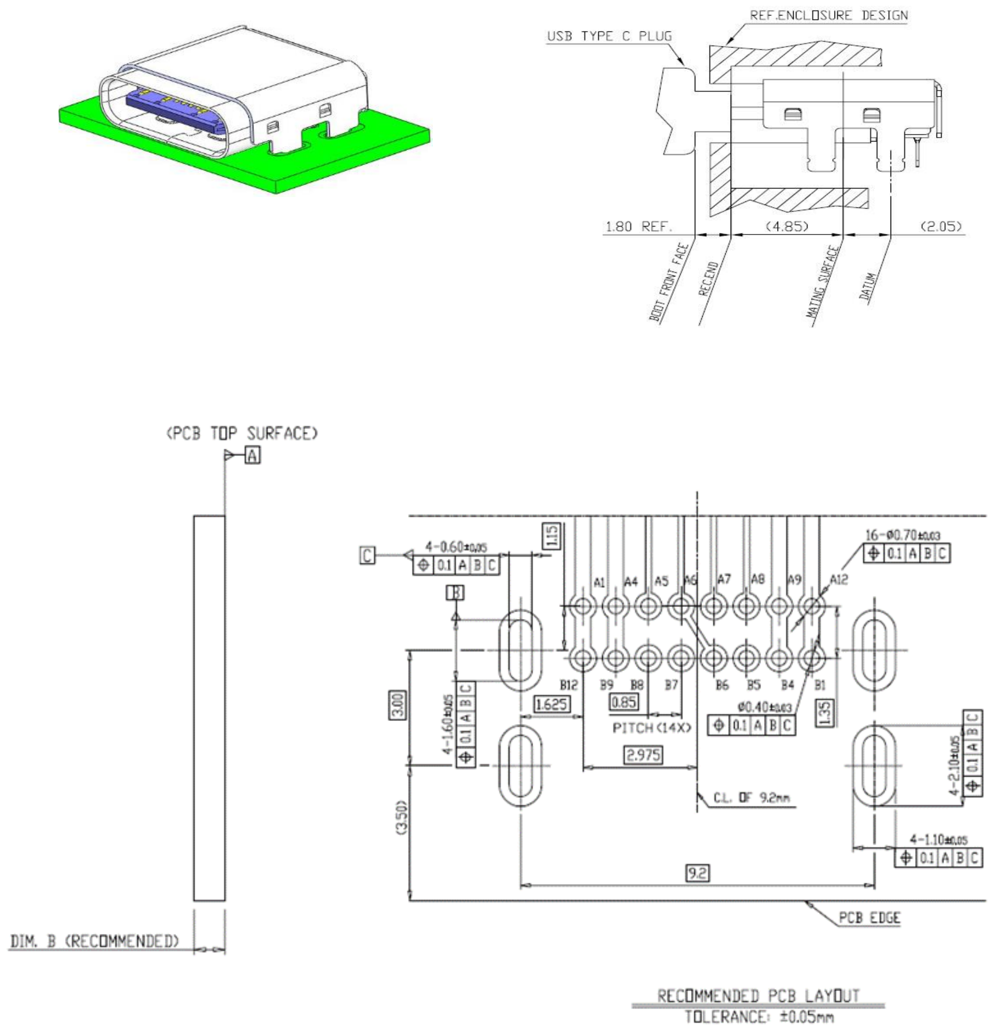
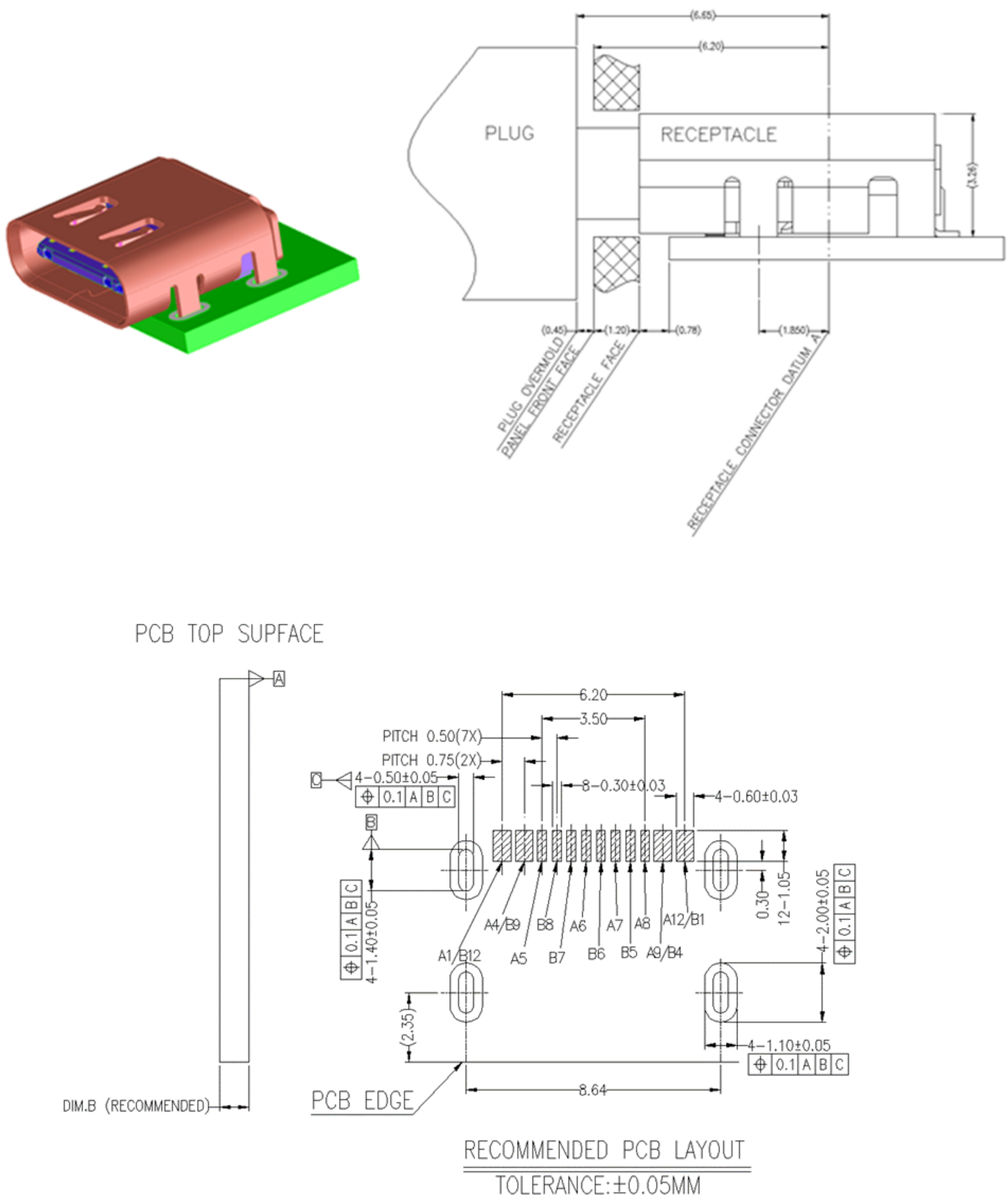


Figure 3-10 Reference Footprint for a USB 2.0 Type-C Single Row Right Angle Receptacle (Informative)



This specification requires that all contacts be present in the mating interface of the USB Full-Featured Type-C receptacle connector and all contacts except the *USB 3.2* or *USB4* signals (i.e., A2, A3, A10, A11, B2, B3, B10 and B11) be present in the mating interface of the *USB 2.0* Type-C receptacle connector, but allows the plug to include only the contacts required for *USB PD* and *USB 2.0* functionality for applications that only support *USB 2.0*. The *USB 2.0* Type-C plug is shown in Figure 3-11. The following design simplifications may be made when only *USB 2.0* is supported:

- Only the contacts necessary to support *USB PD* and *USB 2.0* are required in the plug. All other pin locations may be unpopulated. See Table 3-5. All contacts are required to be present in the mating interface of the USB Type-C receptacle connector.
- Unlike the USB Full-Featured Type-C plug, the internal EMC springs may be formed from the same strip as the signal, power, and ground contacts. The internal EMC springs contact the inner surface of the plug shell and mate with the receptacle EMC pads when the plug is seated in the receptacle. Alternately, the *USB 2.0* Type-C plug may use the same EMC spring configuration as defined for the USB Full-Featured Type-C plug. The *USB 2.0* Type-C plug four EMC spring locations are defined in Figure 3-11. The alternate configuration using the six spring locations is defined in Figure 3-1. Also refer to the reference designs in 3.2.2.3 for further clarification.
- A paddle card inside the plug may not be necessary if wires are directly attached to the contact pins.

Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions

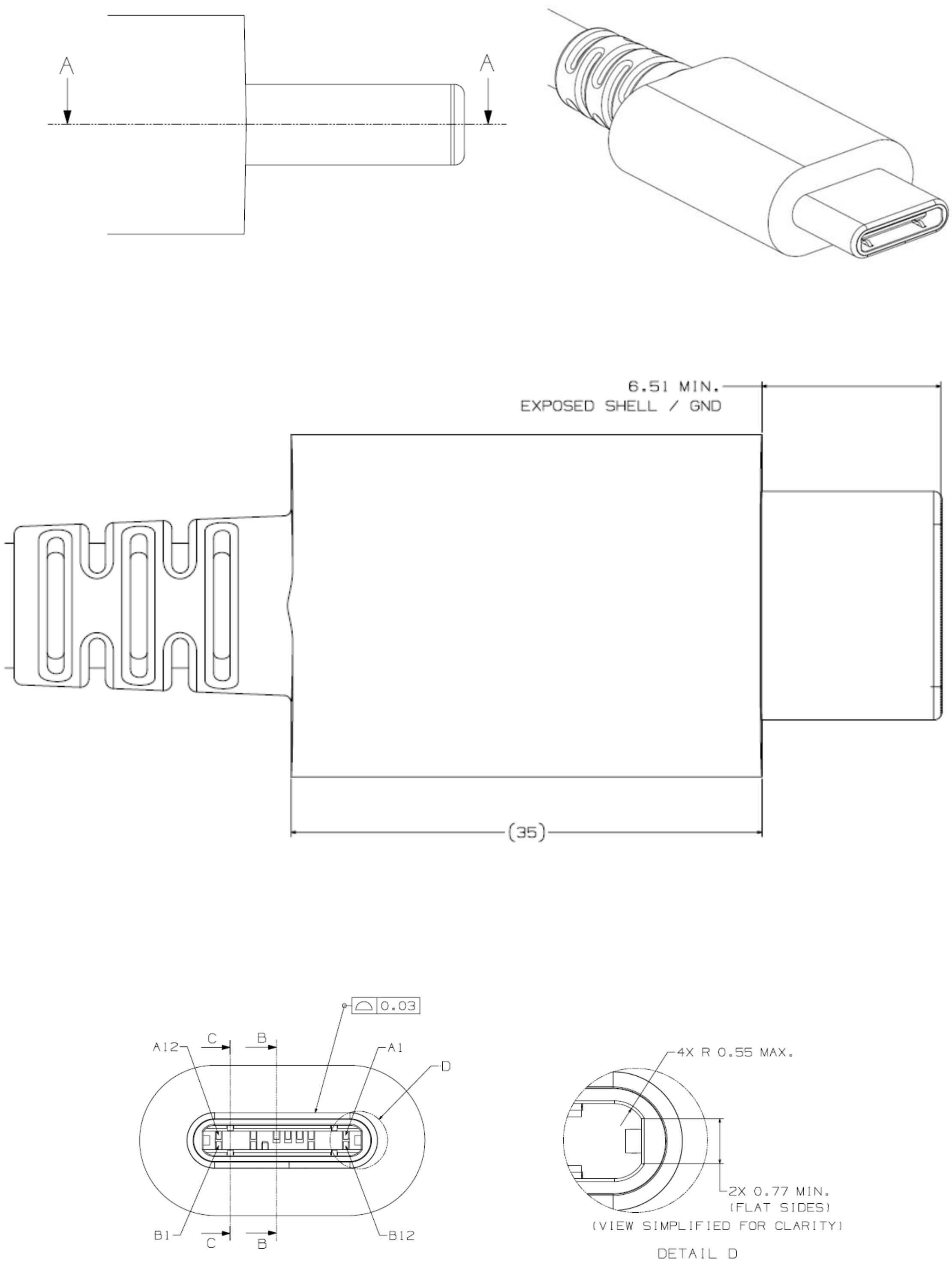
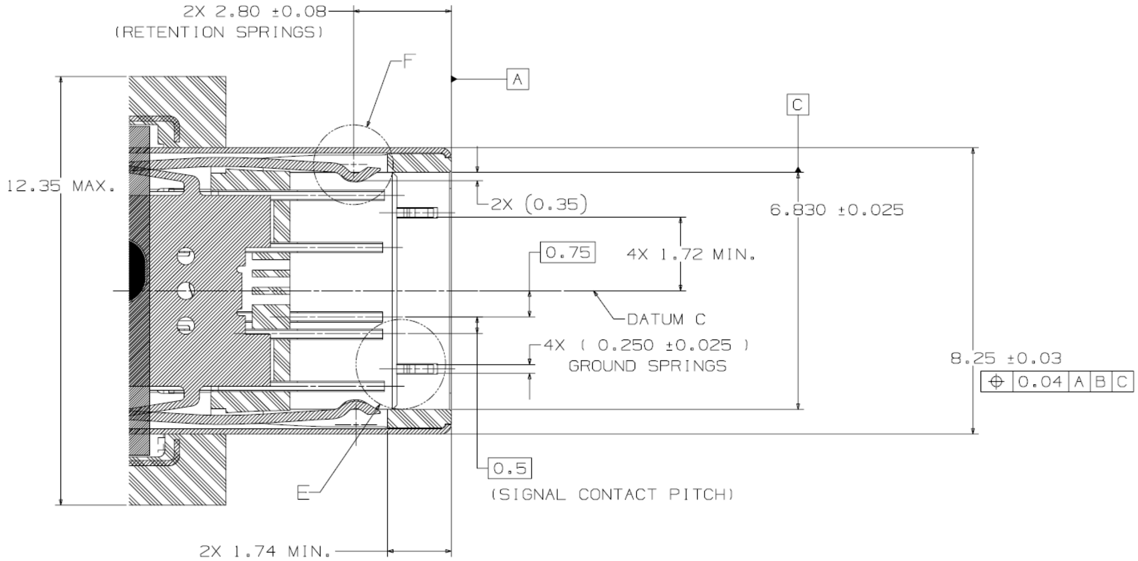
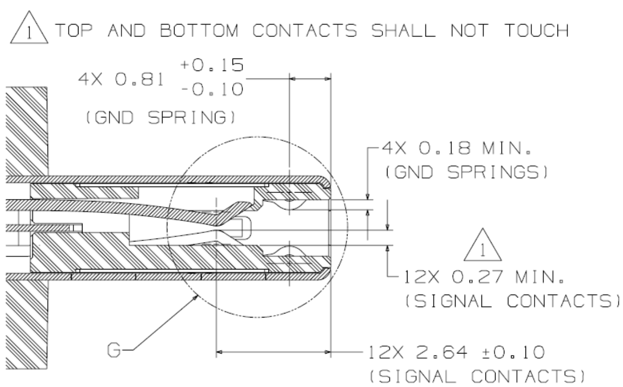


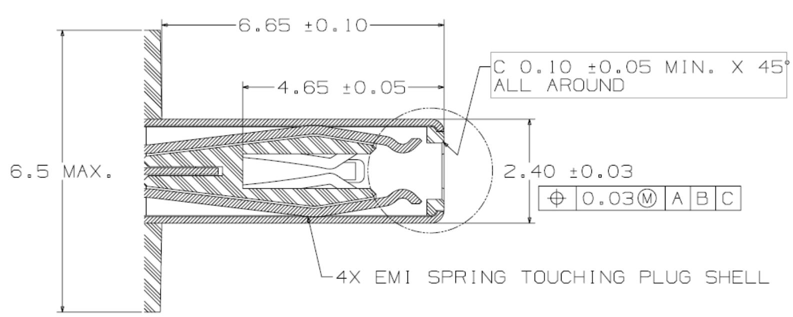
Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions, cont.



SECTION A-A

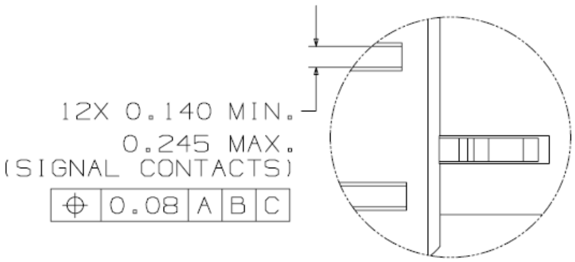


SECTION B-B

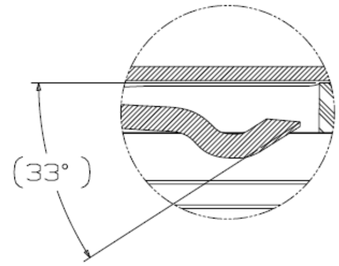


SECTION C-C

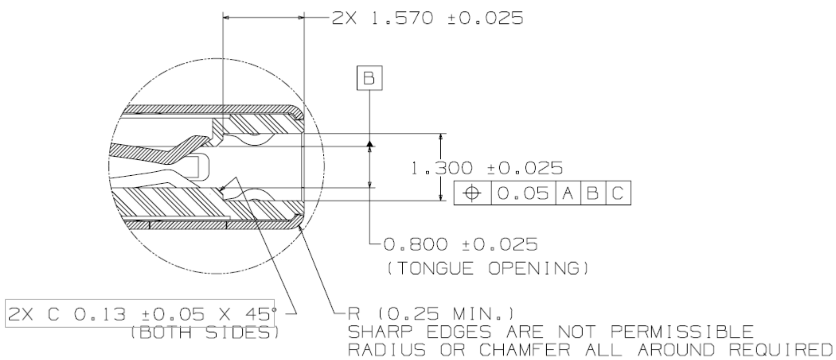
Figure 3-11 *USB 2.0* Type-C Plug Interface Dimensions, cont.



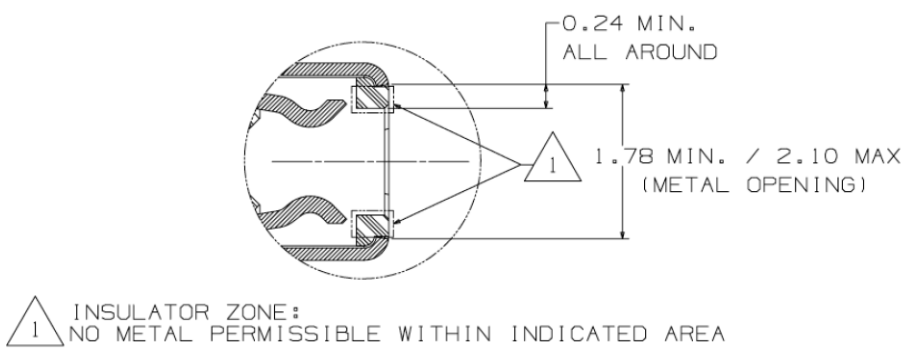
DETAIL E



DETAIL F

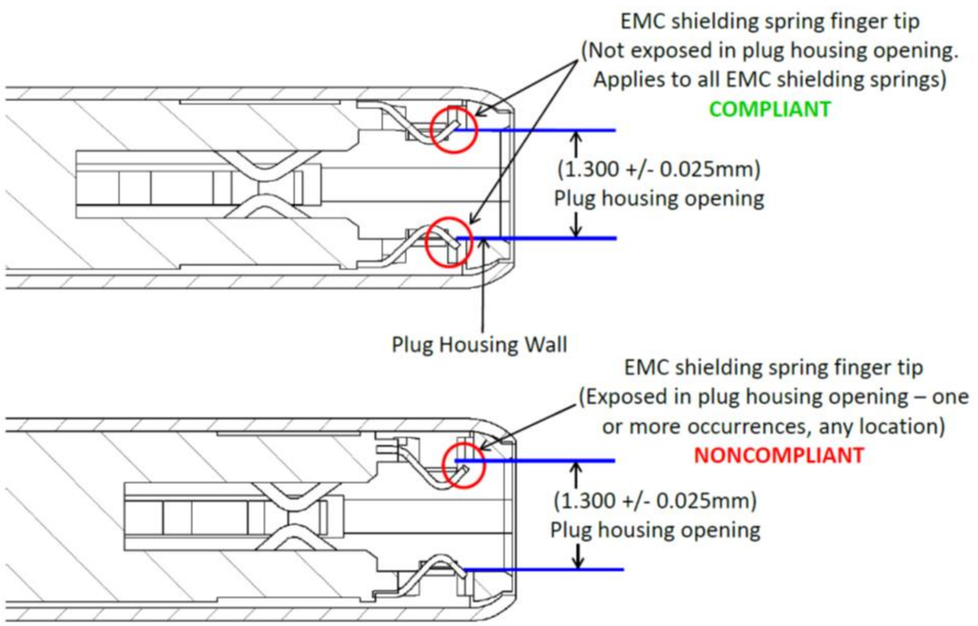


DETAIL G



DETAIL H

Figure 3-12 USB Type-C Plug EMC Shielding Spring Tip Requirements



3.2.2 Reference Designs

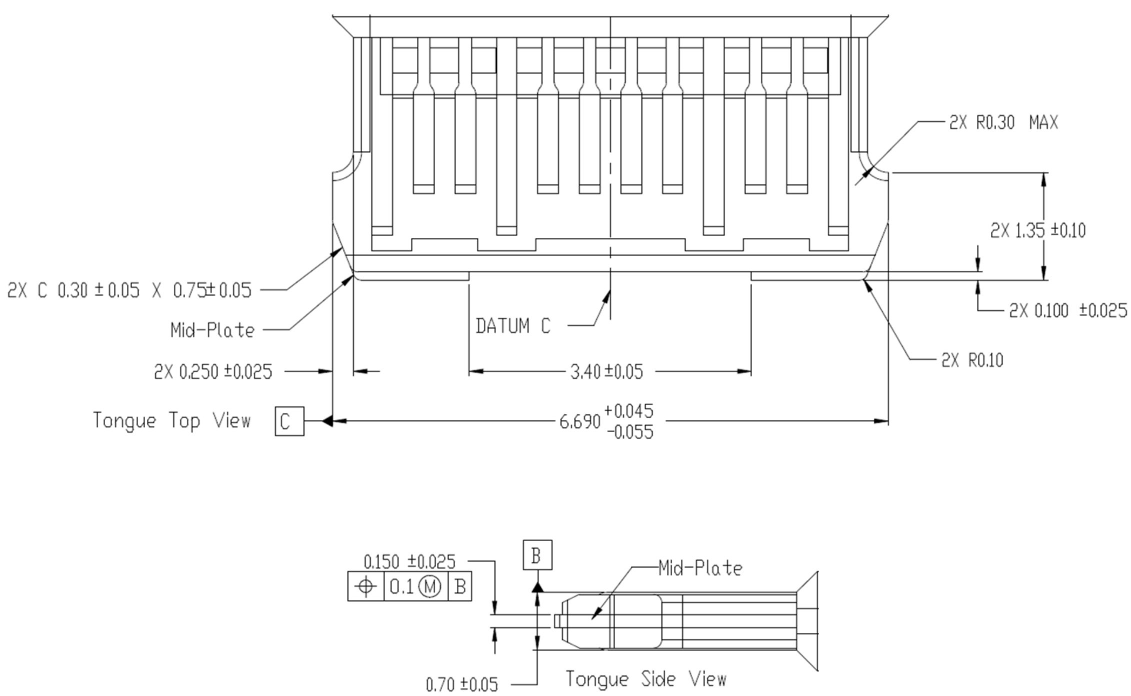
This section provides reference designs for a few key features of the USB Type-C connector. The reference designs are provided as acceptable design examples. They are not normative.

3.2.2.1 Receptacle Mid-Plate (Informative)

The signals between the top and bottom of the receptacle tongue are isolated by a mid-plate inside the tongue. Figure 3-13 shows a reference design of the mid-plate. It is important to pay attention to the following features of the middle plate:

- The distance between the signal contacts and the mid-plate should be accurately controlled since the variation of this distance may significantly impact impedance of the connector.
- The mid-plate in this particular design protrudes slightly beyond the front surface of the tongue. This is to protect the tongue front surface from damage caused by miss-insertion of small objects into the receptacle.
- The mid-plate is required to be directly connected to the PCB ground with at least two grounding points.
- The sides of the mid-plate mate with the plug side latches, making ground connections to reduce EMC. Proper surface finishes are necessary in the areas where the side latches and mid-plate connections occur.

Figure 3-13 Reference Design of Receptacle Mid-Plate



3.2.2.2 Side Latch (informative)

The side latches (retention latches) are located in the plug. Figure 3-14 shows a reference design of a blanked side latch. The plug side latches should contact the receptacle mid-plate to provide an additional ground return path.

Figure 3-14 Reference Design of the Retention Latch

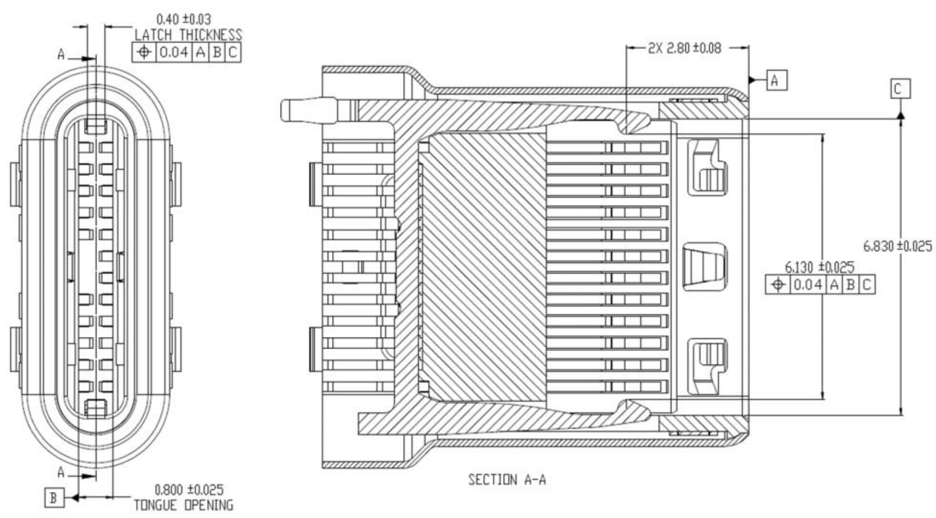
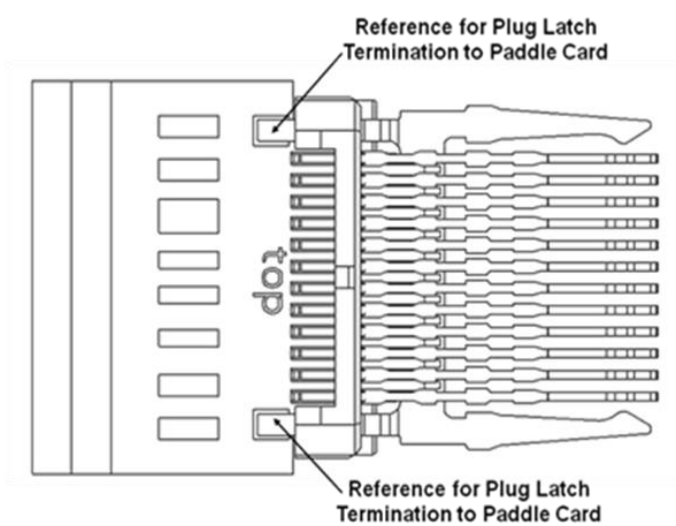


Figure 3-15 Illustration of the Latch Soldered to the Paddle Card Ground



3.2.2.3 Internal EMC Springs and Pads (Informative)

Figure 3-16 is a reference design of the internal EMC spring located inside the USB Full-Featured Type-C plug. Figure 3-17 is a reference design of the internal EMC spring located inside the *USB 2.0* Type-C plug.

Figure 3-16 Reference Design of the USB Full-Featured Type-C Plug Internal EMC Spring

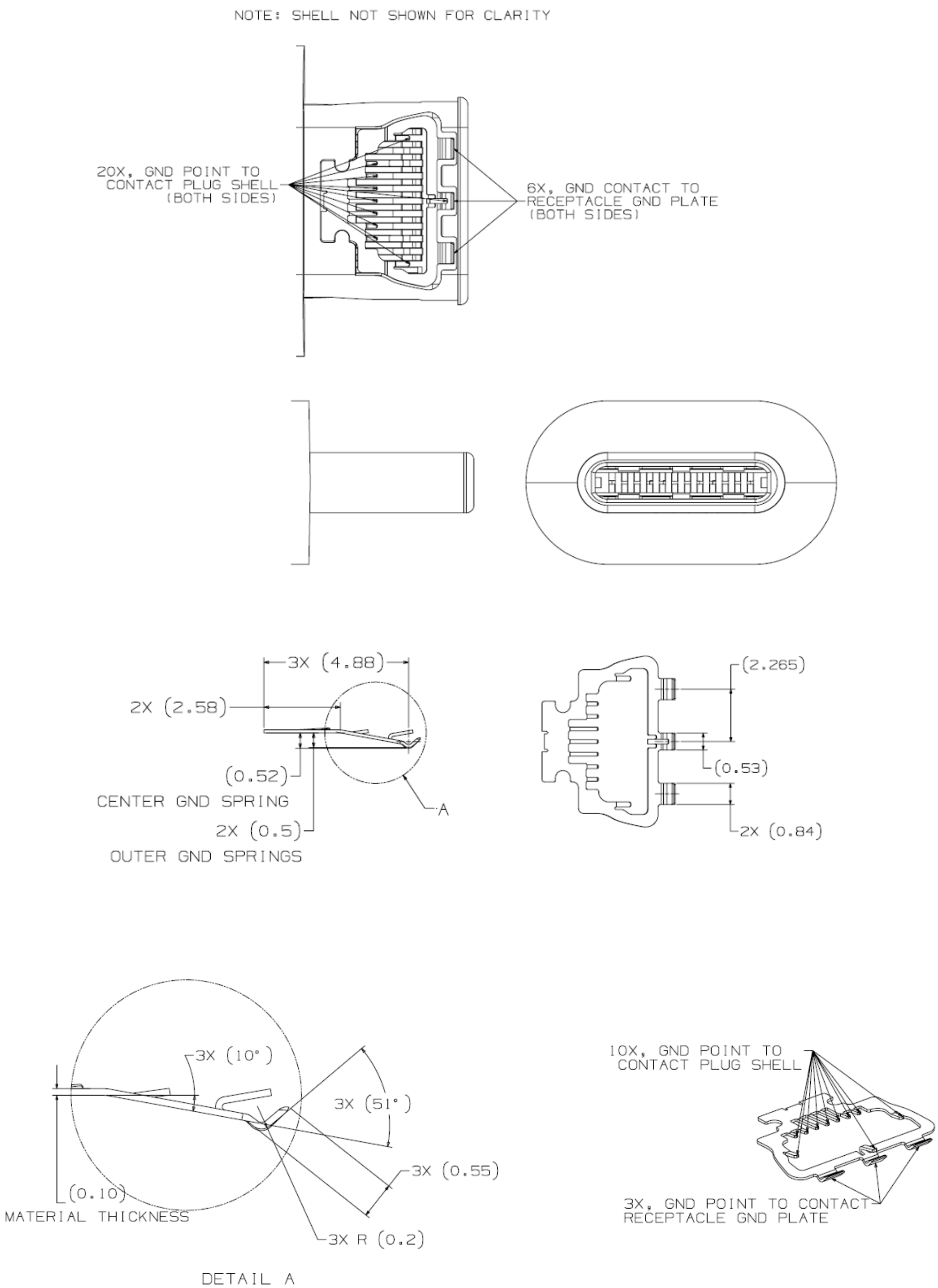
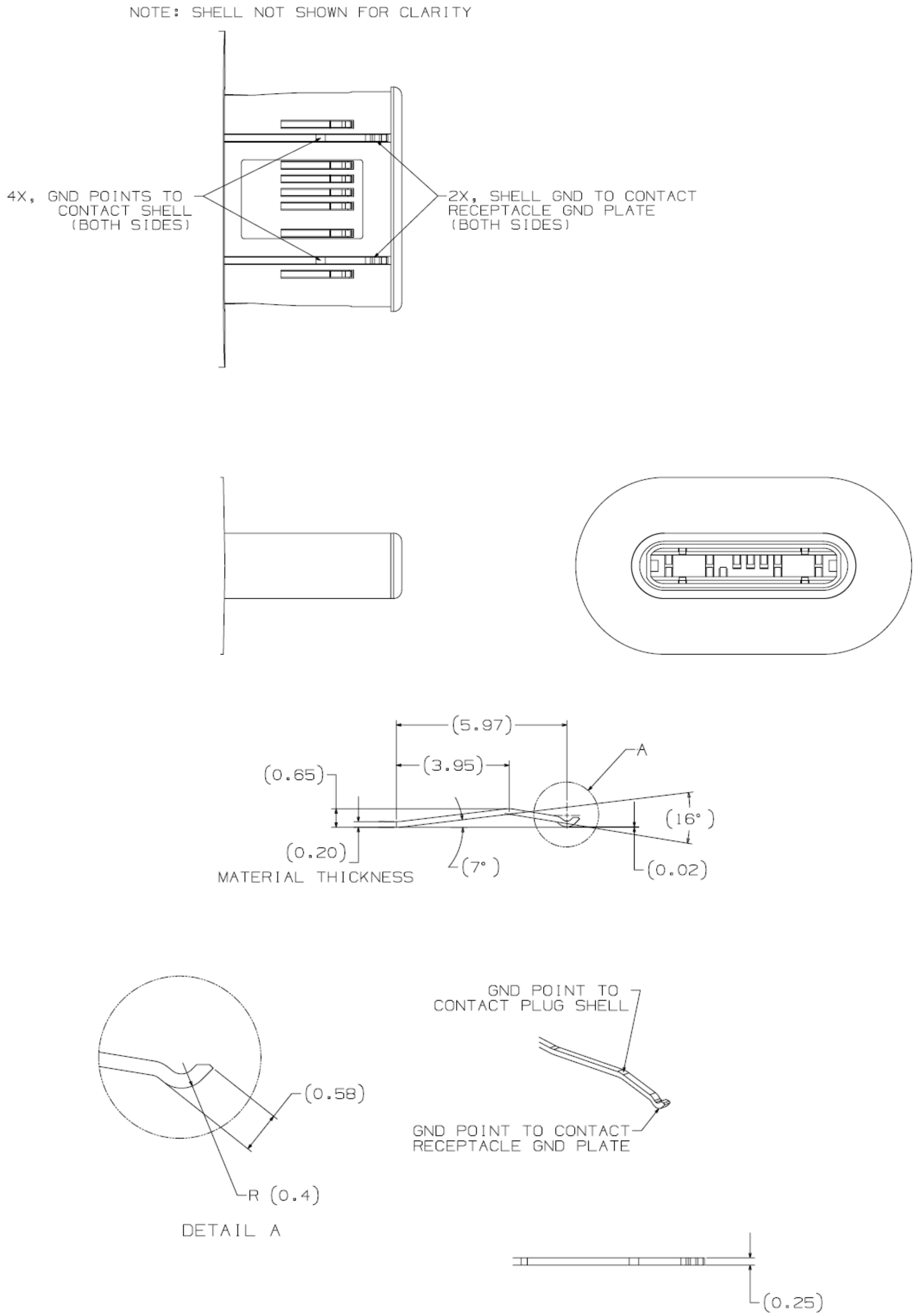


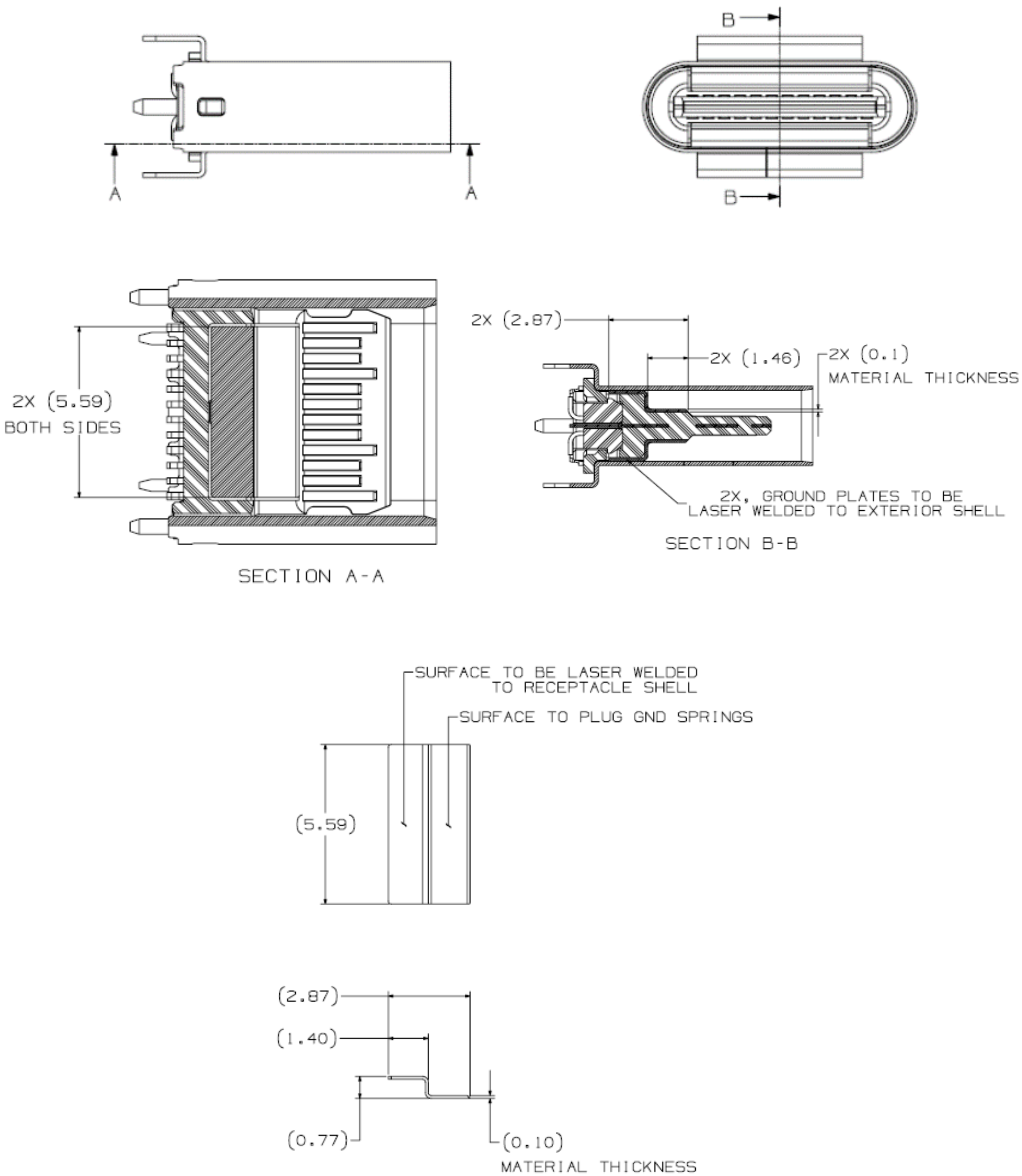
Figure 3-17 Reference Design of the *USB 2.0* Type-C Plug Internal EMC Spring



It is critical that the internal EMC spring contacts the plug shell as close to the EMC spring mating interface as possible to minimize the length of the return path.

The internal EMC pad (i.e., ground plate) shown in Figure 3-18 is inside the receptacle. It mates with the EMC spring in the plug. To provide an effective ground return, the EMC pads should have multiple connections with the receptacle shell.

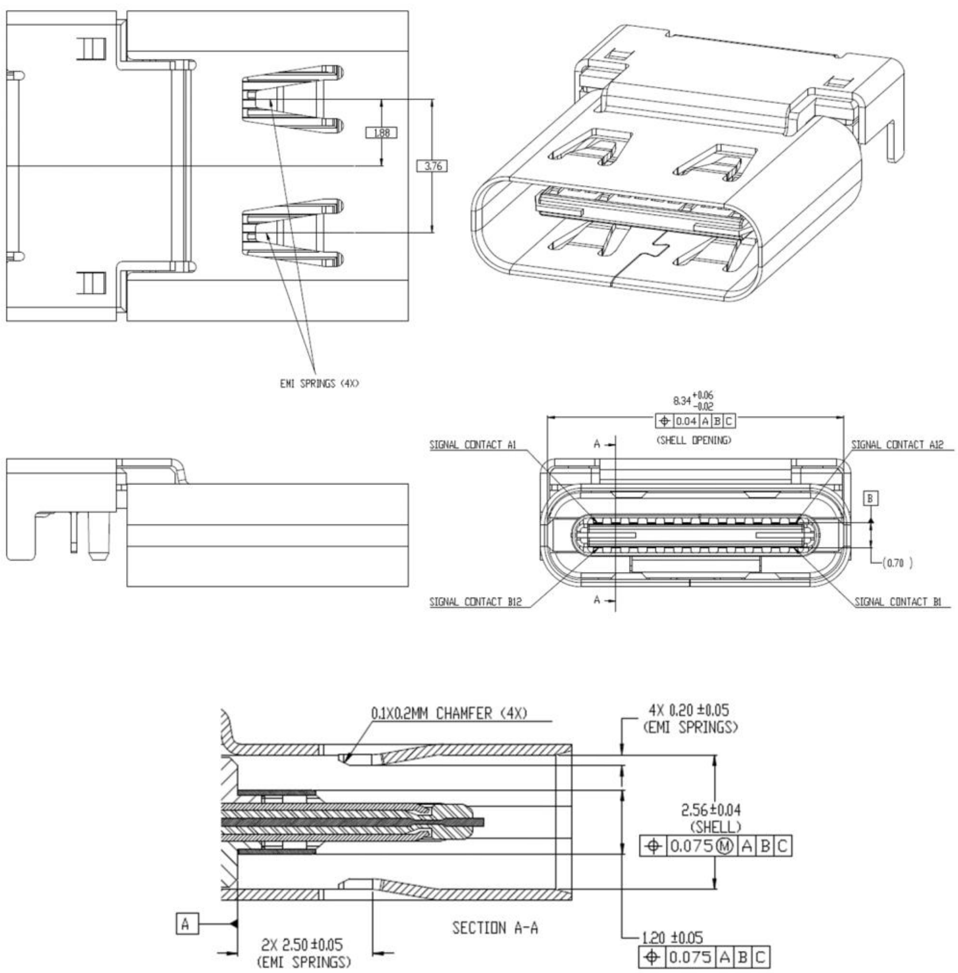
Figure 3-18 Reference Design of Internal EMC Pad



3.2.2.4 Optional External Receptacle EMC Springs (Informative)

Some applications may use receptacles with EMC springs that contact the outside of the plug shell. Figure 3-19 shows a reference receptacle design with external EMC springs. The EMC spring contact landing zones for the fully mated condition are normative and defined in Section 3.2.1.

Figure 3-19 Reference Design of a USB Type-C Receptacle with External EMC Springs

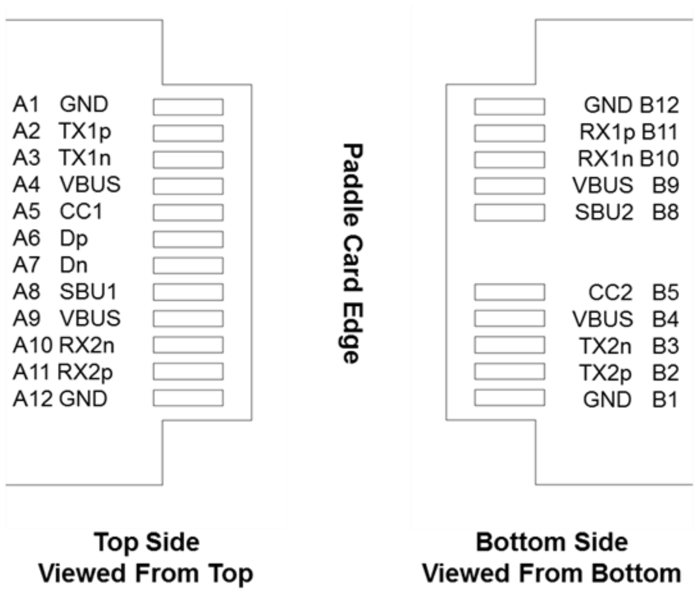


3.2.2.5 USB Full-Featured Type-C Plug Paddle Card (Informative)

The use of a paddle card is expected in the USB Full-Featured Type-C Plug. Figure 3-20 illustrates the paddle card pin assignment and contact spring connection location for a USB Full-Featured Type-C plug. The following guidelines are provided for the paddle card design:

- The paddle card should use high performance substrate material. The recommended paddle card thickness should have a tolerance less than or equal to ± 10%.
- The SuperSpeed USB traces should be as short as possible and have a nominal differential characteristic impedance of 85 Ω.
- The wire attach should have two high speed differential pairs on one side and two other high-speed differential pairs on the other side, separated as far as practically allowed.
- It is recommended that a grounded coplanar waveguide (CPWG) system be selected as a transmission line method.
- Use of vias should be minimized.
- VBUS pins should be bussed together on the paddle card.
- GND pins should be bussed together on the paddle card.

Figure 3-20 Reference Design for a USB Full-Featured Type-C Plug Paddle Card



3.2.3 Pin Assignments and Descriptions

The usage and assignments of the 24 pins for the USB Type-C receptacle interface are defined in Table 3-4.

Table 3-4 USB Type-C Receptacle Interface Pin Assignments

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2	TXp1	Positive half of first TX differential pair	Second	B11	RXp1	Positive half of first RX differential pair	Second
A3	TXn1	Negative half of first TX differential pair	Second	B10	RXn1	Negative half of first RX differential pair	Second
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10	RXn2	Negative half of second RX differential pair	Second	B3	TXn2	Negative half of second TX differential pair	Second
A11	RXp2	Positive half of second RX differential pair	Second	B2	TXp2	Positive half of second TX differential pair	Second
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the *USB 2.0* differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3.5 mm.
2. All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
3. All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
4. If the contact dimensions shown in Figure 3-1 ALTERNATE SECTION A-A are used, then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A2, A3, A5, A6, A7, A8, A10, A11, B2, B3, B5, B6, B7, B8, B10 and B11) mate third.

The usage and assignments of the signals necessary for the support of only *USB 2.0* with the USB Type-C mating interface are defined in Table 3-5.

Table 3-5 USB Type-C Receptacle Interface Pin Assignments for USB 2.0-only Support

Pin	Signal Name	Description	Mating Sequence	Pin	Signal Name	Description	Mating Sequence
A1	GND	Ground return	First	B12	GND	Ground return	First
A2				B11			
A3				B10			
A4	VBUS	Bus Power	First	B9	VBUS	Bus Power	First
A5	CC1	Configuration Channel	Second	B8	SBU2	Sideband Use (SBU)	Second
A6	Dp1	Positive half of the *USB 2.0* differential pair – Position 1	Second	B7	Dn2	Negative half of the *USB 2.0* differential pair – Position 2	Second
A7	Dn1	Negative half of the *USB 2.0* differential pair – Position 1	Second	B6	Dp2	Positive half of the *USB 2.0* differential pair – Position 2	Second
A8	SBU1	Sideband Use (SBU)	Second	B5	CC2	Configuration Channel	Second
A9	VBUS	Bus Power	First	B4	VBUS	Bus Power	First
A10				B3			
A11				B2			
A12	GND	Ground return	First	B1	GND	Ground return	First

Notes:

1. Unused contact locations shall be electrically isolated from power, ground or signaling (i.e., not connected).
2. Contacts B6 and B7 should not be present in the USB Type-C plug. The receptacle side shall support the *USB 2.0* differential pair present on Dp1/Dn1 or Dp2/Dn2. The plug orientation determines which pair is active. In one implementation, Dp1 and Dp2 may be shorted on the host/device as close to the receptacle as possible to minimize stub length; Dn1 and Dn2 may also be shorted. The maximum shorting trace length should not exceed 3.5 mm.
3. Contacts A8 and B8 (SBU1 and SBU2) shall be not connected unless required for a specified purpose (e.g., Audio Adapter Accessory Mode).
4. All VBUS pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all VBUS pins bussed together on the PCB).
5. All Ground return pins shall be connected together within the USB Type-C plug and shall be connected together at the USB Type-C receptacle connector when the receptacle is in its mounted condition (e.g., all ground return pins bussed together on the PCB).
6. If the contact dimensions shown in Figure 3-1 ALTERNATE SECTION A-A are used then the VBUS contacts (A4, A9, B4 and B9) mate second, and signal contacts (A5, A6, A7, A8, B5, B6, B7 and B8) mate third.

3.3 Cable Construction and Wire Assignments

This section discusses the USB Type-C cables, including cable construction, wire assignments, and wire gauges.

3.3.1 Cable Construction (Informative)

Figure 3-21 illustrates an example of USB Full-Featured Type-C cable cross-section, using micro-coaxial wires for TX/RX pairs. There are four groups of wires: USB D+/D– (typically unshielded twisted pairs (UTP)), TX/RX signal pairs (coaxial wires, twin-axial or shielded twisted pairs), sideband signal wires, and power and ground wires. In this example, the optional VCONN wire is shown whereas in Figure 3-22 the example is shown with the VCONN wire removed – the inclusion of VCONN or not relates to the implementation approach chosen for Electronically Marked Cables (See Section 4.9).

Figure 3-21 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example with VCONN

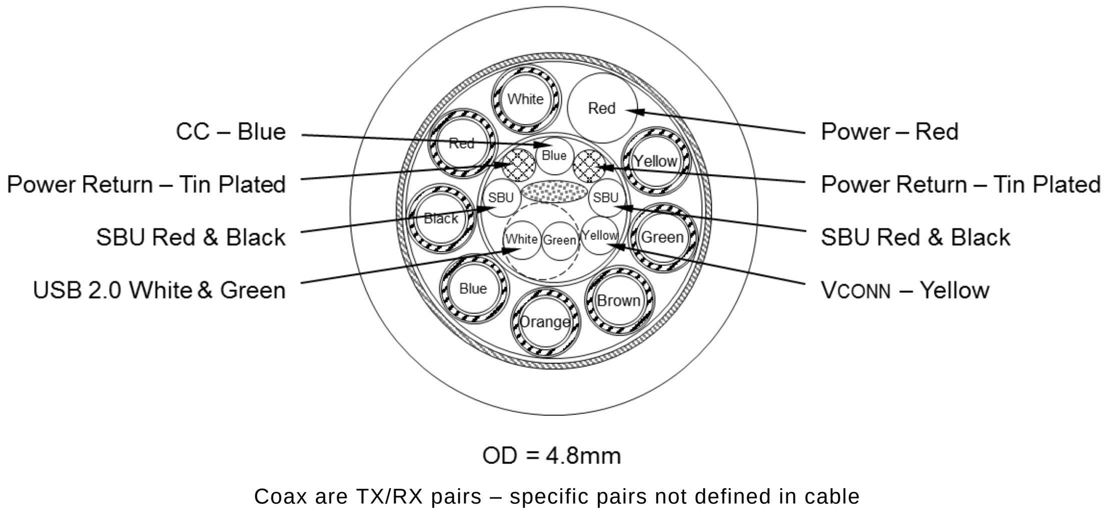
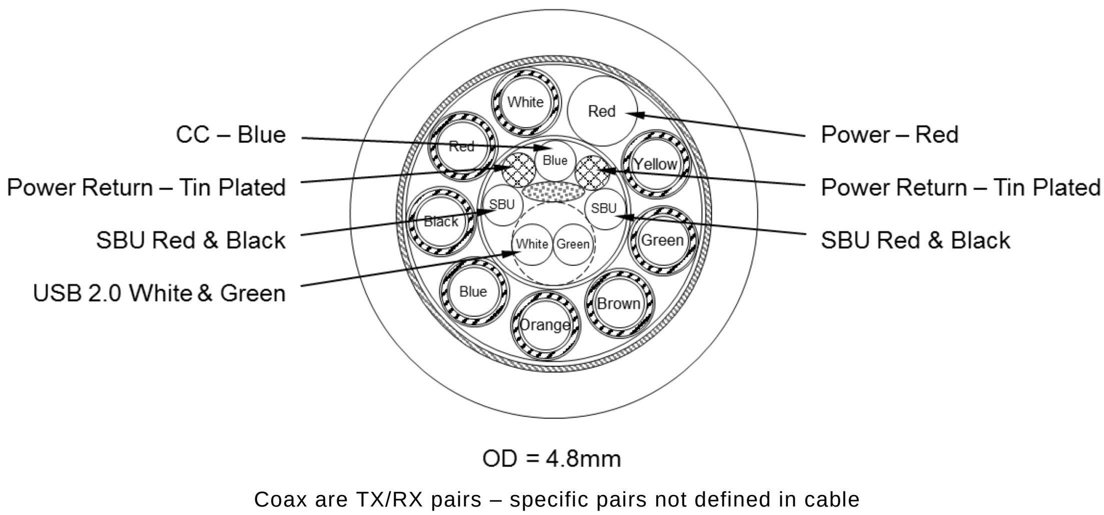


Figure 3-22 Illustration of a USB Full-Featured Type-C Cable Cross Section, a Coaxial Wire Example without VCONN



The USB D+/D− signal pair is intended to transmit the *USB 2.0* Low-Speed, Full-Speed and High-Speed signaling while the TX/RX signal pairs are used for either *USB 3.2* or *USB4* signaling. Shielding is needed for the TX/RX differential pairs for signal integrity and EMC performance.

3.3.2 Wire Assignments

Table 3-6 defines the full set of possible wires needed to produce all standard USB Type-C cables assemblies. For some cable assemblies, not all of these wires are used. For example, a USB Type-C cable that only provides *USB 2.0* functionality will not include wires 6–15.

Table 3-6 USB Type-C Standard Cable Wire Assignments

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	CC	Configuration Channel
4	UTP_Dp	Unshielded twist pair, positive
5	UTP_Dn	Unshielded twist pair, negative
6	SDPp1	Shielded differential pair #1, positive
7	SDPn1	Shielded differential pair #1, negative
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDPp3	Shielded differential pair #3, positive
11	SDPn3	Shielded differential pair #3, negative
12	SDPp4	Shielded differential pair #4, positive
13	SDPn4	Shielded differential pair #4, negative
14	SBU_A	Sideband Use
15	SBU_B	Sideband Use
16	GND_PWRrt2	Ground for power return (optional)
17	PWR_VBUS2	VBUS power (optional)
18	PWR_VCONN	VCONN power (optional, see Section 4.9)
Braid	Shield	Cable external braid

Note:

1. This table assumes that coaxial wire construction is used for all SDP's and there are no drain wires. The signal ground return is through the shields of the coaxial wires. If shielded twisted or twin-axial pairs are used, then drain wires are needed.

Table 3-7 defines the full set of possible wires needed to produce USB Type-C to legacy cable assemblies. For some cable assemblies, not all of these wires are needed. For example, a USB Type-C to USB 2.0 Standard-B cable will not include wires 5–10.

Table 3-7 USB Type-C Cable Wire Assignments for Legacy Cables/Adapters

Wire Number	Signal Name	Description
1	GND_PWRrt1	Ground for power return
2	PWR_VBUS1	VBUS power
3	UTP_Dp	Unshielded twist pair, positive
4	UTP_Dn	Unshielded twist pair, negative
5	SDPp1	Shielded differential pair #1, positive
6	SDPn1	Shielded differential pair #1, negative
7	SDP1_Drain	Drain wire for SDPp1 and SDPn1
8	SDPp2	Shielded differential pair #2, positive
9	SDPn2	Shielded differential pair #2, negative
10	SDP2_Drain	Drain wire for SDPp2 and SDPn2
Braid	Shield	Cable external braid

Note:

a. This table assumes that shielded twisted pair is used for all SDP’s and there are drain wires. If coaxial wire construction is used, then no drain wires are needed, and the signal ground return is through the shields of the coaxial wires.

3.3.3 Wire Gauges and Cable Diameters (Informative)

This specification does not specify wire gauge. Table 3-8 and Table 3-9 list typical wire gauges for reference purposes only. A large gauge wire incurs less loss, but at the cost of cable diameter and flexibility. Multiple wires may be used for a single wire such as for VBUS or Ground. It is recommended to use the smallest possible wire gauges that meet the cable assembly electrical and mechanical requirements.

To maximize cable flexibility, all wires should be stranded, and the cable outer diameter should be minimized as much as possible. A typical USB Full-Featured Type-C cable outer diameter may range from 4 mm to 6 mm while a typical USB 2.0 Type-C cable outer diameter may range from 2 mm to 4 mm. A typical USB Type-C to USB 3.1 legacy cable outer diameter may range from 3 mm to 5 mm.

Table 3-8 Reference Wire Gauges for standard USB Type-C Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	CC	32-34
4	UTP_Dp	28-34
5	UTP_Dn	28-34
6	SDPp1	26-34
7	SDPn1	26-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDPp3	26-34
11	SDPn3	26-34
12	SDPp4	26-34
13	SDPn4	26-34
14	SBU_A	32-34
15	SBU_B	32-34
16	GND_PWRrt2	20-28
17	PWR_VBUS2	20-28
18	PWR_VCONN	32-34

Table 3-9 Reference Wire Gauges for USB Type-C to Legacy Cable Assemblies

Wire Number	Signal Name	Wire Gauge (AWG)
1	GND_PWRrt1	20-28
2	PWR_VBUS1	20-28
3	UTP_Dp	28-34
4	UTP_Dn	28-34
5	SDPp1	26-34
6	SDPn1	26-34
7	SDP1_Drain	28-34
8	SDPp2	26-34
9	SDPn2	26-34
10	SDP2_Drain	28-34

3.4 Standard USB Type-C Cable Assemblies

Two standard USB Type-C cable assemblies are defined and allowed by this specification. In addition, captive cables are allowed (see Section 3.4.3). Shielding (braid) is required to enclose all the wires in the USB Type-C cable. The shield shall be terminated to the plug metal shells. The shield should be physically connected to the plug metal shell as close to 360° as possible, to control EMC.

Note: Up until Release 1.4 of this specification, the TX and RX signals used in this specification were named SSTX and SSRX. With the introduction of USB4, these signals were renamed such that they generically can apply to both SuperSpeed USB and USB4 signaling. It is intended that the TX and RX signal names are synonymous with the original SSTX and SSRX names for implementations prior to Release 2.0 of this specification.

3.4.1 USB Full-Featured Type-C Cable Assembly

Figure 3-23 shows a USB Full-Featured Type-C standard cable assembly.

Figure 3-23 USB Full-Featured Type-C Standard Cable Assembly

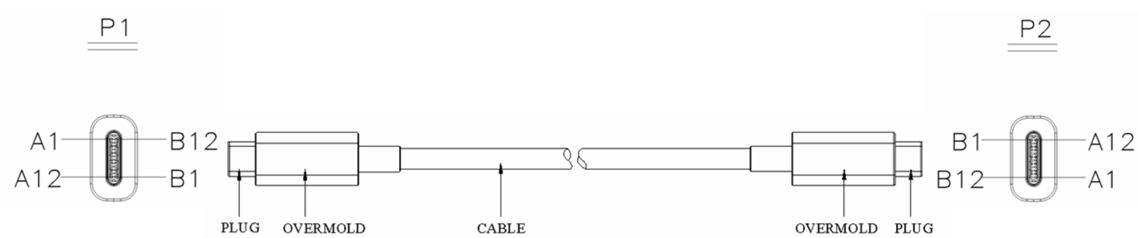


Table 3-10 defines the wire connections for the USB Full-Featured Type-C standard cable assembly.

Table 3-10 USB Full-Featured Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 [16]	GND_PWRrt1 [GND_PWRrt2]	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2 [17]	PWR_VBUS1 [PWR_VBUS2]	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
A2	TXp1	6	SDPp1	B11	RXp1
A3	TXn1	7	SDPn1	B10	RXn1
B11	RXp1	8	SDPp2	A2	TXp1
B10	RXn1	9	SDPn2	A3	TXn1
B2	TXp2	10	SDPp3	A11	RXp2
B3	TXn2	11	SDPn3	A10	RXn2
A11	RXp2	12	SDPp4	B2	TXp2
A10	RXn2	13	SDPn4	B3	TXn2
A8	SBU1	14	SBU_A	B8	SBU2
B8	SBU2	15	SBU_B	A8	SBU1
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. This table assumes that coaxial wire construction is used for all SDP's and there are no drain wires. The shields of the coaxial wires are connected to the ground pins. If shielded twisted pair is used, then drain wires are needed and shall be connected to the GND pins.
2. Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor (minimum recommended voltage rating of 30 V, 63 V if EPR-capable) is required for the VBUS pin in the full-featured cable at each end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad.
5. All GND pins shall be connected together within the USB Type-C plug
6. Shield and GND shall be connected within the USB Type-C plug on both ends of the cable assembly.

3.4.2 USB 2.0 Type-C Cable Assembly

A *USB 2.0* Type-C standard cable assembly has the same form factor shown in Figure 3-23.

Table 3-11 defines the wire connections for the *USB 2.0* Type-C standard cable assembly.

Table 3-11 *USB 2.0* Type-C Standard Cable Assembly Wiring

USB Type-C Plug #1		Wire		USB Type-C Plug #2	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	A1, B1, A12, B12	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	A4, B4, A9, B9	VBUS
A5	CC	3	CC	A5	CC
B5	VCONN	18	PWR_VCONN (See Section 4.9)	B5	VCONN
A6	Dp1	4	UTP_Dp	A6	Dp1
A7	Dn1	5	UTP_Dn	A7	Dn1
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin B5 (VCONN) of the USB Type-C plug shall be used in electronically marked versions of this cable. See Section 4.9.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is not required for the VBUS pin in the *USB 2.0* Type-C cable.
4. All GND pins shall be connected together within the USB Type-C plug.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).
6. Shield and GND grounds shall be connected within the USB Type-C plug on both ends of the cable assembly.

3.4.3 USB Type-C Captive Cable Assemblies

A captive cable assembly is a cable assembly that is terminated on one end with a USB Type-C plug and has a vendor-specific connect means (hardwired or custom detachable) on the opposite end. The cable assembly that is hardwired is not detachable from the device.

The assembly wiring for captive USB Type-C cables follow the same wiring assignments as the standard cable assemblies (see Table 3-10 and Table 3-11) with the exception that the hardwired attachment on the device side substitutes for the USB Type-C Plug #2 end.

The CC wire in a captive cable shall be terminated and behave as appropriate to the function of the product to which it is captive (e.g. host or device).

A device (Sink, UFP or DRP) with a captive cable assembly shall respond to SOP' cable identity inquiries when the device either sinks higher than 3A current or supports *USB4* operation. The physical location of the eMarker can be either within the captive cable or the device with the cable.

This specification does not define how the hardwired attachment is physically done on the device side.

3.4.4 USB Type-C Thumb Drive Assemblies

A thumb drive assembly is an assembly that incorporates a USB Type-C plug as its primary USB interface. This assembly does not functionally include a cable assembly.

A thumb drive device (Sink, UFP or DRP) shall respond to SOP' cable identity inquiries when it either sinks higher than 3A current or supports *USB4* operation.

3.5 Legacy Cable Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy cable assemblies are defined. Only the cables defined within this specification are allowed.

Legacy cable assemblies that source power to a USB Type-C connector (e.g. a USB Type-C to USB Standard-A plug cable assembly and a USB Type-C plug to USB Micro-B receptacle adapter assembly) are required to use the Default USB Type-C Current Rp resistor (56 kΩ). The value of Rp is used to inform the Sink how much current the Source can provide. Since the legacy cable assembly does not comprehend the capability of the Source it is connected to, it is only allowed to advertise Default USB Type-C Current as defined by the *USB 2.0*, *USB 3.1* and *USB BC 1.2* specifications. No other Rp values are permitted because these may cause a USB Type-C Sink to overload a legacy power supply.

3.5.1 USB Type-C to *USB 3.1* Standard-A Cable Assembly

Figure 3-24 shows a USB Type-C to *USB 3.1* Standard-A cable assembly.

Figure 3-24 USB Type-C to USB 3.1 Standard-A Cable Assembly

Table 3-12 defines the wire connections for the USB Type-C to *USB 3.1* Standard-A cable assembly.

Table 3-12 USB Type-C to USB 3.1 Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Standard-A plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 2			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
A2	TXp1	5	SDPp1	6	StdA_SSRX+
A3	TXn1	6	SDPn1	5	StdA_SSRX−
B11	RXp1	8	SDPp2	9	StdA_SSTX+
B10	RXn1	9	SDPn2	8	StdA_SSTX−
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
2. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-24 for the functional description and value of Rp.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Standard-A plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. Shield and GND grounds shall be connected within the USB Type-C and USB 3.1 Standard-A plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.2 USB Type-C to *USB 2.0* Standard-A Cable Assembly

Figure 3-25 shows a USB Type-C to *USB 2.0* Standard-A cable assembly.

Figure 3-25 USB Type-C to *USB 2.0* Standard-A Cable Assembly

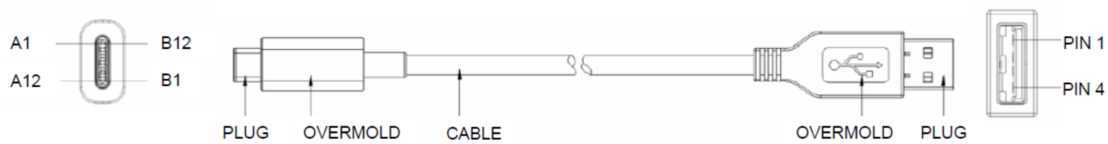


Table 3-13 defines the wire connections for the USB Type-C to *USB 2.0* Standard-A cable assembly.

Table 3-13 USB Type-C to *USB 2.0* Standard-A Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-A plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-24 for the functional description and value of Rp.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Shield and GND grounds shall be connected within the USB Type-C and *USB 2.0* Standard-A plugs on both ends of the cable assembly.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.3 USB Type-C to USB 3.1 Standard-B Cable Assembly

Figure 3-26 shows a USB Type-C to USB 3.1 Standard-B cable assembly.

Figure 3-26 USB Type-C to USB 3.1 Standard-B Cable Assembly

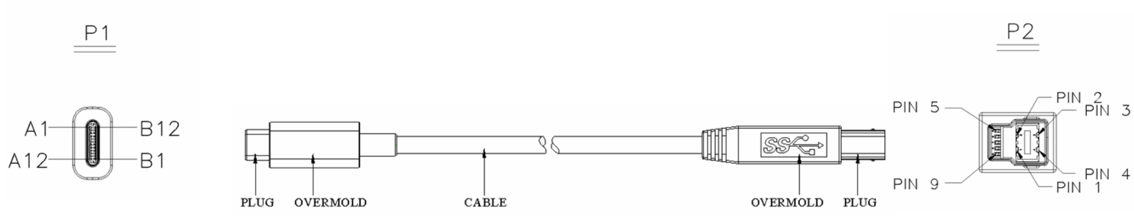


Table 3-14 defines the wire connections for the USB Type-C to USB 3.1 Standard-B cable assembly.

Table 3-14 USB Type-C to USB 3.1 Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Standard-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
A2	TXp1	5	SDPp1	9	StdB_SSRX+
A3	TXn1	6	SDPn1	8	StdB_SSRX−
B11	RXp1	8	SDPp2	6	StdB_SSTX+
B10	RXn1	9	SDPn2	5	StdB_SSTX−
Shell	Shield	Outer Shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Standard-B plug. The bypass capacitor shall be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. Shield and GND grounds shall be connected within the USB Type-C and USB 3.1 Standard-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.4 USB Type-C to USB 2.0 Standard-B Cable Assembly

Figure 3-27 shows a USB Type-C to USB 2.0 Standard-B cable assembly.

Figure 3-27 USB Type-C to USB 2.0 Standard-B Cable Assembly

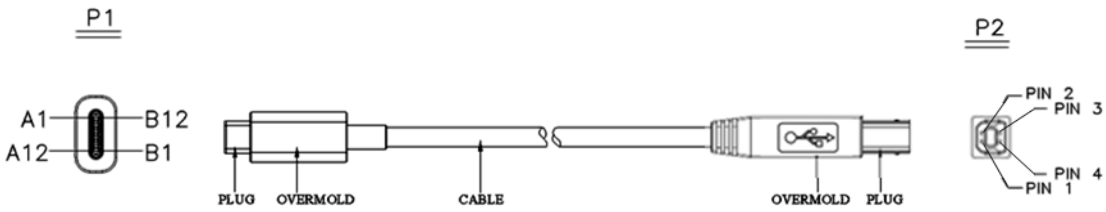


Table 3-15 defines the wire connections for the USB Type-C to USB 2.0 Standard-B cable assembly.

Table 3-15 USB Type-C to USB 2.0 Standard-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Standard-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	4	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Shield and GND grounds shall be connected within the USB Type-C and USB 2.0 Standard-B plugs on both ends of the cable assembly.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.5 USB Type-C to USB 2.0 Mini-B Cable Assembly

Figure 3-28 shows a USB Type-C to USB 2.0 Mini-B cable assembly.

Figure 3-28 USB Type-C to USB 2.0 Mini-B Cable Assembly

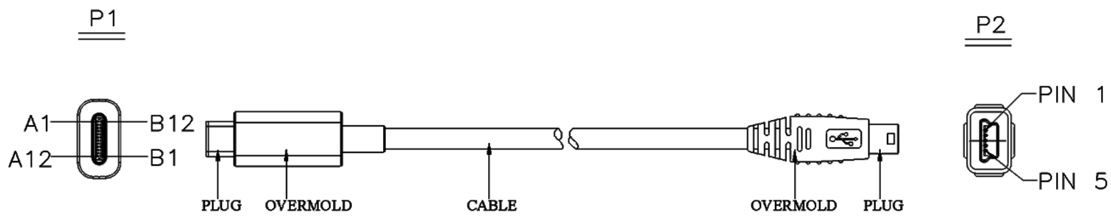


Table 3-16 defines the wire connections for the USB Type-C to USB 2.0 Mini-B cable assembly.

Table 3-16 USB Type-C to USB 2.0 Mini-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Mini-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the USB 2.0 Mini-B plug shall be terminated as defined in the applicable specification for the cable type.
6. Shield and GND grounds shall be connected within the USB Type-C and USB 2.0 Mini-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.6 USB Type-C to *USB 3.1* Micro-B Cable Assembly

Figure 3-29 shows a USB Type-C to *USB 3.1* Micro-B cable assembly.

Figure 3-29 USB Type-C to *USB 3.1* Micro-B Cable Assembly

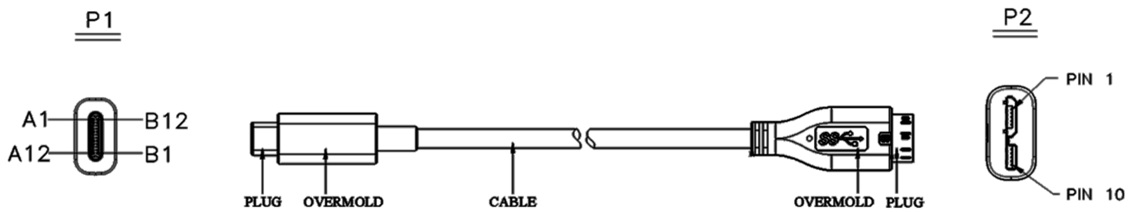


Table 3-17 defines the wire connections for the USB Type-C to *USB 3.1* Micro-B cable assembly.

Table 3-17 USB Type-C to USB 3.1 Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 3.1 Micro-B plug	
Pin	Signal Name	Wire Number	Signal Name	Pin	Signal Name
A1, B1, A12, B12	GND	1 7, 10	GND_PWRrt1 SDP1_Drain, SDP2_Drain	5 8	GND GND_DRAIN
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
A2	TXp1	5	SDPp1	10	MicB_SSRX+
A3	TXn1	6	SDPn1	9	MicB_SSRX−
B11	RXp1	8	SDPp2	7	MicB_SSTX+
B10	RXn1	9	SDPn2	6	MicB_SSTX−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A bypass capacitor is required between the VBUS and ground pins in the USB Type-C plug side of the cable. The bypass capacitor shall be 10nF ± 20% in cables which incorporate a USB Micro-B plug. The bypass capacitor should be placed as close as possible to the power supply pad.
5. All Ground return pins shall be connected together within the USB Type-C plug.
6. Pin 4 (ID) of the *USB 3.1* Micro-B plug shall be terminated as defined in the applicable specification for the cable type.
7. Shield and GND grounds shall be connected within the USB Type-C and *USB 3.1* Micro-B plugs on both ends of the cable assembly.
8. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.5.7 USB Type-C to *USB 2.0* Micro-B Cable Assembly

Figure 3-30 shows a USB Type-C to *USB 2.0* Micro-B cable assembly.

Figure 3-30 USB Type-C to *USB 2.0* Micro-B Cable Assembly

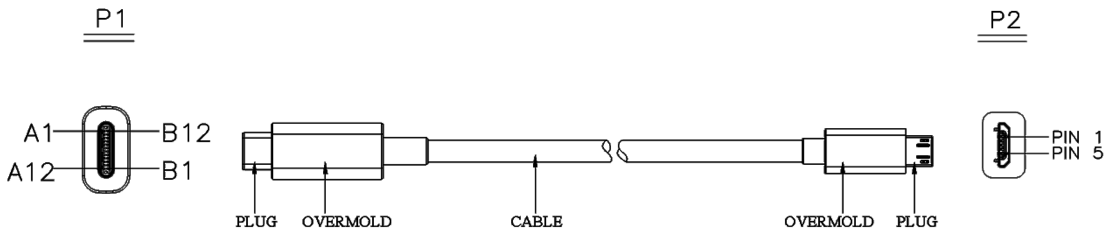


Table 3-18 defines the wire connections for the USB Type-C to *USB 2.0* Micro-B cable assembly.

Table 3-18 USB Type-C to *USB 2.0* Micro-B Cable Assembly Wiring

USB Type-C Plug		Wire		USB 2.0 Micro-B plug	
Pin	**Signal Name**	**Wire Number**	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	1	GND_PWRrt1	5	GND
A4, B4, A9, B9	VBUS	2	PWR_VBUS1	1	VBUS
A5	CC	See Note 1			
B5	VCONN				
A6	Dp1	3	UTP_Dp	3	D+
A7	Dn1	4	UTP_Dn	2	D−
				4	ID
Shell	Shield	Outer shield	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins in this cable.
4. All Ground return pins shall be connected together within the USB Type-C plug.
5. Pin 4 (ID) of the *USB 2.0* Micro-B plug shall be terminated as defined in the applicable specification for the cable type.
6. Shield and GND grounds shall be connected within the USB Type-C and *USB 2.0* Micro-B plugs on both ends of the cable assembly.
7. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.6 Legacy Adapter Assemblies

To enable interoperability between USB Type-C-based products and legacy USB products, the following standard legacy adapter assemblies are defined. Only the adapter assemblies defined in this specification are allowed.

3.6.1 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

Figure 3-31 shows a USB Type-C to *USB 3.1* Standard-A receptacle adapter assembly. This cable assembly is defined for direct connect to a USB device (e.g., a thumb drive). System functionality of using this adaptor assembly together with another USB cable assembly is not guaranteed.

Figure 3-31 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly

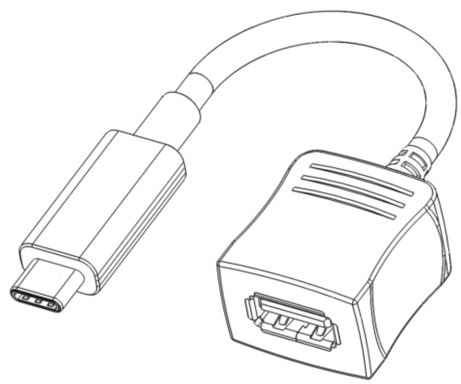


Table 3-19 defines the wire connections for the USB Type-C to *USB 3.1* Standard-A receptacle adapter assembly.

Table 3-19 USB Type-C to *USB 3.1* Standard-A Receptacle Adapter Assembly Wiring

USB Type-C Plug		USB 3.1 Standard-A receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	4 7	GND GND_DRAIN
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
B5	VCONN		
A6	Dp1	3	D+
A7	Dn1	2	D−
A2	TXp1	9	StdA_SSTX+
A3	TXn1	8	StdA_SSTX−
B11	RXp1	6	StdA_SSRX+
B10	RXn1	5	StdA_SSRX−
Shell	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to GND through a resistor Rd (5.1 kΩ ± 20%). See Section 4.5.3.2.1 and Table 4-25 for the functional description and value of Rd.
2. This table assumes that shielded twisted pair is used for all SDP's and there are drain wires. If coaxial wire construction is used, then no drain wires are present, and the shields of the coaxial wires are connected to the ground pins.
3. Contacts B6 and B7 should not be present in the USB Type-C plug.
4. All VBUS pins shall be connected together within the USB Type-C plug. A 10 nF bypass capacitor is required for the VBUS pin in the USB Type-C plug end of the cable. The bypass capacitor should be placed as close as possible to the power supply pad. A bypass capacitor is not required for the VBUS pin in the Standard-A receptacle.
5. Shield and GND grounds shall be connected within the USB Type-C plug and *USB 3.1* Standard-A receptacle on both ends of the adapter assembly.
6. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.6.2 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly

Figure 3-32 shows a USB Type-C to *USB 2.0* Micro-B receptacle adapter assembly.

Figure 3-32 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly

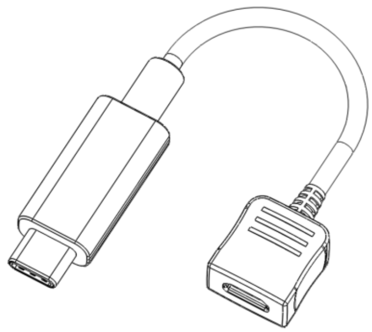


Table 3-20 defines the wire connections for the USB Type-C to *USB 2.0* Micro-B receptacle adapter assembly.

Table 3-20 USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly Wiring

USB Type-C Plug		USB 2.0 Micro-B receptacle	
Pin	**Signal Name**	**Pin**	**Signal Name**
A1, B1, A12, B12	GND	5	GND
A4, B4, A9, B9	VBUS	1	VBUS
A5	CC	See Note 1	
A6	Dp1	3	D+
A7	Dn1	2	D−
		4	ID
Shell	Shield	Shell	Shield

Notes:

1. Pin A5 (CC) of the USB Type-C plug shall be connected to VBUS through a resistor Rp (56 kΩ ± 5%). See Section 4.5.3.2.2 and Table 4-24 for the functional description and value of Rp.
2. Contacts B6 and B7 should not be present in the USB Type-C plug.
3. All VBUS pins shall be connected together within the USB Type-C plug. Bypass capacitors are not required for the VBUS pins at the Micro-B receptacle end of this cable.
4. Shield and GND grounds shall be connected within the USB Type-C plug and *USB 2.0* Micro-B receptacle on both ends of the adapter assembly.
5. All USB Type-C plug pins that are not listed in this table shall be open (not connected).

3.7 Electrical Characteristics

This section defines the USB Type-C raw cable, connector, and cable assembly electrical requirements, including signal integrity, shielding effectiveness, and DC requirements. Chapter 3.11.1 defines additional requirements regarding functional signal definition, host/device discovery and configuration, and power delivery.

Unless otherwise specified, all measurements are made at a temperature of 15° to 35° C, a relative humidity of 25% to 85%, and an atmospheric pressure of 86 to 106 kPa and all S-parameters are normalized with an 85 Ω differential impedance.

3.7.1 Raw Cable (Informative)

Informative raw cable electrical performance targets are provided to help cable assembly manufacturers manage the procurement of raw cable. These targets are not part of the USB Type-C compliance requirements. The normative requirement is that the cable assembly meets the performance characteristics specified in Sections 3.7.2 and 3.7.5.3.

The differential characteristic impedance for shielded differential pairs is recommended to be 90 Ω ± 5 Ω. The single-ended characteristic impedance of coaxial wires is recommended to be 45 Ω ± 3 Ω. The impedance should be evaluated using a 200 ps (10%-90%) rise time; a faster rise time is not necessary for raw cable since it will make cable test fixture discontinuities more prominent.

3.7.1.1 Intra-Pair Skew (Informative)

The intra-pair skew for a differential pair is recommended to be less than 10 ps/m. It should be measured with a Time Domain Transmission (TDT) in a differential mode using a 200 ps (10%-90%) rise time with a crossing at 50% of the input voltage.

3.7.1.2 Differential Insertion Loss (Informative)

Cable loss depends on wire gauges, plating and dielectric materials. Table 3-21 and Table 3-22 show examples of differential insertion losses.

Table 3-21 Differential Insertion Loss Examples for TX/RX with Twisted Pair Construction

Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.4 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.5 dB/m	−2.0 dB/m	−1.7 dB/m	−1.4 dB/m
2.50 GHz	−3.7 dB/m	−2.9 dB/m	−2.5 dB/m	−2.1 dB/m
5.00 GHz	−5.5 dB/m	−4.5 dB/m	−3.9 dB/m	−3.1 dB/m
7.50 GHz	−7.0 dB/m	−5.9 dB/m	−5.0 dB/m	−4.1 dB/m
10.00 GHz	−8.4 dB/m	−7.2 dB/m	−6.1 dB/m	−4.8 dB/m
12.50 GHz	−9.5 dB/m	−8.2 dB/m	−7.3 dB/m	−5.5 dB/m
15.00 GHz	−11.0 dB/m	−9.5 dB/m	−8.7 dB/m	−6.5 dB/m

Table 3-22 Differential Insertion Loss Examples for USB TX/RX with Coaxial Construction

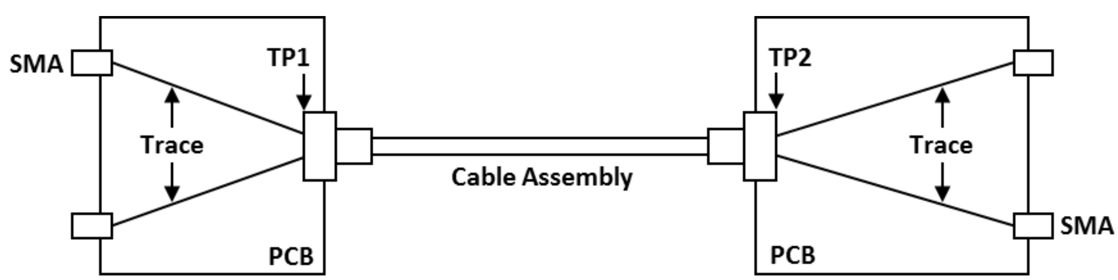
Frequency	34AWG	32AWG	30AWG	28AWG
0.625 GHz	−1.8 dB/m	−1.5 dB/m	−1.2 dB/m	−1.0 dB/m
1.25 GHz	−2.8 dB/m	−2.2 dB/m	−1.8 dB/m	−1.3 dB/m
2.50 GHz	−4.2 dB/m	−3.4 dB/m	−2.7 dB/m	−1.9 dB/m
5.00 GHz	−6.1 dB/m	−4.9 dB/m	−4.0 dB/m	−3.1 dB/m
7.50 GHz	−7.6 dB/m	−6.5 dB/m	−5.2 dB/m	−4.2 dB/m
10.0 GHz	−8.8 dB/m	−7.6 dB/m	−6.1 dB/m	−4.9 dB/m
12.5 GHz	−9.9 dB/m	−8.6 dB/m	−7.1 dB/m	−5.7 dB/m
15.0 GHz	−12.1 dB/m	−10.9 dB/m	−9.0 dB/m	−6.5 dB/m

3.7.2 USB Type-C to Type-C Passive Cable Assemblies (Normative)

A USB Type-C to Type-C cable assembly shall be tested using a test fixture with the receptacle tongue fabricated in the test fixture. This is illustrated in Figure 3-33. The USB Type-C receptacles are not present in the test fixture. Hosts and devices should account for the additional signal degradation the receptacle introduces.

The requirements are for the entire signal path of the cable assembly mated with the fixture PCB tongues, not including lead-in PCB traces. As illustrated in Figure 3-33, the measurement is between TP1 (test point 1) and TP2 (test point 2). Refer to documentation located at Cables and Connectors page on the USB-IF website for a detailed description of a standardized test fixture.

Figure 3-33 Illustration of Test Points for a Mated Cable Assembly



The cable assembly requirements are divided into informative and normative requirements. The informative requirements are provided as design targets for cable assembly manufacturers. The normative requirements are the pass/failure criteria for cable assembly compliance.

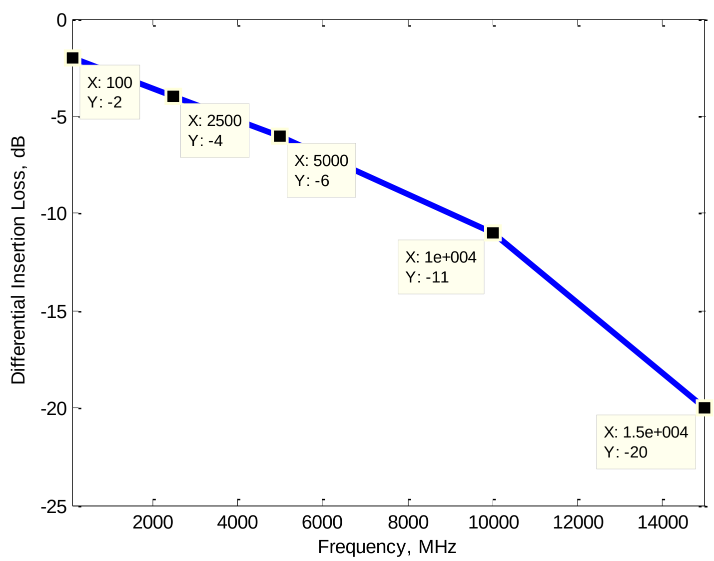
3.7.2.1 Recommended TX/RX Passive Cable Assembly Characteristics (USB 3.2 Gen2 and USB4 Gen2)

The recommended electrical characteristics defined in this section are informative design guidelines. Cable assemblies that do not meet these recommended electrical characteristics may still pass USB certification testing. Similarly, cable assemblies that meet these recommended electrical characteristics may or may not pass USB certification testing.

3.7.2.1.1 Differential Insertion Loss (Informative – USB 3.2 Gen2 and USB4 Gen2)

Figure 3-34 shows the differential insertion loss limit for a USB 3.2 Gen2 or a USB4 Gen2 Type-C cable assembly, which is defined by the following vertices: (100 MHz, −2 dB), (2.5 GHz, −4 dB), (5.0 GHz, −6 dB), (10 GHz, −11 dB) and (15 GHz, −20 dB).

Figure 3-34 Recommended Differential Insertion Loss Requirement (USB 3.2 Gen2 and USB4 Gen2)

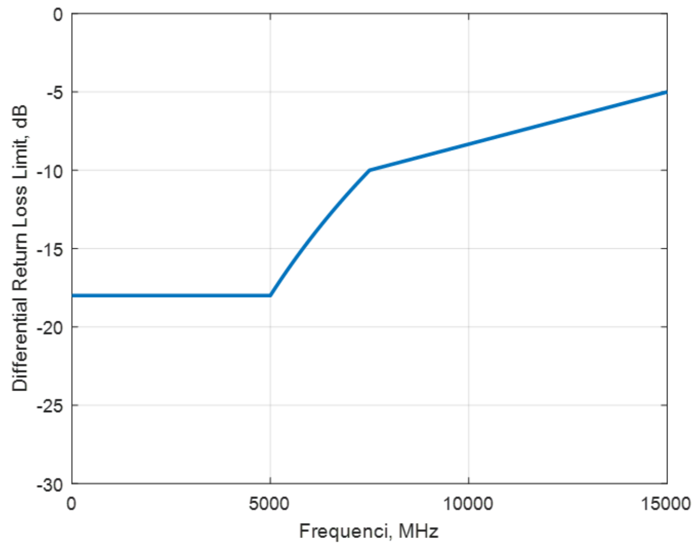


3.7.2.1.2 Differential Return Loss (Informative – USB 3.2 Gen2 and USB4 Gen2)

Figure 3-35 shows the differential return loss limit, which is defined by the following equation:

$$RL\ mask = \begin{cases} -18\ dB,\ f < 5\ Ghz \\ -18 + 45.43 \times \log_{10}\left(\frac{f}{5}\right)\ dB,\ 5\ Ghz < f\ \le 7.5\ Ghz \\ -15 + \frac{2}{3} \times f\ dB,\ 7.5\ Ghz < f \le 15\ Ghz \end{cases}$$

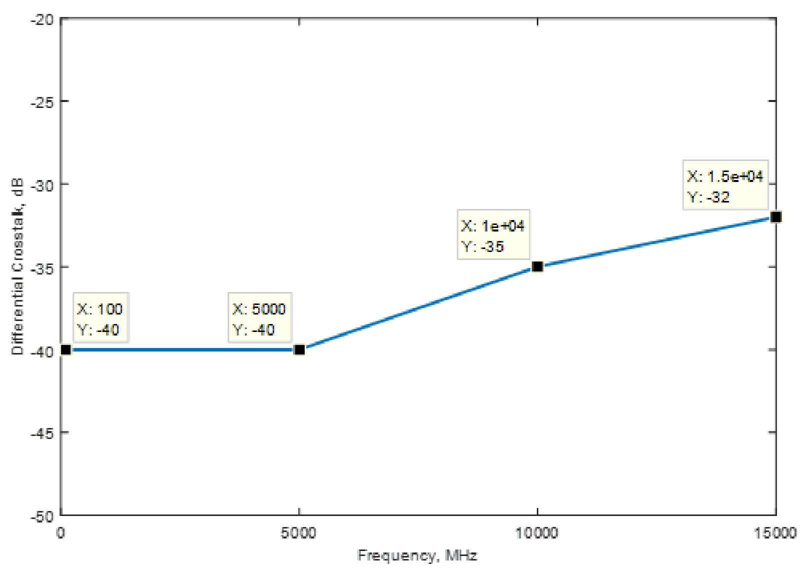
Figure 3-35 Recommended Differential Return Loss Requirement



3.7.2.1.3 Differential Near-End and Far-End Crosstalk between TX/RX Pairs (Informative – USB 3.2 Gen2 and USB4 Gen2)

Both the near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are specified, as shown in Figure 3-36. The DDNEXT/DDFEXT limits are defined by the following vertices: (100 MHz, −40 dB), (5 GHz, −40 dB), (10 GHz, −35 dB), and (15 GHz, −32 dB).

Figure 3-36 Recommended Differential Crosstalk Requirement

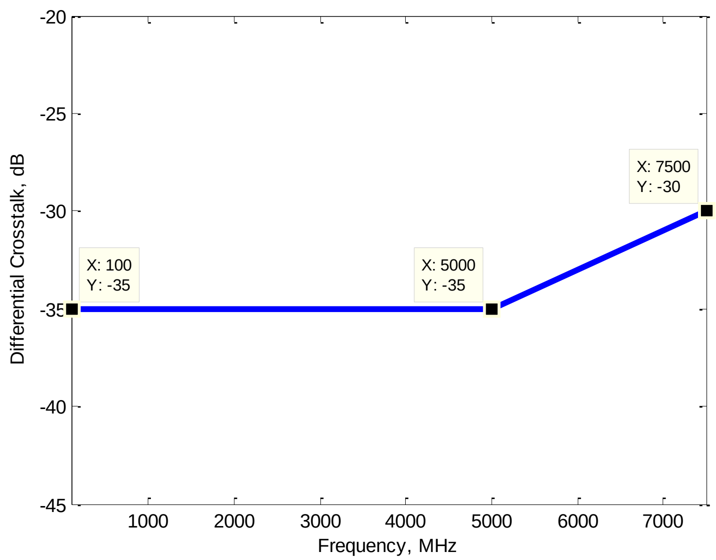


3.7.2.1.4 Differential Crosstalk between USB D+/D− and TX/RX Pairs (Informative – USB 3.2 Gen2 and USB4 Gen2)

The differential near-end and far-end crosstalk between the USB D+/D− pair and the TX/RX pairs should be managed not to exceed the limits shown in Figure 3-37. The USB D+/D− pair and the TX/RX pairs should be considered in the context of both an aggressor and a victim. It should also be considered that the D+/D− pair maximum frequency for similar tests is

1.2 GHz (see Table 3-31), but in this case the crosstalk on the D+/D− pair is extended to 7.5 GHz. The limits are defined by the following points: (100 MHz, −35 dB), (5 GHz, −35 dB), and (7.5 GHz, −30 dB).

Figure 3-37 Recommended Differential Near-End and Far-End Crosstalk Requirement between USB D+/D− Pair and TX/RX Pair

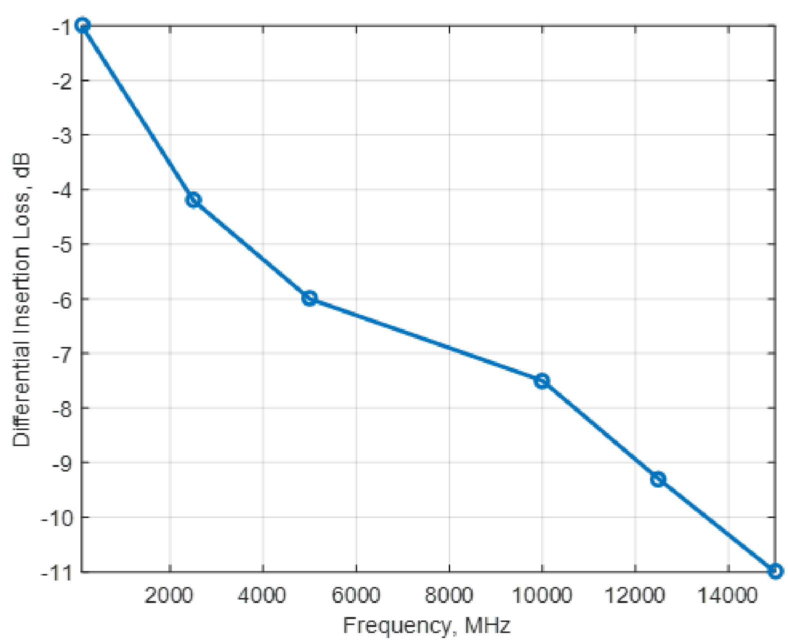


3.7.2.2 Recommended TX/RX Passive Cable Assembly Characteristics (USB4 Gen3)

3.7.2.2.1 Differential Insertion Loss (Informative – USB4 Gen3)

Figure 3-38 shows the recommended differential insertion loss limit for a *USB4* Gen3 Type-C cable assembly, which is defined by the following vertices: (100 MHz, −1 dB), (2.5 GHz, −4.2 dB), (5.0 GHz, −6 dB), (10 GHz, −7.5 dB), (12 GHz, −9.3 dB), and (15 GHz, −11 dB).

Figure 3-38 Recommended Differential Insertion Loss Requirement (USB4 Gen3)



3.7.2.2.2 Differential Return Loss (Informative – USB4 Gen3)

The informative differential return loss mask is identical in Section 3.7.2.1.2.

3.7.2.2.3 Differential Near-End and Far-End Crosstalk between TX/RX Pairs (Informative – USB4 Gen3)

The recommended near-end crosstalk (DDNEXT) and far-end crosstalk (DDFEXT) are defined in Section 3.7.2.1.3. To minimize crosstalk, it is important to optimize the paddle card and wire termination designs inside the cable plug.

3.7.2.2.4 Differential Crosstalk between USB D+/D− and TX/RX Pairs (Informative – USB4 Gen3)

The informative near-end and far-end crosstalk between the USB D+/D− pair and the TX/RX pairs are the same as in Section 3.7.2.1.4.

3.7.2.3 Normative TX/RX Passive Cable Assembly Requirements (USB 3.2 Gen2 and USB4 Gen2)

The integrated parameters are used for cable assembly compliance (except for insertion loss and differential-to-common-mode conversion) to avoid potential rejection of a functioning cable assembly that may fail the traditional S-parameters spec at a few frequencies.

3.7.2.3.1 Insertion Loss Fit at Nyquist Frequencies (Normative – USB 3.2 Gen2 and USB4 Gen2)

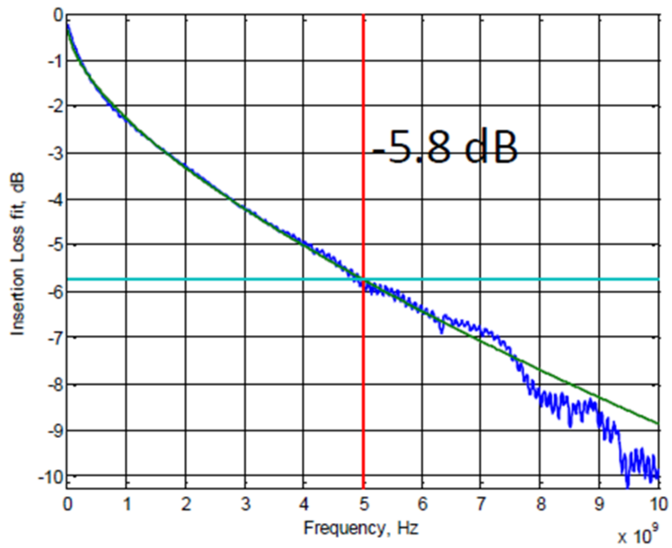
The insertion loss fit at Nyquist frequency measures the attenuation of the cable assembly. To obtain the insertion loss fit at Nyquist frequency, the measured cable assembly differential insertion loss is fitted with a smooth function. A standard fitting algorithm and tool shall be used to extract the insertion loss fit at Nyquist frequencies. The fitting equation is defined by the following equation:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

where f is the frequency and a, b, c, and d are the fitting coefficients.

Figure 3-39 illustrates an example of a measured cable assembly insertion loss fitted with a smooth function; the insertion loss fit at the Nyquist frequency of SuperSpeed USB Gen2 (5.0 GHz) is −5.8 dB.

Figure 3-39 Illustration of Insertion Loss Fit at Nyquist Frequency



The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:

- ≥ −4 dB at 2.5 GHz,
- ≥ −6 dB at 5 GHz, and
- ≥ −11 dB at 10 GHz.

2.5 GHz, 5.0 GHz and 10 GHz are the Nyquist frequencies for SuperSpeed USB Gen1, SuperSpeed USB Gen2, and USB4 Gen3 data rate, respectively.

3.7.2.3.2 Integrated Multi-reflection (Normative – USB 3.2 Gen2 and USB4 Gen2)

The insertion loss deviation, ILD, is defined as

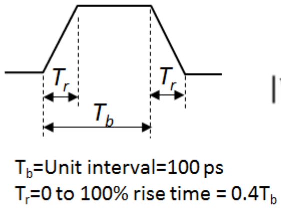
$$ILD(f) = IL(f) - ILfit(f)$$

It measures the ripple of the insertion loss, caused by multiple reflections inside the cable assembly (mated with the fixture). The integration of *ILD(f)* is called the integrated multi-reflection (IMR):

$$IMR = dB\left(\sqrt{\frac{\int_0^{f_{max}} |ILD(f)|^2 |Vin(f)|^2 df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where *fmax* = 12.5 GHz and *Vin(f)* is the input trapezoidal pulse spectrum, defined in Figure 3-40.

Figure 3-40 Input Pulse Spectrum



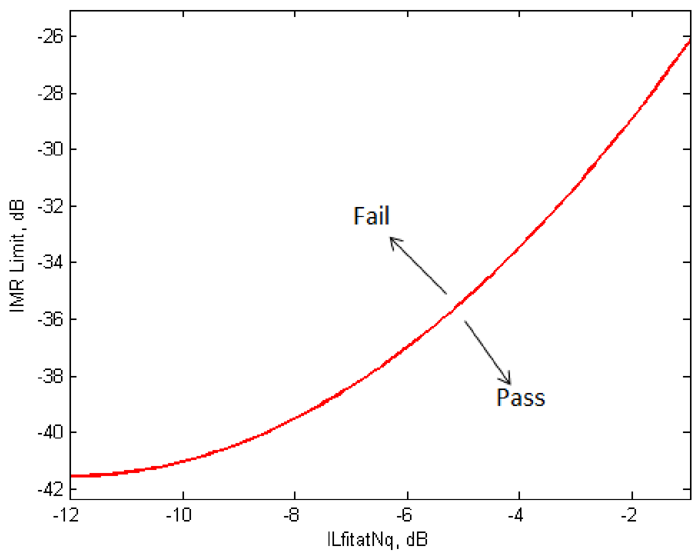
$$|V_{in}(f)| = \left|\frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}\right|$$

IMR has dependency on ILfitatNq. More IMR may be tolerated when ILfitatNq decreases. The IMR limit is specified as a function of ILfitatNq:

$$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 23.392.$$

This is plotted in Figure 3-41.

Figure 3-41 IMR Limit as Function of ILfitatNq



3.7.2.3.3 Integrated Crosstalk between TX/RX Pairs (Normative – USB 3.2 Gen2 and USB4 Gen2)

The integrated crosstalk between all TX/RX pairs is calculated with the following equations:

$$INEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|NEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\,|FEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

where *NEXT(f)*, *FEXT(f)*, and *C2D(f)* are the measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude. *NEXTd(f)* and *FEXTd(f)* are, respectively, the near-end and far-end crosstalk from the D+/D− pair to TX/RX pairs. *Vdd(f)* is the input pulse spectrum evaluated using the equation in Figure 3-40 with Tb=2.08 ns.

The integration shall be done for each NEXT and FEXT between all differential pairs. The largest values of INEXT and IFEXT shall meet the following requirements:

- INEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2,
- IFEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2.

The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four SuperSpeed pairs transmit or receive signals simultaneously, for example in SuperSpeed USB dual-lane operation.

3.7.2.3.4 Integrated Crosstalk between TX/RX Pairs to USB 2.0 D+/D− (Normative – USB 3.2 Gen2 and USB4 Gen2)

Crosstalk from the TX/RX pairs to USB 2.0 D+/D− shall be controlled to ensure the robustness of the USB 2.0 link. Since USB Type-C to Type-C Full-Featured cable assemblies may support the usage of *USB 3.2*, *USB4* or an Alternate Mode (e.g., DisplayPort™), the crosstalk from the four high speed differential pairs to D+/D− may be from near-end crosstalk, far-end crosstalk, or a combination of the two. The integrated crosstalk to D+/D− is calculated with the following equations:

$$\text{IDDXT\_1NEXT + FEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |FEXT(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

where:

NEXT = Near-end crosstalk from TX pair to D+/D−

FEXT = Far-end crosstalk from RX pair to D+/D−

fmax = 1.2 GHz

$$\text{IDDXT\_2NEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |NEXT2(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

where:

NEXT1 = Near-end crosstalk from TX pair to D+/D−

NEXT2 = Near-end crosstalk from RX (the RX functioning in TX mode) pair to D+/D−

fmax = 1.2 GHz

The integration shall be done for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at A2, A3, B10 and B11 (see Figure 2-2) and for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at B2, B3 A10 and A11 (see Figure 2-2). Measurements are made in two sets to minimize the number of ports required for each measurement. The integrated differential crosstalk on D+/D− shall meet the following requirements:

- IDDXT_1NEXT + FEXT ≤ −34.5 dB,

- IDDXT_2NEXT ≤ −33 dB.

3.7.2.3.5 Integrated Return Loss (Normative – USB 3.2 Gen2 and USB4 Gen2)

The integrated return loss (IRL) manages the reflection between the cable assembly and the rest of the system (host and device). It is defined as:

$$IRL = dB\left(\sqrt{\frac{\int_0^{fmax}|Vin(f)|^2|SDD21(f)|^2(|SDD11(f)|^2+|SDD22(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2df}}\right)$$

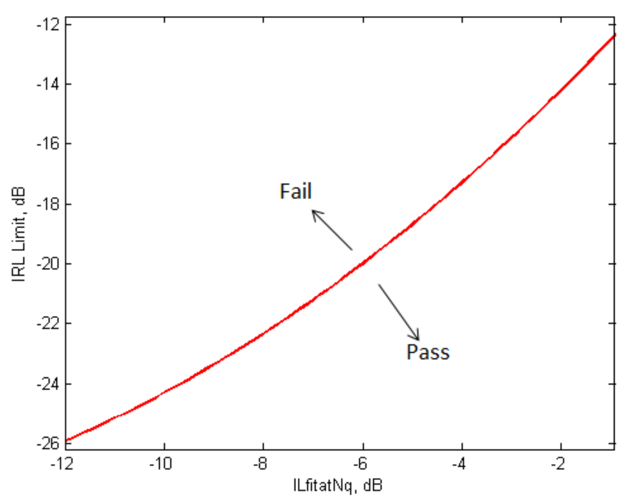
where *SDD21(f)* is the measured cable assembly differential insertion loss, *SDD11(f)* and *SDD22(f)* are the measured cable assembly return losses on the left and right sides, respectively, of a differential pair.

The IRL also has a strong dependency on ILfitatNq, and its limit is specified as a function of ILfitatNq:

$IRL \leq 0.046 \cdot ILfitatNq^2 + \ 1.812 \cdot ILfitatNq - 10.784.$

It is shown in Figure 3-42.

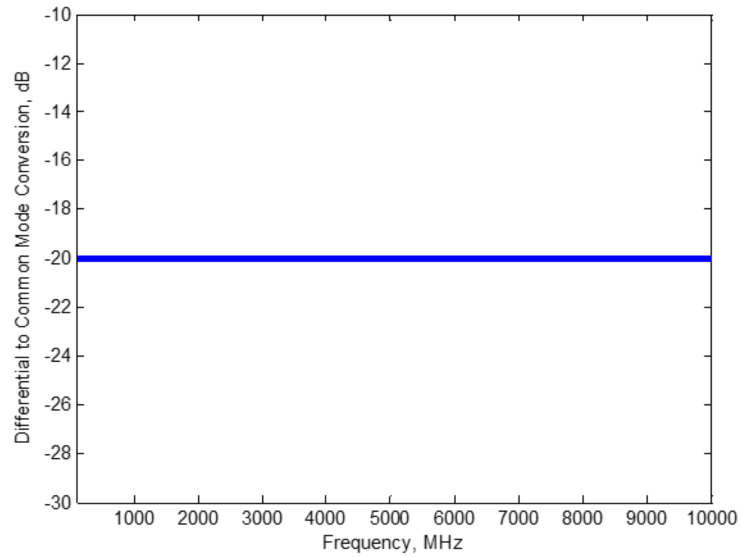
Figure 3-42 IRL Limit as Function of ILfitatNq



3.7.2.3.6 Differential-to-Common-Mode Conversion (Normative – USB 3.2 Gen2 and USB4 Gen2)

The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Figure 3-43 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −20 dB from 100 MHz to 10 GHz.

Figure 3-43 Differential-to-Common-Mode Conversion Requirement



3.7.2.4 TX/RX Passive Cable Assembly Requirements for USB 3.2 Gen1 and USB4 Gen2 (Normative)

3.7.2.4.1 Insertion Loss Fit at Nyquist Frequencies

The integrated S-parameter requirements for *USB 3.2* Gen1 and *USB4* Gen2 follow the same methodology as defined in Section 3.7.2.3. There are parameter adjustments made to suit the *USB4* Gen2 data rate. Unless otherwise specified, the following parameters shall be used to calculate insertion loss fit and integrated parameters:

- T_b, the unit interval, is set to 100 ps, reflecting the *USB4* Gen2 data rate.
- T_r, the rise time, remains at 0.4 * T_b.
- f_{max}, the maximum frequency over which the integration or fitting is performed is increased to 12.5 GHz.
- The fitting equation is defined by the following equation:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3}$$

where *f* is the frequency and *a*, *b*, *c*, and *d* are the fitting coefficients.

The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:

- ≥ −7.0 dB at 2.5 GHz, and
- > −11.5 dB at 5 GHz.

3.7.2.4.2 Integrated Multi-reflection

The insertion loss deviation, ILD, is defined as

$$ILD(f) = IL(f) - ILfit(f)$$

It measures the ripple of the insertion loss, caused by multiple reflections inside the cable assembly (mated with the fixture). The integration of *ILD(f)* is called the integrated multi-reflection (IMR):

$$IMR = dB\left(\sqrt{\frac{\int_0^{fmax}|ILD(f)|^2|Vin(f)|^2 df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

where *fmax* = 12.5 GHz and *Vin(f)* is the input trapezoidal pulse spectrum.

For USB 3.2 Gen1 and USB4 Gen2 cable assemblies, IMR limit is specified as:

$$IMR \le 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 24.792.$$

3.7.2.4.3 Integrated Crosstalk from TX/RX Pairs

The integrated crosstalk between all TX/RX pairs is calculated with the following equations:

$$INEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|NEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\ |NEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

$$IFEXT = dB\left(\sqrt{\frac{\int_0^{fmax}(|Vin(f)|^2(|FEXT(f)|^2 + 0.125^2 \cdot |C2D(f)|^2) + |Vdd(f)|^2\ |FEXTd(f)|^2)df}{\int_0^{fmax}|Vin(f)|^2 df}}\right)$$

where *NEXT(f)*, *FEXT(f)*, and *C2D(f)* are the measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude. *NEXTd(f)* and *FEXTd(f)* are, respectively, the near-end and far-end crosstalk from the D+/D− pair to TX/RX pairs. *Vdd(f)* is the input pulse spectrum with Tb=2.08 ns.

The largest values of INEXT and IFEXT shall meet the following requirements:

- INEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2,
- IFEXT ≤ −40 dB to 12.5GHz, for TX1 to RX1, TX2 to RX2, TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2.

The port-to-port crosstalk (TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) is specified to support the usages in which all the four high speed pairs transmit or receive signals simultaneously (e.g., USB dual-lane operation).

3.7.2.4.4 Integrated Crosstalk from TX/RX Pairs to USB 2.0 D+/D−

Crosstalk from the TX/RX pairs to USB 2.0 D+/D− shall be controlled to ensure the robustness of the USB 2.0 link. Since USB Type-C to Type-C Full-Featured cable assemblies may support the usage of USB 3.2, USB4 or an Alternate Mode (e.g., DisplayPort™), the crosstalk from the four high speed differential pairs to D+/D− may be from near-end crosstalk, far-end crosstalk, or a combination of the two. The integrated crosstalk to D+/D− is calculated with the following equations:

$$\mathrm{IDDXT\_1NEXT + FEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2(|NEXT1(f)|^2 + |FEXT(f)|^2)df}{\int_0^{f_{max}}|Vin(f)|^2 df}}\right)$$

where:

NEXT = Near-end crosstalk from TX pair to D+/D−

FEXT = Far-end crosstalk from RX pair to D+/D−

fmax = 1.2 GHz

$$\text{IDDXT\_2NEXT} = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2(|NEXT1(f)|^2 + |NEXT2(f)|^2)df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where:

NEXT1 = Near-end crosstalk from TX pair to D+/D−

NEXT2 = Near-end crosstalk from RX (the RX functioning in TX mode) pair to D+/D−

fmax = 1.2 GHz

The integration shall be done for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at A2, A3, B10 and B11 (see Figure 2-2) and for NEXT + FEXT and 2NEXT on D+/D− from the two differential pairs located at B2, B3 A10 and A11 (see Figure 2-2). Measurements are made in two sets to minimize the number of ports required for each measurement.

The integrated differential crosstalk on D+/D− shall meet the following requirements:

- IDDXT_1NEXT + FEXT ≤ −34.5 dB,
- IDDXT_2NEXT ≤ −33 dB.

3.7.2.4.5 Integrated Return Loss

The integrated return loss (IRL) manages the reflection between the cable assembly and the rest of the system (host and device). It is defined as:

$$IRL = dB\left(\sqrt{\frac{\int_0^{f_{max}} |Vin(f)|^2 |SDD21(f)|^2(|SDD11(f)|^2 + |SDD22(f)|^2)df}{\int_0^{f_{max}} |Vin(f)|^2 df}}\right)$$

where *SDD21(f)* is the measured cable assembly differential insertion loss, *SDD11(f)* and *SDD22(f)* are the measured cable assembly return losses on the left and right sides, respectively, of a differential pair.

For USB 3.2 Gen 1 and USB4 Gen 2 cable assemblies, IRL limit is specified as:

$$IRL \le 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 9.784.$$

3.7.2.4.6 Differential-to-Common-Mode Conversion

The differential-to-common-mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −17 dB from 100 MHz to 10 GHz.

3.7.2.5 Normative TX/RX Passive Cable Assembly Requirements (USB4 Gen3)

The integrated S-parameter requirements for USB4 Gen3 follow the same methodology as defined in Section 3.7.2.3. There are parameter adjustments made to suit the USB4 Gen3 data rate. Unless otherwise specified, the following parameters shall be used to calculate insertion loss fit and integrated parameters:

- T_b, the unit interval, is set to 50 ps, reflecting the *USB4* Gen3 data rate.
- T_r, the rise time, remains at 0.4 * T_b.
- f_{max}, the maximum frequency over which the integration or fitting is performed is increased to 20 GHz.
- An f-square term is added to the insertion loss fit equation to improve fitting quality:

$$IL_{fit} = a + b * \sqrt{f} + c * \sqrt{f^2} + d * \sqrt{f^3} + e * \sqrt{f^4}$$

USB4 Gen3 introduces a system-level COM (Channel Operating Margin) specification for the cable assembly. The details are defined in Section 3.7.2.5.7.

3.7.2.5.1 Insertion Loss Fit at Nyquist Frequencies (Normative – USB4 Gen3)

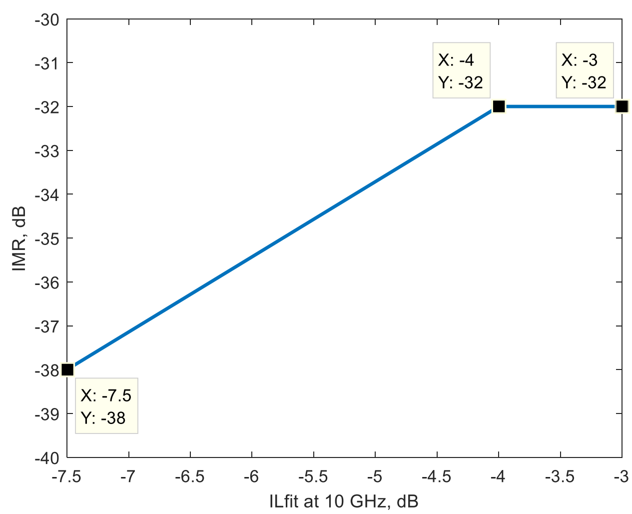
The insertion loss fit at Nyquist frequency (ILfitatNq) shall meet the following requirements:

- ≥ −1 dB at 100 MHz,
- ≥ −4.2 dB at 2.5 GHz,
- ≥ −6 dB at 5 GHz,
- ≥ −7.5 dB at 10 GHz,
- ≥ −9.3 dB at 12.5 GHz, and
- ≥ −11 dB at 15 GHz.

3.7.2.5.2 Integrated Multi-Reflection (Informative – USB4 Gen3)

The IMR limit is plotted in Figure 3-44.

Figure 3-44 IMR Limit as Function of ILfit at 10 GHz (USB4 Gen3)



3.7.2.5.3 Integrated Crosstalk between TX/RX Pairs (Normative – USB4 Gen3)

The integrated crosstalk within a port for TX1 to RX1 and TX2 to RX2 is recommended to meet the following informative requirements:

- INEXT ≤ −43 dB and

- IFEXT ≤ −43 dB.

The recommended informative requirement for the integrated port-to-port crosstalk for TX1 to RX2, TX2 to RX1, TX1 to TX2, and RX1 to RX2) are defined as:

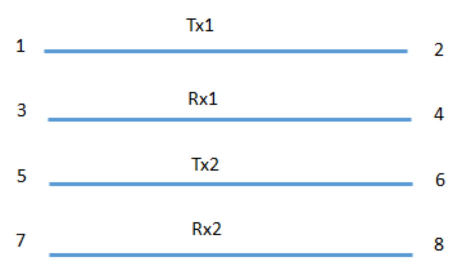
- INEXT_p2p ≤ −50 dB and
- IFEXT_p2p ≤ −50 dB.

The total crosstalk is defined for both the DP Alternate Mode and *USB4* operation. In DP Alternate Mode, all crosstalk is FEXT, while in *USB4* operation both FEXT and NEXT exist. The total crosstalk is defined in the equation below:

$$\text{IXTi\_DP or IXTi\_USB} = dB\left(\sqrt{\frac{\int_0^{f_{max}}|Vin(f)|^2\sum_j|SDDij|^2df}{\int_0^{f_{max}}|Vin(f)|^2df}}\right)$$

where the victims i = 1 to 8 and the aggressors j are defined in Figure 3-45.

Figure 3-45 Definition of Port, Victim, and Aggressor



IXT_DP

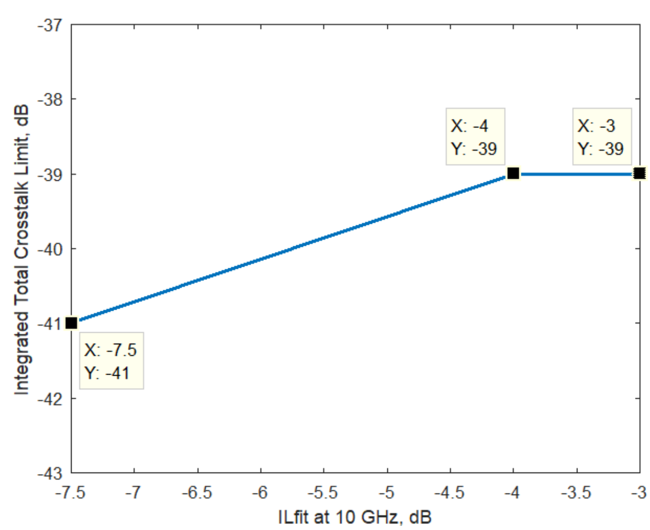
i	j		
1	4	6	8
2	3	5	7
3	2	6	8
4	1	5	7
5	2	4	8
6	1	3	7
7	2	4	6
8	1	3	5

IXT_USB

i	j		
1	3	7	6
2	4	8	5
3	1	5	8
4	2	6	7
5	3	7	2
6	4	8	1
7	1	5	4
8	2	6	3

The total crosstalk for the DP Alternate Mode and *USB4* operation shall be controlled. Its normative limit is defined in Figure 3-46.

Figure 3-46 IXT_DP and IXT_USB Limit as Function of ILfit at 10 GHz (USB4 Gen3)



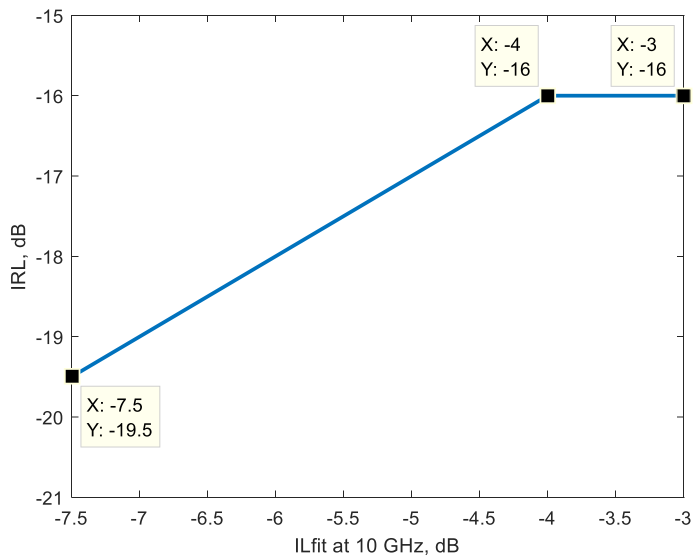
3.7.2.5.4 Integrated Crosstalk from TX/RX Pairs to USB 2.0 D+/D− (Normative – USB4 Gen3)

The requirements for the integrated crosstalk from the TX/RX pairs to USB 2.0 D+/D− are defined in Section 3.7.2.3.4.

3.7.2.5.5 Integrated Return Loss (Normative – USB4 Gen3)

The IRL limit is shown in Figure 3-47.

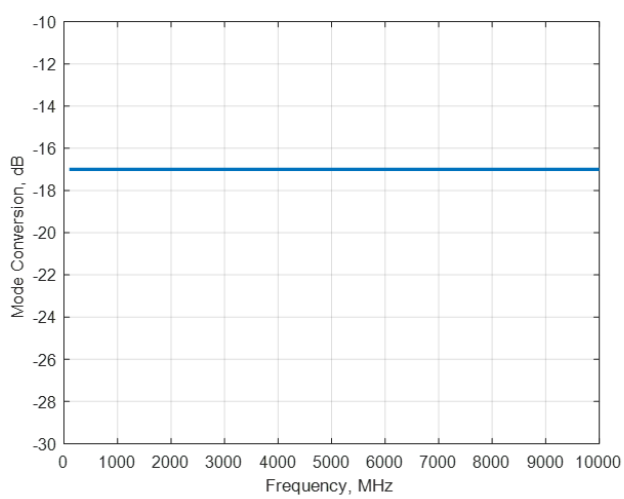
Figure 3-47 IRL Limit as Function of ILfitatNq (USB4 Gen3)



3.7.2.5.6 Differential-to-Common-Mode Conversion (Normative – USB4 Gen3)

Figure 3-48 illustrates the differential-to-common mode conversion (SCD12/SCD21) requirement. A mated cable assembly passes if its SCD12/SCD21 is less than or equal to −17 dB from 100 MHz to 10 GHz. Note that −17 dB is the worst-case limit; no *USB4* Gen3 Type-C cable is allowed to exceed it.

Figure 3-48 Differential-to-Common-Mode Conversion Requirement (USB4 Gen3)



3.7.2.5.7 COM Requirement (Normative – USB4 Gen3)

Channel Operating Margin (COM) is a figure of merit to measure the channel electrical quality. The technical detail of COM may be found in IEEE Std 802.3bj™-2014 Clause 93a.

COM is essentially the channel signal-to-noise ratio:

$$COM = 20log10(\frac{A}{N})$$

where A is the signal amplitude and N is the combined noise at BER (bit-error-ratio), which includes the noise sources from ISI (inter-symbol-interference), crosstalk, transmitter jitter, etc.

To calculate COM, reference hosts/devices, which represent the worst-case hosts/devices, shall be defined and the reference TX and RX shall be used. As illustrated in Figure 3-49, the measured cable assembly S-parameters are cascaded with the reference host and reference device models to form the complete channel; the TX and RX die-loading and equalizers are then applied to the channel to calculate COM.

Figure 3-49 Cable Assembly in System

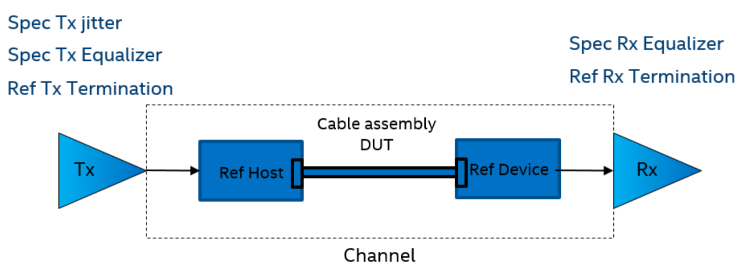


Table 3-23 defines the key parameters in the COM configuration file. It uses the standard COM notations. Note that all the TX and RX equalization settings follow the *USB4* specification.

Table 3-23 Key Parameters in COM Configuration File

Parameter	Setting	Unit	Information
f_b	20	GBd	USB4 Gen 3 data rate
C_d	[0 0]	nF	TX and RX capacitive loading. It is set to zeros as the die-loading is treated as part of the channel
R_d	[42.5 42.5]	Ohm	TX and RX termination resistance
ffe_preset	Table 3-4 of *USB4* Specification		TX equalization presets
g_DC	[-9:1:0]	dB	CTLE DC gain
f_p1	5	GHz	CTLE pole 1
f_p2	10	GHz	CTLE pole 2
f_z	3.55	GHz	CTLE zero
A_v	0.4	V	Signal swing
A_fe	0.4	V	FEXT aggressor swing
A_ne	0.6	V	NEXT aggressor swing
N_b	1		Number of DFE tap

Parameter	Setting	Unit	Information
b_max(1)	0.7		DFE bound, ratio to cursor
Sigma_RJ	0.01	UI	TX random jitter, rms.
A_DD	0.085	UI	TX deterministic jitter, mean-to-peak
DER_0	1e-12		Target raw bit-error-rate
eta_0	3.3e-8	V^2/GHz	One sided noise spectral density
SNR_TX	40	dB	TX signal to noise ratio
COM Threshold	3	dB	Pass/fail criterion

To support the calculation of the cable assembly COM, the following collaterals is provided and may be obtained from USB-IF website:

- Reference host/device S-parameter models
- Reference TX and RX die-loading S-parameter models
- COM configuration file
- Tool to compute COM

3.7.2.6 Low-Speed Signal Requirements (Normative)

This section specifies the electrical requirements for CC and SBU wires and the coupling among CC, USB D+/D−, VBUS and SBU.

The CC and SBU wires may be unshielded or shielded and shall have the properties specified in Table 3-24.

Table 3-24 Electrical Requirements for CC and SBU wires

Name	Description	Min	Max	Units
zCable_CC	Cable characteristic impedance on the CC wire	32	93	Ω
rCable_CC	Cable DC resistance on the CC wire		15	Ω
tCableDelay_CC	Cable propagation delay on the CC wire		26	ns
cCablePlug_CC	Capacitance for each cable plug on the CC wire		25	pF
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wires		26	ns
rCable_SBU	DC resistance of SBU wires in the cable		5	Ω
SBU SE Insertion Loss	Cable SBU single-ended insertion loss		2.0 @ 0.5 MHz 4.0 @ 1 MHz 9.0 @ 10 MHz 10.7 @ 25 MHz 11.9 @ 50 MHz 13.0 @ 100 MHz	dB

Coupling or crosstalk, both near-end and far-end, among the low speed signals shall be controlled. Table 3-25 shows the matrix of couplings specified.

Table 3-25 Coupling Matrix for Low Speed Signals

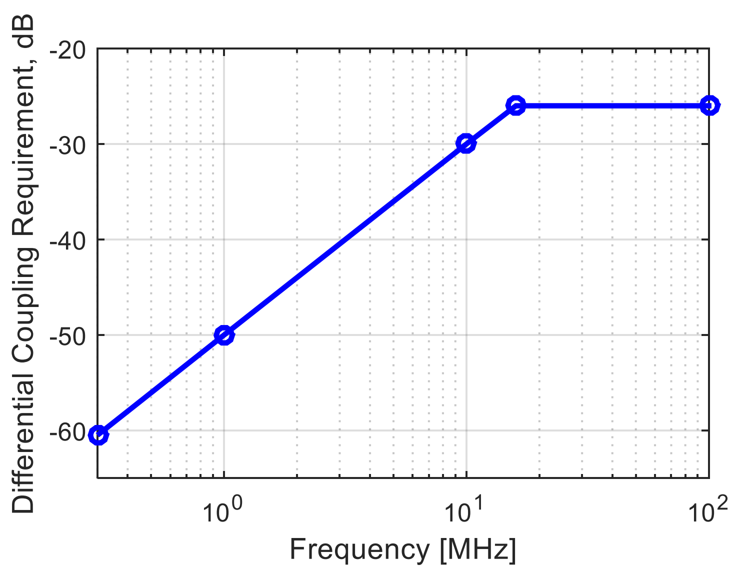
Coupling Matrix	D− (SE)	D+/D− (DF)	VBUS	SBU_B/SBU_A (SE)
CC	FF, CT	FF, CT	FF, CT, CTVPD	FF
D+/D− (DF)	N/A	N/A	FF, CT	FF
SBU_A/SBU_B	N/A	FF	FF	FF

DF: Differential; FF: Full-featured cable; CT: Charge-through cable (including USB 2.0 function); CTVPD: Charge-Through VCONN-Powered USB Device.

3.7.2.6.1 CC to USB D+/D− (Normative)

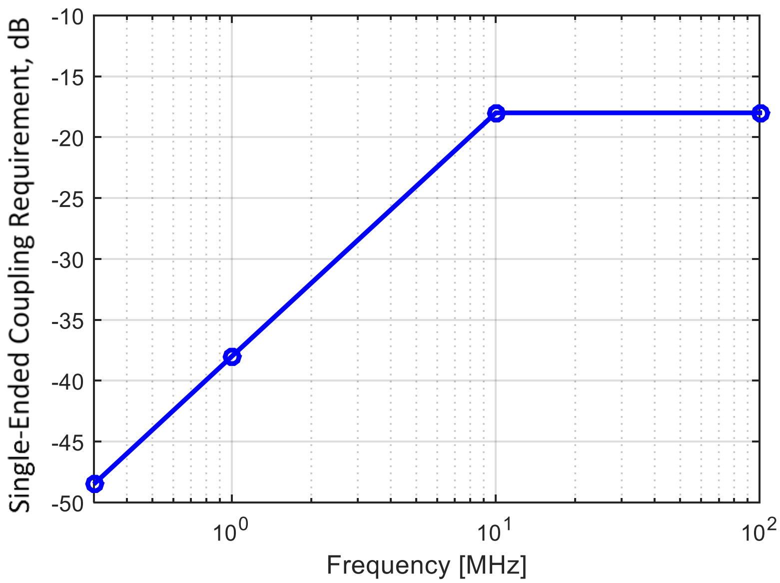
The differential coupling between the CC and D+/D− shall be below the limit shown in Figure 3-50. The limit is defined with the vertices of (0.3 MHz, -60.5 dB), (1 MHz, −50 dB), (10 MHz, −30 dB), (16 MHz, −26 dB) and (100 MHz, −26 dB).

Figure 3-50 Requirement for Differential Coupling between CC and D+/D−



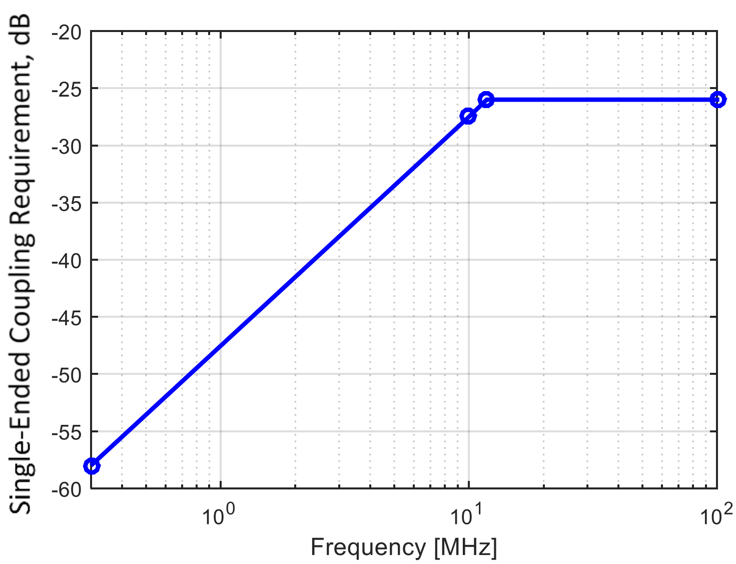
For USB 2.0 Type-C cables, the singled-ended coupling between the CC and D− shall be below the limit shown in Figure 3-51. The limit is defined with the vertices of (0.3 MHz, −48.5 dB), (1 MHz, −38 dB), (10 MHz, −18 dB) and (100 MHz, −18 dB).

Figure 3-51 Requirement for Single-Ended Coupling between CC and D− in USB 2.0 Type-C Cables



For USB Full-Featured Type-C cables, the singled-ended coupling between the CC and D− shall be below the limit shown in Figure 3-52. The limit is defined with the vertices of (0.3 MHz, −58 dB), (10 MHz, −27.5 dB), (11.8 MHz, −26 dB) and (100 MHz, −26 dB).

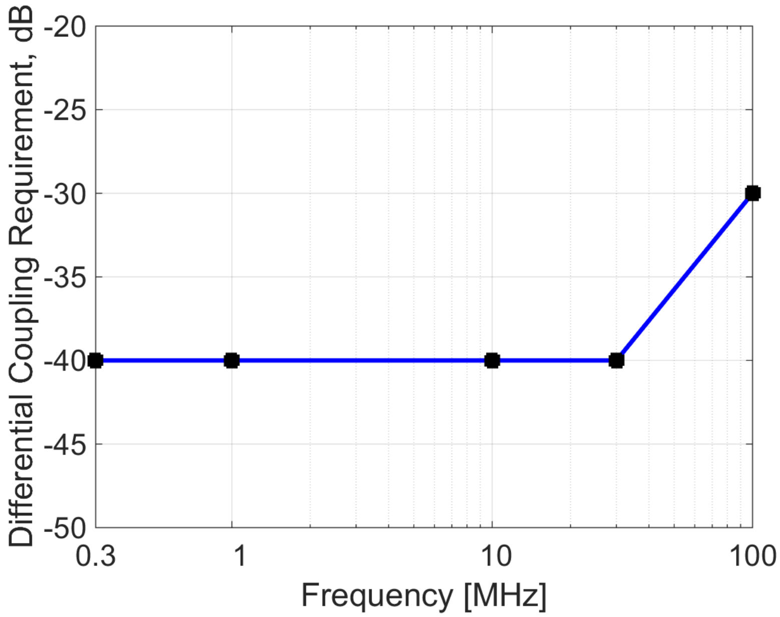
Figure 3-52 Requirement for Single-Ended Coupling between CC and D− in USB Full-Featured Type-C Cables



3.7.2.6.2 VBUS Coupling to SBU_A/SBU_B, CC, and USB D+/D− (Normative)

The differential coupling between VBUS and USB D+/D− shall be less than the limit shown in Figure 3-53. The limit is defined by the following vertices: (0.3 MHz, −40 dB), (1 MHz, −40 dB), (30 MHz, −40 dB), and (100 MHz, −30 dB).

Figure 3-53 Requirement for Differential Coupling between VBUS and D+/D−



The maximum VBUS loop inductance shall be 900 nH and the maximum mutual inductance (M) between VBUS and low speed signal lines (CC, SBU_A, SBU_B, D+, D−) shall be as specified in Table 3-26 to limit VBUS inductive noise coupling on low speed signal lines. For full-featured cables, the range of VBUS bypass capacitance shall be 8nF up to 500nF as any of the values in the range is equally effective for high-speed return-path bypassing.

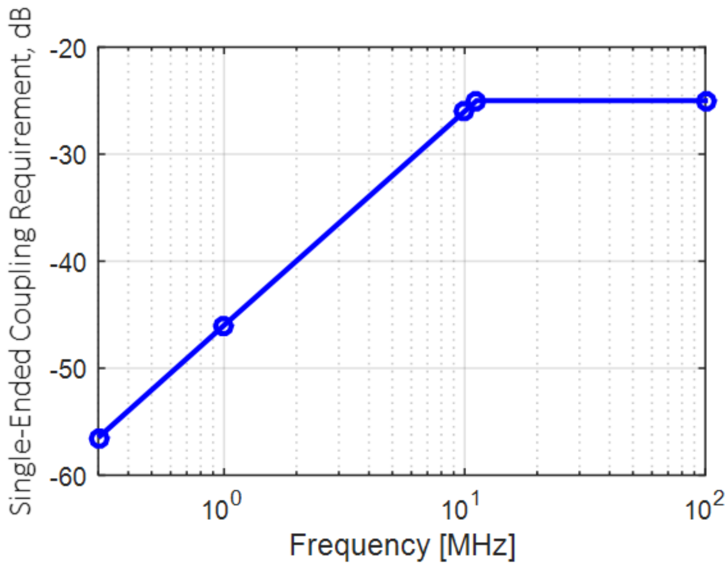
Table 3-26 Maximum Mutual Inductance (M) between VBUS and Low Speed Signal Lines

Low Speed Wire	Max Mutual Inductance (nH)
CC	350
SBU_A, SBU_B	330
D+, D−	330

3.7.2.6.3 Coupling between SBU_A and SBU_B (Normative)

The single-ended coupling between SBU_A and SBU_B shall be less than the limit shown in Figure 3-54. The limit is defined with the vertices of (0.3 MHz, −56.5 dB), (1 MHz, −46 dB), (10 MHz, −26 dB), (11.2 MHz, −25 dB), and (100 MHz, −25 dB).

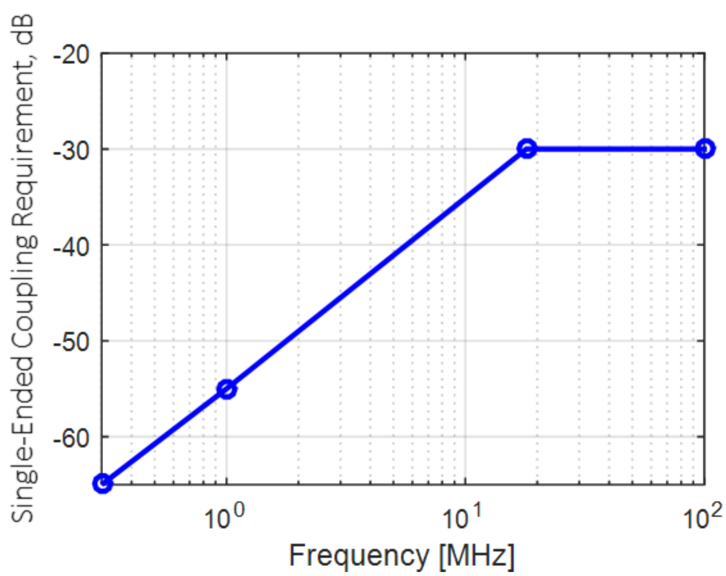
Figure 3-54 Requirement for Single-Ended Coupling between SBU_A and SBU_B



3.7.2.6.4 Coupling between SBU_A/SBU_B and CC (Normative)

The single-ended coupling between SBU_A and CC, and between SBU_B and CC shall be less than the limit shown in Figure 3-55. The limit is defined with the vertices of (0.3 MHz, −65 dB), (1 MHz, −55 dB), (18 MHz, −30 dB), and (100 MHz, −30 dB).

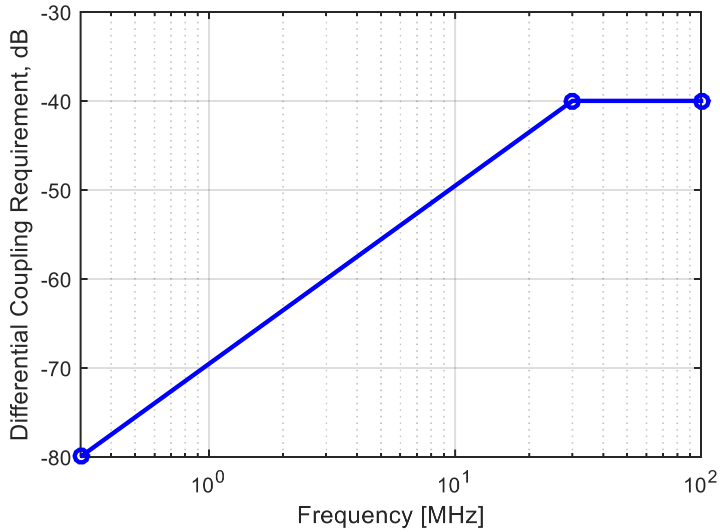
Figure 3-55 Requirement for Single-Ended Coupling between SBU_A/SBU_B and CC



3.7.2.6.5 Coupling between SBU_A/SBU_B and USB D+/D− (Normative)

The coupling between SBU_A and differential D+/D−, and between SBU_B and differential D+/D− shall be less than the limit shown in Figure 3-56. The limit is defined with the vertices of (0.3 MHz, −80 dB), (30 MHz, −40 dB), and (100 MHz, −40 dB).

Figure 3-56 Requirement for Coupling between SBU_A and differential D+/D−, and SBU_B and differential D+/D−



3.7.2.7 USB D+/D− Signal Requirements (Normative)

The USB D+/D− lines of the USB Type-C to USB Type-C passive cable assembly shall meet the requirements defined in Table 3-27.

Table 3-27 USB D+/D− Signal Integrity Requirements for USB Type-C to USB Type-C Passive Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	26 ns max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	3.5 ohms max.

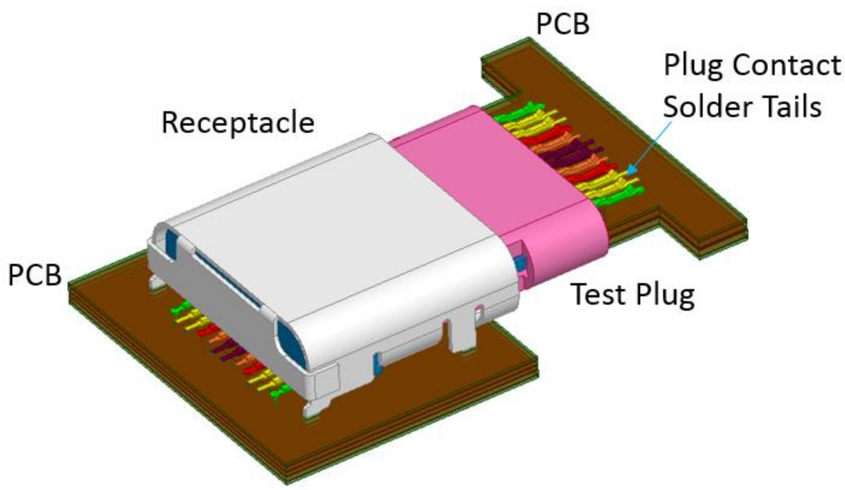
3.7.2.8 VBUS DC Voltage Tolerance (Normative)

A USB Type-C to USB Type-C cable assembly shall tolerate a VBUS voltage of 21 V DC at the cable rated current (i.e. 3 A or 5 A) applied for one hour as a pre-condition of the testing of the electrical aspects of the cable assembly.

3.7.3 Mated Connector (Informative – USB 3.2 Gen2 and USB4 Gen2)

The mated connector as defined in this specification for USB Type-C consists of a receptacle mounted on a PCB, representing how the receptacle is used in a product, and a test plug also mounted on a PCB (paddle card) without cable. This is illustrated in Figure 3-57. Note that the test plug is used in host/device TX/RX testing also.

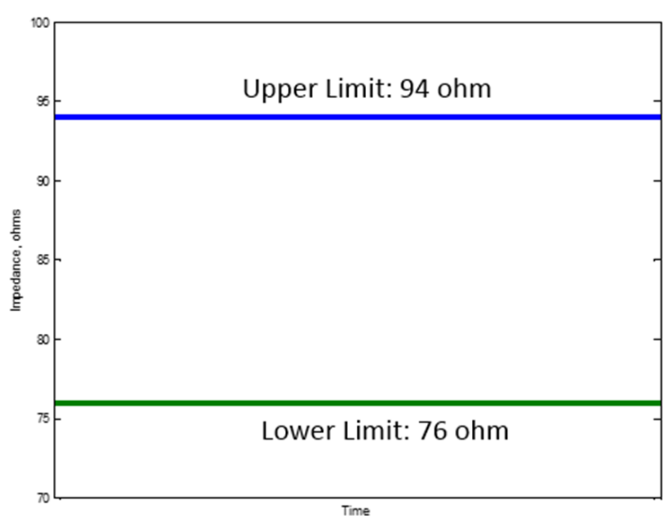
Figure 3-57 Illustration of USB Type-C Mated Connector



3.7.3.1 Differential Impedance (Informative)

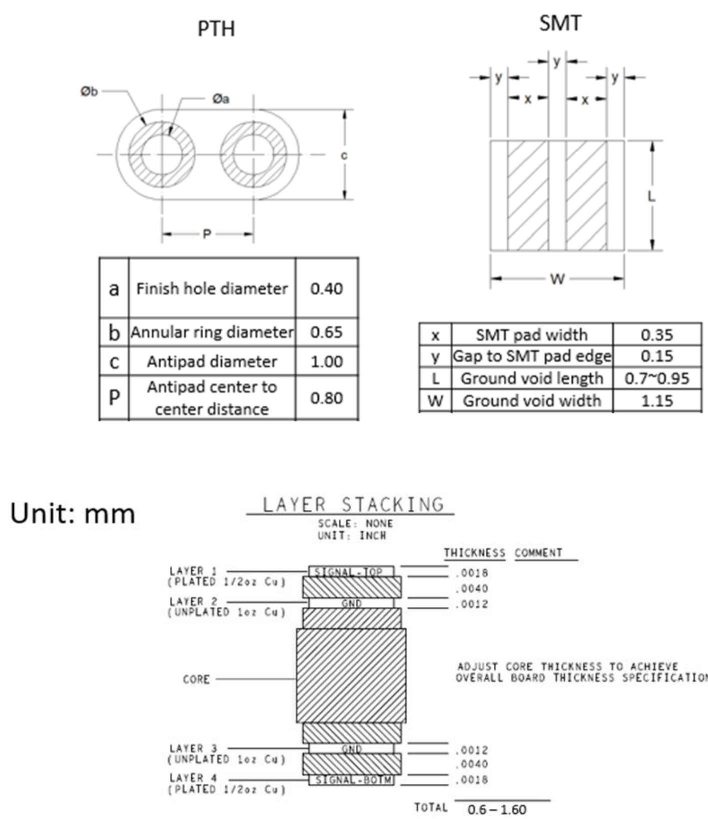
The mated connector impedance target is specified to minimize reflection from the connector. The differential impedance of a mated connector should be within 85 Ω ± 9 Ω, as seen from a 40 ps (20% – 80%) rise time. The impedance profile of a mated connector should fall within the limits shown in Figure 3-58.

Figure 3-58 Recommended Impedance Limits of a USB Type-C Mated Connector



The PCB stack up, lead geometry, and solder pad geometry should be modeled in 3D field-solver to optimize electrical performance. Example ground voids under signal pads are shown in Figure 3-59 based on pad geometry, mounting type, and PCB stack-up shown.

Figure 3-59 Recommended Ground Void Dimensions for USB Type-C Receptacle



3.7.3.2 Mated Connector Recommended Differential S-Parameter and Signal Integrity Characteristics (Informative)

The recommended signal integrity characteristics of USB Type-C mated connector pair are listed in Table 3-28.

Table 3-28 USB Type-C Mated Connector Recommended Signal Integrity Characteristics (Informative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at the TX/RX Gen1, Gen2 and Gen3 generation Nyquist frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}} \lvert ILD(f)\rvert^2 \lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}} \lvert Vin(f)\rvert^2 df}}\right)$	≤ −40 dB ≤ −39 dB (with fmax = 20 GHz and Vin(f) defined with Tb (UI) = 50 ps; USB4 Gen3)

Items	Descriptions and Procedures	Requirements
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2+0.125^2\cdot\lvert C2D(f)\rvert^2)df+\int_0^{fmax}\lvert Vdd(f)\rvert^2\ \lvert NEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = NEXT between TX/RX pairs *NEXTd* = NEXT between D+/D− and TX/RX pairs	≤ −44 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2+0.125^2\cdot\lvert C2D(f)\rvert^2)df+\int_0^{fmax}\lvert Vdd(f)\rvert^2\ \lvert FEXTd(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = FEXT between TX/RX pairs *FEXTd* = FEXT between D+/D− and TX/RX pairs	≤ −44 dB
Differential Crosstalk of TX/RX on D+/D−	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors.	See Figure 3-60
Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors.	See Figure 3-60
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −18 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	See Figure 3-61

Note: *fmax* = 12.5 GHz (unless otherwise specified);

Vin(f) is defined in Figure 3-40 with Tb (UI) = 100 ps (unless otherwise specified);

Vdd(f) is also defined in Figure 3-40 with Tb (UI) = 2.08 ns.

C2D(f) =measured near-end and far-end crosstalk between TX/RX pairs, and the common-mode-to-differential conversion, respectively. The factor of 0.125^2 accounts for the assumption that the common mode amplitude is 12.5% of the differential amplitude.

Figure 3-60 Recommended Differential Near-End and Far-End Crosstalk Limits between D+/D− Pair and TX/RX Pairs

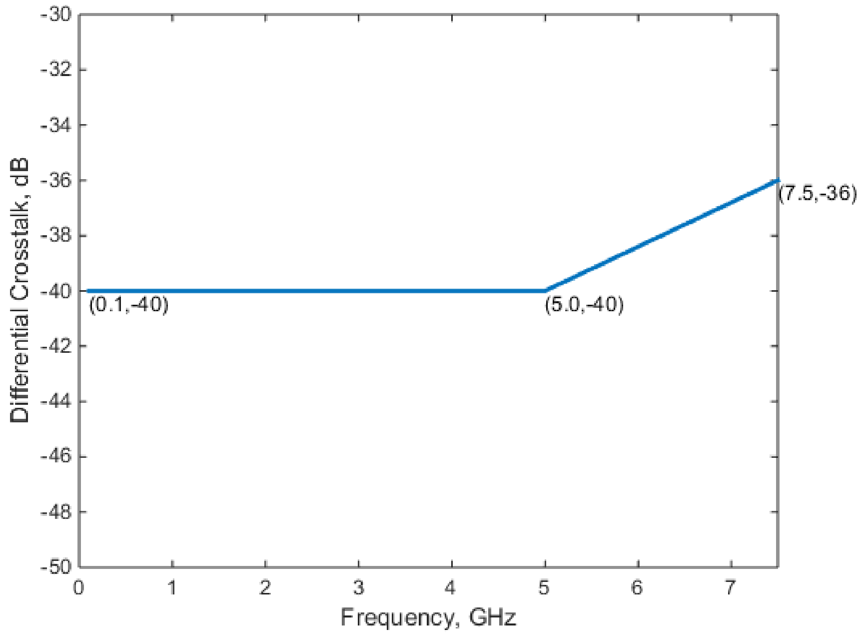
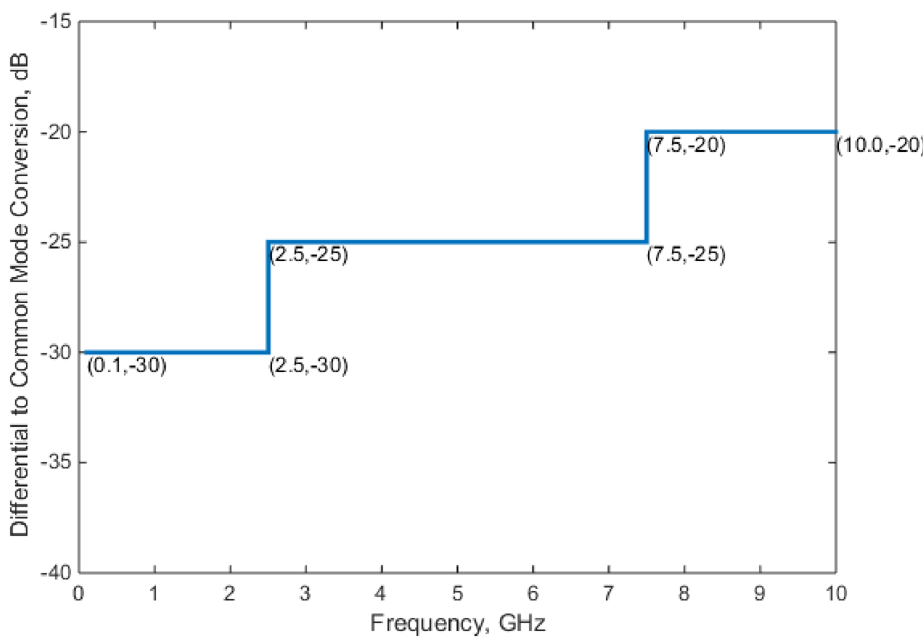


Figure 3-61 Recommended Limits for Differential-to-Common-Mode Conversion



3.7.4 Receptacle Connector SI Requirements and Testing (Normative – USB4 Gen3)

The USB Type-C receptacle connector requirements for *USB4* Gen3 are normative and listed in Table 3-29. Unless otherwise specified, the items to be specified are identical to what is defined in Section 3.7.3 and the parameters used to calculate the integrated parameters are the same as defined in Section 3.7.2.4 for the *USB4* Gen3 cable assembly.

Table 3-29 USB Type-C Receptacle Connector Signal Integrity Characteristics for USB4 Gen3 (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at a few different frequencies.	≥ −0.6 dB @ 2.5 GHz ≥ −0.8 dB @ 5.0 GHz ≥ −1.0 dB @ 10 GHz ≥ −1.25 dB @ 12.5 GHz ≥ −1.5 dB @ 15 GHz
Integrated Differential Near-end Crosstalk on TX/RX (INEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = NEXT between TX1and RX1, and TX2 and RX2.	≤ −43 dB
Integrated Differential Far-end Crosstalk on TX/RX (IFEXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = FEXT between TX1 and RX1, and TX2 and RX2.	≤ −43 dB
Differential Crosstalk of TX/RX on D+/D− Differential Crosstalk of D+/D− on TX/RX	The differential near-end and far-end crosstalk of the TX/RX pairs on the D+/D− pair in mated connectors, and the differential near-end and far-end crosstalk of the D+/D− pair on the TX/RX pairs in mated connectors. $dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert FEXT(f)\rvert^2+\lvert NEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *FEXT* = Far-end crosstalk between TX/RX and D+/D− pairs *NEXT* = Near-end crosstalk between TX/RX and D+/D− pairs *fmax* = 1.2 GHz	≤ −50 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −15 dB
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB

Note: *fmax* = 20 GHz (unless otherwise specified);
Vin(f) is defined with Tb (UI) = 50 ps.

The requirements defined in this section do not apply to the USB Type-C plug connector, as the limits Table 3-29 factor in the electrical characteristics of test fixture that includes a USB Type-C plug connector specifically selected for testing of the USB Type-C receptacle. The USB Type-C plug connector does not have a set of requirements defined at the mated connector level as there are tradeoffs allowed to achieve acceptable performance at the finished cable assembly level.

3.7.5 USB Type-C to Legacy Cable Assemblies (Normative)

The USB Type-C to legacy cable assemblies may support USB 2.0 only or USB 3.2 Gen2; USB 3.2 Gen1-only Type-C to legacy cable assemblies are not allowed.

3.7.5.1 USB 2.0-only Cable Assemblies (Normative)

The *USB 2.0*-only Type-C to legacy USB cable assemblies include:

- USB Type-C plug to *USB 2.0* Standard-A plug
- USB Type-C plug to *USB 2.0* Standard-B plug
- USB Type-C plug to *USB 2.0* Micro-B plug
- USB Type-C plug to *USB 2.0* Mini-B plug

The USB D+/D− signal integrity requirements are specified in Table 3-30.

Table 3-30 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Cable Assemblies

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the cable assembly have the proper impedance. For the entire cable assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Propagation Delay	EIA 364-103 The purpose of the test is to verify the end-to-end propagation of the D+/D− lines of the cable assembly.	10 ns max for USB Type-C to Micro-B cable assembly; 20 ns max for all other USB Type-C to legacy USB cable assemblies. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of cable assembly arrive at the receiver at the same time.	100 ps max. 400 ps rise time (20%-80%).
D+/D− Pair Attenuation	EIA 364 – 101 This test ensures the D+/D− pair of a cable assembly is able to provide adequate signal strength to the receiver in order to maintain a low error rate.	≥ −1.02 dB @ 50 MHz ≥ −1.43 dB @ 100 MHz ≥ −2.40 dB @ 200 MHz ≥ −4.35 dB @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	3.5 ohms max.

3.7.5.2 *USB 3.1* Gen2 Cable Assemblies (Normative)

The USB Type-C to *USB 3.1* Gen2 legacy cable assemblies include:

- USB Type-C plug to *USB 3.1* Standard-A plug
- USB Type-C plug to *USB 3.1* Standard-B plug
- USB Type-C plug to *USB 3.1* Micro-B plug

The informative design targets for these cables are provided in Table 3-31.

Table 3-31 Design Targets for USB Type-C to USB 3.1 Gen2 Legacy Cable Assemblies (Informative)

Items	Design Targets
Differential Impedance	76 ohms min and 96 ohms max. 40 ps rise time (20%-80%).
Differential Insertion Loss	≥ −2 dB @ 100 MHz ≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥−3.5 dB @ 2.5 GHz −6.0 dB max @ 5.0 GHz
Differential NEXT between SuperSpeed Pairs	≤ −34 dB to 5 GHz
Differential NEXT and FEXT between D+/D- and SuperSpeed Pairs	≤ −30 dB to 5 GHz

The normative requirements include the USB D+/D− signaling as specified in Table 3-30, and the SuperSpeed USB parameters specified in Table 3-32.

Table 3-32 USB Type-C to USB 3.1 Gen2 Legacy Cable Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)	ILfitatNq is evaluated at both the SuperSpeed Gen1 and Gen2 Nyquist frequencies.	≥ −4 dB @ 2.5 GHz, except for the USB Type-C plug to USB 3.1 Standard-A plug cable assembly which is ≥ −3.5 dB @ 2.5 GHz ≥ −6.0 dB at 5.0 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert ILD(f)\rvert^2 \lvert Vin(f)\rvert^2 df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 21.392$ See Figure 3-62.
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}(\lvert Vin(f)\rvert^2 \lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2 \lvert NEXTd(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXTs* = NEXT between SuperSpeed pairs *NEXTd* = NEXT between D+/D− and SuperSpeed pairs *Vdd(f)* = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −38 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$ where: *NEXT* = Near-end crosstalk from SuperSpeed to D+/D− *FEXT* = Far-end crosstalk from SuperSpeed to D+/D− *fmax* = 1.2 GHz	≤ −28.5 dB

Items	Descriptions and Procedures	Requirements
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{fmax}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{fmax}\lvert Vin(f)\rvert^2 df}}\right)$	$\leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 9.784$ See Figure 3-63.
Differential to Common Mode Conversion (SCD12 and SCD21)	The differential to common mode conversion is specified to control the injection of common mode noise from the cable assembly into the host or device. Frequency range: 100 MHz ~ 10.0 GHz	≤ −20 dB

Note: *fmax* = 10 GHz (unless otherwise specified); *Vin(f)* is defined in Figure 3-40 with Tb (UI) = 100 ps; and *Vdd(f)* is also defined in Figure 3-40 with Tb (UI) = 2.08 ns.

Figure 3-62 IMR Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly

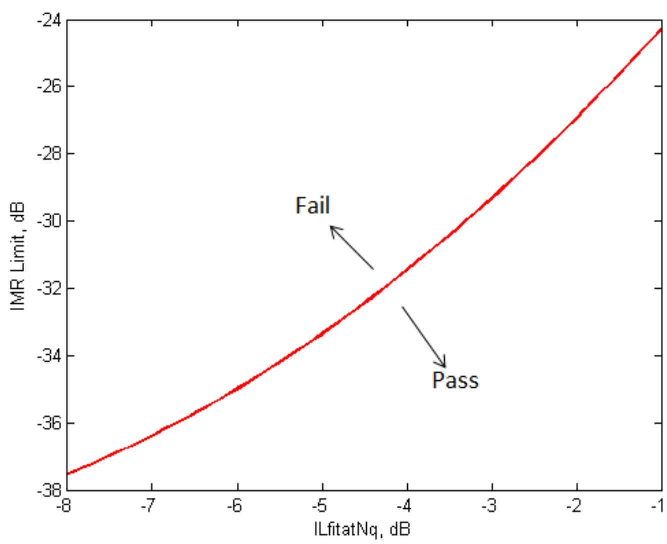
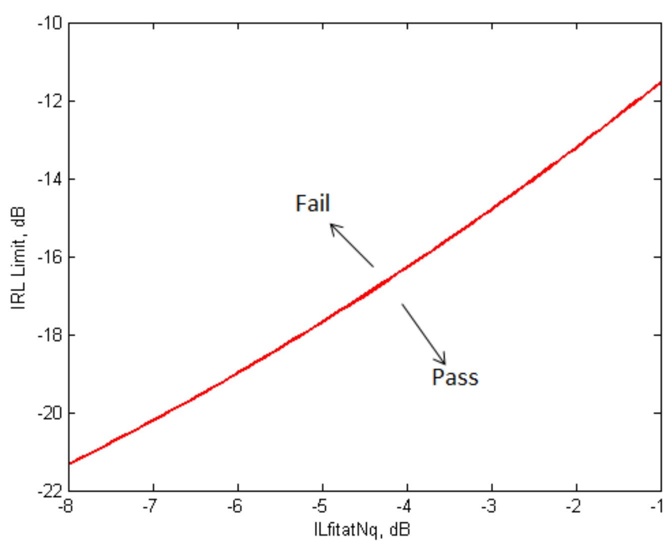


Figure 3-63 IRL Limit as Function of ILfitatNq for USB Type-C to Legacy Cable Assembly



3.7.5.3 Compliant USB Legacy Plugs used in USB Type-C to Legacy Cable Assemblies

The following requirements are incremental to the existing requirements for legacy connectors when used in compliant USB Type-C to legacy cable assemblies.

3.7.5.3.1 Contact Material Requirements for USB Type-C to USB Micro-B Assemblies

For USB Type-C to USB Micro-B assemblies, change the contact material in the USB Micro-B connector to achieve the following Low-Level Contact Resistance (EIA 364-23B):

- 20 milliohms (Max) initial for VBUS and GND contacts,
- Maximum change (delta) of +10 milliohms after environmental stresses.

3.7.5.3.2 Contact Current Ratings for USB Standard-A, USB Standard-B and USB Micro-B Connector Mated Pairs (EIA 364-70, Method 2)

When a current of 3 A is applied to the VBUS pin and its corresponding GND pin (i.e., pins 1 and 4 in a USB Standard-A or USB Standard-B connector or pins 1 and 5 in a USB Micro-B connector), the delta temperature shall not exceed +30° C at any point on the connectors under test, when measured at an ambient temperature of 25° C.

3.7.6 USB Type-C to USB Legacy Adapter Assemblies (Normative)

Only the following standard legacy adapter assemblies are defined:

- *USB 2.0* Type-C plug to *USB 2.0* Micro-B receptacle
- USB Full-Featured Type-C plug to *USB 3.1* Standard-A receptacle

3.7.6.1 USB 2.0 Type-C Plug to *USB 2.0* Micro-B Receptacle Adapter Assembly (Normative)

This adapter assembly supports only the *USB 2.0* signaling. It shall not exceed 150 mm total length, measured from end to end. Table 3-33 defines the electrical requirements.

Table 3-33 USB D+/D− Signal Integrity Requirements for USB Type-C to Legacy USB Adapter Assemblies (Normative)

Items	Descriptions and Procedures	Requirements
Differential Impedance	EIA 364-108 This test ensures that the D+/D− lines of the adapter assembly have the proper impedance. For the entire adaptor assembly.	75 ohms min and 105 ohms max. 400 ps rise time (20%-80%).
Intra-pair Skew	EIA 364 – 103 This test ensures that the signal on both the D+ and D− lines of adapter assembly arrive at the receiver at the same time.	20 ps max. 400 ps rise time (20%-80%).
Differential Insertion Loss	EIA 364 – 101 This test ensures the D+/D− pair of an adapter assembly can provide adequate signal strength to the receiver.	−0.7 dB max @ 400 MHz
D+ or D− DC Resistance	This test ensures the D+/D− has the proper DC resistance range in order to predict the EOP level and set the *USB 2.0* disconnect level.	2.5 ohms max.

3.7.6.2 USB Full-Featured Type-C Plug to *USB 3.1* Standard-A Receptacle Adapter Assembly (Normative)

The USB Full-Featured Type-C plug to *USB 3.1* Standard–A receptacle adapter assembly is intended to be used with a direct-attach device (e.g., USB thumb drive). A system is not guaranteed to function when using an adapter assembly together with a Standard USB cable assembly.

To minimize the impact of the adapter assembly to system signal integrity, the adapter assembly should meet the informative design targets in Table 3-34.

Table 3-34 Design Targets for USB Type-C to *USB 3.1* Standard-A Adapter Assemblies (Informative)

Items	Design Targets
Differential Return Loss	≤ −15 dB to 5 GHz Normalized with 85 ohms.
Differential Insertion Loss	≥ −2.4 dB to 2.5 GHz, ≥ −3.5 dB to 5 GHz
Differential NEXT between SuperSpeed Pairs	≤ −40 dB to 2.5 GHz ≤ −34 dB at 5 GHz
Differential NEXT and FEXT between D+/D− and SuperSpeed Pairs	≤ −30 dB to 2.5 GHz

The normative requirements for the adapter assembly are defined in Table 3-33 and Table 3-35. The adapter assembly total length is limited to 150 mm max.

Table 3-35 USB Type-C to USB 3.1 Standard-A Receptacle Adapter Assembly Signal Integrity Requirements (Normative)

Items	Descriptions and Procedures	Requirements
Differential Insertion Loss Fit at Nyquist Frequency (ILfitatNq)	ILfitatNq is evaluated at the SuperSpeed Gen1 Nyquist frequency.	≥ −2.4 dB at 2.5 GHz ≥ −3.5 dB at 5 GHz
Integrated Differential Multi-reflection (IMR)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert ILD(f)\rvert^2\lvert Vin(f)\rvert^2 df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −38 dB, Tb = 200 ps ≤ −27 dB, Tb = 100 ps
Integrated Differential Crosstalk on SuperSpeed (ISSXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}(\lvert Vin(f)\rvert^2\lvert NEXTs(f)\rvert^2 + \lvert Vdd(f)\rvert^2\lvert NEXTd(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXTs$ = NEXT between SuperSpeed pairs $NEXTd$ = NEXT between D+/D− and SuperSpeed pairs *Vdd(f)* = Input pulse spectrum on D+/D− pair, evaluated using equation shown in Figure 3-40 with Tb (UI) = 2.08 ns.	≤ −37 dB
Integrated Differential Crosstalk on D+/D- (IDDXT)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2(\lvert NEXT(f)\rvert^2 + \lvert FEXT(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$ where: $NEXT$ = Near-end crosstalk from SuperSpeed to D+/D− $FEXT$ = Far-end crosstalk from SuperSpeed to D+/D− f_{max} = 1.2 GHz	≤ −30 dB
Integrated Return Loss (IRL)	$dB\left(\sqrt{\frac{\int_0^{f_{max}}\lvert Vin(f)\rvert^2\lvert SDD21(f)\rvert^2(\lvert SDD11(f)\rvert^2+\lvert SDD22(f)\rvert^2)df}{\int_0^{f_{max}}\lvert Vin(f)\rvert^2 df}}\right)$	≤ −14.5 dB, Tb = 200 ps ≤ −12.0 dB, Tb = 100 ps
Diff to Comm mode	Differential to Common Mode conversion (SCD12, SCD21)	≤ −15 dB

Note: *fmax* = 7.5 GHz; *Vin(f)* is defined in Figure 3-40 with Tb (UI) = 200 ps; and *Vdd(f)* is also specified in Figure 3-40 with Tb (UI) = 2.08 ns.

3.7.6.3 Compliant USB Legacy Receptacles used in USB Type-C to Legacy Adapter Assemblies

3.7.6.3.1 Contact Material Requirements

Refer to Section 3.7.5.3.1 for contact material requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

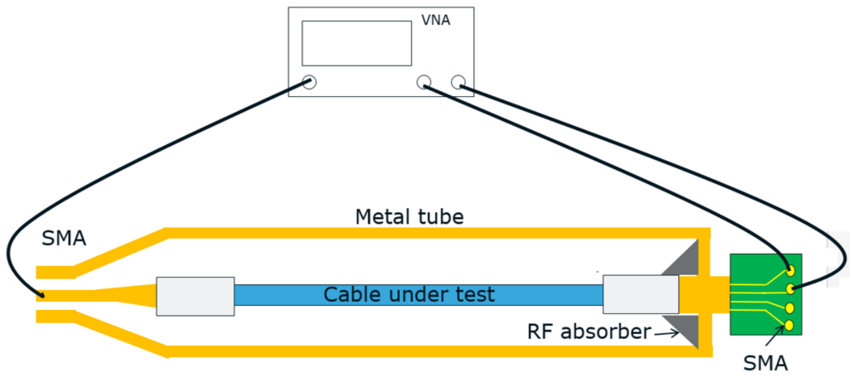
3.7.6.3.2 Contact Current Ratings

Refer to Section 3.7.5.3.2 for contact current rating requirements as these apply to legacy USB Standard-A and USB Micro-B receptacles used in USB Type-C to Legacy Adapter Assemblies.

3.7.7 Shielding Effectiveness Requirements (Normative)

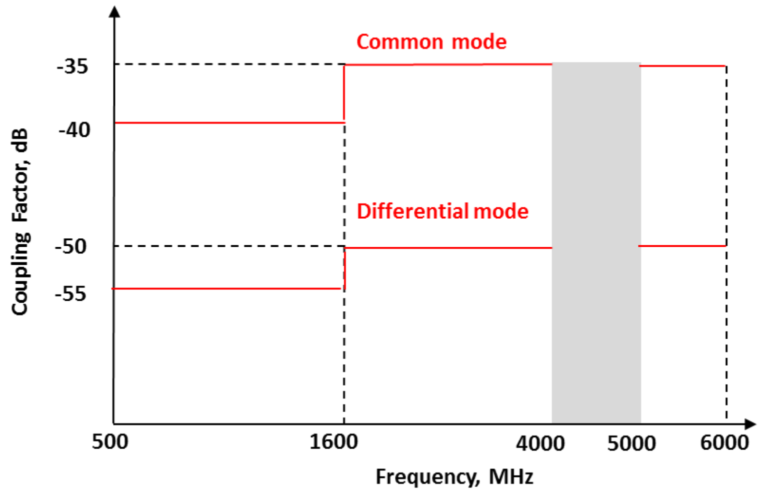
The cable assembly shielding effectiveness (SE) test measures the EMI and RFI levels from the cable assembly. To perform the measurement, the cable assembly shall be installed in the cable SE test fixture as shown in Figure 3-64. The coupling factors from the cable to the fixture are characterized with a VNA.

Figure 3-64 Cable Assembly Shielding Effectiveness Testing

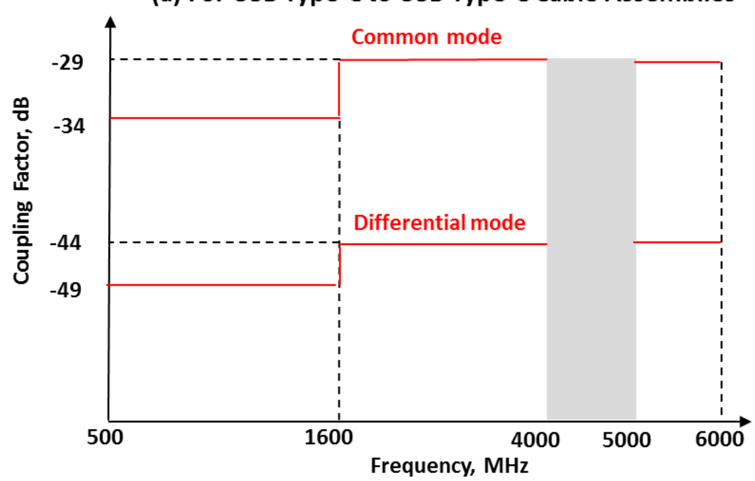


All USB Type-C cable assemblies shall pass the shielding effectiveness test for compliance. Figure 3-65 shows the pass/fail criteria for (a) USB Type-C to USB Type-C cable assemblies, (b) USB Type-C to legacy USB cable assemblies, and (c) the USB Type-C to *USB 3.1* Standard-A Receptacle Adapter assembly. Note that the shielding effectiveness for the frequency band from 4 GHz to 5 GHz is not specified since there is no antenna operating in this frequency range.

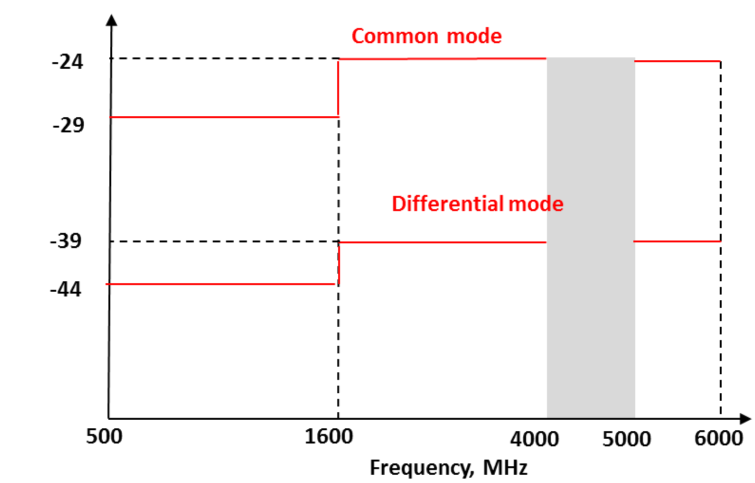
Figure 3-65 Shielding Effectiveness Pass/Fail Criteria



(a) For USB Type-C to USB Type-C Cable Assemblies



(b) For USB Type-C to legacy USB Cable Assemblies



(c) For USB Type-C to USB3.1 Standard-A Receptacle Adapter Assembly

3.7.8 DC Electrical Requirements (Normative)

Unless otherwise stated, the tests in this section are performed on mated connector pairs.

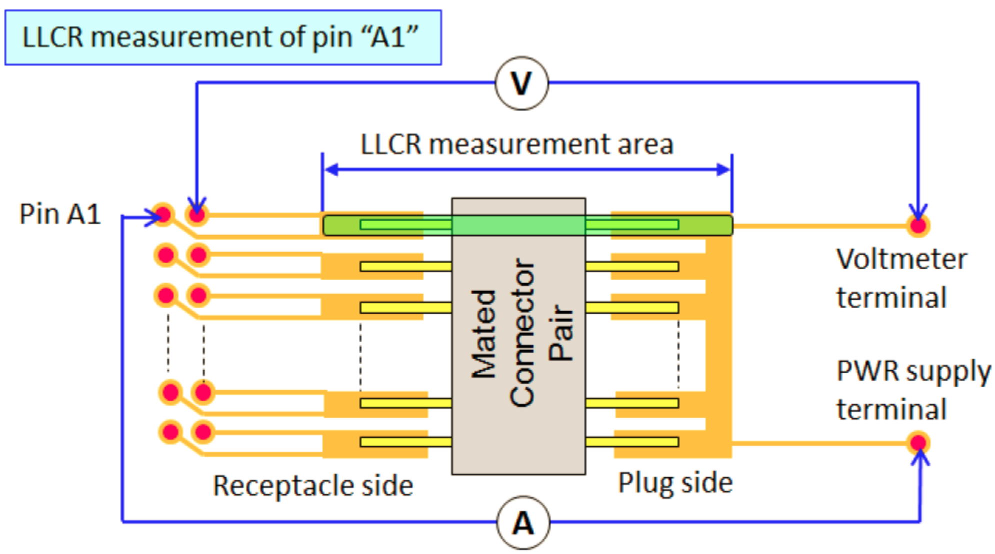
3.7.8.1 Low Level Contact Resistance (EIA 364-23B)

The low-level contact resistance (LLCR) measurement is made across the plug and receptacle mated contacts and does not include any internal paddle cards or substrates of the plug or receptacle. See Figure 3-66. The following apply to the power and signal contacts:

- 40 mΩ (Max) initial for VBUS, GND and all other contacts.
- 50 mΩ (Max) after environmental stresses.
- Measure at 20 mV (Max) open circuit at 100 mA.

Refer to Section 3.8 for environmental requirements and test sequences.

Figure 3-66 LLCR Measurement Diagram



3.7.8.2 Dielectric Strength (EIA 364-20)

No breakdown shall occur when 100 Volts AC (RMS) is applied between adjacent contacts of unmated and mated connectors.

3.7.8.3 Insulation Resistance (EIA 364-21)

A minimum of 100 MΩ insulation resistance is required between adjacent contacts of unmated and mated connectors.

3.7.8.4 Contact Current Rating

The current rating testing for the USB Type-C connector (plug and receptacle) shall be conducted per the following set up and procedures:

- A current of 5 A shall be applied collectively to VBUS pins (i.e., pins A4, A9, B4, and B9) and 1.25 A shall be applied to the VCONN pin (i.e., B5) as applicable, terminated through the corresponding GND pins (i.e., pins A1, A12, B1, and B12). A minimum current of 0.25 A shall also be applied individually to all the other contacts, as applicable. When current is applied to the contacts, the temperature of the connector pair shall be allowed to stabilize. The temperature rise of the outside shell surface of the mated pair above the VBUS and GND contacts shall not exceed 30 °C above the ambient temperature. Figure 3-67 provides an illustration of the measurement location.

- The measurement shall be done in still air.
- The connectors shall be oriented such that the accessible outer shell surface is on top and horizontal to the ground.
- The plug and receptacle may require modification to access solder tails or cable attachment points.
- Either thermocouple or thermo-imaging (preferred) method may be used for temperature measurement
- For certification, the connector manufacturer shall provide the receptacle and plug samples under test mounted on a current rating test PCB with no copper planes. A cable plug may use short wires to attach the cable attachment points together rather than using a current rating test PCB.
    - The current rating test PCBs shall be of a 2-layer construction. If 2-layer construction is not possible due to the solder tail configuration, VBUS and ground traces shall be located on the outer layers with the inner layers reserved for signal traces, as required; VCONN traces may be routed either on internal or external layers. Table 3-36 defines the requirements for the test PCB thickness and traces. The trace length applies to each PCB (receptacle PCB and plug PCB) and is from the contact terminal to the current source tie point. Figure 3-68 provides an informative partial trace illustration of the current rating test PCB.
    - If short wires are used instead of a current rating test PCB, the wire length shall not exceed 70 mm, measured from the plug contact solder point to the other end of the wire. There shall be no paddle card or overmold included in the test set-up. Each plug solder tail shall be attached with a wire with the wire gauge of AWG 36 for signals, AWG 32 for power (VBUS and VCONN), and AWG 30 for ground.

Figure 3-67 Temperature Measurement Point

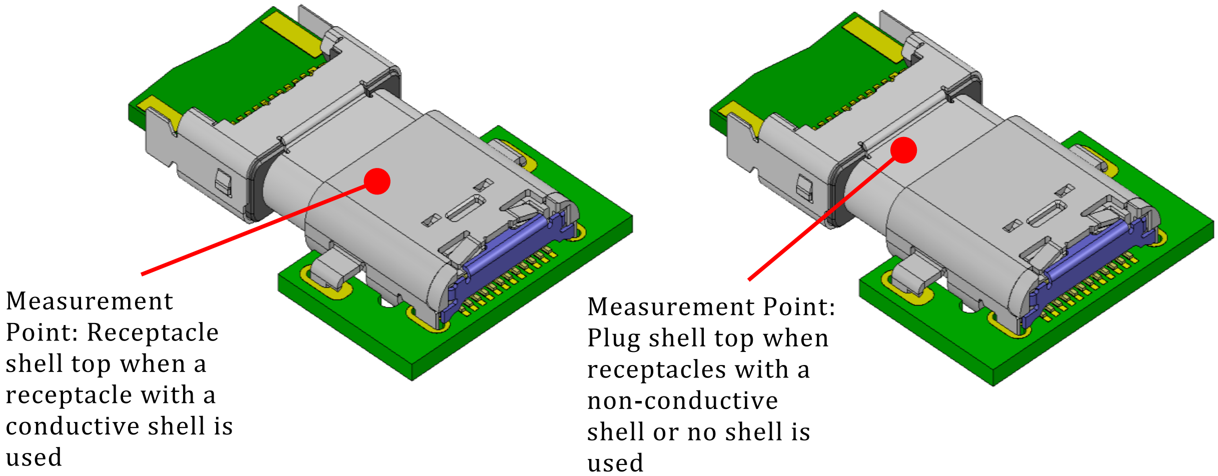
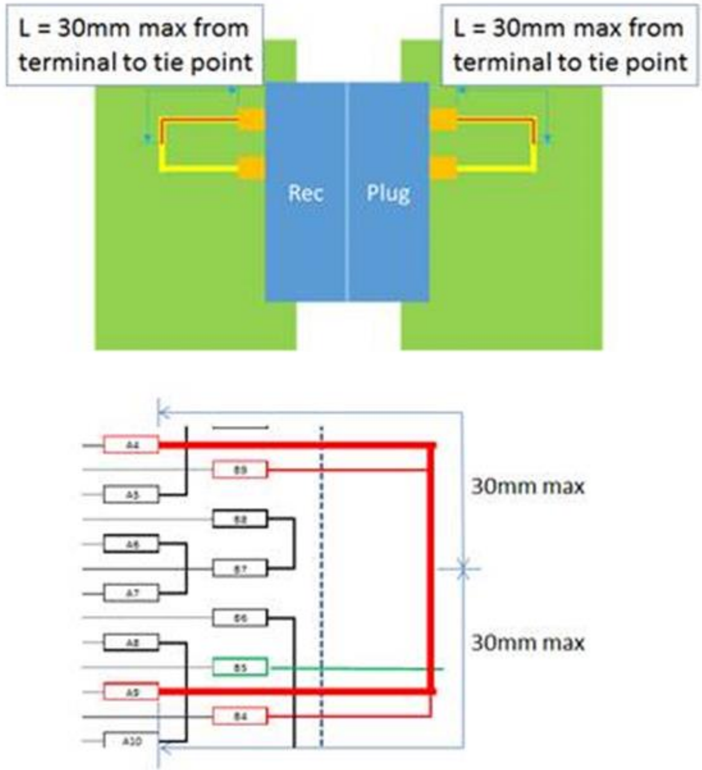


Table 3-36 Current Rating Test PCB

Item	Trace width (mm)	Trace length (mm) on each PCB	Thickness
Signal trace	0.25 max.	13 max.	35 µm (1 oz. copper)
Ground trace	1.57 max.	38 max.	35 µm (1 oz. copper)
VBUS and VCONN	1.25 max.	30 max.	35 µm (1 oz. copper)
PCB	N/A	N/A	0.80 – 1.20 mm

Figure 3-68 Example Current Rating Test Fixture Trace Configuration



3.7.8.5 DC Resistance of D+ and D−

The DC Resistance of the D+ and D− in *USB 2.0* High-Speed capable USB Type-C devices and *USB 2.0* High-Speed capable USB Type-C Captive devices shall be equal or less than the maximum value specified in Table 3-37. The D+ and D− DC Resistance is the series combination of any resistance in switches, multiplexers, and the USB PHY.

Table 3-37 Maximum DC Resistance Requirement (Normative)

	Maximum DC Resistance
USB Type-C Device (USB 2.0 High-speed capable)	19 Ω
USB Type-C Captive Device (USB 2.0 High-speed capable)	25 Ω

A USB Type-C Host operating in *USB 2.0* High-Speed mode shall implement a disconnect threshold voltage (V_{HSDSC}) level as defined in the *USB 2.0* DCR ECN.

3.8 Mechanical and Environmental Requirements (Normative)

The requirements in this section apply to all USB Type-C connectors and/or cable assemblies unless otherwise specified. For USB Type-C plug connectors and cable assemblies, the test methods are based on an assumption that the cable exits the overmold in line with mating direction to a USB Type-C receptacle (i.e., straight out the back of the overmold). For USB Type-C plug connectors and cable assemblies with the cable exiting the overmold in a different direction than straight out the back (e.g., right angle to the mating direction), test fixtures and procedures shall be modified as required to accomplish the measurement.

3.8.1 Mechanical Requirements

3.8.1.1 Insertion Force (EIA 364-13)

The initial connector insertion force shall be within the range from 5 N to 20 N at a maximum rate of 12.5 mm (0.492") per minute. This requirement does not apply when the connectors are used in a docking application.

It is recommended to use a non-silicone-based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.2 Extraction Force (EIA 364-13)

The initial connector extraction force shall be within the range of 8 N to 20 N, measured after a preconditioning of five insertion/extraction cycles (i.e., the sixth extraction). After an additional twenty-five insertion/extraction cycles, the extraction force shall be measured again (i.e., the thirty-second extraction) and the extraction force shall be:

a. within 33% of the initial reading, and
b. within the range of 8 N to 20 N.

The extraction force shall be within the range of 6 N to 20 N after 10,000 insertion/ extraction cycles. The extraction force measurement shall be performed at a maximum speed of 12.5 mm (0.492”) per minute. The extraction force requirement does not apply when the connectors are used in a mechanical docking application.

It is recommended to use a non-silicone-based lubricant on the latching mechanism to reduce wear. The effects of lubricants should be restricted to insertion and extraction characteristics and should not increase the resistance of the mated connection.

3.8.1.3 Durability or Insertion/Extraction Cycles (EIA 364-09)

The durability rating shall be 10,000 cycles minimum for the USB Type-C connector family. The durability test shall be done at a rate of 500 ± 50 cycles per hour and no physical damage to any part of the connector and cable assembly shall occur.

3.8.1.4 Cable Flexing (EIA 364-41, Condition 1)

No physical damage or discontinuity over 1ms during flexing shall occur to the cable assembly with Dimension X = 3.7 times the cable diameter and 500 cycles in each of two planes.

3.8.1.5 Cable Pull-Out (EIA 364-38, Method A)

No physical damage to the cable assembly shall occur when it is subjected to a 40 N axial load for a minimum of 1 minute while clamping one end of the cable plug.

3.8.1.6 Cable Pull-Out (EIA 364-38, Method A)

The USB Type-C connector family shall be tested for continuity under stress using a test fixture shown in Figure 3-69 or equivalent.

Figure 3-69 Example of 4-Axis Continuity Test Fixture

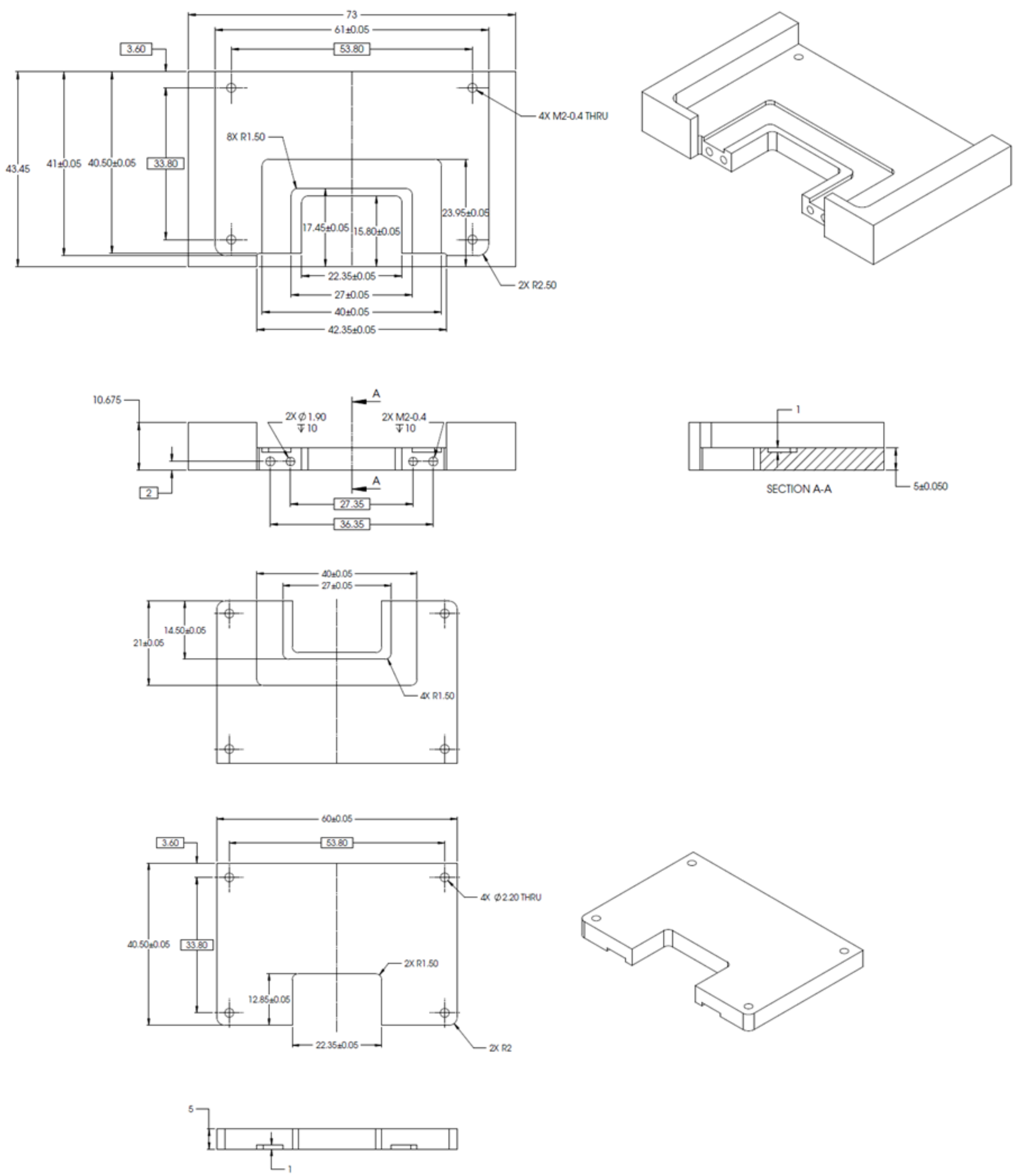
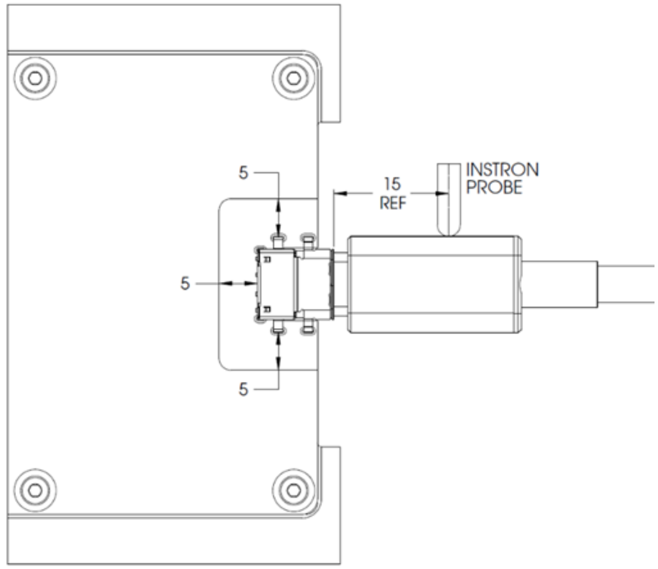


Figure 3-69 Example of 4-Axis Continuity Test Fixture, cont.



Plugs shall be supplied with a representative overmold or mounted on a 2-layer printed circuit board (PCB) between 0.8 mm and 1.0 mm thickness as applicable. A USB Type-C receptacle shall be mounted on a 2-layer PCB between 0.8 mm and 1.0 mm thickness. The PCB shall be clamped on three sides of the receptacle no further than 5 mm away from the receptacle outline. The receptacle PCB shall initially be placed in a horizontal plane, and a perpendicular moment shall be applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds at a distance of 15 mm from the mating edge of the receptacle shell in a downward direction, perpendicular to the axis of insertion. See Table 3-38 for the force and moment to be applied. Any configuration of non-conductive shell receptacles shall be tested at the values specified for the vertical receptacle configuration.

Table 3-38 Force and Moment Requirements

Receptacle configuration with respect to mounting surface	Force at 15 mm from receptacle shell mating edge (N)	Moment with respect to receptacle shell mating edge (Nm)
Right angle	20	0.30
Vertical[1]	8	0.12
Notes: 1. Any configuration of non-conductive shell receptacles shall be tested at the values specified for the vertical receptacle configuration.		

The continuity across each contact shall be measured throughout the application of the tensile force. Each non-ground contact shall also be tested to confirm that it does not short to the shell during the stresses. The PCB shall then be rotated 90 degrees such that the cable is still inserted horizontally and the tensile force in Table 3-38 shall be applied again in the downward direction and continuity measured as before. This test is repeated for 180 degree and 270 degree rotations. Passing parts shall not exhibit any discontinuities or shorting to the shell greater than 1 μs duration in any of the four orientations.

One method for measuring the continuity through the contacts is to short all the wires at the end of the cable pigtail and apply a voltage through a pull-up to each of VBUS, USB D+, USB D−, SBU, CC, and TX/RX pins, with the GND pins connected to ground.

Alternate methods are allowed to verify continuity through all pins.

3.8.1.7 Wrenching Strength

USB Type-C plugs on cable assemblies and fixture plugs without overmold (including PCB-mount USB Type-C plugs) shall be tested using the mechanical wrenching test fixture defined in the Universal Serial Bus Type-C Connectors and Cable Assemblies Compliance Document. For plug without overmold, the supplier shall provide a plug test fixture that conforms to the specified plug overmold dimensions for the USB Type-C plug (see Figure 3-70). The fixture may be metal or other suitable material. Perpendicular moments are applied to the plug with a 5 mm ball tipped probe for a period of at least 10 seconds when inserted in the test fixture to achieve the defined moments in four directions of up or down (i.e., perpendicular to the long axis of the plug opening) and left or right (i.e., in the plane of the plug opening). Compliant connectors shall meet the following force thresholds:

- A moment of 0-0.75 Nm (e.g., 50 N at 15 mm from the edge of the receptacle) is applied to a plug inserted in the test fixture in each of the four directions. A single plug shall be used for this test. Some mechanical deformation may occur. The plug shall be mated with the continuity test fixture after the test forces have been applied to verify no damage has occurred that causes discontinuity or shorting. The continuity test fixture shall provide a planar surface on the mating side located 6.20 ± 0.20 mm from the receptacle Datum A, perpendicular to the direction of insertion. No moment forces are applied to the plug during this continuity test. Figure 3-71 illustrates an example continuity test fixture to perform the continuity test. The Dielectric Withstanding Voltage test shall be conducted after the continuity test to verify plug compliance.

Figure 3-70 Example Wrenching Strength Test Fixture for Plugs without Overmold

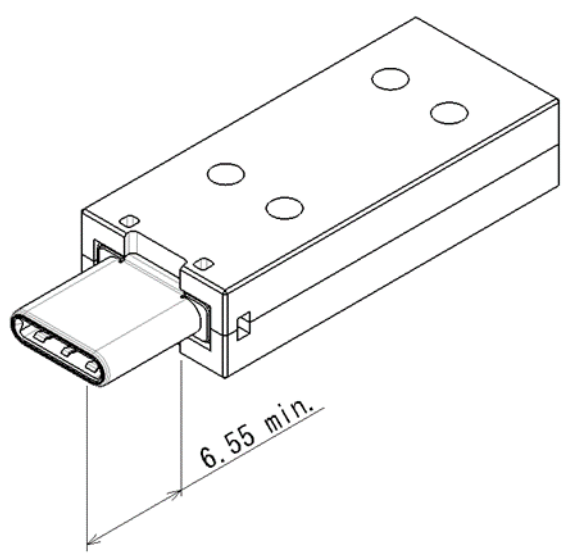
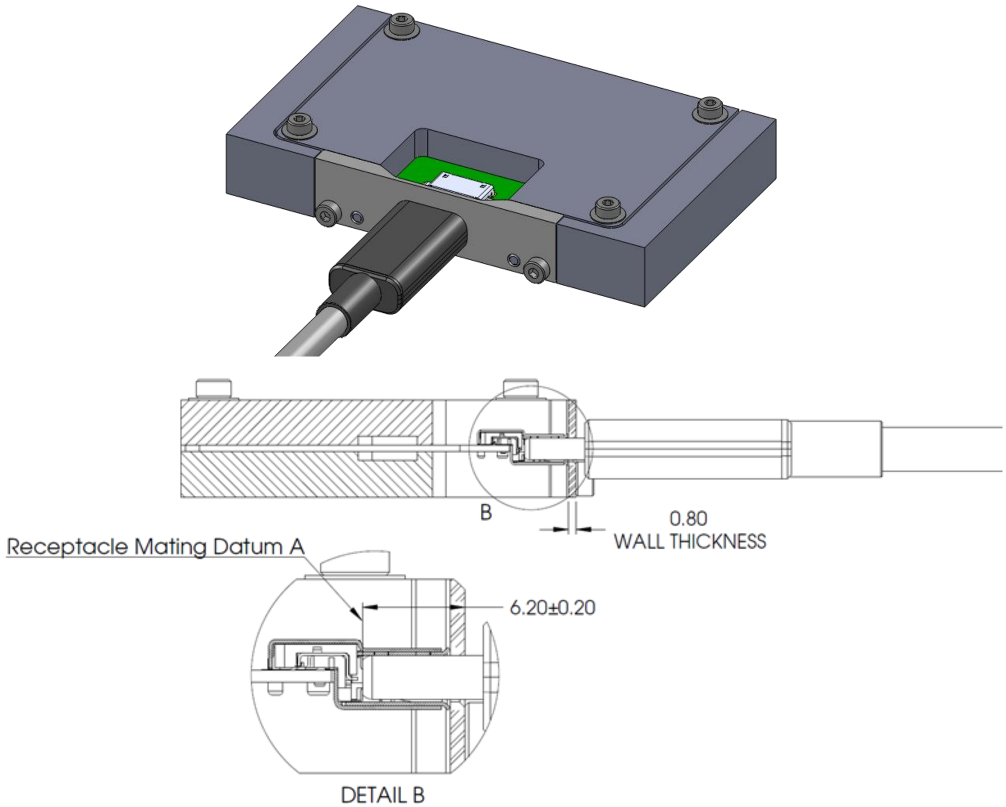


Figure 3-71 Reference Wrenching Strength Continuity Test Fixture



- The plug shall disengage from the test fixture or demonstrate mechanical failure (i.e., the force applied during the test procedure peaks and drops off) when a moment of 2.0 Nm is applied to the plug in the up and down directions and a moment 3.5 Nm is applied to the plug in the left and right directions. A new plug is required for each of the four test directions. An example of the mechanical failure point and an illustration of the wrenching test fixture are shown in Figure 3-72 and Figure 3-73, respectively.

Figure 3-72 Example of Wrenching Strength Test Mechanical Failure Point

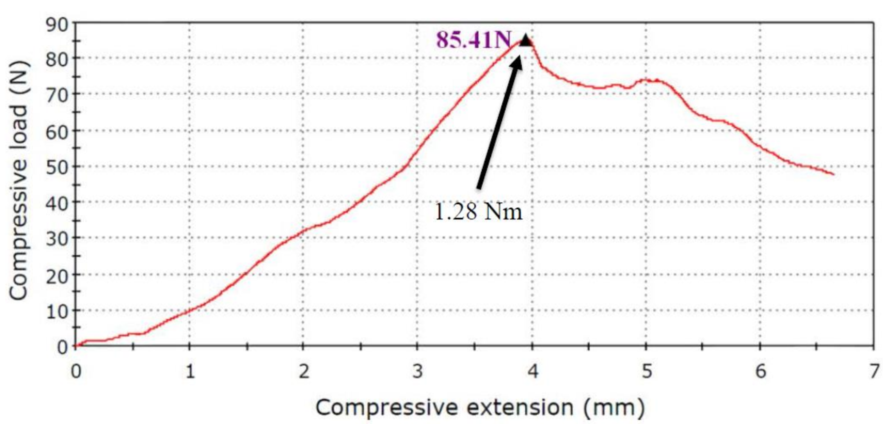
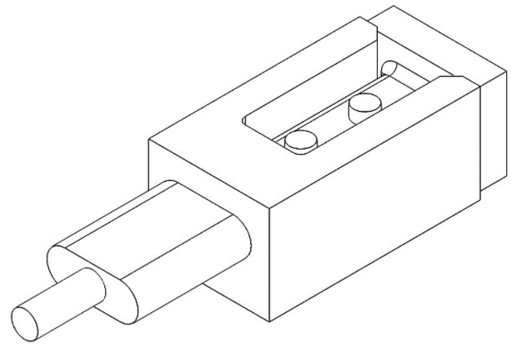


Figure 3-73 Wrenching Strength Test with Cable in Fixture



3.8.1.8 Restriction of Hazardous Substances

It is recommended that components be RoHS compliant.

3.8.2 Environmental Requirements

The connector interface environmental tests shall follow EIA 364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications.

Since the connector defined has more than 0.127 mm wipe length, Test Group 6 in EIA 364-1000.01 is not required. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA 364-1000.01 based on the field temperature per the following.

Table 3-39 Environmental Test Conditions

Temperature Life test temperature and duration	105 °C for 120 hours
Temperature Life test temperature and duration for preconditioning	105 °C for 72 hours
Mixed flowing gas test duration	7 days

The pass/fail criterion for the low-level contact resistance (LLCR) is as defined in Section 3.7.8.1. The durability ratings are defined in Section 3.8.1.3.

3.8.2.1 Reference Materials (Informative)

This specification does not specify materials for connectors and cables. Connector and cable manufacturers should select appropriate materials based on performance requirements. The information below is provided for reference only.

Note: Connector and cable manufacturers should comply with contact plating requirements per the following options:

Option I

Receptacle

Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

Plug

Contact area: (Min) 0.05 µm Au + (Min) 0.75 µm Ni-Pd on top of (Min) 2.0 µm Ni

Option II

Receptacle

Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Plug

Contact area: (Min) 0.75 µm Au on top of (Min) 2.0 µm Ni

Other reference materials that connector and cable manufacturers select based on performance parameters listed in Table 3-40 are for reference only.

Table 3-40 Reference Materials

Component	Materials
Cable	Conductor: copper with tin or silver plating
	SDP Shield: AL foil or AL/mylar foil
	Coaxial shield: copper strand
	Braid: Tin plated copper or aluminum
	Jacket: PVC or halogen free substitute material
Cable Overmold	Thermoset or thermoplastic
Connector Shells	Stainless steel or phosphor bronze
Plug Side Latches	Stainless steel
Receptacle Mid-Plate	Stainless steel
Plug Internal EMC Spring	Stainless steel or high yield strength copper alloy
Receptacle EMC Pad	Stainless steel or phosphor bronze
Receptacle Shell	Stainless steel or phosphor bronze
Receptacle Tongue	Glass-filled nylon
Housing	Thermoplastics capable of withstanding lead-free soldering temperature

Note: Halogen-free materials should be considered for all plastics

3.9 Docking Applications (Informative)

In this specification, docking refers to plugging a device directly into a dock without using a cable assembly. The USB Type-C connector is defined to support such applications.

The connector is only part of a docking solution. A complete docking solution at the system level may also include retention or locking mechanisms, alignment mechanisms, docking plug mounting solutions, and protocols supported through the connector. This specification does not attempt to standardize system docking solutions, therefore there is no interoperability requirement for docking solutions.

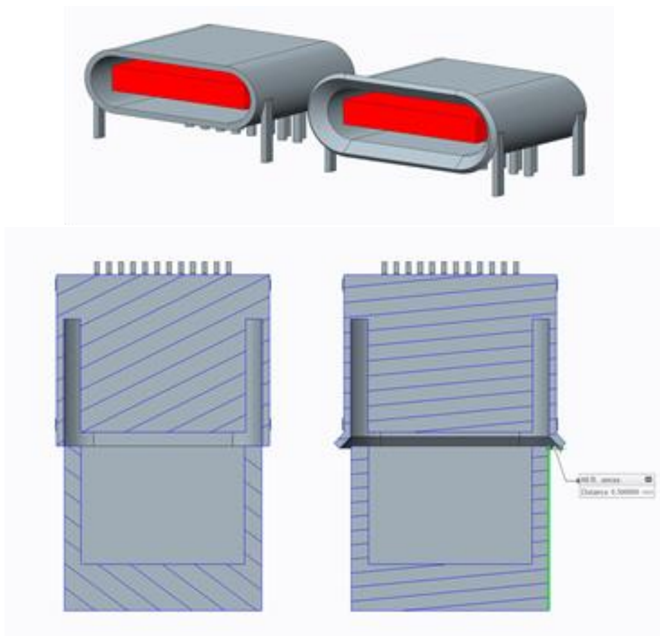
The following list includes the requirements and guidelines when using the USB Type-C connector for docking:

1. The USB Type-C plug used for docking shall work with compliant USB Type-C receptacle. It shall comply with all dimensional, electrical and mechanical requirements.
2. If the plug on the dock does not include the side latches, then the dock should provide a retention or locking mechanism to secure the device to the plug. The retention latches also serve as one of the ground return paths for EMC. The docking

design should ensure adequate EMC performance without the side latches if they are not present.

3. The internal EMC fingers are not required for the docking plug as long as the receptacle and plug shells have adequate electrical connection.
4. Alignment is critical for docking. Depending on system design, standard USB Type-C connectors alone may not provide adequate alignment for mating. System level alignment is highly recommended. Alignment solutions are implementation-specific.
5. Fine alignment is provided by the connector. The receptacle front face may have lead-in features for fine alignment. Figure 3-74 shows an example of a USB Type-C receptacle with a lead-in flange compared to a receptacle without the flange.

Figure 3-74 USB Type-C Cable Receptacle Flange Example



3.10 Implementation Notes and Design Guides

This section discusses a few implementation notes and design guides to help users design and use the USB Type-C connectors and cables.

3.10.1 EMC Management (Informative)

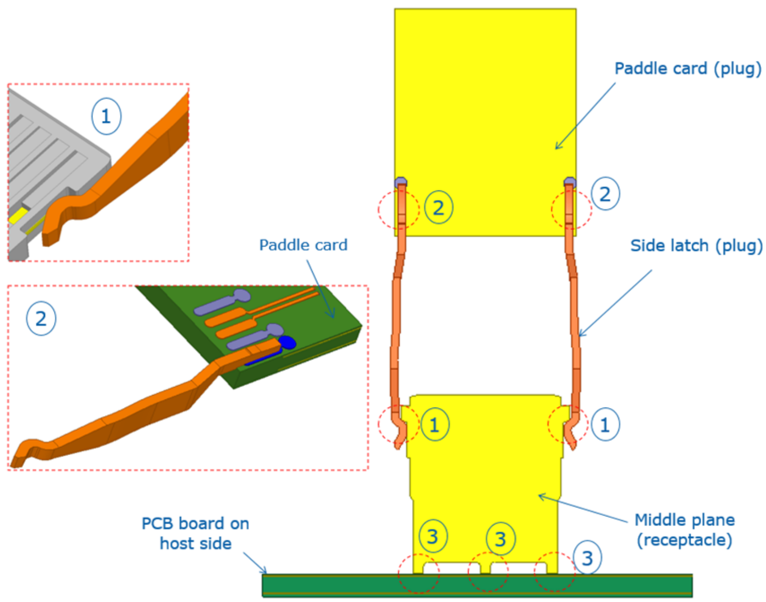
Connector and cable assembly designers, as well as system implementers should pay attention to receptacle and cable assembly shielding to ensure a low-impedance grounding path. The following are guidelines for EMC management:

- The quality of raw cables should be ensured. The intra-pair skew or the differential to common mode conversion of the TX/RX pairs has a significant impact on cable EMC and should be controlled within the limits of this specification.
- The cable external braid should be physically connected to the plug metal shell as close to 360° as possible to control EMC. Without appropriate shielding termination, even a perfect cable with zero intra-pair skew may not meet EMC requirements. Copper tape may be needed to shield off the braid termination area.
- The wire termination contributes to common-mode noise. The breakout distance for the wire termination should be kept as small as possible to optimize EMC and signal

integrity performance. If possible, symmetry should be maintained for the two lines within a differential pair.

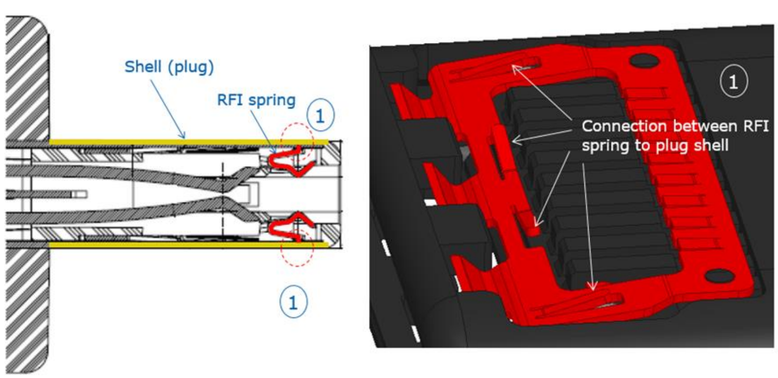
- Besides the mechanical function, the side latches on the plug and the mid-plate in the receptacle also play a role for EMC. This is illustrated in Figure 3-75:
  1. The side latch should have electrical connection to the receptacle mid-plate (a docking plug may not have side latches).
  2. The side latches should be terminated to the paddle card GND plane inside the plug.
  3. The mid-plate should be directly connected to system PCB GND plane with three or more solder leads/tails.

Figure 3-75 EMC Guidelines for Side Latch and Mid-plate



- The internal RFI finger inside the plug should have adequate connection points to the inner surface of the plug shell. Four or more connection points are recommended as illustrated in Figure 3-76.

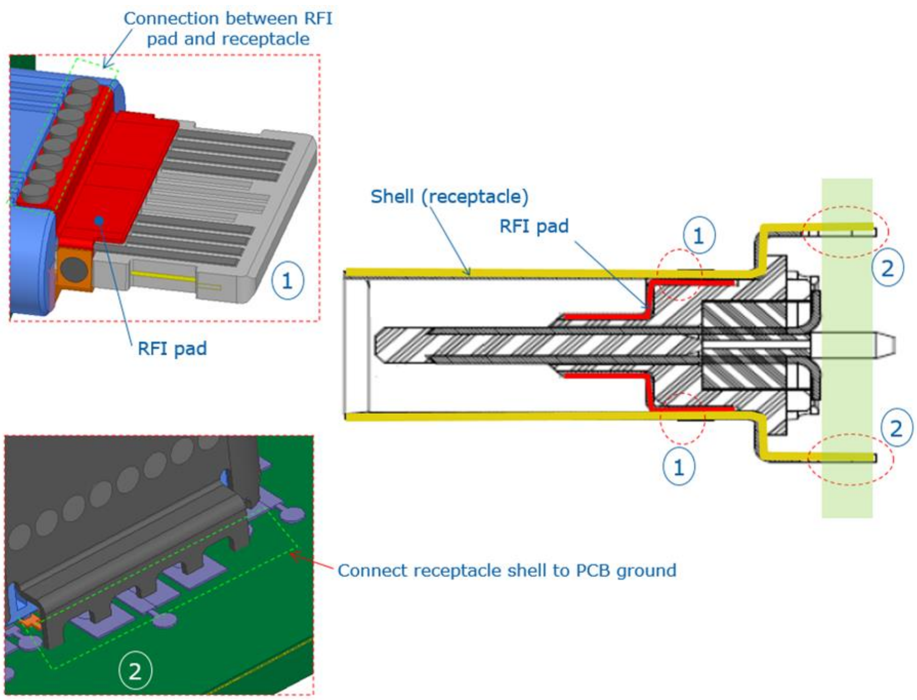
Figure 3-76 EMC Finger Connections to Plug Shell



- The EMC fingers inside the plug mates with the EMC pad in the receptacle. It is important for the EMC pad to have adequate connections to the receptacle shell. As illustrated in Figure 3-77, there are multiple laser welding points between the EMC pads and the receptacle shell, top and bottom.

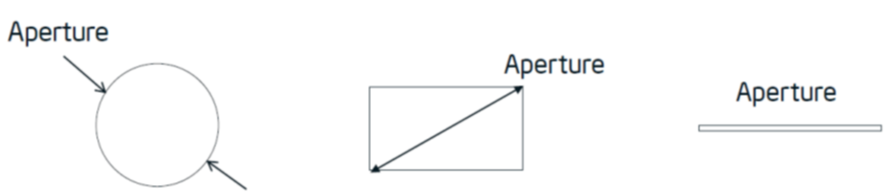
- The receptacle shell should have sufficient connection points to the system PCB GND plane with apertures as small as possible. Figure 3-77 illustrates an example with multiple solder tails to connect the receptacle shell to system PCB GND.

Figure 3-77 EMC Pad Connections to Receptacle Shell



- Apertures in the receptacle and plug shells should be minimized. If apertures are unavoidable, a maximum aperture size of 1.5 mm is recommended. See Figure 3-78 for aperture illustrations. Copper tape may be applied to seal the apertures inside the cable plug.

Figure 3-78 Examples of Connector Apertures

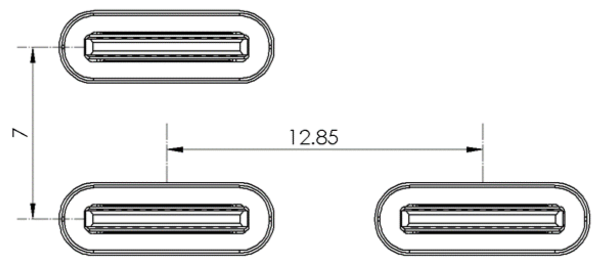


- The receptacle connectors should be connected to metal chassis or enclosures through grounding fingers, screws, or any other way to manage EMC.

3.10.2 Stacked and Side-by-Side Connector Physical Spacing (Informative)

Stacked and side-by-side USB connectors are commonly used in PC systems. Figure 3-79 illustrates the recommended spacing between connectors for stacked and side-by-side configurations.

Figure 3-79 Recommended Minimum Spacing between Connectors



3.10.3 Cable Mating Considerations (Informative)

The receptacle mounting location, exterior product surfaces, cable overmold, and plug mating length need to be considered to ensure the USB Type-C plug is allowed to fully engage the USB Type-C receptacle. Figure 3-80 illustrates the recommended minimum plug overmold clearance to allow the cable plug to fully seat in the product receptacle.

Figure 3-80 Recommended Minimum Plug Overmold Clearance

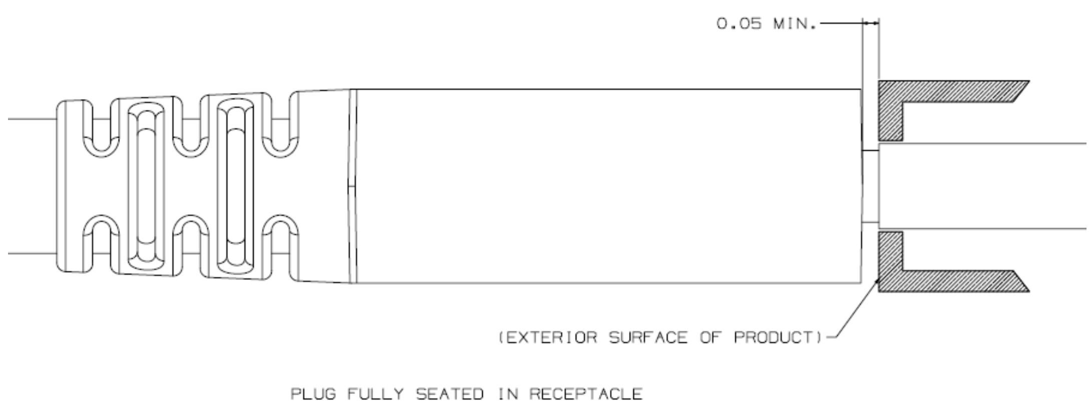
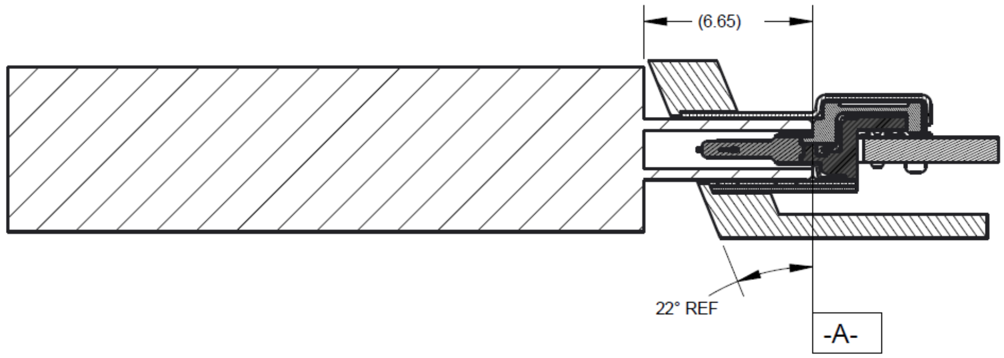


Figure 3-81 illustrates special considerations required when external walls are angled. For such applications, the USB Type-C receptacle shell may not provide as much mechanical alignment protection to the receptacle tongue as in the full shell design. Design options to allow the receptacle to pass mechanical test requirements include relief in the exterior wall surface to allow use of a full shell receptacle or use of a receptacle specifically designed for the application.

Figure 3-81 Cable Plug Overmold and an Angled Surface



3.11 Extended Power Range (EPR) Cables

3.11.1 Electrical Requirements

Extended Power Range cables have additional requirements to assure that these cables can deliver the full defined voltage and current range for *USB PD* EPR operation.

EPR cables shall functionally support a reported 50 V and 5 A operation. The minimum functional voltage that a cable shall support is 53.65 V. The electrical components potentially in the path of VBUS in an EPR cable, e.g. bypass capacitors, should be minimally rated for 63 V.

To control the impact of inductive kickback and ringing that can increase the chance of arcing between a USB Type-C plug and receptacle when a cable is removed while power is still applied, an EPR cable may include a snubber capacitor within the plug at each end of the cable. See Appendix H for more information.

3.11.2 EPR Cable Identification Requirements

All EPR cables shall be Electronically Marked and include EPR-specific information in the eMarker as defined by the USB PD specification. As defined in the *USB PD* specification, EPR cables are marked as 50 V and 5 A capable.

All EPR cables shall be visibly identified with EPR cable identification icons as defined by the USB-IF. This is required so that end users will be able to confirm visually that the cable supports up to as high of PDP = 240W as defined in the *USB PD* specification.

4 Functional

This chapter covers the functional requirements for the signaling across the USB Type-C® cables and connectors. This includes functional signal definition, discovery and configuration processes, and power delivery.

4.1 Signal Summary

Table 4-1 summarizes the list of signals used on the USB Type-C connectors.

Table 4-1 USB Type-C List of Signals

Signal Group	Signal	Description
USB 3.2 / USB4™	**TXp1, TXn1** **RXp1, RXn1** **TXp2, TXn2** **RXp2, RXn2**	Both the USB 3.2 SuperSpeed USB and USB4 serial data interfaces defines 1 differential transmit pair and 1 differential receive pair per lane. On a USB Type-C receptacle, two sets of signal pins are defined to support dual-lane operation and enable plug flipping feature.
USB 2.0	**Dp1, Dn1** **Dp2, Dn2**	USB 2.0 serial data interface defines a differential pair. On a USB Type-C receptacle, two set of USB 2.0 signal pins are defined to enable plug flipping feature.
Configuration	**CC1, CC2** (receptacle) **CC** (plug)	CC channel in the plug used for connection detect, interface configuration and VCONN.
Auxiliary signals	**SBU1, SBU2**	Sideband Use. For USB4, these signals are used for SBTX and SBRX.
Power	**VBUS**	USB cable bus power
	VCONN (plug)	USB plug power
	GND	USB cable return current path

4.2 Signal Pin Descriptions

4.2.1 SuperSpeed USB Pins

TXp1, TXn1
TXp2, TXn2

These pins are required to implement the system's transmit path of either a USB 3.2 SuperSpeed or USB4 TX/RX interface. The transmitter differential pair in a port are routed to the receiver differential pair in the port at the opposite end of the path. Depending on the established connection, the *USB 3.2 Specification* or *USB4 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.

RXp1, RXn1
RXp2, RXn2

These pins are required to implement the system's receive path of a USB 3.2 SuperSpeed or USB4 TX/RX interface. The receiver differential pair in a port are routed to the transmitter differential pair in the port at the opposite end of the path. Depending on the established connection, the *USB 3.2 Specification* or *USB4 Specification* defines all electrical characteristics, enumeration, protocol, and management features for this interface.

Two pairs of pins are defined to enable dual-lane operation – see Section 4.5.1.1 for further definition.

4.2.2 USB 2.0 Pins

Dp1, Dn1 (Dp2, Dn2)	These pins are required to implement *USB 2.0* functionality. *USB 2.0* in all three modes (LS, FS, and HS) is supported. The *USB 2.0 Specification* defines all electrical characteristics, enumeration, and bus protocol and bus management features for this interface. Two pairs of pins are defined to enable the plug flipping feature – see Section 4.5.1.1 for further definition.

4.2.3 Auxiliary Signal Pins

SBU1, SBU2	These pins are assigned to sideband use. For *USB4*, these signals are used for SBTX and SBRX. Refer to Section 4.3 for the functional requirements.

4.2.4 Power and Ground Pins

VBUS	These pins are for USB cable bus power as defined by the USB specifications. VBUS is only present when a Source-to-Sink connection across the CC channel is present – see Section 4.5.1.2.1. Refer to Section 4.4.2 for the functional requirements for VBUS.
VCONN	VCONN is applied to the unused CC pin to supply power to the local plug. Refer to Section 4.4.3 for the functional requirements for VCONN.
GND	Return current path.

4.2.5 Configuration Pins

CC1, CC2, CC	These pins are used to detect connections and configure the interface across the USB Type-C cables and connectors. Refer to Section 4.5 for the functional definition. Once a connection is established, CC1 or CC2 will be reassigned for providing power over the VCONN pin of the plug – see Section 4.5.1.2.1.

4.3 Sideband Use (SBU)

The Sideband Use pins (SBU1 and SBU2) are limited to the uses as defined by this specification and additional functionality defined in the *USB4 Specification*. See Appendix E and Appendix A for use of the SBU pins in Alternate Modes and Audio Adapter Accessory Mode.

The SBU pins on a port shall either be open circuit or have a weak pull-down to ground no stronger than zSBUTermination when in *USB 3.2* or *USB 2.0*.

These pins are pre-wired in the standard USB Full-Featured Type-C cable as individual single-ended wires (SBU_A and SBU_B). Note that SBU1 and SBU2 are cross-connected in the cable.

When operating in *USB4*, these pins are used as the *USB4* Sideband Channel with SBU1 mapping to SBTX and SBU2 mapping to SBRX. SBTX and SBRX functional requirements are as defined in the *USB4 Specification*. When a port determines that the locally-inserted plug is flipped (i.e. CC1 is open, CC2 is terminated), the *USB4 Specification* (reference Sideband Channel Lane Reversal) dictates that the port flip the SBTX and SBRX mappings to SBU1 and SBU2 in order to assure proper sideband transmit-to-receive end-to-end operation.

4.4 Power and Ground

4.4.1 IR Drop

The maximum allowable cable IR drop for ground (including ground on a captive cable) shall be 250 mV and for VBUS shall be 500 mV through the cable to the cable's maximum rated VBUS current capacity. When VCONN is being sourced, the IR drop for the ground shall still be met considering any additional VCONN return current.

Figure 4-1 illustrates what parameters contribute to the IR drop and where it shall be measured. The IR drop includes the contact resistance of the mated plug and receptacles at each end.

Figure 4-1 Cable IR Drop

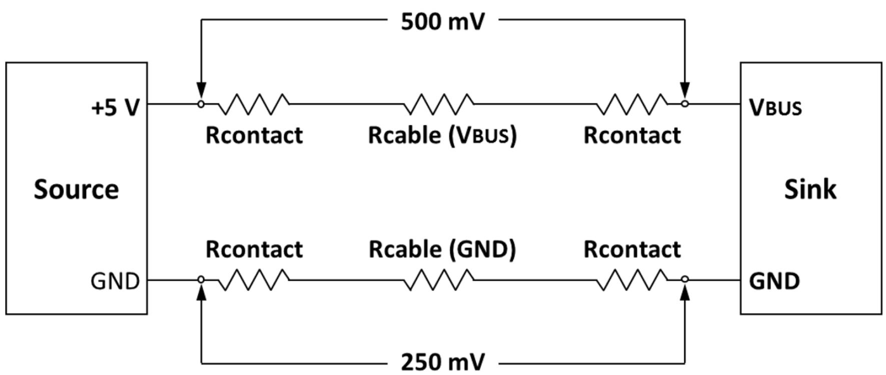
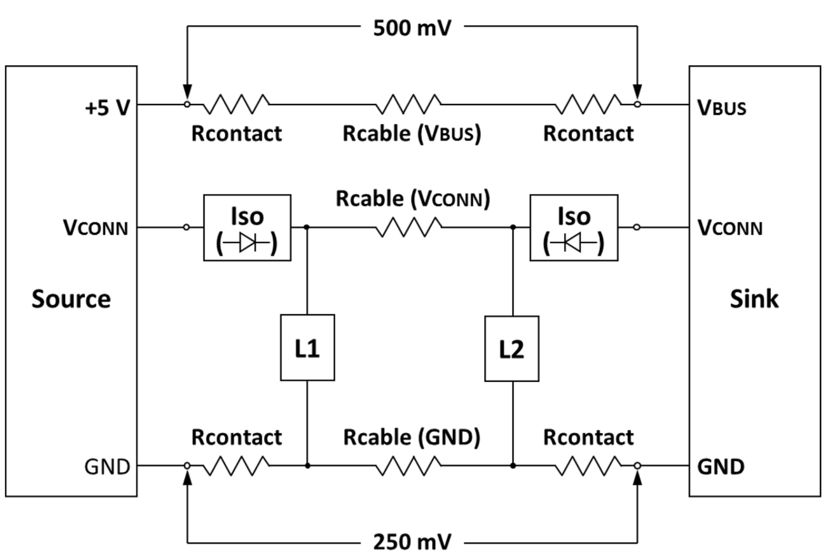


Figure 4-2 illustrates what parameters contribute to the IR drop for a powered cable and where it shall be measured. Note that the powered cable includes isolation elements (Iso) and loads (L1 and L2) for the functions in the powered cable such as *USB PD* controllers. The IR drop shall remain below 250 mV in all cases.

Figure 4-2 Cable IR Drop for powered cables



4.4.2 VBUS

The allowable default range for VBUS as measured at the Source receptacle shall be as defined by the *USB 2.0 Specification* and *USB 3.2 Specification*. For *USB4*, the *USB 3.2 Specification* is used for this requirement. NOTE that due to higher currents allowed, legacy devices may experience a higher voltage (up to 5.5V maximum) at light loads.

The Source's USB Type-C receptacle VBUS pin shall remain unpowered and shall limit the capacitance between VBUS and GND as specified in Table 4-2 until a Sink is attached. The VBUS pin shall return to the unpowered state when the Sink is detached. See Table 4-29 for VBUS timing values. Legacy hosts/chargers that by default source VBUS when connected using any legacy USB connector (Standard-A, Micro-B, etc.) to USB Type-C cable or adapter are exempted from these two requirements.

A DRP or Source (or device with Accessory Support) implementing an Rp pull-up as its method of connection detection shall provide an impedance between VBUS and GND on its receptacle pins as specified in Table 4-2 when not sourcing power on VBUS (i.e., when in states Unattached.SRC or Unattached.Accessory).

Table 4-2 VBUS Source Characteristics

	Minimum	Maximum	Notes
VBUS Leakage Impedance	72.4 kΩ		Leakage between VBUS pins and GND pins on receptacle when VBUS is not being sourced.
VBUS Capacitance		3000 µF	Capacitance for source-only ports between VBUS and GND pins on receptacle when VBUS is not being sourced.
		10 µF	Capacitance for DRP ports between VBUS and GND pins on receptacle when VBUS is not being sourced.

Table 4-3 specifies VBUS Sink characteristics with regard to disconnect behavior based on monitoring VBUS. Sinks may monitor the CC pin for the removal of Rp by the Source as an additional indication of disconnect.

Table 4-3 VBUS Sink Characteristics

	Minimum	Maximum	Notes
tSinkDisconnect		40 ms	Time limit for transition from Attached.SNK to Unattached.SNK
vSinkDisconnect[1]	0.8V	3.67V	Threshold used for transition from Attached.SNK to Unattached.SNK when VBUS is 5 V. This also applies for *USB PD* contracts at 5 V. For *USB PD* contracts at 5 V, the Sink shall take IR drop and margin into account when selecting this threshold.
		PPS_APDO_ Min_Voltage * 0.95	Threshold used for transition from Attached.SNK to Unattached.SNK. This applies for *USB PD* PPS contracts for RDO Output Voltage less than or equal to 5 V. This also applies for *USB PD* PPS contracts operating in the Current Limit mode. The Sink shall take IR drop and margin into account when selecting this threshold.
vSinkPD_min[1]		vNew – 750 mV + vValid	Minimum valid VBUS voltage seen by sink when negotiated through *USB PD*. vNew = vSrcNew (min) or vPpsNew (min) as defined in *USB PD*. 750 mV= 500 mV + 250 mV (maximum IR drop) vValid = vSrcValid (min) or vPpsValid (min) as defined in *USB PD*.
vSinkDisconnectPD[1]	90% of vSinkPD_min	vSinkPD_min	VBUS disconnect threshold when VBUS voltage was negotiated through *USB PD* to a value above 5 V. This applies for *USB PD* PPS contracts for RDO Output Voltage above 5 V. This also applies for *USB PD* PPS contracts operating in the Constant Voltage mode.
VBUS Capacitance		10 µF	Capacitance between VBUS and GND pins on receptacle when not in Attached.SNK.

Note 1: See Section 4.5.2.2.5.2 with regard to applicability of this requirement.

4.4.3 VCONN

VCONN is provided by the Source to power cables with electronics in the plug. VCONN is provided over the CC pin that is determined not to be connected to the CC wire of the cable.

Initially, VCONN shall be sourced on all Source USB Type-C receptacles that utilize the TX and RX pins during specific connection states as described in Section 4.5.2.2. Subsequently, if VCONN is not explicitly required by the cable or device as indicated in its eMarker, VCONN may be removed as described in Table 4-4. VCONN may also be sourced by USB Type-C receptacles that do not utilize the TX and RX pins as described in Section 4.5.2.2. *USB PD* VCONN_Swap command also provides the Source a means to request that the attached Sink source VCONN.

Table 4-4 USB Type-C Source Port's VCONN Requirements Summary

D+/D−	TX/RX, VPD	> 3 A	VCONN Requirements
No	No	No	Not required to source VCONN
Yes	No	No	Not required to source VCONN
Yes	Yes	No	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If after reading the cable's eMarker, the Source has determined that the cable is not a VPD and the Cable Termination Type field is 00b, it may remove VCONN power.
No	No	Yes	Required to source 100 mW. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	No	Yes	Required to source 100 mW. VCONN power may be removed after the source has read the cable's eMarker and has determined the cable's current carrying capacity.
Yes	Yes	Yes	Required to source 1 W for x1 implementations and 1.5 W for x2 implementations. If after reading the cable's eMarker, the Source has determined the cable's current carrying capacity and the cable is not a VPD and the Cable Termination Type field is 00b, it may remove VCONN power.

Table 4-5 provides the voltage and power requirements that shall be met for VCONN. See Section 4.9 for more details about Electronically Marked Cables. See Appendix E regarding optional support for an increased VCONN power range in Alternate Modes.

Table 4-5 VCONN Source Characteristics

	Minimum	Maximum	Notes
vVCONNValid	3.0 V	5.5 V	The voltage range over which VCONN is considered valid.
Power for Sources with TX/RX Signals	x1 1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage. Source may disable VCONN per Table 4-4. Alternate modes may require higher power.
	x2 1.5 W		
Power for Sources with VPD support	1 W		Source may latch-off VCONN if excessive power is drawn beyond the specified inrush and mode wattage.
Power for Sources in USB Suspend or without TX/RX Signals	100 mW		Minimum power Source must provide in USB Suspend or without TX/RX signals.[1] Source may disable VCONN per Table 4-4.
Rdch	30 Ω	6120 Ω	Discharge resistance applied in UnattachedWait.SRC between the CC pin being discharged and GND.

Note 1: During transition from U3 to U0, VCONN Source shall provide up to max U0 power.

To aid in reducing the power associated with supplying VCONN, a Source is allowed to either not source VCONN or turn off VCONN under any of the following conditions:

- Ra is not detected on the CC pin after tCCDebounce when the other CC pin is in the SRC.Rd state, or
- if there is no GoodCRC response to *USB PD* Discover Identity messages sent to SOP'.

If the power source used to supply VCONN power is a shared power source for other USB VCONN and VBUS outputs, it must be bypassed with capacitance identical to the VBUS capacitance requirements of *USB 3.2* Section 11.4.4 – Dynamic Attach and Detach. Any VCONN power source bypass capacitance must be isolated from the CC pins when VCONN is not being provided.

Table 4-6 provides the requirements that shall be met for cables that consume VCONN power.

Table 4-6 Cable VCONN Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0	5.5V	Voltage range (vVCONNValid) when VCONN is valid.
Inrush Capacitance		10 µF	A cable shall not present more than the equivalent inrush capacitance to the VCONN source. The active cable is responsible for discharging its capacitance.
Power for Electronically Marked Passive Cables		20mW	See Section 4.9. Measured with no USB PD traffic at least tRaWeaken after VCONN applied. Note: 75mW max allowed for the first tRaWeaken after VCONN applied.
USB 3.2 Power for Active Cables in U-states		See Table 6-20	U0, U1, U2, U3, Rx.Detect, and eSS.Disabled.
tVCONNDischarge		230ms	Time from cable disconnect to vVCONNDischarge met.
vVCONNDischarge		800mV	VCONN voltage after tVCONNDischarge
vVCONNDisconnect	1 V	2.4 V	Threshold used to detect VCONN disconnect.
iRaDetect		10 mA	The maximum current drawn from VCONN when the voltage is below vVCONNValid. Note: This current is below the 75 mW allowance for the first 500 ms at 5.5 V.
tRaReconnect		1 ms	Time from VCONN falling below vVCONNDisconnect at the cable plug until the cable has re-applied Ra.
tRaWeaken	21 ms	1.2 s	Time from VCONN exceeding vVCONNDisconnect until the cable removes or weakens Ra.
tVCONNSwitch		tVCONNStable	Cables that optionally use VBUS shall power from VCONN within tVCONNStable.

The cable shall remove or weaken Ra according to the state diagram behavior in 4.5.2.5. The cable shall reapply Ra according to the state diagram behavior in 4.5.2.5. The cable shall discharge VCONN to below vVCONNDischarge on a cable disconnect. The cable shall control Ra at each of its ends independently based on the VCONN on that end.

Implementation Note: Increasing Ra to 20KΩ will meet both the power dissipation for electronically marked passive cables and discharge 10µF to less than vVCONNDischarge in tVCONNDischarge.

Table 4-7 VCONN-Powered Accessory (VPA) Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	Voltage range (vVCONNValid) when VCONN is valid.
Inrush Capacitance		10 µF	An accessory shall not present more than the equivalent inrush capacitance to the VCONN source. The accessory is responsible for discharging its capacitance when detached from a port.
Power before Alternate Mode Entry		35 mW	Maximum power in USB suspend Note: Power shall be reduced 5 seconds after VCONN is applied if no Alternate Mode Entry has occurred. A VCONN power cycle may be required to re-enable USB-PD communication. Note: 75 mW max allowed for the first 500 ms after VCONN is applied.
tVCONNDischarge		230 ms	Time from VPA disconnect to vVCONNDischarge met.
vVCONNDischarge		800 mV	VCONN voltage after tVCONNDischarge
iRaDetect		10 mA	The maximum current drawn from VCONN when the voltage is below vVCONNValid. Note: This current is below the 75 mW allowance for the first 500 ms at 5.5 V.
vRaReconnect	800 mV		Voltage at which the VPA shall reapply Ra on the falling edge of VCONN.
tRaWeaken		1.2 s	Time from VCONN entering the valid region until the VPA removes or weakens Ra.
vVCONNDisconnect	1 V	2.4 V	Threshold used to detect VCONN disconnect.

The VPA shall remove or weaken Ra within tRaWeaken (as defined in Table 4-7) after VCONN enters the valid voltage range (vVCONNValid).

The VPA shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-7. The VPA shall discharge VCONN to below vVCONNDischarge within tVCONNDischarge on a cable disconnect. The VPA shall consider the VCONN capacitance present in the accessory when discharging VCONN.

The maximum power consumption while in an Alternate Mode is defined by the specification specific to the Alternate Mode being used.

Table 4-8 VCONN-Powered USB Device (VPD) Sink Characteristics

	Minimum	Maximum	Notes
Voltage	3.0 V	5.5 V	Voltage range (vVCONNValid) when VCONN is valid.
Inrush Capacitance		10 µF	A VPD shall not present more than the equivalent inrush capacitance to the VCONN source. The VPD is responsible for discharging its capacitance when detached from a port.
Power before USB enumeration		35 mW	Maximum power in USB suspend Note: 75 mW max allowed for the first 500 ms after VCONN is applied.
Power when active		500 mW (*USB 2.0*) 750 mW (*USB 3.2*)	A VPD shall only expose a low-power interface over USB.
tVCONNDischarge		230 ms	Time from VPD disconnect to vVCONNDischarge met.
vVCONNDischarge		800 mV	VCONN voltage after tVCONNDischarge
iRaDetect		10 mA	The maximum current drawn from VCONN when the voltage is below vVCONNValid. Note: This current is below the 75 mW allowance for the first 500 ms at 5.5 V.
vRaReconnect	800 mV		Voltage at which the VPD shall reapply Ra on the falling edge of VCONN.
tRaWeaken		1.2 s	Time from VCONN entering the valid region until the VPD removes or weakens Ra.
vVCONNDisconnect	1 V	2.4 V	Threshold used to detect VCONN disconnect.

The VPD shall remove or weaken Ra within tRaWeaken (as defined in Table 4-8) after VCONN enters the valid voltage range (vVCONNValid).

The VPD shall reapply Ra when VCONN falls below vRaReconnect as defined in Table 4-8. The VPD shall discharge VCONN to below vVCONNDischarge within tVCONNDischarge on a cable disconnect. The VPD shall consider the VCONN capacitance present in the device when discharging VCONN.

4.5 Configuration Channel (CC)

4.5.1 Architectural Overview

For the USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the Source-to-Sink connection. When the device is connected through a hub, the connection between a Sink (UFP) on the hub and the Source (host port) and the connection between the Sink (device port) and a Source (DFP on the hub), are treated as separate connections. Functionally, the configuration channel is used to serve the following purposes.

- Detect attach of USB ports, e.g. a Source to a Sink
- Resolve cable orientation and twist connections to establish USB data bus routing
- Establish data roles between two attached ports
- Discover and configure VBUS: USB Type-C Current modes or *USB Power Delivery*
- Configure VCONN
- Discover and configure optional Alternate and Accessory modes

4.5.1.1 USB Data Bus Interface and USB Type-C Plug Flip-ability

Since the USB Type-C plug can be inserted in either right-side-up or upside-down position, the hosts and devices that support USB data bus functionality must operate on the signal pins that are actually connected end-to-end. In the case of *USB 2.0*, this is done by shorting together the two D+ signal pins and the two D− signal pins in the host and device receptacles. In the case of *USB 3.2* SuperSpeed USB or *USB4* TX/RX signals in a single-lane implementation, it requires the functional equivalent of a switch in both the host and device to appropriately route the TX and RX signal pairs to the connected path through the cable. For a *USB 3.2* SuperSpeed USB or *USB4* dual-lane implementation, the host and/or device resolves the lane ordering.

Figure 4-3 illustrates the logical data bus model for a USB Type-C-based Host connected to a USB Type-C-based Device that is only capable of SuperSpeed USB single-lane operation. The USB cable that sits between a host and device can be in one of four possible connected states when viewed by the host:

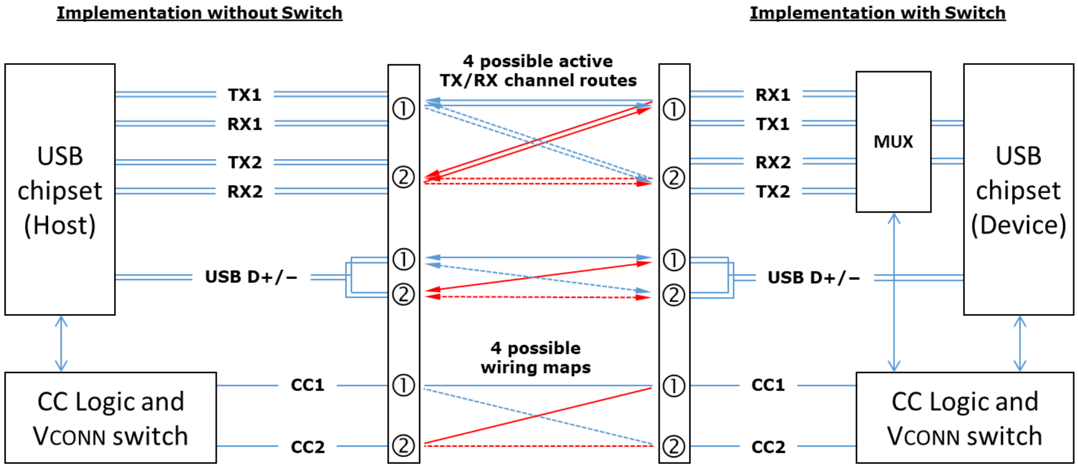
- Un-flipped straight through – Position ① ⇔ Position ①
- Un-flipped twisted through – Position ① ⇔ Position ②
- Flipped straight through – Position ② ⇔ Position ②
- Flipped twisted through – Position ② ⇔ Position ①

To establish the proper routing of the active USB data bus from host to device, the standard USB Type-C cable is wired such that a single CC wire is position aligned with the first TX/RX signal pairs (TXp1/TXn1 and RXp1/RXn1) – in this way, the CC wire and TX/RX data bus wires that are used for single-lane operational signaling within the cable track with regard to the orientation and twist of the cable. By being able to detect which of the CC pins (CC1 or CC2) at the receptacle is terminated by the device, the host is able to determine which TX/RX signals are to be used for the single-lane connection and the host can use this to control the functional switch for routing the TX/RX signal pairs. Similarly in the device, detecting which of the CC pins at the receptacle is terminated by the host allows the device to control the functional switch that routes its TX/RX signal pairs.

For a dual-lane implementation, the TX/RX signal pairs in the cable/plug aligned with the CC wire/pin is Lane 0 and in reference to *USB 3.2*, shall be identified as the Configuration Lane.

The second TX/RX signal pairs (TXp2/TXn2 and RXp2/RXn2) in the cable/plug is Lane 1 of a dual-lane configuration.

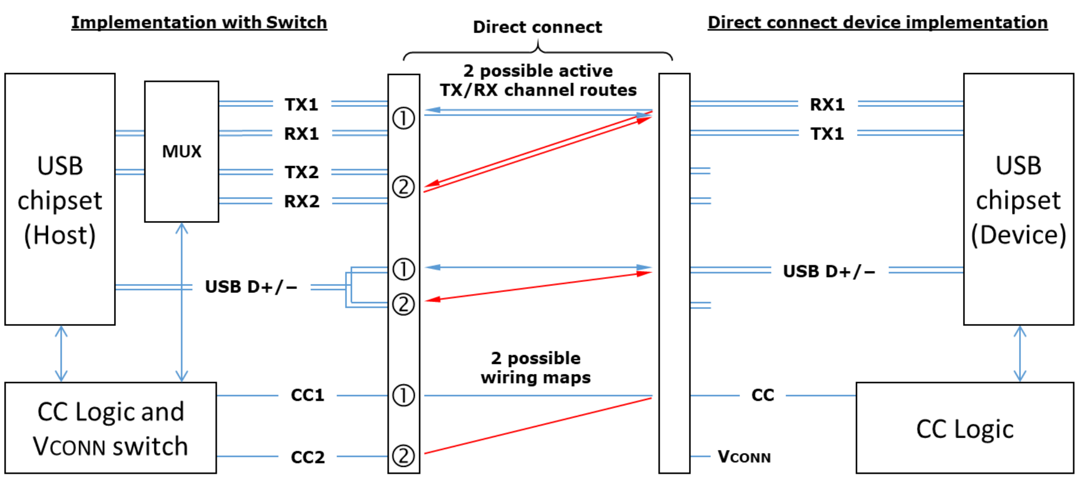
Figure 4-3 Logical Model for Single-Lane Data Bus Routing across USB Type-C-based Ports



While Figure 4-3 illustrates the functional model as a host connected to a device, this model equally applies to a USB hub's downstream ports as well.

Figure 4-4 illustrates the logical data bus model for a single-lane USB Type-C-based Device (implemented with a USB Type-C plug either physically incorporated into the device or permanently attached as a captive cable) connected directly to a USB Type-C-based Host. For the device, the location of the TX/RX data bus, *USB 2.0* data bus, CC and VCONN pins are fixed by design. Given that the device pin locations are fixed, only two possible connected states exist when viewed by the host.

Figure 4-4 Logical Model for USB Type-C-based Ports for a Single-Lane Direct Connect Device



The functional requirements for implementing TX/RX data bus routing for the USB Type-C receptacle are not included in the scope of this specification. There are multiple host, device and hub architectures that can be used to accomplish this which could include either discrete or integrated switching, and could include merging this functionality with other USB 3.2 or USB4 design elements, e.g. a bus repeater.

The functional requirements for addressing SBU1 and SBU2 routing is not included in the scope of this specification. For USB4, where SBTX and SBRX are mapped to SBU1 and SBU2, the adjustment to the mapping of these signals based on the connection state (flipped and/or twisted) of the cable is defined by the USB4 Specification (reference Sideband Channel Lane Reversal).

4.5.1.2 Connecting Sources and Sinks

Given that the USB Type-C receptacle and plug no longer differentiate host and device roles based on connector shape, e.g., as was the case with USB Type-A and Type-B connectors, any two ports that have USB Type-C receptacles can be connected together with a standard USB Type-C cable. Table 4-9 summarizes the expected results when interconnecting Source, Sink and DRP ports.

Table 4-9 USB Type-C-based Port Interoperability

	Source-only	**Sink-only**	**DRP (Dual-Role-Power)**
Source-only	Non-functional	Functional	Functional
Sink-only	Functional	Non-functional	Functional
DRP (Dual-Role-Power)	Functional	Functional	Functional*

* Resolution of roles may be automatic or manually driven

In the cases where no function results, neither port shall be harmed by this connection. The user has to independently realize the invalid combination and take appropriate action to resolve. While these two invalid combinations mimic traditional USB where host-to-host and device-to-device connections are not intended to work, the non-keyed USB Type-C solution does not prevent the user from attempting such interconnects. VBUS and VCONN shall not be applied by a Source (host) in these cases.

The typical flow for the configuration of the interface in the general USB case of a Source (Host) to a Sink (Device) is as follows:

1. Detect a valid connection between the ports (including determining cable orientation, Source/Sink and DFP/UFP relationship)
2. Optionally discover the cable's capabilities
3. Optionally establish alternatives to traditional USB power (See Section 4.6.2)
    a. USB PD communication over CC for advanced power delivery negotiation
    b. USB Type-C Current modes
    c. USB BC 1.2
4. USB Device Enumeration

For cases of Dual-Role-Power (DRP) ports connecting to either Source-only, Sink-only or another DRP, the process is essentially the same except that during the detecting a valid connection step, the DRP alternates between operating as a Source for detecting an attached

Sink and presenting as a Sink to be detected by an attached Source. Ultimately this results in a Source-to-Sink connection.

4.5.1.2.1 Detecting a Valid Source-to-Sink Connection

The general concept for setting up a valid connection between a Source and Sink is based on being able to detect terminations residing in the product being attached.

To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd) termination model is used – actual implementation in hosts and devices may vary, for example, the pull-up termination could be replaced by a current source. Figure 4-5 and Figure 4-6 illustrates two models, the first based on a pull-up resistor in the Source and the second replacing this with a current source.

Figure 4-5 Pull-Up/Pull-Down CC Model

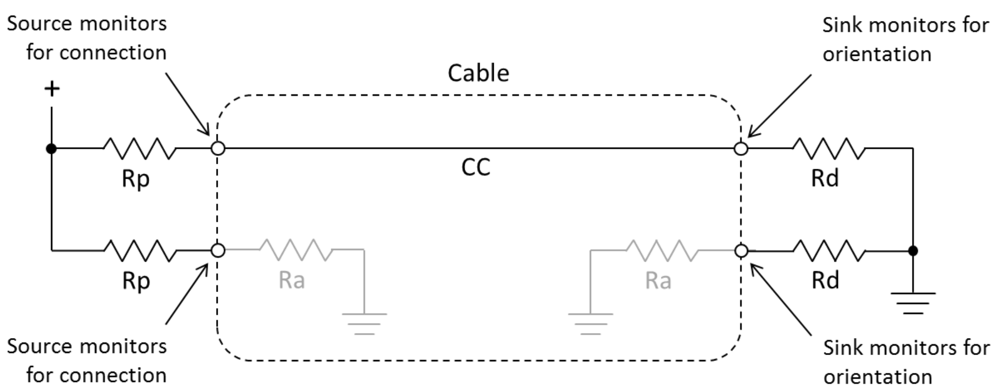
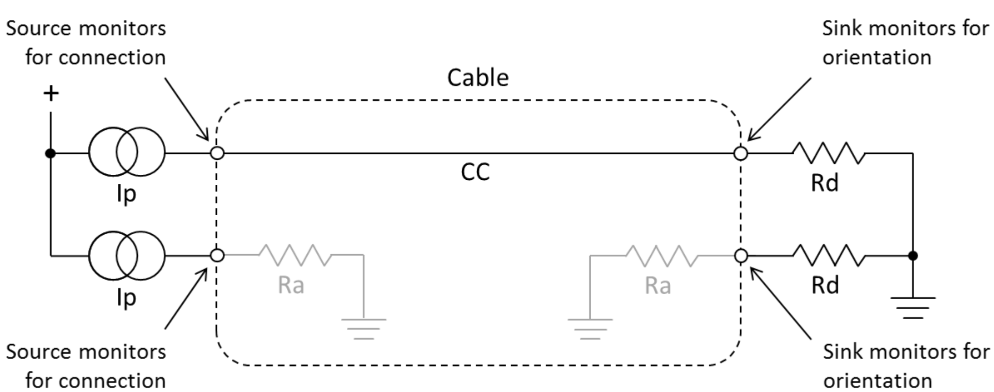


Figure 4-6 Current Source/Pull-Down CC Model



Initially, a Source exposes independent Rp terminations on its CC1 and CC2 pins, and a Sink exposes independent Rd terminations on its CC1 and CC2 pins, the Source-to-Sink combination of this circuit configuration represents a valid connection. To detect this, the Source monitors CC1 and CC2 for a voltage lower than its unterminated voltage – the choice of Rp is a function of the pull-up termination voltage and the Source's detection circuit. This indicates that either a Sink, a powered cable, or a Sink connected via a powered cable has been attached.

Prior to application of VCONN, a powered cable exposes Ra on its VCONN pin. Ra represents the load on VCONN plus any resistive elements to ground. In some cable plugs it might be a pure resistance and in others it may be simply the load.

The Source has to be able to differentiate between the presence of Rd and Ra to know whether there is a Sink attached and where to apply VCONN. The Source is not required to source VCONN unless Ra is detected.

Two special termination combinations on the CC pins as seen by a Source are defined for directly attached Accessory Modes: Ra/Ra for Audio Adapter Accessory Mode (Appendix A) and Rd/Rd for Debug Accessory Mode (Appendix B).

The Source uses de-bounce timers to reliably detect states on the CC pins to de-bounce the connection (tCCDebounce), and hide *USB PD* BMC communications (tPDDebounce).

Table 4-10 summarizes the port state from the Source's perspective.

Table 4-10 Source Perspective

CC1	CC2	State	Position
Open	**Open**	Nothing attached	N/A
Rd	**Open**	Sink attached	①
Open	**Rd**		②
Open	**Ra**	Powered cable without Sink attached	①
Ra	**Open**		②
Rd	**Ra**	Powered cable with Sink, VCONN-Powered Accessory (VPA), or VCONN-Powered USB Device (VPD) attached	①
Ra	**Rd**		②
Rd	**Rd**	Debug Accessory Mode attached (Appendix B)	N/A
Ra	**Ra**	Audio Adapter Accessory Mode attached (Appendix A)	N/A

Once the Sink is powered, the Sink monitors CC1 and CC2 for a voltage greater than its local ground. The CC pin that is at a higher voltage (i.e. pulled up by Rp in the Source) indicates the orientation of the plug.

Table 4-11 summarizes the typical behaviors for simple Sources (Hosts) and Sinks (Devices) for each state in Table 4-10.

Table 4-11 Source (Host) and Sink (Device) Behaviors by State

State	Source Behavior	Sink Behavior
Nothing attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Sink attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN	• Sense CC pins for orientation • Sense loss of VBUS for detach
Powered cable without Sink attached	• Sense CC pins for attach • Do not apply VBUS or VCONN	• Sense VBUS for attach
Powered cable with Sink, VCONN-Powered Accessory, or VCONN-Powered USB Device attached	• Sense CC for orientation • Sense CC for detach • Apply VBUS and VCONN • Detect VPD and remove VBUS	• If accessories or VPDs are supported, see Source Behavior with exception that VBUS is not applied., otherwise, N/A.
Debug Accessory Mode attached	• Sense CC pins for detach • Reconfigure for debug	• Sense VBUS for detach • Reconfigure for debug
Audio Adapter Accessory Mode attached	• Sense CC pins for detach • Reconfigure for analog audio	• If accessories are supported, see Source Behavior, otherwise, N/A

Figure 4-3 shows how the inserted plug orientation is detected at the Source's receptacle by noting on which of the two CC pins in the receptacle an Rd termination is sensed. Now that the Source (Host) has recognized that a Sink (Device) is attached and the plug orientation is determined, it configures the TX/RX data bus routing to the receptacle.

The Source (Host) then turns on VBUS. For the CC pin that does not connect Source-to-Sink through the cable, the Source supplies VCONN and may remove the termination. With the Sink (Device) now powered, it configures the USB data path. This completes the Host-to-Device connection.

The Source monitors the CC wire for the loss of pull-down termination to detect detach. If the Sink is removed, the Source port removes any voltage applied to VBUS and VCONN, resets its interface configuration and resumes looking for a new Sink attach.

Once a valid Source-to-Sink connection is established, alternatives to traditional USB power (VBUS as defined by either *USB 2.0* or *USB 3.2* specifications) may be available depending on the capabilities of the host and device. These include USB Type-C Current, USB Power Delivery, and *USB Battery Charging 1.2*.

In the case where *USB PD* PR_Swap is used to swap the Source and Sink of VBUS, the supplier of VCONN remains unchanged during and after the VBUS power swap. The new Source monitors the CC wire and the new Sink monitors VBUS to detect detach. When a detach event is detected, any voltages applied to VBUS and VCONN are removed, each port resets its interface configuration and resumes looking for an attach event.

In the case where *USB PD* DR_Swap is used to swap the data roles (DFP and UFP), the source of VBUS and VCONN do not change after the data role swap.

In the case where USB PD VCONN_Swap is used to swap the VCONN source, the VBUS Source/Sink and DFP/UFP roles are maintained during and after the VCONN swap.

The last step in the normal USB Type-C connect process is for the USB device to be attached and enumerated per standard USB 2.0 and USB 3.2 processes.

4.5.1.3 Configuration Channel Functional Models

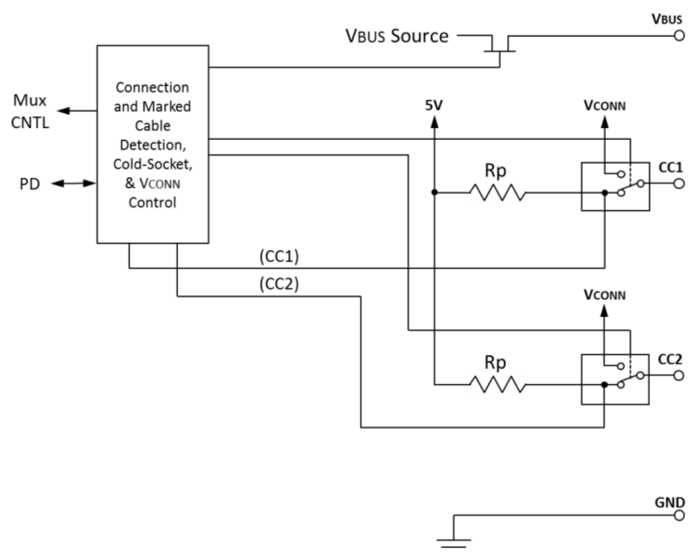
The functional models for the configuration channel behavior based on the CC1 and CC2 pins are described in this section for each port type: Source, Sink and Dual-Role-Power (DRP).

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete. In these figures, VBUS and VCONN may or may not actually be available.

4.5.1.3.1 Source Configuration Channel Functional Model

Figure 4-7 illustrates the functional model for CC1 and CC2 for a Source port prior to attach. This illustration includes consideration for USB PD.

Figure 4-7 Source Functional Model for CC1 and CC2



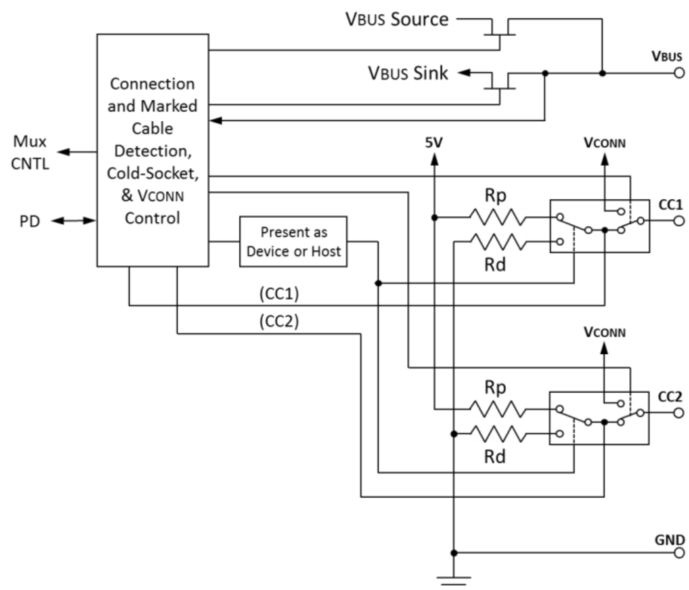
Referring to Figure 4-7, a port that behaves as a Source has the following functional characteristics:

1. The Source uses a FET to enable/disable power delivery across VBUS and initially the Source has VBUS disabled.
2. The Source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a Sink. The presence of an Rd pull-down resistor on either pin indicates that a Sink is being attached. The value of Rp indicates the initial USB Type-C Current level supported by the host.
3. The Source can optionally clamp the voltage on either of its CC pins. The minimum clamping voltage shall be vCC-Clamp. The clamp is intended to protect the Source circuitry associated with CC functionality.
4. The Source uses the CC pin pull-down characteristic to detect and establish the correct routing for the SuperSpeed USB data path and determine which CC pin is intended for supplying VCONN.

5. Once a Sink is detected, the Source enables VBUS and VCONN.
6. The Source can dynamically adjust the value of Rp to indicate a change in available USB Type-C Current to a Sink.
7. The Source monitors the continued presence of Rd to detect Sink detach. When a detach event is detected, the Source removes, if supplied, VBUS and VCONN, and returns to step 2.
8. If the Source supports advanced functions (*USB Power Delivery* and/or Alternate Modes), *USB PD* communication is required.

Figure 4-8 illustrates the functional model for CC1 and CC2 for a Source that supports *USB PD* PR_Swap.

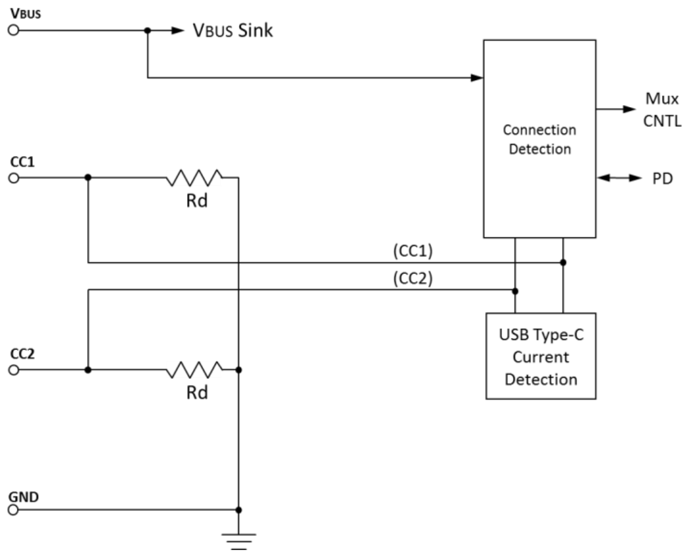
Figure 4-8 Source Functional Model Supporting USB PD PR_Swap



4.5.1.3.2 Sink Configuration Channel Functional Model

Figure 4-9 illustrates the functional model for CC1 and CC2 for a Sink. This illustration includes consideration for both USB Type-C Current and *USB PD*.

Figure 4-9 Sink Functional Model for CC1 and CC2

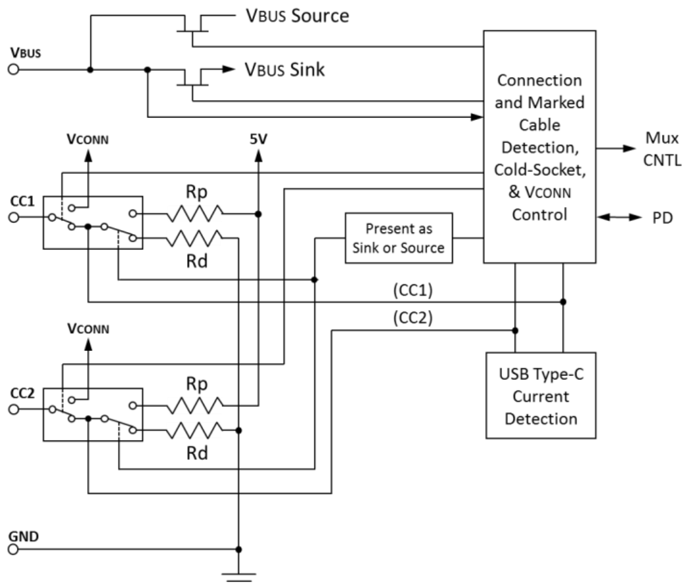


Referring to Figure 4-9, a port that behaves as a Sink has the following functional characteristics:

1. The Sink terminates both CC1 and CC2 to GND using pull-down resistors.
2. The Sink determines that a Source is attached by the presence of power on VBUS.
3. The Sink uses the CC pin pull-up characteristic to detect and establish the correct routing for the SuperSpeed USB data path.
4. The Sink can optionally monitor CC to detect an available higher USB Type-C Current from the Source. The Sink shall manage its load to stay within the detected Source current limit.
5. The Sink can optionally clamp the voltage on either of its CC pins. The minimum clamping voltage shall be vCC-Clamp. The clamp is intended to protect the Sink circuitry associated with CC functionality.
6. If the Sink supports advanced functions (*USB Power Delivery* and/or Alternate Modes), *USB PD* communication is required.

Figure 4-10 illustrates the functional model for CC1 and CC2 for a Sink that supports *USB PD* PR_Swap and supports *USB PD* VCONN_Swap prior to attach.

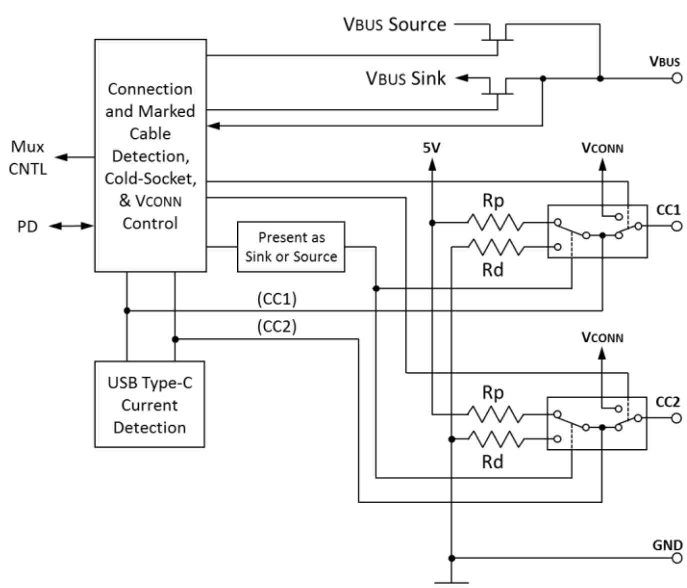
Figure 4-10 Sink Functional Model Supporting USB PD PR_Swap and VCONN_Swap



4.5.1.3.3 Dual-Role-Power (DRP) Configuration Channel Functional Model

Figure 4-11 illustrates the functional model for CC1 and CC2 for a DRP presenting as a Source prior to attach. This illustration includes consideration for both the USB Type-C Current and the *USB PD* features.

Figure 4-11 DRP Functional Model for CC1 and CC2



Referring to Figure 4-11, a port that can alternate between DFP and UFP behaviors has the following functional characteristics:

1. The DRP uses a FET to enable/disable power delivery across VBUS and initially when in Source mode has VBUS disabled.

2. The DRP uses switches for presenting as a Source or Sink.
3. The DRP has logic used during initial attach to toggle between Source and Sink operation:
    a. Until a specific stable state is established, the DRP alternates between exposing itself as a Source and Sink. The timing of this process is dictated by a period (tDRP), percentage of time that a DRP exposes Rp (dcSRC.DRP) and role transition time (tDRPTransition).
    b. When the DRP is presenting as a Source, it follows Source operation to detect an attached Sink – if a Sink is detected, it applies VBUS, VCONN, and continues to operate as a Source (e.g., cease alternating).
    c. When the DRP is presenting as a Sink, it monitors VBUS to detect that it is attached to a Source – if a Source is detected, it continues to operate as a Sink (cease alternating).
4. If the DRP supports advanced functions (*USB Power Delivery* and/or Alternate Modes), *USB PD* communication is required.

4.5.1.4 USB Type-C Port Power Roles and Role Swapping Mechanisms

USB Type-C ports on products (USB hosts, USB devices, USB chargers, etc.) can be generally characterized as implementing one of seven power role behavioral models:

- Source-only
- Source (Default) – strong preference toward being a Source but subsequently capable of becoming a Sink using USB PD swap mechanisms.
- Sink-only
- Sink (Default) – strong preference toward being a Sink but subsequently capable of becoming a Source using USB PD swap mechanisms.
- DRP: Toggling (Source/Sink)
- DRP: Sourcing Device
- DRP: Sinking Host

Two independent sets of swapping mechanisms are defined for USB Type-C port implementations, one based on role swapping within the initial state machine connection process and the other based on subsequent use of *USB PD*-based swapping mechanisms.

4.5.1.4.1 USB Type-C State-Machine-Based Role Swapping

During the initial USB Type-C state machine connection process, the products being connected end up in one of the two following roles associated with the termination of its port:

- Rp → VBUS and VCONN source and behaving as a downstream facing port (USB Host)
- Rd → VBUS sink and behaving as an upstream facing port (USB Device)

A USB Type-C DRP-based product may incorporate either or both the Try.SRC and Try.SNK swap mechanisms to affect the resulting role. Try.SRC allows a DRP that has a policy-based preference to be a Source when connecting to another DRP to affect a transition from a destined Sink role to the Source role. Alternately, Try.SNK allows a DRP that has a policy-based preference to be a Sink when connecting to another DRP to effect a transition from a destined Source role to the Sink role. Connection timing and other factors are involved in this process as defined in the USB Type-C state machine operation (see Section 4.5.2). It is important to note that these mechanisms, Try.SRC and Try.SNK, can only be used once as part of the initial connection process.

Try.SRC and Try.SNK are intended to ensure more predictable power roles when initially connecting two DRPs, especially if the port partner does not support *USB PD*. For example, a small mobile device may want to implement Try.SNK, so that when attaching to a DRP laptop, the mobile device will always initially be the power sink. Similarly, a laptop or Power Bank may wish to implement Try.SRC to ensure it always sources power to attached DRPs. Self-powered devices such as AMAs or those whose primary function is a data UFP may also consider implementing Try.SNK to ensure they can properly expose their functionality. If both sides support *USB PD*, the appropriate roles may then be further refined or swapped as per the *USB PD* specification.

4.5.1.4.2 USB PD-based Power Role, Data Role and VCONN Swapping

Following the completion of the initial USB Type-C state machine connection process, products may use *USB PD*-based swapping mechanisms to command a change power roles, data roles and which end of the cable will supply VCONN. These mechanisms are:

- *USB PD* PR_Swap : swaps Source (Rp) and Sink (Rd)
- *USB PD* DR_Swap : swaps DFP (host data) and UFP (device data) roles
- *USB PD* VCONN_Swap : swaps which port supplies VCONN

Table 4-12 summarizes the behaviors of a port in response to the three *USB PD* swap commands.

Table 4-12 USB PD Swapping Port Behavior Summary

	DFP/UFP Data Roles	Rp/Rd	VBUS Source/Sink	VCONN Source
PR_Swap	Unchanged	Swapped	Swapped	Unchanged
DR_Swap	Swapped	Unchanged	Unchanged	Unchanged
VCONN_Swap	Unchanged	Unchanged	Unchanged	Swapped*

* Swapping of VCONN source port

4.5.1.4.3 Power Role Behavioral Model Summary

Table 4-13 provides a summary of the defining characteristics of the seven fundamental power roles.

Table 4-13 Power Role Behavioral Model Summary

Power Role		Toggles	PR_Swap	USB Host	USB Device	DFP	UFP	DR_Swap	Try.SRC/ Try.SNK	Connects with
Source-Only		No	NA	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink/ DRP
Source (Default)		No	Req.	Opt.	Opt.[1]	Req.	Opt.	Opt.	NA	Sink/ DRP
Sink-Only		No	NA	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source/ DRP
Sink (Default)		No	Req.	Opt.[1]	Opt.	Opt.	Req.	Opt.	NA	Source/ DRP
DRP	**Toggling (Source/Sink)**	Req.	Req.	Opt.	Opt.	Req.	Req.	Req.	Opt.	Source/ Sink/ DRP
	Sourcing Device	Req.	Req.	NA	Req.	Req.	Req.	Req.	Opt.	
	Sinking Host	Req.	Req.	Req.	NA	Req.	Req.	Req.	Opt.	

Note: 1. Requires use of DR_Swap

4.5.2 CC Functional and Behavioral Requirements

This section provides the functional and behavioral requirements for implementing CC. The first sub-section provides connection state diagrams that are the basis for the remaining sub-sections.

The terms Source (SRC) and Sink (SNK) used in this section refer to the port's power role while the terms DFP and UFP refer to the port's data role. A DRP (Dual-Role-Power) port is capable of acting as either a Source or Sink. Typically, Sources are found on hosts and supply VBUS while a Sink is found on a device and consumes power from VBUS. When a connection is initially made, the port's initial power state and data role are established. *USB PD* introduces three swap commands that may alter a port's power or data role:

- The PR_Swap command changes the port's power state as reflected in the following state machines. PR_Swap does not change the port sourcing VCONN.
- The DR_Swap command has no effect on the following state machines or VCONN as it only changes the port's data role.
- VCONN_Swap command changes the port sourcing VCONN. The PR_Swap command and DR_Swap command have no effect on the port sourcing VCONN.

Note: A VCONN-Powered USB Device that supports the optional Charge-Through capability, once detected via *USB PD* messaging, will also change the Host-side port's power state without changing the port sourcing VCONN.

Note: *USB PD* defines another optional swapping mechanism (FR_Swap) that is used in a special case where a user interaction could inadvertently trigger a need to change the source of VBUS. A variant of PR_Swap, FR_Swap similarly swaps Source (Rp) and Sink (Rd) between two connected ports. For purposes of this specification, only PR_Swap is explicitly considered in the behavior requirements and implementations that support FR_Swap should, where applicable, apply PR_Swap-related behaviors to FR_Swap. See the *USB PD* specification for further details regarding FR_Swap.

The connection state diagrams and CC behavior descriptions in this section describe the behavior of receptacle-based ports. The plug on a direct connect device or a device with a captive cable shall behave as a plug on a cable that is attached at its other end in normal orientation to a receptacle, These devices shall apply and sense CC voltage levels on pin A5 only and pin B5 shall have an impedance above zOPEN, unless it is a VCONN-Powered Accessory, in which case B5 shall have an impedance Ra.

4.5.2.1 Connection State Diagrams

This section provides reference connection state diagrams for CC-based behaviors.

Refer to Section 4.5.2.2 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section 4.5.2.4 for a description of which states are mandatory for each port type, and a list of states where *USB PD* communication is permitted.

Figure 4-12 illustrates a connection state diagram for a Source (Host/Hub DFP).

Figure 4-12 Connection State Diagram: Source

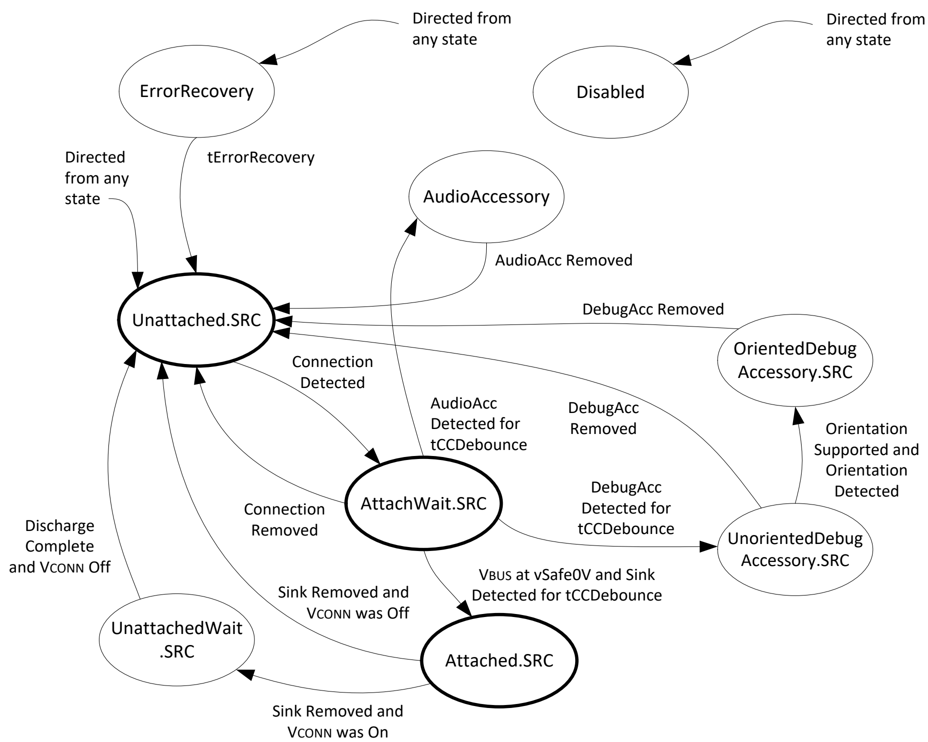


Figure 4-13 illustrates a connection state diagram for a simple Sink (Device/Hub UFP).

Figure 4-13 Connection State Diagram: Sink

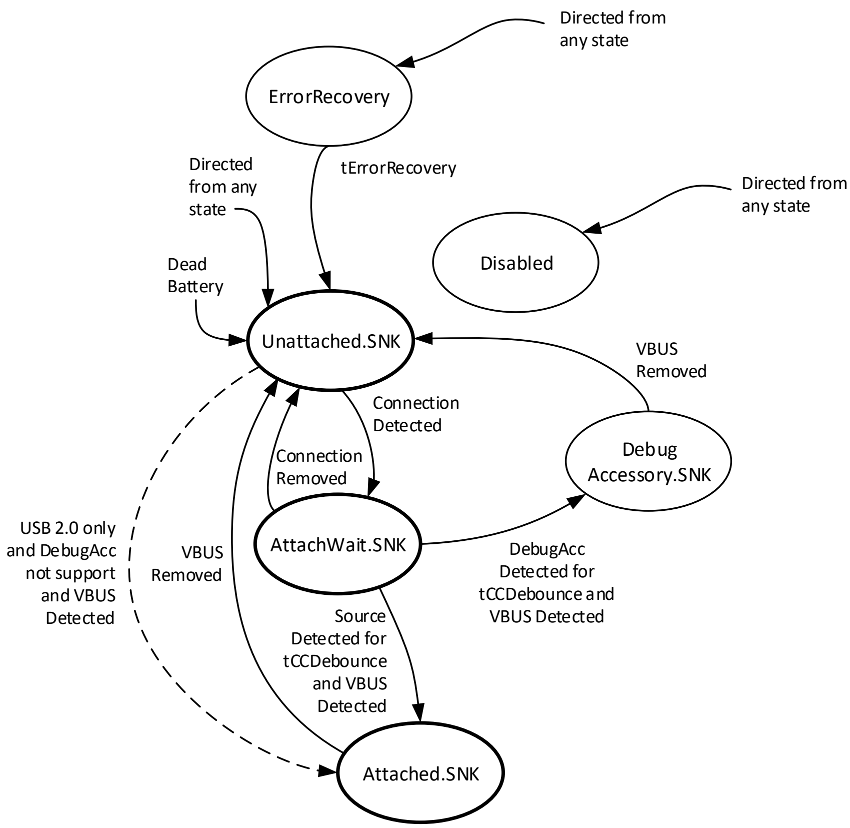


Figure 4-14 illustrates a connection state diagram for a Sink that supports Accessory Modes.

Figure 4-14 Connection State Diagram: Sink with Accessory Support

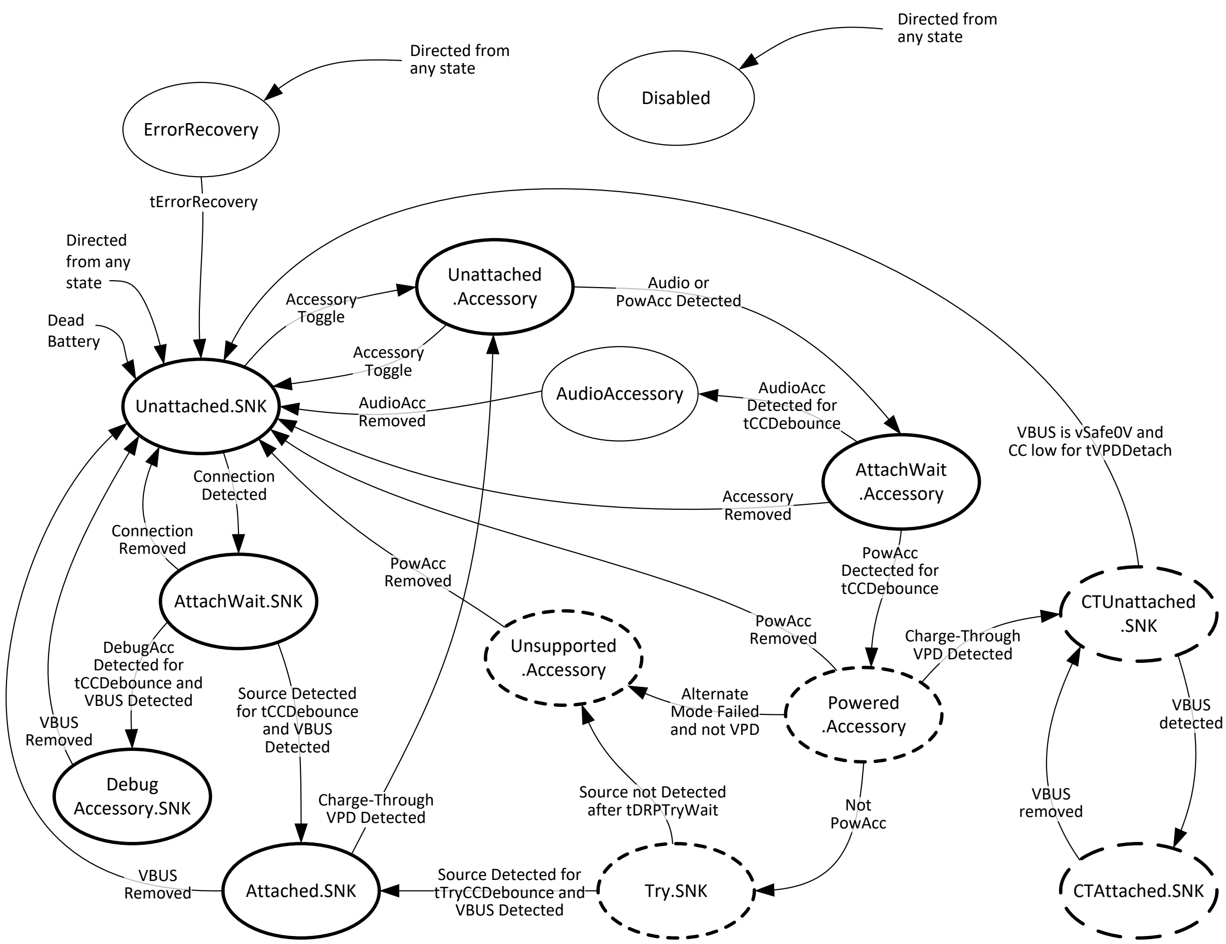


Figure 4-15 illustrates a connection state diagram for a simple DRP (Dual-Role-Power) port.

Figure 4-15 Connection State Diagram: DRP

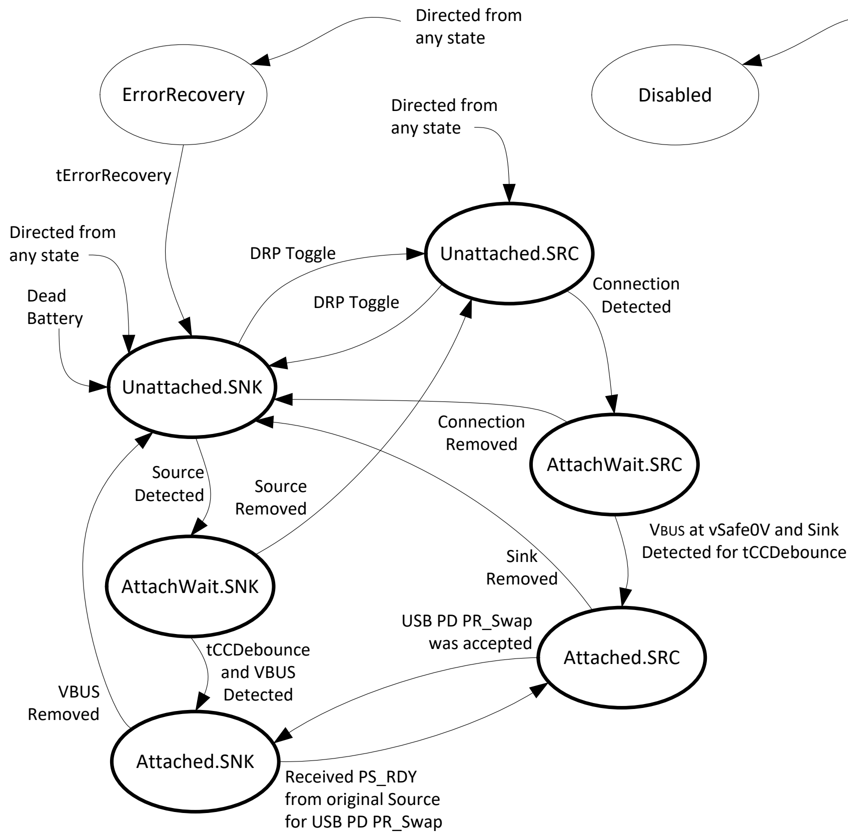


Figure 4-16 illustrates a connection state diagram for a DRP that supports Try.SRC and Accessory Modes.

Figure 4-16 Connection State Diagram: DRP with Accessory and Try.SRC Support

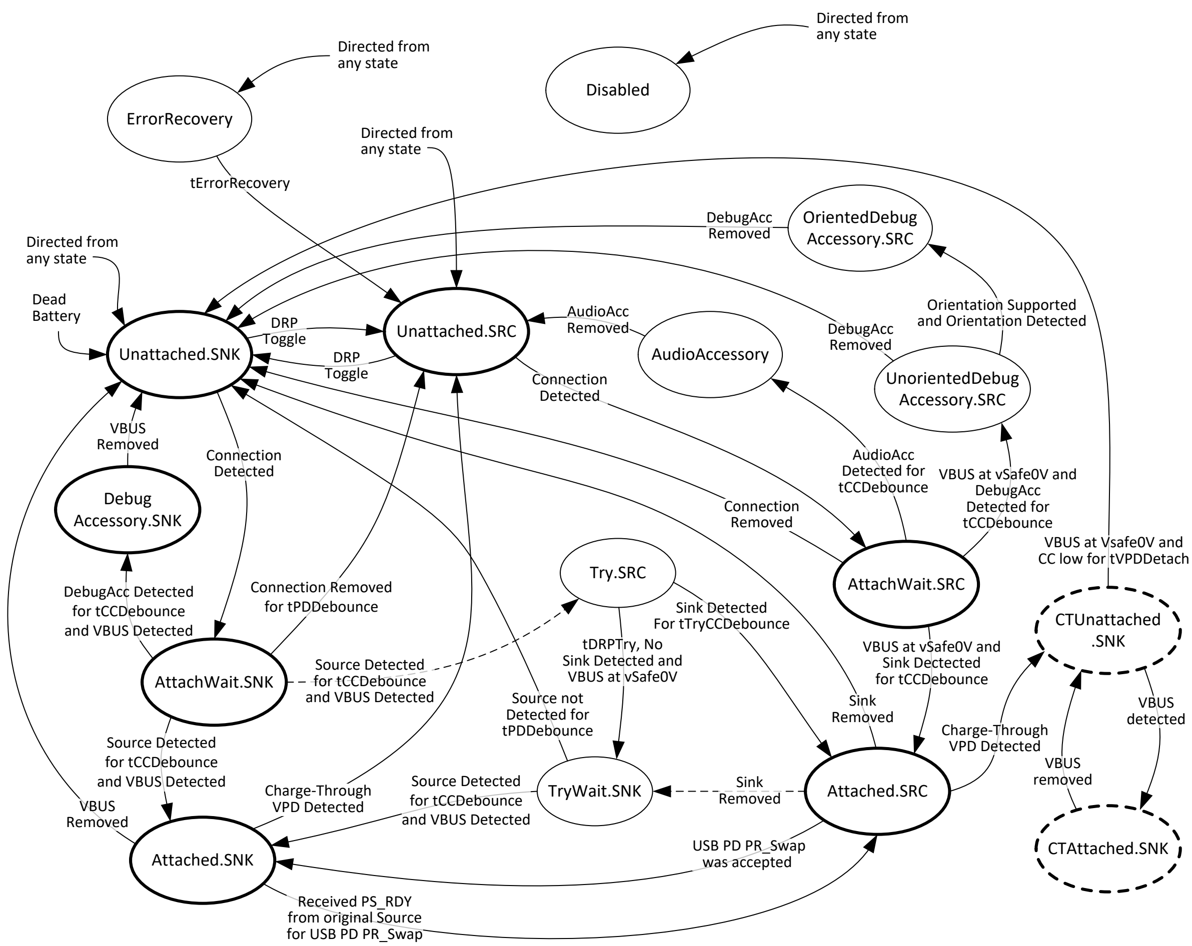


Figure 4-17 illustrates a connection state diagram for a DRP that supports Try.SNK and Accessory Modes.

Figure 4-17 Connection State Diagram: DRP with Accessory and Try.SNK Support

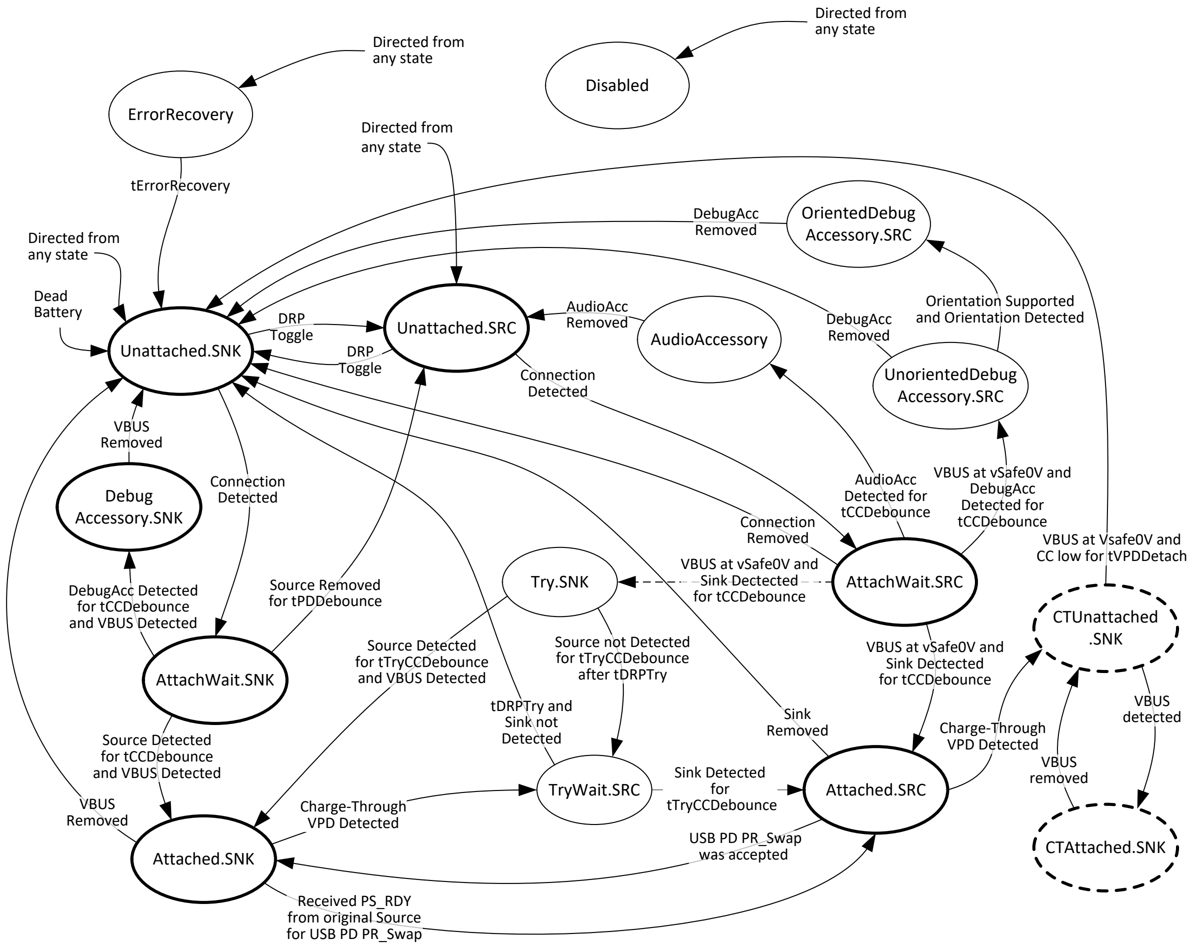
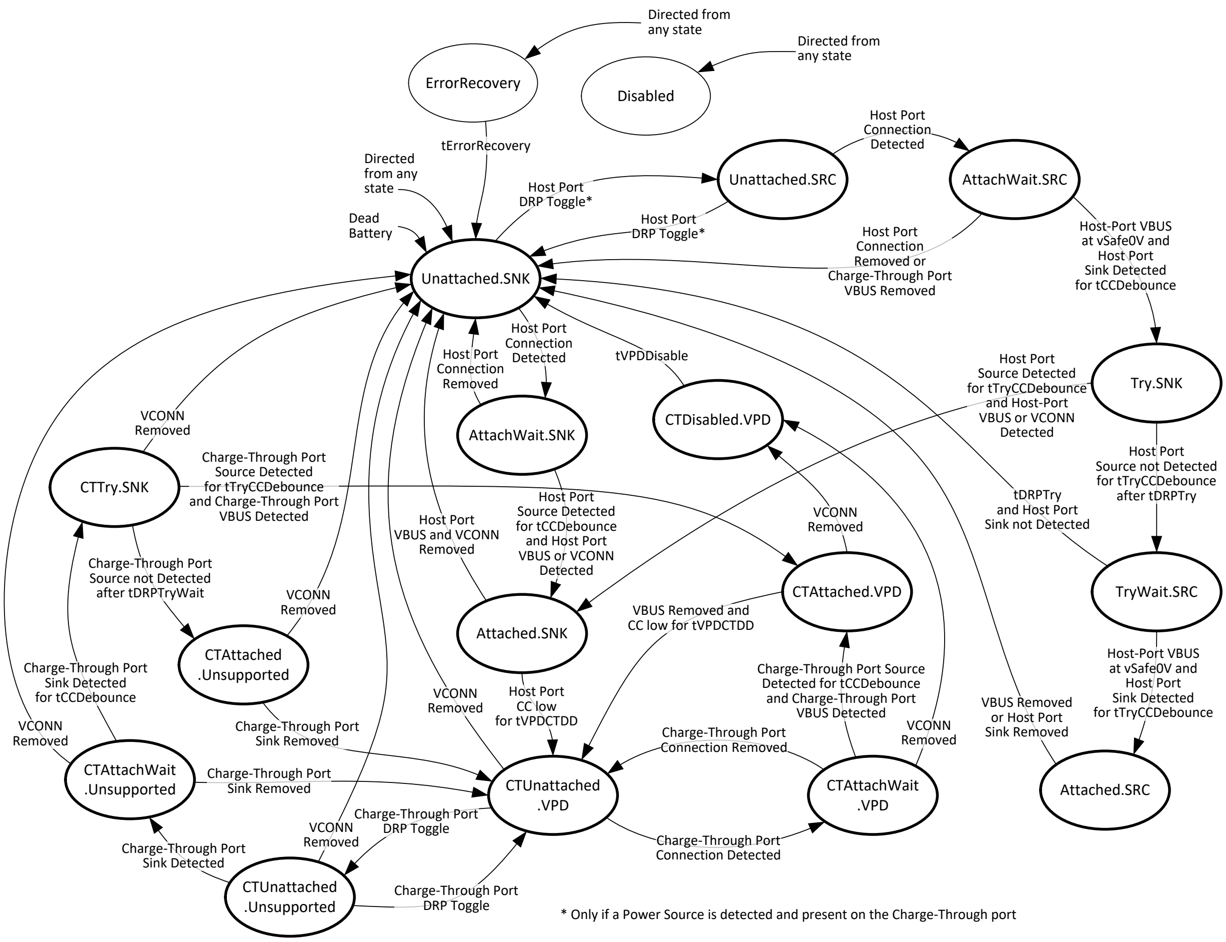


Figure 4-18 illustrates a connection state diagram for a Charge-Through VCONN-Powered USB Device.

Figure 4-18 Connection State Diagram: Charge-Through VPD



4.5.2.2 Connection State Machine Requirements

Entry into any unattached state when "directed from any state" shall not be used to override tDRP toggle.

A DRP or a Sink may consume default power from VBUS in any state where it is not required to provide VBUS.

The following two tables define the electrical states for a CC pin in both a Source and a Sink. Every port has CC1 and CC2 pins, each with its own individual CC pin state. The combination of a port's CC1 and CC2 pin states are be used to define the conditions under which a port transitions from one state to another.

Table 4-14 Source Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rp
SRC.Open	**Open, Rp**	Above vOPEN
SRC.Rd	**Rd**	Within the vRd range (i.e., between minimum vRd and maximum vRd)
SRC.Ra	**Ra**	Below maximum vRa

Table 4-15 Sink Port CC Pin State

CC Pin State	Port partner CC Termination	Voltage Detected on CC when port asserts Rd
SNK.Rp	**Rp**	Above minimum vRd-Connect
SNK.Open	**Open, Ra, Rd**	Below maximum vRa

4.5.2.2.1 Disabled State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

The Disabled state is where the port prevents connection from occurring by removing all terminations from the CC pins.

The port should transition to the Disabled state from any other state when directed. When the port transitions to the Disabled state from Attached.SNK, it shall keep all terminations on the CC pins removed for a minimum of tErrorRecovery.

A port may choose not to support the Disabled state. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states after power-on.

4.5.2.2.1.1 Disabled State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.

4.5.2.2.1.2 Exiting from Disabled State

A Sink shall transition to Unattached.SNK when directed.

A Source shall transition to Unattached.SRC when directed.

A DRP shall transition to either Unattached.SNK or Unattached.SRC when directed.

4.5.2.2.2 ErrorRecovery State

This state appears in Figure 4-12, Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16 and Figure 4-17.

The ErrorRecovery state is where the port removes the terminations from the CC1 and CC2 pins for tErrorRecovery followed by transitioning to the appropriate Unattached.SNK or Unattached.SRC state based on port type. This is the equivalent of forcing a detach event and looking for a new attach.

Ports that support *USB Power Delivery* shall support the ErrorRecovery state.

Ports that support the ErrorRecovery state shall transition to the ErrorRecovery state from any other state when directed.

A port that does not support *USB Power Delivery* may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the port shall be directed to the Disabled state if supported. If the Disabled state is not supported, the port shall be directed to either the Unattached.SNK or Unattached.SRC states.

4.5.2.2.2.1 ErrorRecovery State Requirements

The port shall not drive VBUS or VCONN, and shall present a high-impedance to ground (above zOPEN) on its CC1 and CC2 pins.

4.5.2.2.2.2 Exiting from ErrorRecovery State

A Sink shall transition to Unattached.SNK after tErrorRecovery.

A Source shall transition to Unattached.SRC after tErrorRecovery.

A DRP (Figure 4-15) and a DRP with Accessory and Try.SNK Support (Figure 4-17) shall transition to Unattached.SNK after tErrorRecovery.

A DRP with Accessory and Try.SRC Support (Figure 4-16) shall transition to Unattached.SRC after tErrorRecovery.

4.5.2.2.3 Unattached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Unattached.SNK state, the port is waiting to detect the presence of a Source.

A port with a dead battery shall enter this state while unpowered.

4.5.2.2.3.1 Unattached.SNK Requirements

The port shall not drive VBUS or VCONN.

Both CC1 and CC2 pins shall be independently terminated to ground through Rd.

A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.

4.5.2.2.3.2 Exiting from Unattached.SNK State

If the port supports *USB PD* or accessories, the port shall transition to AttachWait.SNK when the SNK.Rp state is present on at least one of its CC pins.

The maximum times that a Port shall take to transition to AttachWait.SNK are the following:

- tNoToggleConnect when neither Port Partner is toggling
- tOnePortToggleConnect when one Port Partner only is toggling

When both Port Partners are toggling, a Port should transition to AttachWait.SNK within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.

Note: The times tOnePortToggleConnect and tTwoPortToggleConnect relate to how long toggling ports may take to sync and detect a connection.

A *USB 2.0* only Sink that doesn't support accessories and is self-powered or requires only default power and does not support *USB PD* may transition directly to Attached.SNK when VBUS is detected.

A DRP shall transition to Unattached.SRC within tDRPTransition after the state of both CC pins is SNK.Open for tDRP − dcSRC.DRP · tDRP, or if directed.

A Sink with Accessory support shall transition to Unattached.Accessory within tDRPTransition after the state of both the CC1 and CC2 pins is SNK.Open for tDRP − dcSRC.DRP · tDRP, or if directed.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SRC within tDRPTransition after the state of the Host-side port's CC pin is SNK.Open for tDRP − dcSRC.DRP · tDRP and both of the following is detected on the Charge-Through port.

- SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce
- VBUS is detected

A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK when a Source connection is detected, as indicated by the SNK.Rp state on its Host-side port's CC pin.

4.5.2.2.4 AttachWait.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the AttachWait.SNK state, the port has detected the SNK.Rp state on at least one of its CC pins and is waiting for VBUS.

When in the AttachWait.SNK state, the Charge-Through VCONN-Powered USB Device has detected the SNK.Rp state on its Host-side port's CC pin and is waiting for host-side VBUS.

4.5.2.2.4.1 AttachWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, and independently terminate its Charge-Through port's CC1 and CC2 pins and Host-side port's CC pin to ground through Rd.

It is strongly recommended that a USB 3.2 SuperSpeed device hold off VBUS detection to the device controller until the Attached.SNK state or the DebugAccessory.SNK state is reached, i.e. at least one CC pin is in the SNK.Rp state. Otherwise, it may connect as *USB 2.0* when attached to a legacy host or hub's DFP.

4.5.2.2.4.2 Exiting from AttachWait.SNK State

A Sink shall transition to Unattached.SNK when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

A DRP shall transition to Unattached.SRC when the state of both the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

The port shall transition to Attached.SNK after the state of only one of the CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Open, but this event will not exceed tPDDebounce.

If the port is a VCONN-Powered Accessory or a VCONN-Powered USB Device, the port shall transition to Attached.SNK when either VCONN or VBUS is detected. The port may transition without waiting tCCDebounce on CC.

If the port supports Debug Accessory Mode, the port shall transition to DebugAccessory.SNK if the state of both the CC1 and CC2 pins is SNK.Rp for at least tCCDebounce and VBUS is detected. Note the DAM Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the CC pins with the state of the other CC pin remaining SNK.Rp, but this event will not exceed tPDDebounce.

A Charge-Through VCONN-Powered USB Device shall transition to Attached.SNK after the state of the Host-side port's CC pin is SNK.Rp for at least tCCDebounce and either host-side VCONN or VBUS is detected.

A DRP that strongly prefers the Source role may optionally transition to Try.SRC instead of Attached.SNK when the state of only one CC pin has been SNK.Rp for at least tCCDebounce and VBUS is detected.

4.5.2.2.5 Attached.SNK State

This state appears in Figure 4-13, Figure 4-14, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Attached.SNK state, the port is attached and operating as a Sink. When the port initially enters this state it is also operating as a UFP. The power and data roles can be changed using *USB PD* commands.

A port that entered this state directly from Unattached.SNK due to detecting VBUS shall not determine orientation or availability of higher than Default USB Power and shall not use *USB PD*.

4.5.2.2.5.1 Attached.SNK Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to this state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state).

If the port supports signaling on SuperSpeed USB pairs, it shall functionally connect the SuperSpeed USB pairs and maintain the connection during and after a *USB PD* PR_Swap.

If the port has entered the Attached.SNK state from the AttachWait.SNK or TryWait.SNK states, only one the CC1 or CC2 pins will be in the SNK.Rp state. The port shall continue to terminate this CC pin to ground through Rd.

If the port has entered the Attached.SNK state from the Attached.SRC state following a *USB PD* PR_Swap, the port shall terminate the connected CC pin to ground through Rd.

The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.22.

If the port is a VCONN-Powered USB Device, it shall respond to *USB PD* cable identity queries on SOP'. It shall not send or respond to messages on SOP. It shall ensure there is sufficient capacitance on CC to meet cReceiver as defined in *USB PD*.

A Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS, present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins and terminate its Host-side port's CC pin to ground through Rd.

A Charge-Through VCONN-Powered USB Device shall start a Charge-Through Support Timer when it enters the Attached.SNK state. If a Charge-Through VCONN-Powered USB Device fails to exit the Attached.SNK state before the Charge-Through Support Timer exceeds tAMETimeout, it shall present a USB Billboard Device Class interface indicating that it does not support Charge-Through.

A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it first receives any *USB PD* Structured VDM Command it supports. If a Charge-Through VCONN-Powered USB Device receives a Structured VDM Command multiple times, it shall only reset the Charge-Through Support Timer once. This ensures a Charge-Through VCONN-Powered USB Device will present a USB Billboard Device Class interface if it fails to exit Attached.SNK while receiving repeated or continuous Structured VDM Commands (e.g., Discover Identity).

A Charge-Through VCONN-Powered USB Device shall reset the Charge-Through Support Timer when it receives any Data Message it supports. A Charge-Through VCONN-Powered USB Device shall hold the Charge-Through Support Timer in reset while it is in any *USB PD* BIST mode.

Except for a VCONN-Powered USB Device or Charge-Through VCONN-Powered USB Device, the port may negotiate a *USB PD* PR_Swap, DR_Swap or VCONN_Swap.

If the port supports Charge-Through VCONN-Powered USB Device, and an explicit *USB PD* contract has failed to be negotiated, the port shall query the identity of the cable via *USB PD* on SOP'.

By default, upon entry from AttachWait.SNK or Unattached.SNK, VCONN shall not be supplied in the Attached.SNK state. If Attached.SNK is entered from Attached.SRC as a result of a *USB PD* PR_Swap, it shall maintain VCONN supply state, whether on or off, and its data role/connections. A *USB PD* DR_Swap has no effect on which port sources VCONN.

The port may negotiate a *USB PD* VCONN_Swap. When the port successfully executes *USB PD* VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes *USB PD* VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF.

4.5.2.2.5.2 Exiting from Attached.SNK State

A port that is not a VCONN-Powered USB Device and is not in the process of a *USB PD* PR_Swap or a *USB PD* Hard Reset or a *USB PD* FR_Swap shall transition to Unattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS operating at or below 5 V or below vSinkDisconnectPD when negotiated by *USB PD* to operate above 5 V.

A VCONN-Powered USB Device shall return to Unattached.SNK when VBUS has fallen below vSinkDisconnect and VCONN has fallen below vVCONNDisconnect.

A port that has entered into *USB PD* communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.

A port that is monitoring the CC voltage for disconnect (but is not in the process of a *USB PD* PR_Swap or *USB PD* FR_Swap) shall transition to Unattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.

If supplying VCONN, the port shall cease to supply it within tVCONNOFF of exiting Attached.SNK.

A Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD if VCONN is present and the state of its Host-side port's CC pin is SNK.Open for tVPDCTDD.

A port that via SOP' has detected an attached Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if implemented, or transition to Unattached.SRC or Unattached.Accessory if TryWait.SRC is not supported. This transition may be delayed until the device has sufficient battery charge needed to remain powered until it reaches the CTAttached.SNK state.

After receiving a *USB PD* PS_RDY from the original Source during a *USB PD* PR_Swap, the port shall transition directly to the Attached.SRC state (i.e., remove Rd from CC, assert Rp on CC and supply VBUS), but shall maintain its VCONN supply state, whether off or on, and its data role/connections.

4.5.2.2.6 UnattachedWait.SRC State

This state appears in Figure 4-12.

When in the UnattachedWait.SRC state, the port is discharging the CC pin that was providing VCONN in the previous Attached.SRC state.

4.5.2.2.6.1 UnattachedWait.SRC Requirements

The port shall not enable VBUS or VCONN.

The port shall complete the VCONN turn off initiated when leaving the previous Attached.SRC state.

The port shall continue to provide an Rp termination, as specified in Table 4-24, on the CC pin not being discharged.

The port shall not provide an Rp termination on the CC pin being discharged.

The port shall provide an Rdch termination on the CC pin being discharged.

The port shall discharge the CC pin being discharged below vVCONNDischarge.

4.5.2.2.6.2 Exiting from UnattachedWait.SRC State

The port shall transition to Unattached.SRC when VCONN is below vVCONNDischarge. The port may delay this transition to allow the cable plug more time to reapply Ra.

4.5.2.2.7 Unattached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Unattached.SRC state, the port is waiting to detect the presence of a Sink or an Accessory.

When in the Unattached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Source on its Charge-Through port and is independently monitoring its Host-side port to detect the presence of a Sink.

4.5.2.2.7.1 Unattached.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide a separate Rp termination on the CC1 and CC2 pins as specified in Table 4-24. Note: A Source with a captive cable or just a plug presents a single Rp termination on its CC pin (A5).

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.

Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall remove its Rd termination to ground on the Host-side port CC and provide an Rp termination instead advertising Default USB Power, as specified in Table 4-24, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.

4.5.2.2.7.2 Exiting from Unattached.SRC State

The port shall transition to AttachWait.SRC when:

- The SRC.Rd state is present on either the CC1 or CC2 pin or
- The SRC.Ra state is present on both the CC1 and CC2 pins.

The maximum times that a Port shall take to transition to AttachWait.SRC are the following:

- tNoToggleConnect when neither Port Partner is toggling
- tOnePortToggleConnect when one Port Partner only is toggling

When both Port Partners are toggling, a Port should transition to AttachWait.SRC within tTwoPortToggleConnect. Note that when both Port Partners are DRPs it is indeterminate whether the local port will transition to AttachWait.SRC or AttachWait.SNK.

Note: The times tOnePortToggleConnect and tTwoPortToggleConnect relate to how long toggling ports may take to sync and detect a connection.

Note: A cable without an attached device can be detected, when the SRC.Ra state is detected on one of the CC1 or CC2 pins and the other CC pin is SRC.Open. However in this case, the port shall not transition to AttachWait.SRC.

The Charge-Through VCONN-Powered USB Device shall transition to AttachWait.SRC when host-side VBUS is vSafe0V and SRC.Rd state is detected on the Host-side port's CC pin.

A DRP shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if Charge-Through VBUS is removed.

4.5.2.2.8 AttachWait.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

The AttachWait.SRC state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a Sink is connected.

When in the AttachWait.SRC state, the Charge-Through VCONN-Powered USB Device ensures that the state of Host-side port's CC pin is stable after a Sink is connected.

4.5.2.2.8.1 AttachWait.SRC Requirements

The requirements for this state are identical to Unattached.SRC.

4.5.2.2.8.2 Exiting from AttachWait.SRC State

The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Try.SNK when the host-side VBUS is at vSafe0V and the SRC.Rd state is on the Host-side port's CC pin for at least tCCDebounce.

If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the SRC.Ra state is detected on both the CC1 and CC2 pins for at least tCCDebounce.

If the port supports Debug Accessory Mode, it shall transition to UnorientedDebugAccessory.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both the CC1 and CC2 pins for at least tCCDebounce.

A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on both the CC1 and CC2 pins. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

A Source shall transition to Unattached.SRC and a DRP to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin and the other CC pin is SRC.Ra. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when the SRC.Open state is detected on the Host-side port's CC or if Charge-Through VBUS falls below vSinkDisconnect. The Charge-Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

A DRP that strongly prefers the Sink role may optionally transition to Try.SNK instead of Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tCCDebounce.

4.5.2.2.9 Attached.SRC State

This state appears in Figure 4-12, Figure 4-15, Figure 4-16, Figure 4-17 and Figure 4-18.

When in the Attached.SRC state, the port is attached and operating as a Source. When the port initially enters this state it is also operating as a DFP. Subsequently, the initial power and data roles can be changed using *USB PD* commands.

When in the Attached.SRC state, the Charge-Through VCONN-Powered USB Device has detected a Sink on its Host-side port and has connected the Charge-Through port VBUS to the Host-side port VBUS.

4.5.2.2.9.1 Attached.SRC Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the Attached.SRC state by detecting which of the CC1 or CC2 pins is connected through the cable, i.e., which CC pin is in the SRC.Rd state.

If the port has entered this state from the AttachWait.SRC state or the Try.SRC state, the SRC.Rd state will be on only one of the CC1 or CC2 pins. The port shall source current on this CC pin and monitor its state.

If the port has entered this state from the Attached.SNK state as the result of a *USB PD* PR_Swap, the port shall source current on the connected CC pin and monitor its state.

The port shall provide an Rp as specified in Table 4-24.

The port shall supply VBUS current at the level it advertises on Rp.

The port shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.

The port shall not initiate any *USB PD* communications until VBUS reaches vSafe5V.

If the port supports signaling on SuperSpeed USB pairs, it shall:

- Functionally connect the SuperSpeed USB pairs
- For VCONN, do one of two things:
    - Supply VCONN unconditionally to the CC pin not in the SRC.Rd state, or
    - Supply VCONN to the CC pin in the SRC.Ra state.

A port that does not support signaling on SuperSpeed USB pairs may supply VCONN in the same manner described above.

The port may negotiate a *USB PD* PR_Swap, DR_Swap or VCONN_Swap.

If the port supplies VCONN, it shall do so within tVCONNON.

The port may query the identity of the cable via *USB PD* on SOP'. If it detects that it is connected to a VCONN-Powered USB Device, the port may remove VBUS and discharge it to vSafe0V, while continuing to remain in this state with VCONN applied. The port may also initiate other SOP' communication.

The port shall not supply VCONN if it has entered this state as a result of a *USB PD* PR_Swap and was not previously supplying VCONN. A *USB PD* DR_Swap has no effect on which port sources VCONN.

The port may negotiate a *USB PD* VCONN_Swap. When the port successfully executes *USB PD* VCONN_Swap operation and was sourcing VCONN, it shall stop sourcing VCONN within tVCONNOFF. The port shall execute the VCONN_Swap in a make-before-break sequence in order to keep active USB Type-C to USB Type-C cables powered. When the port successfully executes *USB PD* VCONN_Swap operation and was not sourcing VCONN, it shall start sourcing VCONN within tVCONNON.

The Charge-Through VCONN-Powered USB Device shall continue to isolate its Host-side port's CC pin from its Charge-Through CC pins.

The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising Default USB Power on the Host-side port's CC pin, and continue to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.

The Charge-Through VCONN-Powered USB Device shall immediately connect the Charge-Through port's VBUS through to the Host-side port's VBUS.

The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

4.5.2.2.9.2 Exiting from Attached.SRC State

A Source that is supplying VCONN or has yielded VCONN source responsibility to the Sink through *USB PD* VCONN_Swap messaging shall transition to UnattachedWait.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

A Source that is not supplying VCONN and has not yielded VCONN responsibility to the Sink through *USB PD* VCONN_Swap messaging shall transition to Unattached.SRC when the SRC.Open state is detected on the monitored CC pin. The Source shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

When the SRC.Open state is detected on the monitored CC pin, a DRP shall transition to Unattached.SNK unless it strongly prefers the Source role. In that case, it shall transition to TryWait.SNK. This transition to TryWait.SNK is needed so that two devices that both prefer the Source role do not loop endlessly between Source and Sink. In other words, a DRP that would enter Try.SRC from AttachWait.SNK shall enter TryWait.SNK for a Sink detach from Attached.SRC.

A DRP that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONN-Powered USB Device in its Discover Identity Command response. The DRP may delay this transition in order to perform further SOP' communication.

A port shall cease to supply VBUS within tVBUSOFF of exiting Attached.SRC.

A port that is supplying VCONN shall cease to supply it within tVCONNOFF of exiting Attached.SRC, unless it is exiting as a result of a *USB PD* PR_Swap or is transitioning into the CTUnattached.SNK state.

After a *USB PD* PR_Swap is accepted (i.e., either an Accept message is received or acknowledged), a DRP shall transition directly to the Attached.SNK state (i.e., remove Rp from CC, assert Rd on CC and stop supplying VBUS) and maintain its current data role, connection and VCONN supply state.

A Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK when VBUS falls below vSinkDisconnect or the Host-side port's CC pin is SRC.Open. The Charge-Through VCONN-Powered USB Device shall detect the SRC.Open state within tSRCDisconnect, but should detect it as quickly as possible.

4.5.2.2.10 Try.SRC State

This state appears in Figure 4-16.

When in the Try.SRC state, the port is querying to determine if the port partner supports the Sink role.

Note: if both Try.SRC and Try.SNK mechanisms are implemented, only one shall be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.10.1 Try.SRC Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide an Rp as specified in Table 4-24.

4.5.2.2.10.2 Exiting from Try.SRC State

The port shall transition to Attached.SRC when the SRC.Rd state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce.

The port shall transition to TryWait.SNK after tDRPTry and the SRC.Rd state has not been detected and VBUS is within vSafe0V, or after tTryTimeout and the SRC.Rd state has not been detected.

4.5.2.2.11 TryWait.SNK State

This state appears in Figure 4-16.

When in the TryWait.SNK state, the port has failed to become a Source and is waiting to attach as a Sink. Alternatively the port is responding to the Sink being removed while in the Attached.SRC state.

4.5.2.2.11.1 TryWait.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

4.5.2.2.11.2 Exiting from TryWait.SNK State

The port shall transition to Attached.SNK after tCCDebounce if or when VBUS is detected. Note the Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tPDDebounce.

The port shall transition to Unattached.SNK when the state of both of the CC1 and CC2 pins is SNK.Open for at least tPDDebounce.

4.5.2.2.12 Try.SNK State

This state appears in Figure 4-14, Figure 4-17 and Figure 4-18.

When in the Try.SNK state, the port is querying to determine if the port partner supports the Source role.

When in the Try.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Host-side port supports the Source role.

Note: if both Try.SRC and Try.SNK mechanisms are implemented, only one shall be enabled by the port at any given time. Deciding which of these two mechanisms is enabled is product design-specific.

4.5.2.2.12.1 Try.SNK Requirements

The port shall not drive VBUS or VCONN.

Both the CC1 and CC2 pins shall be independently terminated to ground through Rd.

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VBUS from the Charge-Through port.

The Charge-Through VCONN-Powered USB Device shall remove its Rp termination (Default USB Power advertisement) on the Host-side port CC and provide an Rd termination to ground instead, as specified in Table 4-24 and remain to independently terminate its Charge-Through port's CC1 and CC2 pins to ground through Rd.

4.5.2.2.12.2 Exiting from Try.SNK State

The port shall wait for tDRPTry and only then begin monitoring the CC1 and CC2 pins for the SNK.Rp state.

The port shall then transition to Attached.SNK when the SNK.Rp state is detected on exactly one of the CC1 or CC2 pins for at least tTryCCDebounce and VBUS is detected.

Alternatively, the port shall transition to TryWait.SRC if SNK.Rp state is not detected for tTryCCDebounce.

The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Host-side port's CC pin for the SNK.Rp state.

The Charge-Through VCONN-Powered USB Device shall then transition to Attached.SNK when the SNK.Rp state is detected on the Host-side port's CC pin for at least tTryCCDebounce and VBUS or VCONN is detected on Host-side port.

Alternatively, the Charge-Through VCONN-Powered USB Device shall transition to TryWait.SRC if Host-side SNK.Rp state is not detected for tTryCCDebounce.

A Sink with Accessory Support shall transition to Unsupported.Accessory if SNK.Rp state is not detected for tDRPTryWait.

Note: The Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tTryCCDebounce.

4.5.2.2.13 TryWait.SRC State

This state appears in Figure 4-17 and Figure 4-18.

When in the TryWait.SRC state, the port has failed to become a Sink and is waiting to attach as a Source.

When in the TryWait.SRC state, the Charge-Through VCONN-Powered USB Device has failed to become a Sink on its Host-side port and is waiting to attach as a Source on its Host-side port.

4.5.2.2.13.1 TryWait.SRC Requirements

The requirements for this state are identical to Unattached.SRC.

4.5.2.2.13.2 Exiting from TryWait.SRC State

The port shall transition to Attached.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on exactly one of the CC pins for at least tTryCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Attached.SRC when host-side VBUS is at vSafe0V and the SRC.Rd state is detected on the Host-side port's CC pin for at least tTryCCDebounce.

The port shall transition to Unattached.SNK after tDRPTry if neither of the CC1 or CC2 pins are in the SRC.Rd state.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tDRPTry if the Host-side port's CC pin is not in the SRC.Rd state.

4.5.2.2.14 Unattached.Accessory State

This state appears in Figure 4-14.

The Unattached.Accessory state allows accessory-supporting Sinks to connect to audio or VCONN-Powered Accessories.

This state is functionally equivalent to the Unattached.SRC state in a DRP, except that Attached.SRC is not supported.

4.5.2.2.14.1 Unattached.Accessory Requirements

The port shall not drive VBUS or VCONN.

The port shall source current on both the CC1 and CC2 pins independently.

The port shall provide an Rp as specified in Table 4-24.

4.5.2.2.14.2 Exiting from Unattached.Accessory State

A port that supports Audio Adapter Accessory Mode shall transition to AttachWait.Accessory when the state of both CC pins is SRC.Ra.

A port that supports VCONN-Powered Accessories also shall transition to AttachWait.Accessory when the state of either CC1 or CC2 pin is SRC.Ra and the other CC pin is SRC.Rd.

The maximum time the local port shall take to transition from Unattached.Accessory to the AttachWait.Accessory state when an Audio Adapter Accessory or VCONN-Powered Accessory is present is tOnePortToggleConnect.

Otherwise, the port shall transition to Unattached.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

4.5.2.2.15 AttachWait.Accessory State

This state appears in Figure 4-14.

The AttachWait.Accessory state is used to ensure that the state of both of the CC1 and CC2 pins is stable after a cable is plugged in.

4.5.2.2.15.1 AttachWait.Accessory Requirements

The requirements for this state are identical to Unattached.Accessory.

4.5.2.2.15.2 Exiting from AttachWait.Accessory State

If the port supports Audio Adapter Accessory Mode, it shall transition to AudioAccessory when the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.

The port shall transition to Unattached.SNK when the state of either the CC1 or CC2 pin is SRC.Open for at least tCCDebounce.

If the port supports VCONN-Powered Accessories, it shall transition to PoweredAccessory state if the state of either the CC1 or CC2 pin is SRC.Rd and the other CC pin is SRC.Ra concurrently for at least tCCDebounce.

4.5.2.2.16 AudioAccessory State

This state appears in Figure 4-12, Figure 4-14, Figure 4-16 and Figure 4-17.

The AudioAccessory state is used for the Audio Adapter Accessory Mode specified in Appendix A.

4.5.2.2.16.1 AudioAccessory Requirements

The port shall reconfigure its pins as detailed in Appendix A.

The port shall not drive VBUS or VCONN. A port that sinks current from the audio accessory over VBUS shall not draw more than 500 mA.

The port shall provide an Rp as specified in Table 4-24.

The port shall source current on at least one of the CC1 or CC2 pins and monitor to detect when the state is no longer SRC.Ra. If the port sources and monitors only one of CC1 or CC2, then it shall ensure that the termination on the unmonitored CC pin does not affect the monitored signal when the port is connected to an Audio Accessory that may short both CC1 and CC2 pins together.

4.5.2.2.16.2 Exiting from AudioAccessory State

If the port is a Sink, the port shall transition to Unattached.SNK when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.

If the port is a Source or DRP, the port shall transition to Unattached.SRC when the state of the monitored CC1 or CC2 pin(s) is SRC.Open for at least tCCDebounce.

4.5.2.2.17 UnorientedDebugAccessory.SRC

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The UnorientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.17.1 UnorientedDebugAccessory.SRC Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.

The port may connect any non-orientation specific debug signals for Debug Accessory Mode operation only after entry to this state.

4.5.2.2.17.2 Exiting from UnorientedDebugAccessory.SRC State

If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.

The port shall transition to OrientedDebugAccessory.SRC state if orientation is required and detected as described in Section B.2.6.1.2.

4.5.2.2.18 OrientedDebugAccessory.SRC State

This state appears in Figure 4-12, Figure 4-16 and Figure 4-17.

The OrientedDebugAccessory.SRC state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.18.1 OrientedDebugAccessory.SRC State Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall provide an Rp as specified in Table 4-24 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

The port shall supply VBUS current at the level it advertises on Rp. The port shall not drive VCONN.

The port shall connect any orientation specific debug signals for Debug Accessory Mode operation only after entry to this state. Any non-orientation specific debug signals for Debug Accessory Mode operation shall be connected or remain connected in this state.

If the port needs to establish *USB PD* communications, it shall do so only after entry to this state. The port shall not initiate any *USB PD* communications until VBUS reaches vSafe5V. In this state, the port takes on the initial *USB PD* role of DFP/Source.

4.5.2.2.18.2 Exiting from OrientedDebugAccessory.SRC State

If the port is a Source, the port shall transition to Unattached.SRC when the SRC.Open state is detected on either the CC1 or CC2 pin.

If the port is a DRP, the port shall transition to Unattached.SNK when the SRC.Open state is detected on either the CC1 or CC2 pin.

4.5.2.2.19 DebugAccessory.SNK

This state appears in Figure 4-13, Figure 4-14, Figure 4-16 and Figure 4-17.

The DebugAccessory.SNK state is used for the Debug Accessory Mode specified in Appendix B.

4.5.2.2.19.1 DebugAccessory.SNK Requirements

This mode is for debug only and shall not be used for communicating with commercial products.

The port shall not drive VBUS or VCONN.

The port shall provide an Rd as specified in Table 4-25 on both the CC1 and CC2 pins and monitor to detect when the state of either is SRC.Open.

If supported, orientation is determined as outlined in Section B.2.6.1.1. The port shall connect any debug signals for Debug Accessory Mode operation only after entry to this state.

4.5.2.2.19.2 Exiting from DebugAccessory.SNK State

The port shall transition to Unattached.SNK when VBUS is no longer present.

4.5.2.2.20 PoweredAccessory State

This state appears in Figure 4-14.

When in the PoweredAccessory state, the port is powering a VCONN–Powered Accessory or VCONN-Powered USB Device.

4.5.2.2.20.1 PoweredAccessory Requirements

If the port needs to determine the orientation of the connector, it shall do so only upon entry to the PoweredAccessory state by detecting which of the CC1 or CC2 pins is connected through the cable (i.e., which CC pin is in the SRC.Rd state).

The SRC.Rd state is detected on only one of the CC1 or CC2 pins. The port shall advertise either 1.5 A or 3.0 A (see Table 4-24) on this CC pin and monitor its state.

The port shall supply VCONN on the unused CC pin within tVconnON-PA of entering the PoweredAccessory state.

The port shall not drive VBUS.

When the port initially enters the PoweredAccessory state it shall operate as a *USB Power Delivery* Source with a DFP data role. In addition, the port shall support at least one of the following:

- Use *USB PD* to establish an explicit contract and then use Structured Vendor Defined Messages (Structured VDMs) to identify a VCONN–Powered Accessory and enter an Alternate Mode.

- Use *USB PD* to query the identity of a VCONN-Powered USB Device (that operates as a cable plug responding to SOP').

4.5.2.2.20.2 Exiting from PoweredAccessory State

The port shall transition to Unattached.SNK when the SRC.Open state is detected on the monitored CC pin.

The port shall transition to Try.SNK if the attached device is not a VCONN–Powered Accessory or VCONN-Powered USB Device. For example, the attached device does not support *USB PD* or does not respond to *USB PD* commands required for a VCONN–Powered Accessory (e.g., Discover SVIDs, Discover Modes, etc.) or is a Sink or DRP attached through a Powered Cable.

The port shall transition to Unsupported.Accessory if the attached device is a VCONN–Powered Accessory but the port has not successfully entered an Alternate Mode within tAMETimeout (see Appendix E).

A port that supports Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.SNK if the connected device identifies itself as a Charge-Through VCONN-Powered USB Device in its Discover Identity Command response. The port may delay this transition in order to perform further SOP' communication.

The port shall cease to supply VCONN within tVCONNOFF of exiting the PoweredAccessory state unless it is transitioning into the CTUnattached.SNK state.

4.5.2.2.21 Unsupported.Accessory State

This state appears in Figure 4-14.

If a VCONN–Powered Accessory does not enter an Alternate Mode, the Unsupported.Accessory state is used to wait until the accessory is unplugged before continuing.

4.5.2.2.21.1 Unsupported.Accessory Requirements

Only one of the CC1 or CC2 pins shall be in the SRC.Rd state. The port shall advertise Default USB Power (see Table 4-24) on this CC pin and monitor its voltage.

The port shall not drive VBUS or VCONN.

A Sink with either VCONN–Powered Accessory or VCONN-Powered USB Device support shall provide user notification that it does not recognize or support the attached accessory or device.

4.5.2.2.21.2 Exiting from Unsupported.Accessory

The port shall transition to Unattached.SNK when the SRC.Open state is detected on the monitored CC pin.

4.5.2.2.22 CTUnattached.VPD State

This state appears in Figure 4-18.

When in the CTUnattached.VPD state, the Charge-Through VCONN-Powered USB Device has detected SNK.Open on its host port for tVPDCTDD, indicating that it is connected to a Charge-Through capable Source, and is independently monitoring its Charge-Through port for the presence of a pass-through Power Source.

This state may also have been entered through detach of a Power Source on the Charge-Through port or detach of a sink from the CTVPD's Charge-through port.

4.5.2.2.22.1 CTUnattached.VPD Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the device shall remove its Rd termination to ground (if present) on the Host-side port CC and provide an Rp termination advertising 3.0 A instead, as specified in Table 4-24. Note that because VBUS is not provided, the Rp termination signals continued connection to the port partner but does not carry with it any current advertisement.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

The Charge-Through VCONN-Powered USB Device shall independently terminate both the Charge-Through port's CC1 and CC2 pins to ground through Rd.

The Charge-Through VCONN-Powered USB Device shall provide a bypass capacitance of CCTB on the Charge-Through Port's VBUS pins.

4.5.2.2.22.2 Exiting from CTUnattached.VPD

The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.VPD when a Source connection is detected on the Charge-Through port, as indicated by the SNK.Rp state on exactly one of the Charge-Through port's CC pins.

Debug accessories are not supported on the Charge-Through port.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.Unsupported within tDRPTransition after the state of both the Charge-Through port's CC1 and CC2 pins is SNK.Open for tDRP – dcSRC.DRP ∙ tDRP, or if directed.

4.5.2.2.23 CTAttachWait.VPD State

This state appears in Figure 4-18.

When in the CTAttachWait.VPD state, the device has detected the SNK.Rp state on exactly one of its Charge-Through port's CC pins and is waiting for VBUS on the Charge-Through port.

4.5.2.2.23.1 CTAttachWait.VPD Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

The Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, as well as the independent terminations to ground through Rd on the Charge-Through port's CC1 and CC2 pins.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port, and complete any active queries prior to exiting this state. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

4.5.2.2.23.2 Exiting from CTAttachWait.VPD

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of both the Charge-Through port's CC1 and CC2 pins are SNK.Open for at least tPDDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to CTAttached.VPD after the state of only one of the Charge-Through port's CC1 or CC2 pins is SNK.Rp for at least tCCDebounce and VBUS on the Charge-Through port is detected.

Note the Charge-Through Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on one of the Charge-Through port's CC pins with the state of the Charge-Through port's other CC pin remaining SNK.Open, but this event will not exceed tPDDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to CTDisabled.VPD if VCONN falls below vVCONNDisconnect.

4.5.2.2.24 CTAttached.VPD State

This state appears in Figure 4-18.

When in the CTAttached.VPD state, the Charge-Through VCONN-Powered USB Device has detected a Power Source on its Charge-Through port and has connected the Charge-Through port's CC and VBUS pins directly to the Host-side port's CC and VBUS pins. Hence all power delivery, negotiation and *USB PD* communication are performed directly between the unit on Host-side port and the Power Source connected to the Charge-Through port.

4.5.2.2.24.1 CTAttached.VPD Requirements

Upon entry to this state, the Charge-Through VCONN-Powered USB Device shall detect which of the Charge-Through port's CC1 or CC2 pins is connected through the cable (i.e., the CC pin that is in the SNK.Rp state). The device shall then immediately, in the following order:

1. Remove or reduce any additional capacitance on the Host-side CC port that was introduced in order to meet cReceiver as defined in *USB PD* to present on CC a value equal to or less than two times the maximum value for cCablePlug_CC.
2. Disable the Rp termination advertising 3.0 A on the host port's CC pin.
3. Passively multiplex the detected Charge-Through port's CC pin through to the host port's CC pin with an impedance of less than RccCON.
4. Disable the Rd on the Charge-Through port's CC1 and CC2 pins.
5. Connect the Charge-Through port's VBUS through to the host port's VBUS.

These steps shall be completed within tVPDDetach minimum of entering this state.

The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

The Charge-Through VCONN-Powered USB Device shall not respond to any *USB PD* communication on any CC pin in this state. Any active queries on SOP' shall have been completed prior to entering this state.

4.5.2.2.24.2 Exiting from CTAttached.VPD

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when VBUS falls below vSinkDisconnect and the state of the passed-through CC pin is SNK.Open for tVPDCTDD.

The Charge-Through VCONN-Powered USB Device shall transition to CTDisabled.VPD if VCONN falls below vVCONNDisconnect.

4.5.2.2.25 CTDisabled.VPD State

This state appears in Figure 4-18.

When in the CTDisabled.VPD state, the Charge-Through VCONN-Powered USB Device has detected the detach on its Host-side port but may still potentially be connected to a Power Source on the Charge-Through port, and is thus ensuring that the VBUS from the Power Source is removed.

4.5.2.2.25.1 CTDisabled.VPD Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS.

The device shall present a high-impedance to ground (above zOPEN) on the Host-side port's CC pin and on the Charge-Through port CC1 and CC2 pins.

The Charge-Through VCONN-Powered USB Device shall ensure that it is powered entirely by VBUS.

4.5.2.2.25.2 Exiting from CTDisabled.VPD

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK after tVPDDisable.

4.5.2.2.26 CTUnattached.SNK State

This state appears in Figure 4-14, Figure 4-16 and Figure 4-17.

When in the CTUnattached.SNK state, the port has detected that it is attached to a Charge-Through VCONN-Powered USB Device and is ready if a Power Source is attached to the Charge-Through VCONN-Powered USB Device.

This state may also have been entered through detach of a Charge-Through Power Source.

4.5.2.2.26.1 CTUnattached.SNK Requirements

Upon entry to this state, the port shall remove its Rp termination (if present) and terminate CC to ground through Rd.

The port shall continue to supply VCONN.

The port shall stop sourcing or sinking VBUS and discharge it.

In *USB PD* Version 2.0, the port shall initiate PD messages.

The port may query the state of the attached VCONN-Powered USB Device by sending SOP' messages on *USB PD* to read the VPD's eMarker.

4.5.2.2.26.2 Exiting from CTUnattached.SNK

The port shall transition to CTAttached.SNK when VBUS is detected. Note that by this point, the VCONN-Powered USB Device has already de-bounced the passed-through CC pin.

The port shall transition to Unattached.SNK if the state of the CC pin is SNK.Open for tVPDDetach after VBUS is vSafe0V.

4.5.2.2.27 CTAttached.SNK State

This state appears in Figure 4-14, Figure 4-16 and Figure 4-17.

When in the CTAttached.SNK state, the port is connected to a Charge-Through VCONN-Powered USB Device, which in turn is passing through the connection to a Power Source.

4.5.2.2.27.1 CTAttached.SNK Requirements

The port shall continue to terminate CC to ground through Rd. Since there is now a Power Source connected through to VBUS and CC, the port shall operate in one of the Sink Power Sub-States shown in Figure 4-19, and remain within the Sink Power Sub-States, until either VBUS is removed or a *USB PD* contract is established with the source.

The port shall not negotiate a voltage on VBUS higher than the maximum voltage specified in the Charge-Through VCONN-Powered USB Device's Discover Identity Command response.

The port shall continue to supply VCONN.

The port shall reject a VCONN swap request.

The port shall not perform *USB BC 1.2* primary detection, as that will interfere with VPD functionality.

In *USB PD* Version 2.0, the port shall not initiate *USB PD* messages, although it remains a DFP for USB data.

The port shall neither initiate nor respond to any SOP' communication.

The port shall meet the Sink Power Sub-State requirements specified in Section 4.5.2.2.29.

The port shall meet the additional maximum current constraints described in Section 4.6.2.5.

The port shall follow the restrictions on *USB PD* messages described in Section 4.10.2.

The port shall alter its advertised capabilities to UFP role/sink only role as described in Section 4.10.2.

4.5.2.2.27.2 Exiting from CTAttached.SNK

A port that is not in the process of a *USB PD* Hard Reset shall transition to CTUnattached.SNK within tSinkDisconnect when VBUS falls below vSinkDisconnect for VBUS operating at or below 5 V or below vSinkDisconnectPD when negotiated by *USB PD* to operate above 5 V.

A port that has entered into *USB PD* communications with the Source and has seen the CC voltage exceed vRd-USB may monitor the CC pin to detect cable disconnect in addition to monitoring VBUS.

A port that is monitoring the CC voltage for disconnect shall transition to CTUnattached.SNK within tSinkDisconnect after the CC voltage remains below vRd-USB for tPDDebounce.

4.5.2.2.28 CTUnattached.Unsupported State

This state appears in Figure 4-18.

When in the CTUnattached.Unsupported state, the Charge-Through VCONN-Powered USB Device has previously detected SNK.Open on its host port for tVPDCTDD, indicating that it is connected to a Charge-Through Capable Source, and is now monitoring its Charge-Through port for the presence of an unsupported sink.

A Charge-Through VCONN-Powered USB Device does not support Sinks, Debug Accessory Mode, or Audio Adapter Accessory Mode.

4.5.2.2.28.1 CTUnattached.Unsupported Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.

The Charge-Through VCONN-Powered USB Device shall only respond to *USB PD* Discover Identity queries on SOP' on its Host-side port. It shall ensure there is sufficient capacitance on the Host-side port CC to meet cReceiver as defined in *USB PD*.

4.5.2.2.28.2 Exiting from CTUnattached.Unsupported

The Charge-Through VCONN-Powered USB Device shall transition to CTAttachWait.Unsupported when a Sink connection is detected on the Charge-Through port, as indicated by the SRC.Rd state on at least one of the Charge-Through port's CC pins or SRC.Ra state on both the CC1 and CC2 pins.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

Otherwise, a Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

4.5.2.2.29 CTAttachWait.Unsupported State

This state appears in Figure 4-18.

The CTAttachWait.Unsupported state is used to ensure that the state of both the Charge-Through Port's CC1 and CC2 pins are stable for at least tCCDebounce.

4.5.2.2.29.1 CTAttachWait.Unsupported Requirements

The requirements for this state are identical to CTUnattached.Unsupported state.

4.5.2.2.29.2 Exiting from CTAttachWait.Unsupported

The Charge-Through VCONN-Powered USB Device shall transition to CTTry.SNK if the state of at least one of the Charge-Through port's CC pins is SRC.Rd, or if the state of both the CC1 and CC2 pins is SRC.Ra for at least tCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when the state of either the Charge-Through Port's CC1 or CC2 pin is SRC.Open for at least tCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

4.5.2.2.30 CTTry.SNK State

This state appears in Figure 4-18.

When in the CTTry.SNK state, the Charge-Through VCONN-Powered USB Device is querying to determine if the port partner on the Charge-Through port supports the source role.

4.5.2.2.30.1 CTTry.SNK Requirements

The requirements for this state are identical to CTUnattached.VPD state.

4.5.2.2.30.2 Exiting from CTTry.SNK

The Charge-Through VCONN-Powered USB Device shall wait for tDRPTry and only then begin monitoring the Charge-Through port's CC pins for the SNK.Rp state.

The Charge-Through VCONN-Powered USB Device shall then transition to CTAttached.VPD when the SNK.Rp state is detected on the Charge-Through port's CC pins for at least tTryCCDebounce and VBUS is detected on Charge-Through port.

A Charge-Through VCONN-Powered USB Device shall transition to CTAttached.Unsupported if SNK.Rp state is not detected for tDRPTryWait.

Note: The Source may initiate *USB PD* communications which will cause brief periods of the SNK.Open state on both the CC1 and CC2 pins, but this event will not exceed tTryCCDebounce.

The Charge-Through VCONN-Powered USB Device shall transition to Unattached.SNK if VCONN falls below vVCONNDisconnect.

4.5.2.2.31 CTAttached.Unsupported State

This state appears in Figure 4-18.

If the port partner to the Charge-Through VCONN-Powered USB Device's Charge-Through port either does not support the source power role, or failed to negotiate the source role, the CTAttached.Unsupported state is used to wait until that device is unplugged before continuing.

4.5.2.2.31.1 CTAttached.Unsupported Requirements

The Charge-Through VCONN-Powered USB Device shall isolate its Host-side port from its Charge-Through port, including CCs and VBUS. The Charge-Through VCONN-Powered USB Device shall ensure that it is powered by VCONN, does not consume more than ICCS (*USB 3.2*) / ICCSH (*USB 2.0*) from VBUS for monitoring, and is sufficiently isolated from VBUS to tolerate high voltages during Charge-Through operation.

Upon entry into this state, the Charge-Through VCONN-Powered USB Device shall maintain its Rp termination advertising 3.0 A on the Host-side port's CC pin, remove its Rd terminations to ground on the Charge-Through port's CC1 and CC2 pins, and provide a Rp termination advertising Default USB Power instead.

At least one of the CC1 or CC2 pins will be in the SRC.Rd state or both will be in the SRC.Ra state. The Charge-Through port shall advertise Default USB Power (see Table 4-24) on its CC pins and monitor their voltage.

The Charge-Through VCONN-Powered USB Device shall present a USB Billboard Device Class interface indicating that it does not recognize or support the attached accessory or device.

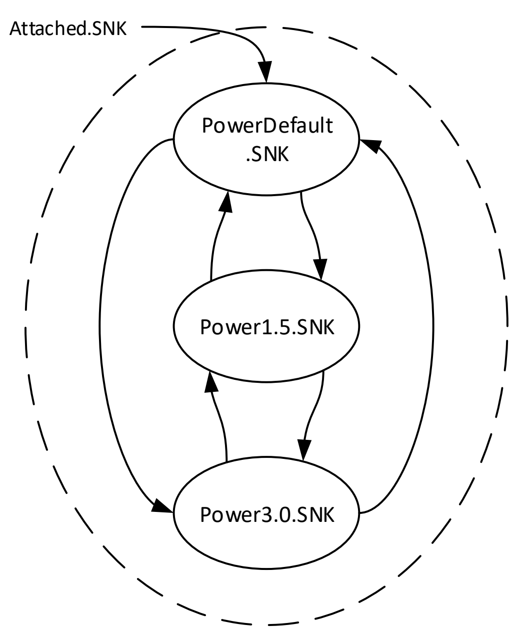
4.5.2.2.31.2 Exiting from CTAttached.Unsupported

The Charge-Through VCONN-Powered USB Device shall transition to CTUnattached.VPD when SRC.Open state is detected on both the Charge-Through port's CC pins or the SRC.Open state is detected on one CC pin and SRC.Ra is detected on the other CC pin.

4.5.2.3 Sink Power Sub-State Requirements

When in the Attached.SNK or CTAttached.SNK states and the Source is supplying default VBUS, the port shall operate in one of the sub-states shown in Figure 4-19. The initial Sink Power Sub-State is PowerDefault.SNK. Subsequently, the Sink Power Sub-State is determined by Source's USB Type-C current advertisement. The port in Attached.SNK shall remain within the Sink Power Sub-States until either VBUS is removed or a *USB PD* contract is established with the Source.

Figure 4-19 Sink Power Sub-States



The Sink is only required to implement Sink Power Sub-State transitions if the Sink wants to consume more than default USB current.

Note that for the CTAttached.SNK state, there are further limitations on maximum current (see Section 4.6.2.5).

4.5.2.3.1 PowerDefault.SNK Sub-State

This sub-state supports Sinks consuming current within the lowest range (default) of Source-supplied current.

4.5.2.3.1.1 PowerDefault.SNK Requirements

The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the port wants to consume more than the default USB power, it shall monitor vRd to determine if more current is available from the Source.

4.5.2.3.1.2 Exiting from PowerDefault.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.

For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State.

For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.

4.5.2.3.2 Power1.5.SNK Sub-State

This sub-state supports Sinks consuming current within the two lower ranges (default and 1.5 A) of Source-supplied current.

4.5.2.3.2.1 Power1.5.SNK Requirements

The port shall draw no more than 1.5 A from VBUS.

The port shall monitor vRd while it is in this sub-state.

4.5.2.3.2.2 Exiting from Power1.5.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.

For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For a vRd in the vRd-3.0 range, the port shall transition to the Power3.0.SNK Sub-State.

4.5.2.3.3 Power3.0.SNK Sub-State

This sub-state supports Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of Source-supplied current.

4.5.2.3.3.1 Power3.0.SNK Requirements

The port shall draw no more than 3.0 A from VBUS.

The port shall monitor vRd while it is in this sub-state.

4.5.2.3.3.2 Exiting from Power3.0.SNK

For any change in vRd indicating a change in allowable power, the port shall not transition until the new vRd has been stable for at least tRpValueChange.

For a vRd in the vRd-USB range, the port shall transition to the PowerDefault.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For a vRd in the vRd-1.5 range, the port shall transition to the Power1.5.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

4.5.2.4 Cable eMarker State Machine Requirements

Figure 4-20 and Figure 4-21 illustrate the cable eMarker connection state diagrams for passive and active cables, respectively.

Figure 4-20 Passive Cable eMarker State Diagram

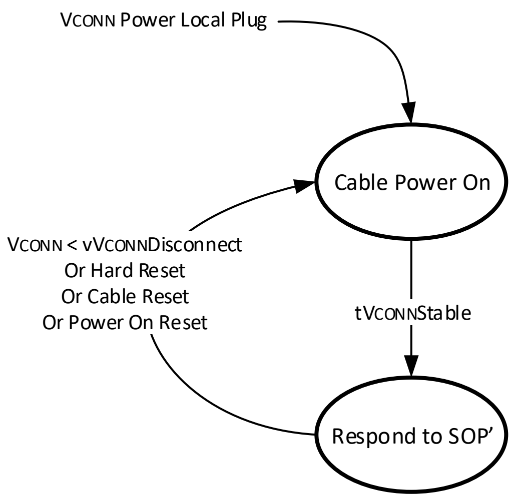
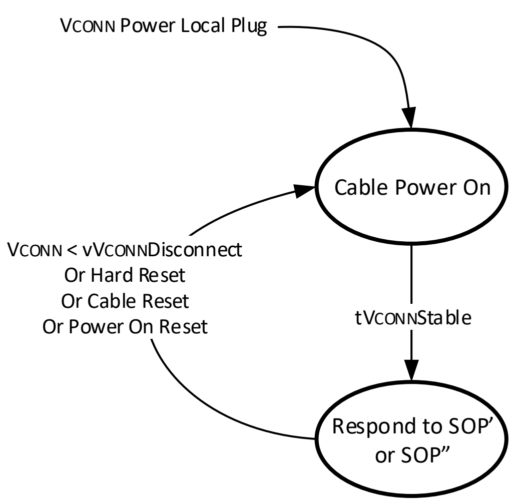


Figure 4-21 Active Cable eMarker State Diagram



4.5.2.4.1 Cable Power On State

This state appears in Figure 4-20. This is the initial power on state for each eMarker in the cable when VCONN is applied.

4.5.2.4.1.1 Cable Power On State Requirements

Each eMarker in the cable shall power on.

The cable shall not respond to SOP' and SOP" commands in this state.

4.5.2.4.1.2 Exiting from Cable Power On State

Each eMarker in a passive or active cable shall transition to Assign Cable SOP* when it has completed its boot process. Each eMarker shall transition to Assign Cable SOP* within tVCONNStable.

4.5.2.4.2 Respond to SOP'/" State

This state appears in Figure 4-20 and Figure 4-21.

A passive cable has only one eMarker powered at a time. This cable eMarker in a passive cable shall respond to SOP' in this state.

Each cable eMarker in an active cable shall respond to a pre-set SOP' or SOP''. If only one eMarker exists in the cable, it shall only respond to SOP'.

Cable designers shall ensure that the eMarker works correctly in the presence of ground and VCONN maximum IR drop.

4.5.2.4.2.1 Respond to SOP'/" State Requirements

Each eMarker in the passive or active cable shall be able to respond to any *USB PD* communication sent to its pre-set SOP' or SOP''. For a passive cable, only one eMarker should be powered at a time and shall respond to SOP' only. If two eMarkers exist in a passive or active cable and are powered at the same time, then only one shall respond to SOP' and the other shall respond to SOP''. The assignment of SOP' and SOP'' is fixed for each eMarker in a cable and shall not be dynamically set when power is applied to VCONN.

4.5.2.4.2.2 Exiting from Respond to SOP'/" State

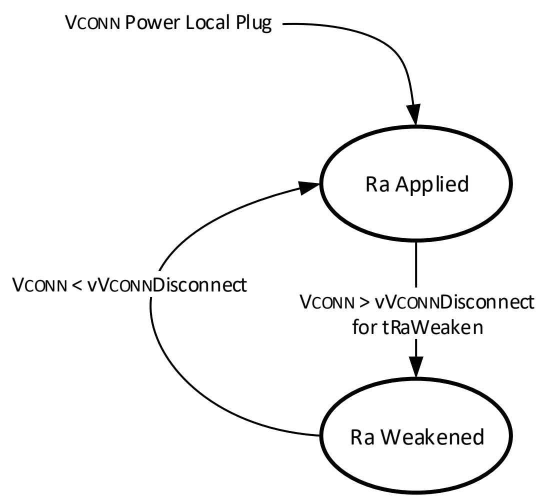
Each eMarker in the cable shall transition to Cable Power On upon sensing VCONN less than vVconnDisconnect or upon a Power On Reset event.

Each eMarker in the cable shall transition to Cable Power On upon sensing a Hard Reset or Cable Reset.

4.5.2.5 Cable Ra Management State Machine Requirements

Figure 4-22 illustrates the cable eMarker state diagram for applying and weakening or removing Ra. This state machine runs independently from the Cable eMarker state machine described in Section 4.5.2.4.

Figure 4-22 Cable Ra Management State Diagram



4.5.2.5.1 Ra Applied State

This state appears in Figure 4-22. This is the initial state at power on for each eMarker in the cable.

4.5.2.5.1.1 Ra Applied State Requirements

Each eMarker in the cable shall apply Ra to VCONN within tRaReconnect.

4.5.2.5.1.2 Exiting from Ra Applied State

Each eMarker in a passive or active cable shall transition to the Ra Weakened state when VCONN is greater than vVCONNDisconnect for tRaWeaken.

4.5.2.5.2 Ra Weakened State

This state appears in Figure 4-22.

4.5.2.5.2.1 Ra Weakened State Requirements

The eMarker in the cable shall remove or weaken Ra.

Passive cables shall meet the Power for electronically marked passive cables defined in Table 4-6. Active cables shall meet the Power for Active Cables in Table 4-6.

4.5.2.5.2.2 Exiting from Ra Weakened State

Each eMarker in a passive or active cable shall transition to the Ra Applied state when VCONN is below vVCONNDisconnect.

4.5.2.6 Connection States Summary

Table 4-16 defines the mandatory and optional states for each type of port.

Table 4-16 Mandatory and Optional States

	SOURCE	SINK	DRP	USB PD Communication
Disabled	Optional	Optional	Optional	Not Permitted

	SOURCE	SINK	DRP	USB PD Communication
ErrorRecovery	Mandatory[10]	Mandatory[10]	Mandatory[10]	Not Permitted
Unattached.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWait.SNK	N/A	Mandatory[1]	Mandatory	Not Permitted
Attached.SNK	N/A	Mandatory	Mandatory	Permitted
UnattachedWait.SRC	Mandatory or N/A[7]	N/A	N/A	Not Permitted
Unattached.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWait.SRC	Mandatory	N/A	Mandatory	Not Permitted
Attached.SRC	Mandatory	N/A	Mandatory	Permitted
Try.SRC[4]	N/A	N/A	Optional	Not Permitted
TryWait.SNK[2]	N/A	N/A	Optional	Not Permitted
Try.SNK[4, 8]	N/A	N/A	Optional	Not Permitted
TryWait.SRC[5, 8]	N/A	N/A	Optional	Not Permitted
AudioAccessory	Optional	Optional	Optional	Not Permitted
UnorientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Not Permitted
OrientedDebugAccessory.SRC	Optional[6]	N/A	Optional[6]	Permitted
DebugAccessory.SNK	N/A	Optional	Optional	Permitted
Unattached.Accessory	N/A	Optional	N/A	Not Permitted
AttachWait.Accessory	N/A	Optional	N/A	Not Permitted
PoweredAccessory	N/A	Optional	N/A	Permitted
Unsupported.Accessory[3]	N/A	Optional	N/A	Not Permitted
CTUnattached.VPD	N/A	N/A	Optional	SOP' Permitted
CTAttachWait.VPD[8]	N/A	N/A	Optional	SOP' Permitted
CTAttached.VPD[8]	N/A	N/A	Optional	Not Permitted
CTDisabled.VPD[8]	N/A	N/A	Optional	Not Permitted
CTUnattached.SNK	N/A	N/A	Optional	SOP' Permitted
CTAttached.SNK[9]	N/A	N/A	Optional	Permitted
CTUnattached.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
CTAttachWait.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
CTTry.SNK[8]	N/A	N/A	Optional	SOP' Permitted
CTAttached.Unsupported[8]	N/A	N/A	Optional	SOP' Permitted
PowerDefault.SNK	N/A	Mandatory	Mandatory	Permitted
Power1.5.SNK	N/A	Optional	Optional	Permitted

	SOURCE	SINK	DRP	USB PD Communication
Power3.0.SNK	N/A	Optional	Optional	Permitted

Notes:

1. Optional for UFP applications that are USB 2.0-only, consume USB Default Power and do not support *USB PD* or accessories.
2. TryWait.SNK is mandatory when Try.SRC is supported.
3. Unsupported.Accessory is mandatory when PoweredAccessory is supported.
4. Try.SRC and Try.SNK shall not be supported at the same time, although an unattached device may dynamically choose between Try.SRC and Try.SNK state machines based on external factors.
5. TryWait.SRC is mandatory when Try.SNK is supported.
6. UnorientedDebugAccessory.SRC is required for any Source or DRP that supports Debug Accessory Mode. OrientedDebugAccessory.SRC is only required if orientation detection is necessary in Debug Accessory Mode.
7. Mandatory for a DFP that was providing VCONN in the previous Attached.SRC state. N/A for a DFP that was not providing VCONN in the previous Attached.SRC state.
8. CTAttachWait.VPD, CTAttached.VPD, CTDisabled.VPD, Try.SNK, TryWait.SRC, CTUnattached.Unsupported, CTAttachWait.Unsupported, CTAttached.Unsupported, and CTTry.SNK are mandatory when CTUnattached.VPD is supported.
9. CTAttached.SNK is mandatory when CTUnattached.SNK is supported.
10. Optional for non-*USB4* and non-*USB PD* implementations.

4.5.3 USB Port Interoperability Behavior

This section describes interoperability behavior between USB Type-C to USB Type-C ports and between USB Type-C to legacy USB ports.

4.5.3.1 USB Type-C Port to USB Type-C Port Interoperability Behaviors

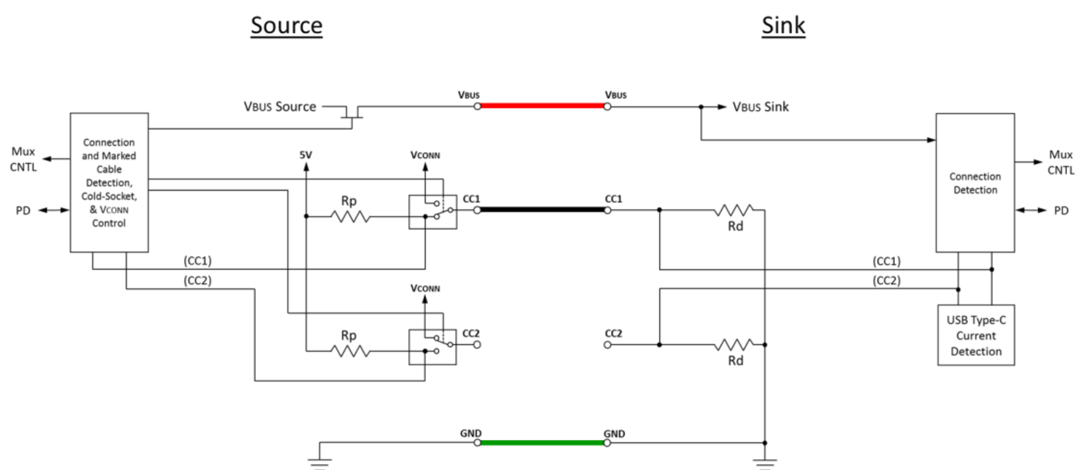
The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs as presented in Table 4-9. In all of the described behaviors, the impact of *USB PD*-based swaps (PR_Swap, DR_Swap or VCONN_Swap) are not considered.

The figures in the following sections illustrate the CC1 and CC2 routing after the CC detection process is complete.

4.5.3.1.1 Source to Sink Behavior

Figure 4-23 illustrates the functional model for a Source connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-23 Source to Sink Functional Model



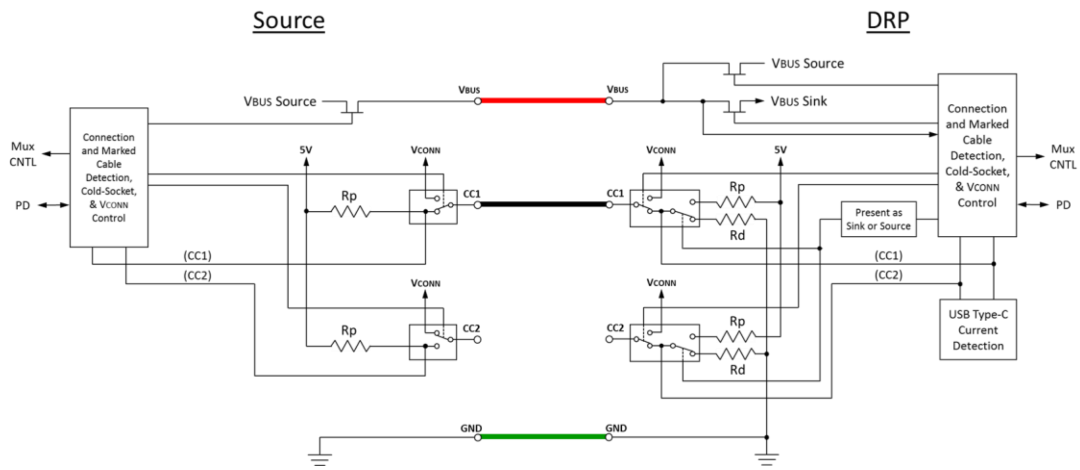
The following describes the behavior when a Source is connected to a Sink.

1. Source and Sink in the unattached state
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the Sink's pull-down on CC and enters Attached.SRC through AttachWait.SRC
   - Source turns on VBUS and VCONN
3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK. Sink may skip AttachWait.SNK if it is USB 2.0 only and does not support accessories.
   - Sink detects VBUS and enters Attached.SNK through AttachWait.SNK
4. While the Source and Sink are in the attached state:
   - Source adjusts Rp as needed to limit the current the Sink may draw
   - Sink detects and monitors vRd for available current on VBUS
   - Source monitors CC for detach and when detected, enters Unattached.SRC
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

4.5.3.1.2 Source to DRP Behavior

Figure 4-24 illustrates the functional model for a Source connected to a DRP. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-24 Source to DRP Functional Model



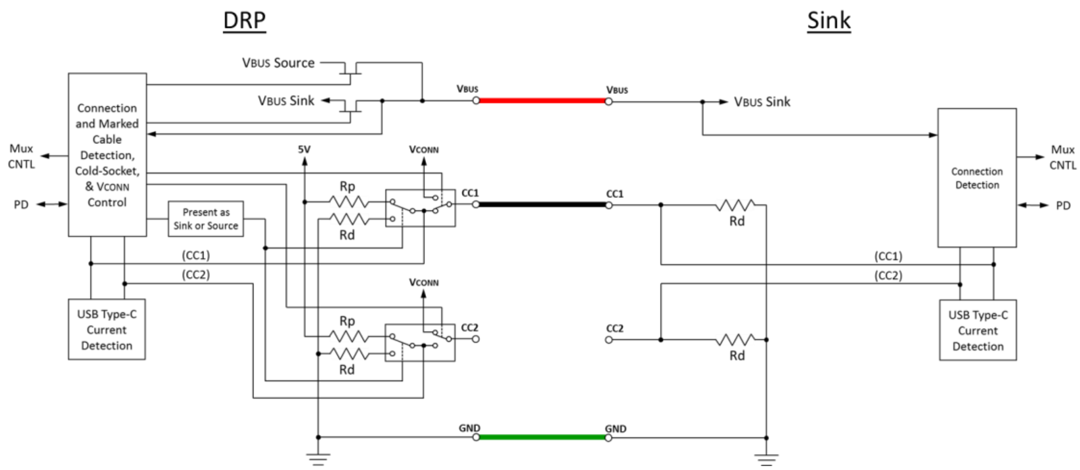
The following describes the behavior when a Source is connected to a DRP.

1. Source and DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the DRP's pull-down on CC and enters AttachWait.SRC. After tCCDebounce it then enters Attached.SRC.
   - Source turns on VBUS and VCONN
3. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   - DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters Attached.SNK.
4. While the Source and DRP are in their respective attached states:
   - Source adjusts Rp as needed to limit the current the DRP (as Sink) may draw
   - DRP (as Sink) detects and monitors vRd for available current on VBUS
   - Source monitors CC for detach and when detected, enters Unattached.SRC
   - DRP (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.5.3.1.3 DRP to Sink Behavior

Figure 4-25 illustrates the functional model for a DRP connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1.

Figure 4-25 DRP to Sink Functional Model



The following describes the behavior when a DRP is connected to a Sink.

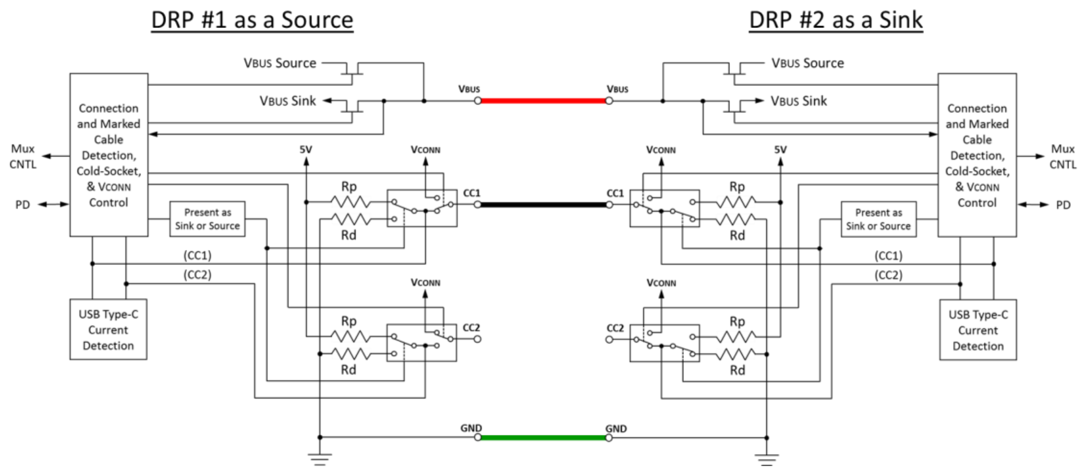
1. DRP and Sink in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to AttachWait.SRC to Attached.SRC
   - DRP in Unattached.SRC detects one of the CC pull-downs of Sink which is in Unattached.SNK and DRP enters AttachWait.SRC
   - DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN
3. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if required.
   - Sink detects VBUS and enters Attached.SNK
4. While the DRP and Sink are in their respective attached states:
   - DRP (as Source) adjusts Rp as needed to limit the current the Sink may draw
   - Sink detects and monitors vRd for available current on VBUS
   - DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

4.5.3.1.4 DRP to DRP Behavior

Two behavior descriptions based on the connection state diagrams are provided below. In the first case, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly whereas in the second case the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.

Figure 4-26 illustrates the functional model for a DRP connected to a DRP in the first case described. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-26 DRP to DRP Functional Model – CASE 1



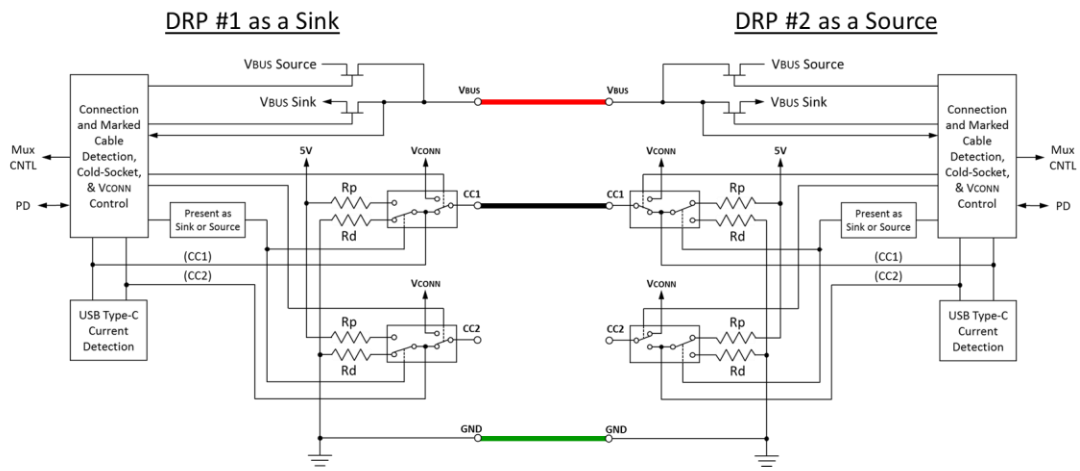
CASE 1: The following describes the behavior when a DRP is connected to another DRP. In this flow, the two DRPs accept the resulting Source-to-Sink relationship achieved randomly.

1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Attached.SRC
   - DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
5. DRP #2 transitions from AttachWait.SNK to Attached.SNK.
   - DRP #2 after having been in AttachWait.SNK for tCCDebounce and having detected VBUS, enters Attached.SNK
6. While the DRPs are in their respective attached states:
   - DRP #1 (as Source) adjusts Rp as needed to limit the current DRP #2 (as Sink) may draw
   - DRP #2 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #1 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

- DRP #2 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

Figure 4-27 illustrates the functional model for a DRP connected to a DRP in the second case described.

Figure 4-27 DRP to DRP Functional Model – CASE 2 & 3



CASE 2: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #2 chooses to drive the random result to the opposite result using the Try.SRC mechanism.

1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Attached.SRC
   - DRP #1 in AttachWait.SRC continues to see CC pull down of DRP #2 for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
5. DRP #2 transitions from AttachWait.SNK to Try.SRC.
   - DRP #2 in AttachWait.SNK has been in this state for tCCDebounce and detects VBUS but strongly prefers the Source role, so transitions to Try.SRC
   - DRP #2 in Try.SRC asserts a pull-up on CC and waits
6. DRP #1 transitions from Attached.SRC to Unattached.SNK to AttachWait.SNK
   - DRP #1 in Attached.SRC no longer detects DRP #2's pull-down on CC and transitions to Unattached.SNK.
   - DRP #1 in Unattached.SNK turns off VBUS and VCONN and applies a pull-down on CC

- DRP #1 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK

7. DRP #2 transitions from Try.SRC to Attached.SRC
   - DRP #2 in Try.SRC detects the DRP #1 in Unattached.SNK's pull-down on CC and enters Attached.SRC
   - DRP #2 in Attached.SRC turns on VBUS and VCONN
8. DRP #1 transitions from AttachWait.SNK to Attached.SNK
   - DRP #1 in AttachWait.SNK after tCCDebounce and detecting VBUS, enters Attached.SNK
9. While the DRPs are in their respective attached states:
   - DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw
   - DRP #1 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

CASE 3: The following describes the behavior when a DRP is connected to another DRP. In this flow, the DRP #1 chooses to drive the random result to the opposite result using the Try.SNK mechanism.

1. Both DRPs in the unattached state
   - DRP #1 and DRP #2 alternate between Unattached.SRC and Unattached.SNK
2. DRP #1 transitions from Unattached.SRC to AttachWait.SRC
   - DRP #1 in Unattached.SRC detects a CC pull down of DRP #2 in Unattached.SNK and enters AttachWait.SRC
3. DRP #2 transitions from Unattached.SNK to AttachWait.SNK
   - DRP #2 in Unattached.SNK detects pull up on a CC and enters AttachWait.SNK
4. DRP #1 transitions from AttachWait.SRC to Try.SNK
   - DRP #1 in AttachWait.SRC has been in this state for tCCDebounce and detects DRP #2's pull-down on CC but strongly prefers the Sink role, so transitions to Try.SNK
   - DRP #1 in Try.SNK asserts a pull down on CC and waits
5. DRP #2 transitions from AttachWait.SNK to Unattached.SRC to AttachWait.SRC.
   - DRP #2 in AttachWait.SNK no longer detects DRP #1's pull up on CC and transitions to Unattached.SRC
   - DRP #2 in Unattached.SRC applies a pull up on CC
   - DRP #2 in Unattached.SRC detects a pull down on a CC pin and enters AttachWait.SRC
   - DRP #1 detects DRP #2's pull up on CC and remains in Try.SNK
6. DRP #2 transitions from AttachWait.SRC to Attached.SRC

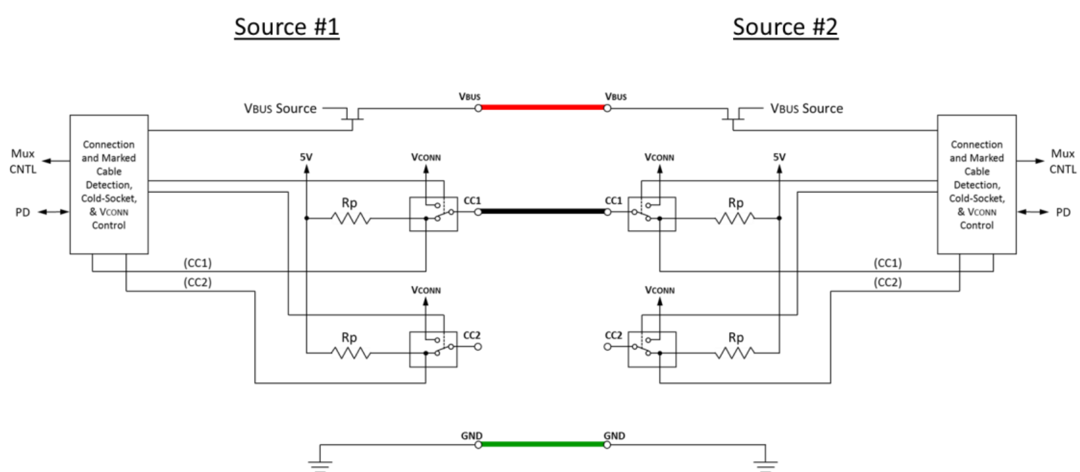
- DRP #2 in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC
- DRP #2 in Attached.SRC turns on VBUS and VCONN

7. DRP #1 transitions from Try.SNK to Attached.SNK
   - DRP #1 in Try.SNK after detecting VBUS, enters Attached.SNK
8. While the DRPs are in their respective attached states:
   - DRP #2 (as Source) adjusts Rp as needed to limit the current DRP #1 (as Sink) may draw
   - DRP #1 (as Sink) detects and monitors vRd for available current on VBUS
   - DRP #2 (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - DRP #1 (as Sink) monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.5.3.1.5 Source to Source Behavior

Figure 4-28 illustrates the functional model for a Source connected to a Source. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-28 Source to Source Functional Model



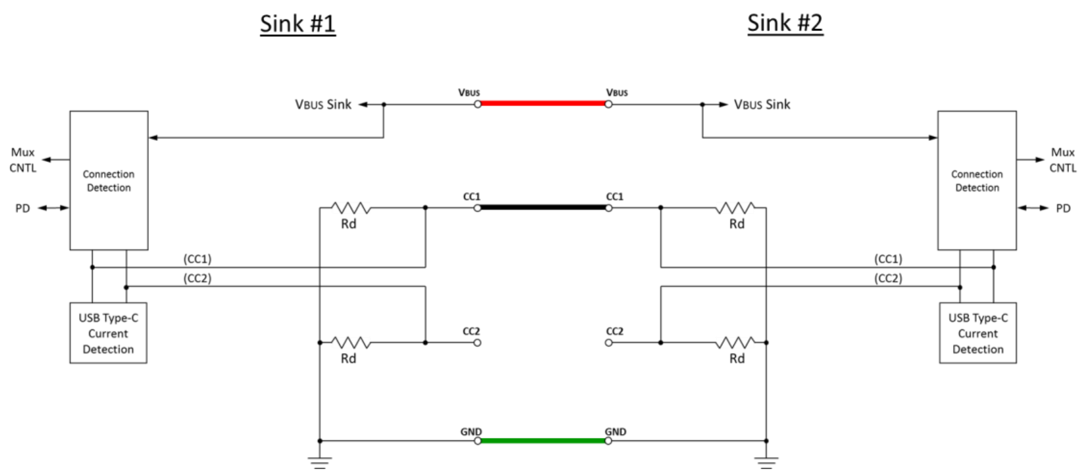
The following describes the behavior when a Source is connected to another Source.

1. Both Sources in the unattached state
   - Source #1 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC
   - Source #2 fails to detect a Sink's pull-down on CC and remains in Unattached.SRC

4.5.3.1.6 Sink to Sink Behavior

Figure 4-29 illustrates the functional model for a Sink connected to a Sink. The single CC wire that is in a standard cable is only shown in one of the four possible connection routes, CC1 to CC1. Port numbers have been arbitrarily assigned in the diagram to assist the reader to understand the process description.

Figure 4-29 Sink to Sink Functional Model



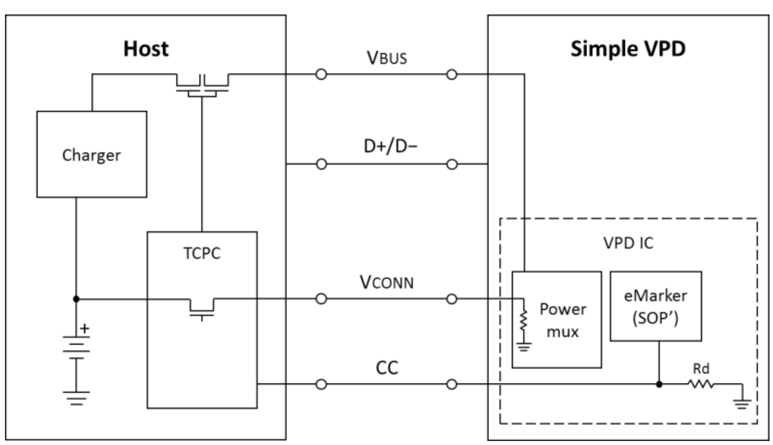
The following describes the behavior when a Sink is connected to another Sink.

1. Both Sinks in the unattached state
   - Sink #1 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK
   - Sink #2 fails to detect pull up on CC or VBUS supplied by a Source and remains in Unattached.SNK

4.5.3.1.7 DRP to VCONN-Powered USB Device (VPD) Behavior

Figure 4-30 illustrates the functional model for a DRP connected to a VCONN-Powered USB Device that does not feature charge-through functionality.

Figure 4-30 DRP to VPD Model



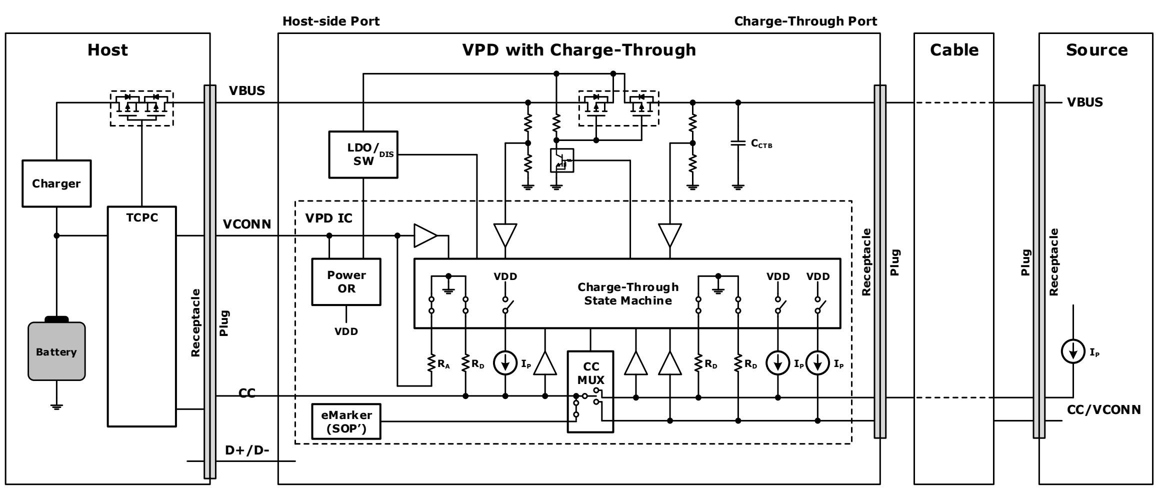
The following describes the behavior when a DRP that supports VPDs is connected to a VPD.

1. DRP and VPD in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - DRP in Unattached.SRC detects the CC pull-down of VPD which is in Unattached.SNK and DRP enters AttachWait.SRC
   - DRP in AttachWait.SRC detects that pull-down on CC persists for tCCDebounce. It then enters Attached.SRC and turns on VBUS and VCONN
3. VPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   - VPD detects VCONN and enters Attached.SNK
4. While DRP and VPD are in their respective attached states, DRP discovers the VPD and removes VBUS
   - DRP (as Source) queries the cable identity via *USB PD* on SOP'.
   - VPD responds on SOP', advertising that it is a VCONN-Powered USB Device that does not support charge-through
   - DRP (as Source) removes VBUS
   - DRP (as Source) maintains its Rp
5. DRP and VPD for detach
   - DRP (as Source) monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
   - VPD monitors VCONN for detach and when detected, enters Unattached.SNK

4.5.3.1.8 DRP to Charge-Through VCONN-Powered USB Device (CTVPD) Behavior

Figure 4-31 illustrates the functional model for a DRP connected to a Charge-Through VCONN-Powered USB Device, with a Source attached to the Charge-Through port on the VCONN-Powered USB Device.

Figure 4-31 Example DRP to Charge-Through VCONN-Powered USB Device Model



CASE 1: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with no Power Source attached to the Charge-Through port on the CTVPD.

1. DRP and CTVPD are both in the unattached state
    a. DRP alternates between Unattached.SRC and Unattached.SNK
    b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
    a. DRP in Unattached.SRC detects a CC pull down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC
    b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS and VCONN
3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
    a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK
    b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK
    c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins
4. While DRP and CTVPD are in their respective attached states, DRP discovers the CTVPD and transitions to CTUnattached.SNK
    a. DRP (as Source) queries the device identity via *USB PD* (Device Identity Command) on SOP'
    b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN-Powered USB Device
    c. DRP (as Source) removes VBUS
    d. DRP (as Source) changes its Rp to a Rd
    e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK
5. CTVPD transitions to CTUnattached.VPD
    a. CTVPD detects VBUS removal, VCONN presence, the low Host-side CC pin and enters CTUnattached.VPD
    b. CTVPD changes its host-side Rd to a Rp advertising 3.0 A
    c. CTVPD isolates itself from VBUS
    d. CTVPD apply Rd on its Charge-Through port's CC1 and CC2 pins
6. While the CTVPD in CTUnattached.VPD state and the DRP in CTUnattached.SNK state:
    a. CTVPD monitors Charge-Though CC pins for a source or sink; when a Power Source attach is detected, enters CTAttachWait.VPD; when a sink is detected, enters CTAttachWait.Unsupported
    b. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK
    c. DRP monitors VBUS and CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK
    d. DRP monitors VBUS for Power Source attach and when detected, enters CTAttached.SNK

CASE 2: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Host already attached to the Host-side port on the CTVPD.

1. DRP is in CTUnattached.SNK state, CTVPD in CTUnattached.VPD, and Power Source in the unattached state
    a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rp termination advertising 3.0 A on the Host-side port's CC pin
2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
    a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC
    b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS
3. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD
    a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD
    b. CTVPD finishes any active *USB PD* communication on SOP' and ceases to respond to SOP' queries
    c. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD
    d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin
    e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin
    f. CTVPD disables its Rd on the Charge-Through CC pins
    g. CTVPD connects VBUS from the Charge-Through side to the Host side
4. DRP (as Sink) transitions to CTAttached.SNK
    a. DRP (as Sink) detects VBUS, monitors vRd for available current and enter CTAttached.SNK
5. While the devices are all in their respective attached states:
    a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD
    b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD
    c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK
    d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)
    e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC

CASE 3: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with no Host attached to the Host-side port on the CTVPD.

1. CTVPD and Power Source are both in the unattached state
    a. CTVPD has applied Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
    a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC
    b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS
3. CTVPD alternates between Unattached.SNK and Unattached.SRC
    a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK
4. While the CTVPD alternates between Unattached.SRC and Unattached.SNK state and the Power Source in Attached.SRC state:
    a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters AttachWait.SRC
    b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK
    c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC

CASE 4: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a Power Source already attached to the Charge-Through side on the CTVPD.

1. DRP and CTVPD are in unattached state and Power Source in Attached.SRC state
    a. DRP alternates between Unattached.SRC and Unattached.SNK
    b. CTVPD alternates between Unattached.SRC and Unattached.SNK
    c. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins
    d. Power Source has applied VBUS
2. DRP transitions from Unattached.SNK to AttachWait.SNK
    a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Unattached.SRC and DRP enters AttachWait.SNK
3. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC
    a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC
    b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK
    c. CTVPD disables Rp termination advertising Default USB Power on the Host-side port's CC pin
    d. CTVPD enables Rd on the Host-side port's CC pin

4. DRP transitions from AttachWait.SNK to Attached.SRC through Unattached.SRC and AttachWait.SRC
   a. DRP in AttachWait.SNK detects the CC pull-up removal of CTVPD which is in Try.SNK and DRP enters Unattached.SRC
   b. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Try.SNK and DRP enters AttachWait.SRC
   c. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN
5. CTVPD transitions from Try.SNK to Attached.SNK
   a. CTVPD detects the CC pull-up of the DRP persists for tTryCCDebounce
   b. CTVPD detects VBUS on the Host-side port and enters Attached.SNK
6. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK
   a. DRP (as Source) queries the device identity via *USB PD* (Discover Identity Command) on SOP'
   b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN-Powered USB Device
   c. DRP (as Source) removes VBUS
   d. DRP (as Source) changes its Rp into an Rd
   e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK
7. CTVPD transitions to CTUnattached.VPD
   a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters CTUnattached.VPD
   b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A
   c. CTVPD isolates itself from VBUS
8. CTVPD transitions from CTUnattached.VPD through CTAttachWait.VPD to CTAttached.VPD
   a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, and transitions to CTAttachWait.VPD
   b. CTVPD in CTAttachWait.VPD detects that the pull up on Charge-Through CC pin persists for tCCDebounce, detects VBUS and enters CTAttached.VPD
   c. CTVPD finishes any active *USB PD* communication on SOP' and ceases to respond to SOP' queries
   d. CTVPD connects the active Charge-Through CC pin to the Host-side port's CC pin
   e. CTVPD disables its Rp termination advertising 3.0 A on the Host-side port's CC pin
   f. CTVPD disables its Rd on the Charge-Through CC pins
   g. CTVPD connects VBUS from the Charge-Through side to the Host side
9. DRP (as Sink) transitions to CTAttached.SNK
   a. DRP (as Sink) detects VBUS and monitors vRd for available current and enter CTAttached.SNK
10. While the devices are all in their respective attached states:

a. CTVPD monitors VCONN for DRP detach and when detected, enters CTDisabled.VPD

b. CTVPD monitors VBUS and CC for Power Source detach and when detected, enters CTUnattached.VPD within tVPDCTDD

c. DRP (as Sink) monitors VBUS for Charge-Through Power Source detach and when detected, enters CTUnattached.SNK

d. DRP (as Sink) monitors VBUS and CC for CTVPD detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

e. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC

CASE 5: The following describes the behavior when a Power Source is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD), with a DRP (with dead battery) attached to the Host-side port on the CTVPD.

1. DRP, CTVPD and Power Source are all in the unattached state
    a. DRP apply dead battery Rd
    b. CTVPD apply Rd on the Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. Power Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
    a. Power Source detects the CC pull-down of the CTVPD and enters AttachWait.SRC
    b. Power Source in AttachWait.SRC detects that pull down on CC persists for tCCDebounce, enters Attached.SRC and turns on VBUS
3. CTVPD alternates between Unattached.SNK and Unattached.SRC
    a. CTVPD detects the Source's Rp on one of its Charge-Through CC pins, detects VBUS for tCCDebounce and starts alternating between Unattached.SRC and Unattached.SNK
4. CTVPD transitions from Unattached.SRC to Try.SNK through AttachWait.SRC
    a. CTVPD in Unattached.SRC detects the CC pull-down of DRP which is in Unattached.SNK and CTVPD enters AttachWait.SRC
    b. CTVPD in AttachWait.SRC detects that pull down on CC persists for tCCDebounce and enters Try.SNK
    c. CTVPD disables Rp termination advertising Default USB Power on the Host-side port's CC pin
    d. CTVPD enables Rd on the Host-side port's CC pin
5. DRP in dead battery condition remains in Unattached.SNK
6. CTVPD transitions from Try.SNK to Attached.SRC through TryWait.SRC
    a. CTVPD didn't detect the CC pull-up of the DRP for tTryCCDebounce after tDRPTry and enters TryWait.SRC
    b. CTVPD disables Rp on the Host-side port's CC pin
    c. CTVPD enables Rp termination advertising Default USB Power on the Host-side port's CC pin

   d. CTVPD detects the CC pull-down of the DRP for tTryCCDebounce and enters Attached.SRC
   e. CTVPD connects VBUS from the Charge-Through side to the Host side
7. DRP transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   a. DRP in Unattached.SNK detects the CC pull-up of CTVPD which is in Attached.SRC and DRP enters AttachWait.SNK
   b. DRP in AttachWait.SNK detects that pull up on CC persists for tCCDebounce, VBUS present and enters Attached.SNK
8. While the devices are all in their respective attached states:
   a. CTVPD monitors the Host-side port's CC pin for device attach and when detected, enters Unattached.SNK
   b. CTVPD monitors VBUS for Power Source detach and when detected, enters Unattached.SNK
   c. Power Source monitors CC for CTVPD detach and when detected, enters Unattached.SRC
   d. DRP monitors VBUS for CTVPD detach and when detected, enters Unattached.SNK
   e. Additionally, the DRP may query the identity of the cable via *USB PD* on SOP' when it has sufficient battery power and when a Charge-Through VPD is identified enters TryWait.SRC if implemented, or enters Unattached.SRC if TryWait.SRC is not supported

CASE 6: The following describes the behavior when a DRP is connected to a Charge-Through VCONN-Powered USB Device (abbreviated CTVPD) and a Sink is attached to the Charge-Through port on the CTVPD.

1. DRP, CTVPD and Sink are all in the unattached state
   a. DRP alternates between Unattached.SRC and Unattached.SNK
   b. CTVPD has applied Rd on its Charge-Through port's CC1 and CC2 pins and Rd on the Host-side port's CC pin
2. DRP transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   a. DRP in Unattached.SRC detects the CC pull-down of CTVPD which is in Unattached.SNK and DRP enters AttachWait.SRC
   b. DRP in AttachWait.SRC detects that pull down on CC persists for tCCDebounce. It then enters Attached.SRC and enable VBUS and VCONN
3. CTVPD transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK
   a. CTVPD detects the host-side CC pull-up of the DRP and CTVPD enters AttachWait.SNK
   b. CTVPD in AttachWait.SNK detects that pull up on the Host-side port's CC persists for tCCDebounce, VCONN present and enters Attached.SNK
   c. CTVPD present a high-impedance to ground (above zOPEN) on its Charge-Through port's CC1 and CC2 pins
4. While DRP and CTVPD are in their respective attached states, DRP discovers the Charge-Through CTVPD and transitions to CTUnattached.SNK

a. DRP (as Source) queries the device identity via *USB PD* (Discover Identity Command) on SOP'

b. CTVPD responds on SOP', advertising that it is a Charge-Through VCONN-Powered USB Device

c. DRP (as Source) removes VBUS

d. DRP (as Source) changes its Rp into an Rd

e. DRP (as Sink) continues to provide VCONN and enters CTUnattached.SNK

5. CTVPD transitions to CTUnattached.VPD

   a. CTVPD detects VBUS removal, VCONN presence, and the low CC pin on its host port and enters CTUnattached.VPD

   b. CTVPD changes its host-side Rd into an Rp termination advertising 3.0 A

   c. CTVPD isolates itself from VBUS

   d. CTVPD apply Rd on its Charge-Through port's CC1 and CC2 pins

6. CTVPD alternates between CTUnattached.VPD and CTUnattached.Unsupported

   a. CTVPD detects SRC.Open on its Charge-Through CC pins and starts alternating between CTUnattached.VPD and CTUnattached.Unsupported

7. CTVPD transitions from CTUnattached.Unsupported to CTTry.SNK through CTAttachWait.Unsupported

   a. CTVPD in CTUnattached.Unsupported detects the CC pull-down of the Sink which is in Unattached.SNK and CTVPD enters CTAttachWait.Unsupported

   b. CTVPD in CTAttachWait.Unsupported detects that pull down on CC persists for tCCDebounce and enters CTTry.SNK

   c. CTVPD disables Rp termination advertising Default USB Power on the Charge-Through port's CC pins

   d. CTVPD enables Rd on the Charge-Through port's CC pins

8. CTVPD transitions from CTTry.SNK to CTAttached.Unsupported

   a. CTVPD didn't detect the CC pull-up of the potential Source for tDRPTryWait after tDRPTry and enters CTAttached.Unsupported

9. While the CTVPD in CTAttached.Unsupported state, the DRP in CTUnattached.SNK state and the Sink in Unattached.SNK state:

   a. CTVPD disables the Rd termination on the Charge-Through port's CC pins and applies Rp termination advertising Default USB Power

   b. CTVPD exposes a USB Billboard Device Class to the DRP indicating that it is connected to an unsupported device on its Charge Through port

   c. CTVPD monitors Charge-Though CC pins for Sink detach and when detected, enters CTUnattached.VPD

   d. CTVPD monitors VCONN for Host detach and when detected, enters Unattached.SNK

   e. DRP monitors CC for CTVPD detach for tVPDDetach and when detected, enters Unattached.SNK

   f. DRP monitors VBUS for CTVPD Charge-Through source attach and, when detected, enters CTAttached.SNK

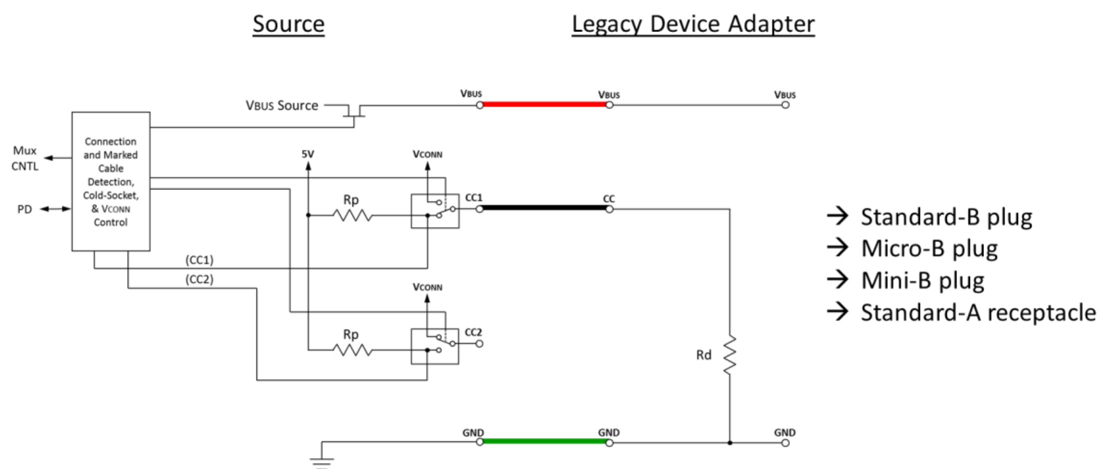
4.5.3.2 USB Type-C port to Legacy Port Interoperability Behaviors

The following sub-sections describe port-to-port interoperability behaviors for the various combinations of USB Type-C Source, Sink and DRPs and legacy USB ports.

4.5.3.2.1 Source to Legacy Device Port Behavior

Figure 4-32 illustrates the functional model for a Source connected to a legacy device port. This model is based on having an adapter present as a Sink to the Source. This adapter has a USB Type-C plug on one end plugged into the Source and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

Figure 4-32 Source to Legacy Device Port Functional Model



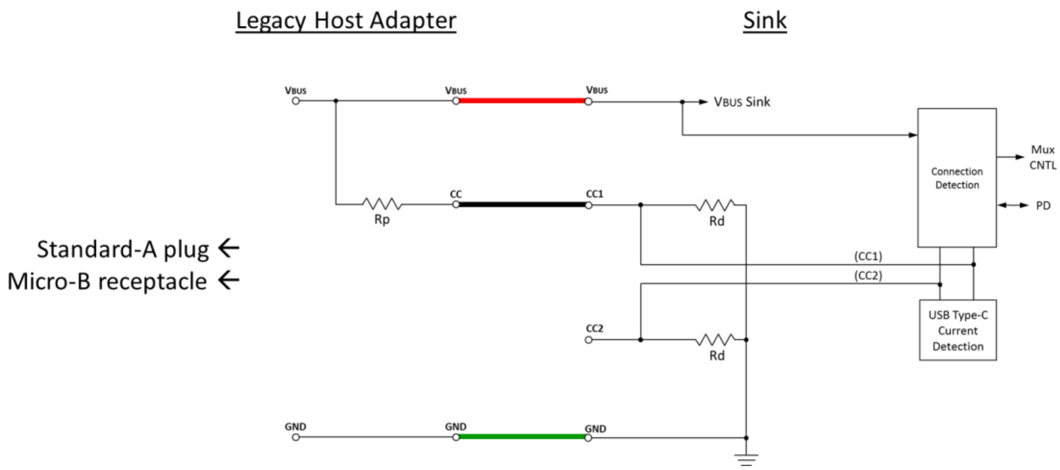
The following describes the behavior when a Source is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.

1. Source in the unattached state
2. Source transitions from Unattached.SRC to Attached.SRC through AttachWait.SRC
   - Source detects the Sink's pull-down on CC and enters AttachWait.SRC. After tCCDebounce, it enters Attached.SRC.
   - Source turns on VBUS and VCONN
3. While the Source is in the attached state:
   - Source monitors CC for detach and when detected, enters Unattached.SRC

4.5.3.2.2 Legacy Host Port to Sink Behavior

Figure 4-33 illustrates the functional model for a legacy host port connected to a Sink. This model is based on having an adapter that presents itself as a Source to the Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a Sink.

Figure 4-33 Legacy Host Port to Sink Functional Model



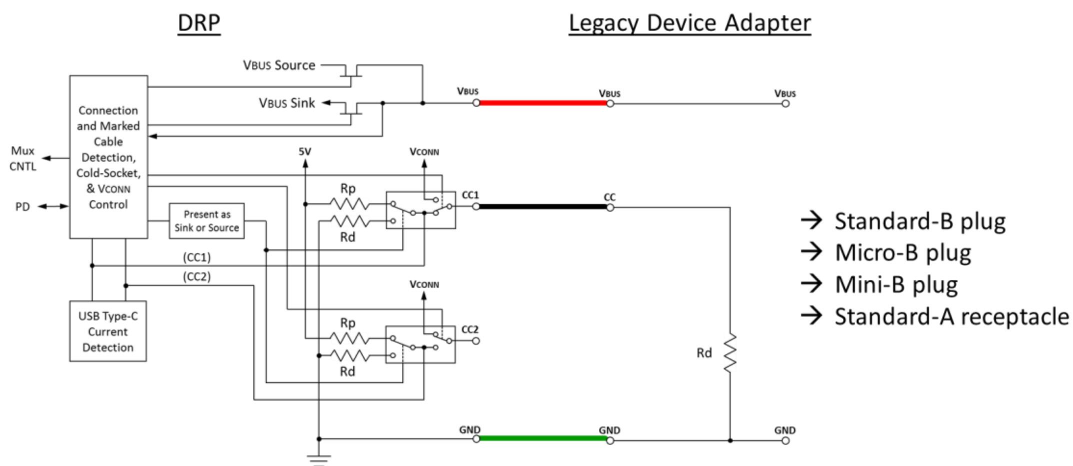
The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source that is connected to a Sink. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via *USB BC 1.2*.

1. Sink in the unattached state
2. Sink transitions from Unattached.SNK to Attached.SNK through AttachWait.SNK if needed.
   - While in Unattached.SNK, if device is not USB 2.0 only, supports accessories or requires more than default power, it enters AttachWait.SNK when it detects a pull up on CC and ignores VBUS. Otherwise, it may enter Attached.SNK directly when VBUS is detected.
   - Sink detects VBUS and enters Attached.SNK
3. While the Sink is in the attached state:
   - Sink monitors VBUS for detach and when detected, enters Unattached.SNK

4.5.3.2.3 DRP to Legacy Device Port Behavior

Figure 4-34 illustrates the functional model for a DRP connected to a legacy device port. This model is based on having an adapter present as a Sink (Device) to the DRP. This adapter has a USB Type-C plug on one end plugged into a DRP and either a USB Standard-B plug, USB Micro-B plug, USB Mini-B plug, or a USB Standard-A receptacle on the other end.

Figure 4-34 DRP to Legacy Device Port Functional Model



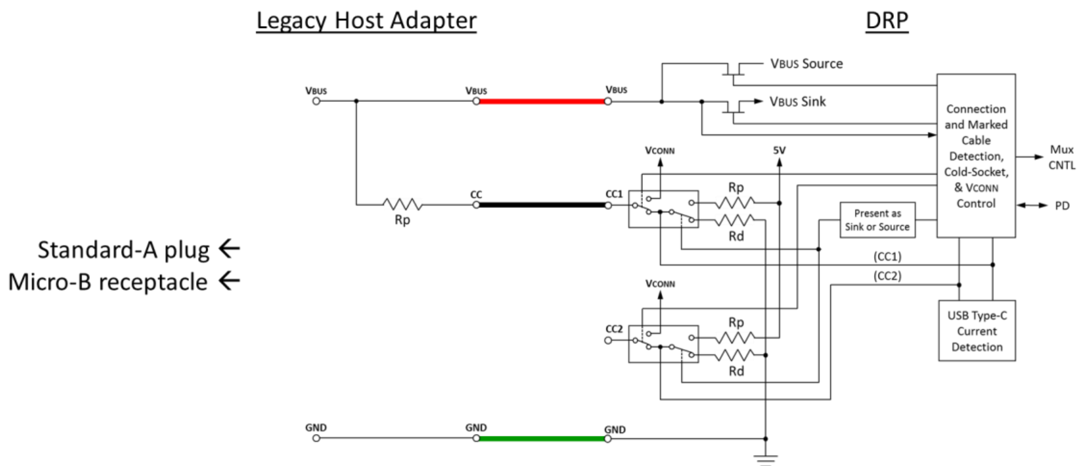
The following describes the behavior when a DRP is connected to a legacy device adapter that has an Rd to ground so as to mimic the behavior of a Sink.

1. DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SRC to Attached.SRC
   - DRP in Unattached.SRC detects the adapter's pull-down on CC and enters AttachWait.SRC
   - DRP in AttachWait.SRC times out (tCCDebounce) and transitions to Attached.SRC
   - DRP in Attached.SRC turns on VBUS and VCONN
   - DRP in AttachWait.SRC may support Try.SNK and if so, may transition through Try.SNK and TryWait.SRC prior to entering Attached.SRC
3. While the DRP is in the attached state:
   - DRP monitors CC for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.5.3.2.4 Legacy Host Port to DRP Behavior

Figure 4-35 illustrates the functional model for a legacy host port connected to a DRP operating as a Sink. This model is based on having an adapter that presents itself as a Source (Host) to the DRP operating as a Sink, this adapter is either a USB Standard-A legacy plug or a USB Micro-B legacy receptacle on one end and the USB Type-C plug on the other end plugged into a DRP.

Figure 4-35 Legacy Host Port to DRP Functional Model



The following describes the behavior when a legacy host adapter that has an Rp to VBUS so as to mimic the behavior of a Source is connected to a DRP. The value of Rp shall indicate an advertisement of Default USB Power (See Table 4-24), even though the cable itself can carry 3 A. This is because the cable has no knowledge of the capabilities of the power source, and any higher current is negotiated via *USB BC 1.2*.

1. DRP in the unattached state
   - DRP alternates between Unattached.SRC and Unattached.SNK
2. DRP transitions from Unattached.SNK to AttachWait.SNK to Attached.SNK
   - DRP in Unattached.SNK detects pull up on CC and enters AttachWait.SNK.
   - DRP in AttachWait.SNK detects VBUS and enters Attached.SNK
   - DRP in AttachWait.SNK may support Try.SRC and if so, may transition through Try.SRC and TryWait.SNK prior to entering Attached.SNK
3. While the DRP is in the attached state:
   - DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

4.6 Power

Power delivery over the USB Type-C connector takes advantage of the existing USB methods as defined by: the *USB 2.0* and *USB 3.2* specifications, the *USB BC 1.2* specification and the *USB Power Delivery* specification. Power for *USB4* operation requires a *USB PD* explicit contract as defined in Section 5.3 and the *USB Power Delivery* specification. Prior to entering a *USB PD* explicit contract, a *USB4* port operates as a *USB 3.2* port regarding power.

The USB Type-C Current mechanism allows the Source to offer more current than defined by the *USB BC 1.2* specification. A USB power source shall not provide more than 20 V nominal on VBUS. *USB PD* power sources that deliver power over a USB Type-C connector shall follow the power rules as defined in Section 10 of the *USB Power Delivery* specification.

All USB Type-C-based devices shall support USB Type-C Current and may support other USB-defined methods for power. The following order of precedence of power negotiation shall be followed: *USB BC 1.2* supersedes the *USB 2.0* and *USB 3.2* specifications, USB Type-C Current at 1.5 A and 3.0 A supersedes *USB BC 1.2*, and *USB Power Delivery* supersedes USB Type-C Current. Table 4-17 summarizes this order of precedence of power source usage.

Table 4-17 Precedence of power source usage

Precedence	Mode of Operation		Nominal Voltage	Maximum Current
Highest	*USB PD*		Configurable	5 A
	USB Type-C Current @ 3.0 A		5 V	3.0 A
↓	USB Type-C Current @ 1.5 A		5 V	1.5 A
	USB BC 1.2		5 V	Up to 1.5 A[1]
	Default USB Power	*USB 3.2*	5 V	See USB 3.2
Lowest		*USB 2.0*	5 V	See USB 2.0

Notes:

1. *USB BC 1.2* permits a power provider to be designed to support a level of power between 0.5 A and 1.5 A. If the *USB BC 1.2* power provider does not support 1.5 A, then it is required to follow power droop requirements. A *USB BC 1.2* power consumer may consume up to 1.5 A provided that the voltage does not drop below 2 V, which may occur at any level of power above 0.5 A.

For example, once the PD mode (e.g. a power contract has been negotiated) has been entered, the device shall abide by that power contract ignoring any other previously made or offered by the USB Type-C Current, *USB BC 1.2* or *USB 2.0* and *USB 3.2* specifications. When the PD mode is exited, the device shall fallback in order to the USB Type-C Current, *USB BC 1.2* or *USB 2.0* and *USB 3.2* specification power levels.

All USB Type-C ports shall tolerate being connected to USB power source supplying default USB power, e.g. a host being connected to a legacy USB charger that always supplies VBUS.

4.6.1 Power Requirements during USB Suspend

USB Type-C implementations with USB Type-C Current, *USB PD* and VCONN, along with active cables, requires the need to expand the traditional USB suspend definition.

4.6.1.1 VBUS Requirements during USB Suspend

The *USB 2.0* and *USB 3.2* specifications define the amount of current a Sink is allowed to consume during suspend.

USB suspend power rules shall apply when the USB Type-C Current is at the Default USB Power level or when *USB PD* is being used and the Suspend bit is set appropriately.

When USB Type-C Current is set at 1.5 A or 3.0 A, the Sink is allowed to continue to draw current from VBUS during USB suspend. During USB suspend, the Sink's requirement to track and meet the USB Type-C Current advertisement remains in force (See Section 4.5.2.3).

USB PD provides a method for the Source to communicate to the Sink whether or not the Sink has to follow the USB power rules for suspend.

4.6.1.2 VCONN Requirements during USB Suspend

If the Source supplies VBUS power during USB suspend, it shall also supply VCONN and meet the requirements defined in Table 4-5.

Electronically Marked Cables shall meet the requirements in Table 4-6 during USB suspend.

VCONN powered accessories shall meet the requirements defined in Table 4-7 during USB suspend.

4.6.2 VBUS Power Provided Over a USB Type-C Cable

The minimum requirement for VBUS power supplied over the USB Type-C cable assembly matches the existing requirement for VBUS supplied over existing legacy USB cable assemblies.

USB Power Delivery in Standard Power Range (SPR) operation is intended to work over unmodified USB Type-C to USB Type-C cables, therefore any USB Type-C cable assembly that incorporates electrical components or electronics shall ensure that it tolerate, or be protected from, a VBUS voltage of 21 V.

USB Power Delivery in Extended Power Range (EPR) operation requires EPR-compatible USB Type-C to USB Type-C cables. Any USB Type-C cable assembly that incorporates electrical components or electronics that may be powered by VBUS shall ensure that it can functionally tolerate, or be protected from, a VBUS voltage of up to 53.65 V (51 V + 5% + 100 mV).

4.6.2.1 USB Type-C Current

Default USB voltage and current are defined by the USB 2.0 and USB 3.2 specifications. All USB Type-C Current advertisements are at the USB VBUS voltage defined by these specifications.

The USB Type-C Current feature provides the following extensions:

- Higher current than defined by the USB 2.0, the USB 3.2 or the BC 1.2 specifications
- Allows the power source to manage the current it provides

The USB Type-C connector uses CC pins for configuration including an ability for a Source to advertise to its port partner (Sink) the amount of current it shall supply:

- Default is the as-configured for high-power operation current value as defined by the USB Specification (500 mA for USB 2.0 ports; 900 mA or 1,500 mA for USB 3.2 ports in single-lane or dual-lane operation, respectively)
- 1.5 A
- 3.0 A

When a Source is advertising USB Type-C Default current, the Sink behavior is defined as follows:

- It connects as a USB 2.0 or USB 3.2 device, after which the Sink shall follow the appropriate USB specification.
- It enters a USB PD contract, after which the Sink shall follow the USB PD specification to determine the current (e.g., Rp will no longer be Default as it is superseded by the USB PD contract).

- It detects a USB BC 1.2 charging port, after which the Sink shall follow the USB BC 1.2 specification.
- It attaches as a USB Type-C Power Sinking Device (PSD), after which the Sink may draw up to 500 mA and shall meet the inrush requirement for *USB 2.0*.

A PSD shall fully support USB Type-C Current operation, should support *USB PD* and may support USB BC 1.2. A PSD may be a Sink or a DRP operating in Sink mode. A PSD shall not have a USB or USB Type-C Alternate Mode communications function.

The relationship of USB Type-C Current and the equivalent *USB PD* Power (PDP) value is shown in Table 4-18.

Table 4-18 USB Type-C Current Advertisement and PDP Equivalent

USB Type-C Current		PDP Equivalent
Default	500 mA (*USB 2.0*)	2.5 W
	900 mA (*USB 3.2* single-lane)	4.5 W
	1,500 mA (*USB 3.2* dual-lane)	7.5 W
1.5 A		7.5 W
3.0 A		15 W

A Sink that takes advantage of the additional current offered (e.g., 1.5 A or 3.0 A) shall monitor the CC pins and shall adjust its current consumption within tSinkAdj to remain within the value advertised by the Source. While a *USB PD* contract is in place, a Sink is not required to monitor USB Type-C current advertisements and shall not respond to USB Type-C current advertisements.

The Source shall supply VBUS to the Sink within tVBUSON. VBUS shall be in the specified voltage range at the advertised current.

A Source (port supplying VBUS) shall protect itself from a Sink that draws current in excess of the port's USB Type-C Current advertisement.

The Source adjusts Rp (or current source) to advertise which of the three current levels it supports. See Table 4-24 for the termination requirements for the Source to advertise currents.

The value of Rp establishes a voltage (vRd) on CC that is used by the Sink to determine the maximum current it may draw.

Table 4-35 defines the CC voltage range observed by the Sink that only support default USB current.

If the Sink wants to consume more than the default USB current, it shall track vRd to determine the maximum current it may draw. See Table 4-36.

Figure 4-36 and Figure 4-37 illustrate where the Sink monitors CC for vRd to detect if the host advertises more than the default USB current.

Figure 4-36 Sink Monitoring for Current in Pull-Up/Pull-Down CC Model

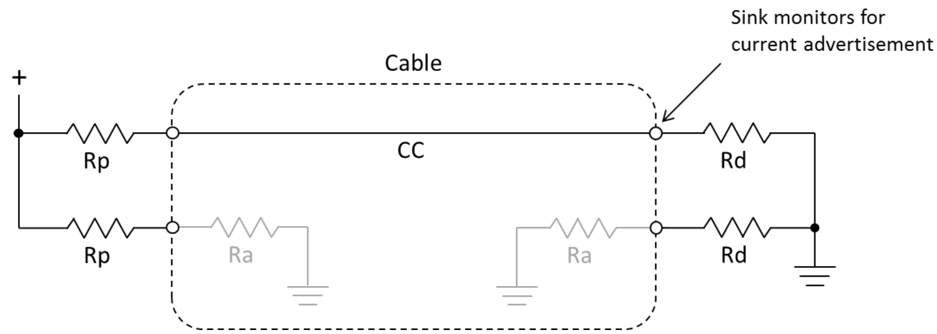
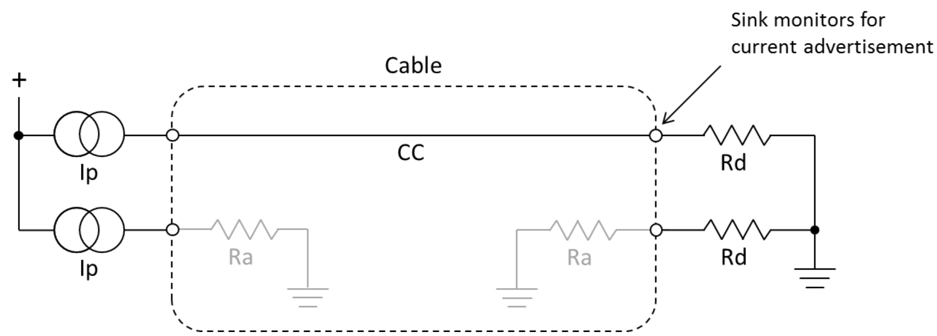


Figure 4-37 Sink Monitoring for Current in Current Source/Pull-Down CC Model



4.6.2.2 USB Battery Charging 1.2

USB Battery Charging Specification, Revision 1.2 defines a method that uses the USB 2.0 D+ and D− pins to advertise VBUS can supply up to 1.5 A. Support for *USB BC 1.2* charging is optional.

A USB Type-C port that implements *USB BC 1.2* that is capable of supplying at least 1.5 A shall advertise USB Type-C Current at the 1.5 A level within tVBUSON of entering the Attached.SRC state, otherwise the port shall advertise USB Type-C Current at the Default USB Power level. A USB Type-C port that implements *USB BC 1.2* that also supports USB Type-C Current at 3.0 A may advertise USB Type-C Current at 3.0 A.

If a Sink that supports *USB BC 1.2* detection, detects Rp at the Default USB Power level and does not discover a *USB BC 1.2*-compliant Source, then it shall limit its maximum current consumption to the standard USB levels based on Table 4-17. This will ensure maximum current limits are not exceeded when connected to a Source which does not support *USB BC 1.2*.

A Sink that supports *USB BC 1.2* detection and has a maximum current draw greater than Default USB Type-C Current shall monitor vRd on the CC pins to detect the Source's Rp and shall implement Sink Power Sub-State transitions (Figure 4-19). If a Sink that supports *USB BC 1.2* detection and has a maximum current draw greater than Default USB Type-C Current detects Rp at USB Type-C Current of 1.5 A or 3.0 A levels but does not detect a *USB BC 1.2* source, it shall limit its maximum current consumption to the appropriate USB Type-C Current level advertised, and shall adjust its current consumption to remain within the value advertised by the Source on Sub-State transitions. For Sub-State transitions starting from a higher power level and ending at a lower power level, the Sink shall reduce power consumption within tSinkAdj. See Sections 4.5.2.3.2.2 and 4.5.2.3.3.2.

While in a Power Delivery Mode, a device acting as a Sink shall not initiate a USB BC 1.2 detection until the port pair is detached or there is an Error Recovery or Hard Reset.

4.6.2.3 Proprietary Power Source

This section has been deprecated. Devices with USB Type-C connectors shall only employ signaling methods defined in USB specifications to negotiate power.

4.6.2.4 USB Power Delivery

USB Power Delivery is a feature on the USB Type-C connector. When USB PD is implemented, USB PD Bi-phase Mark Coded (BMC) carried on the CC wire shall be used for USB PD communications between USB Type-C ports.

At attach, VBUS shall be operationally stable prior to initiating USB PD communications.

Figure 4-38 illustrates how the USB PD BMC signaling is carried over the USB Type-C cable's CC wire.

Figure 4-38 USB PD over CC Pins

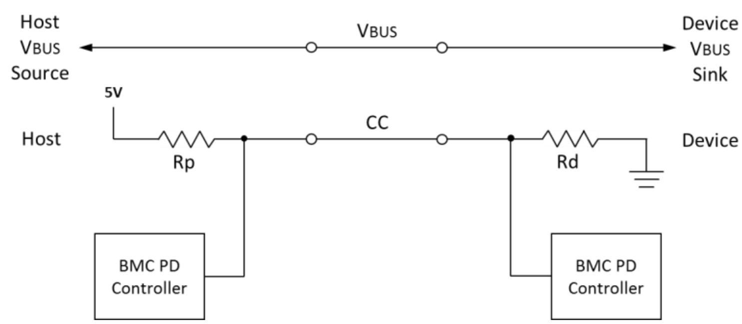
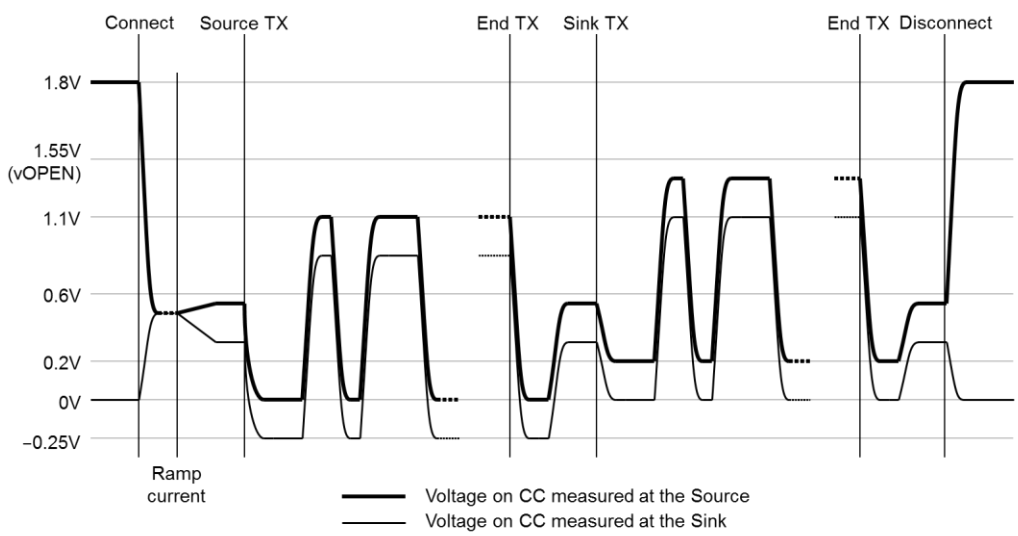


Figure 4-39 illustrates USB PD BMC signaling as seen on CC from both the perspective of the Source and Sink. The breaks in the signaling are intended to represent the passage of time.

Figure 4-39 USB PD BMC Signaling over CC



When not in an Explicit Contract, *USB PD* Sources that are, based on their PDP, capable of supplying:

- 5 V at 3 A or greater shall advertise USB Type-C Current at the 3 A level
- 5 V at 1.5A or greater but less than 3 A shall advertise USB Type-C Current at the 1.5 A level
- 5 V at less than 1.5A shall advertise USB Type-C Current at the Default USB Power level

within tVBUSON of entering the Attached.SRC state. For Multi-Port Shared Capacity Chargers, a *USB PD* Source capable of supplying 5 V at 3A or greater may initially offer USB Type-C Current at the 1.5 A level and subsequently increase the offer after attach (see Section 4.8.6.2). During USB Suspend a *USB PD* Source may set its Rp value to default to indicate that the Sink shall only draw USB suspend current as defined in Section 4.6.1.1.

While a *USB PD* Explicit Contract is in place, a Source compliant with *USB PD* Revision 2 shall advertise a USB Type-C Current of either 1.5 A or 3.0 A. The *USB PD* Revision 2 Source upon entry into an Explicit Contract shall advertise an Rp value of 1.5 A or 3.0 A after it receives the GoodCRC in response to the first PS_RDY Message.

While a *USB PD* Explicit Contract is in place, a Source compliant with USB PD Revision 3 shall set the Rp value according to the collision avoidance scheme defined in Section 5.7 of the *USB PD* Revision 3 specification. The *USB PD* Revision 3 Source upon entry into an Explicit Contract shall advertise an Rp value consistent with the *USB PD* Revision 3 collision avoidance scheme.

Refer to Section 1.6 of the *USB Power Delivery* specification for a definition of an Explicit Contract.

4.6.2.5 Charge-Through VCONN-Powered USB Device (CTVPD) Current Limitations

Since Charge-Through VCONN-Powered USB Devices implement charging by passively connecting the Source's CC and VBUS to the Host, the VCONN-Powered USB Device is effectively increasing the impedance on VBUS, GND, and CC between the Power Source and the Host, resulting in impedances that can exceed the maximum allowed for cables. To avoid communication issues and false disconnects from the increased GND and VBUS drops, the following shall occur:

1. The Charge-Through VCONN-Powered USB Device shall report its worst-case GND and VBUS impedance (including the extra mated connector pair and FETs) in its *USB PD* Discover Identity Command response on SOP'.
2. The Host that supports Charge-Through VCONN-Powered USB Device shall use this information, along with inferred information about the cable, to limit its maximum current in the case where the Power Source advertises a current greater than what the Charge-Through VCONN-Powered USB Device would allow.

The Host has no way to query the cable, as its VCONN source is consumed by the VCONN-Powered USB Device. Instead, the Host may assume the cable is 5 A for the purposes of calculating the Charge-Through current limit only if it receives a *USB PD* SourceCapability PDO of greater than 3 A (even if the Host ultimately does not Request that PDO, or if the host requests a current of 3 A or less).

The Host shall further limit its maximum current beyond that advertised by the Power Source, based on the reported GND impedance and the inferred cable capability. GND impedance is reported in the VPD Discover Identity Command Response in 1-milliohm steps and is used in the following formulas:

- GND-limited current with a 3A cable inferred = 0.25 V / (0.25 V / 3 A + VPD_GND_DCR)
- GND-limited current with a 5A cable inferred = 0.25 V / (0.25 V / 5 A + VPD_GND_DCR)

Some examples are in Table 4-19.

Table 4-19 Sink Maximum Current Limit When Attached to CTVPD

Reported GND Impedance	3A Cable Inferred[1]	5A Cable Inferred[2]
0.010 Ω	2.679 A	4.167 A
0.015 Ω	2.542 A	3.846 A
0.020 Ω	2.419 A	3.571 A
0.025 Ω	2.308 A	3.333 A
0.030 Ω	2.206 A	3.125 A
0.035 Ω	2.113 A	2.941 A
0.040 Ω	2.027 A	2.778 A

Notes:

1. As calculated by 0.25 V / (0.25 V / 3 A + VPD_GND_DCR).
2. As calculated by 0.25 V / (0.25 V / 5 A + VPD_GND_DCR).

In addition, the increased VBUS impedance could result in a greater than 1 V VBUS drop as measured at the input to the Host. Based on the VBUS impedance reported in the VPD Discover Identity Command Response in 2-milliohm steps and the inferred cable capability, the Host shall either lower its VBUS detach threshold or further limit its maximum current based on the following formulas:

- VBUS and GND-limited current with a 3A cable inferred = 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR)
- VBUS and GND-limited current with a 5A cable inferred = 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR)

Table 4-20 Example Charge-Through VPD Sink Maximum Currents based on VBUS Impedance and GND Impedance

Reported VBUS Impedance[4]	Reported GND Impedance[4]	3A Cable Inferred[1]	5A Cable Inferred[2]
0.020 Ω	0.010 Ω	2.679 A	4.167 A
0.030 Ω	0.015 Ω	2.542 A	3.846 A
0.040 Ω	0.020 Ω	2.419 A	3.571 A
0.050 Ω	0.025 Ω	2.308 A	3.333 A
0.060 Ω	0.030 Ω	2.206 A	3.125 A
0.070 Ω	0.035 Ω	2.113 A	2.941 A
0.080 Ω	0.040 Ω	2.027 A	2.778 A

Notes:

1. As calculated by 0.75 V / (0.75 V / 3 A + VPD_VBUS_DCR + VPD_GND_DCR).
2. As calculated by 0.75 V / (0.75 V / 5 A + VPD_VBUS_DCR + VPD_GND_DCR).
3. Table does not show all allowable combinations, only a subset provided for illustration.
4. The ratio of the reported VBUS impedance to the reported GND impedance is 2:1.

4.6.2.6 USB Type-C Sink Requirements for High Voltage Operation

This section sets electrical requirements for USB Type-C Sinks that support high-voltage operation. See Section 3.11 for EPR requirements for USB Type-C cables that support EPR.

The Sink shall keep the voltage on its VBUS contact to within 12 volts of the voltage on the Source VBUS contact at the time of the cable plug withdrawal for a minimum of 250 µs from the time the VBUS contacts separate (see Figure 3-1). Refer to Appendix H for more information related to high-voltage contact arcing and mitigation guidelines.

4.7 USB Hubs

USB 2.0, *USB 3.2*, and *USB4* hubs are defined by the *USB 2.0*, *USB 3.2*, and *USB4* specifications, respectively. USB hubs implemented with one or more USB Type-C connectors shall comply with these specifications as relevant to a USB Type-C implementation. All the downstream facing USB Type-C ports on a USB hub should support the same functionality or shall be clearly marked as to the functionality supported.

USB hubs shall have an upstream facing port (to connect to a host or hub higher in the USB tree) that may be a Sourcing Device (See Section 4.8.4). The hub shall clearly identify to the user its upstream facing port. This may be accomplished by physical isolation, labeling or a combination of both.

USB hub's downstream facing ports shall not have Dual-Role-Data (DRD) capabilities. However, these ports may have Dual-Role-Power (DRP) capabilities.

CC pins are used for port-to-port connections and shall be supported on all USB Type-C connections on the hub.

For *USB 2.0* and *USB 3.2* hubs, downstream-facing ports shall not implement or pass-through Alternate or Accessory Modes and SBU pins shall not be connected (zSBUTermination) on any USB hub port. For *USB4* hubs, see Section 5.2.3.2 regarding support for Alternate Modes.

The USB hub's DFPs shall support power source requirements for a Source. See Section 4.8.1.

Additional requirements for *USB4* hubs are in Chapter 5.

4.8 Power Sourcing and Charging

This section defines requirements and recommendations related to using USB Type-C ports for delivering power. Any USB Type-C port that offers more than Default Current and/or supports USB Power Delivery shall meet the requirements as if it is a charger.

The following lists the most applicable subsections by USB Type-C ports on:

- Host systems: 4.8.1 and 4.8.5. Note: 4.8.6 is not intended for host systems.
- Devices that can supply power: 4.8.4.
- Hubs:
    - Traditional hubs – Refer to USB 2.0/USB 3.2 base specifications and 4.8.1 as applicable if *USB BC 1.2* is supported.
    - Hubs that can supply power beyond the base specs – 4.8.1, 4.8.4, 4.8.5 and 4.8.6.
- Dedicated chargers:
    - Single-port chargers – 4.8.1.
    - Multi-port chargers – 4.8.1 and 4.8.6.

4.8.1 DFP as a Power Source

Sources (e.g. battery chargers, hub downstream ports and hosts) may all be used for battery charging. When a charger is implemented with a USB Type-C receptacle or a USB Type-C captive cable, it shall follow all the applicable requirements.

- A Source shall expose its power capabilities using the USB Type-C Current method and it may additionally support other USB-standard methods (*USB BC 1.2* or *USB-PD*).
- A Source advertising its current capability using *USB BC 1.2* shall meet the requirements in Section 4.6.2.2 regarding USB Type-C Current advertisement.
- A Source that has negotiated a *USB-PD* contract shall meet the requirements in Section 4.6.2.4 regarding USB Type-C Current advertisement.
- If a Source is capable of supplying a voltage greater than default VBUS, it shall fully conform to the *USB-PD* specification and shall negotiate its power contracts using only *USB-PD*.
- If a Source is capable of reversing source and sink power roles, it shall fully conform to the *USB-PD* specification and shall negotiate its power contracts using only *USB-PD*.
- If a Source is capable of supplying a current greater than 3.0 A, it shall use the *USB-PD* Discover Identity to determine the current carrying capacity of the cable.

4.8.1.1 USB-based Chargers with USB Type-C Receptacles

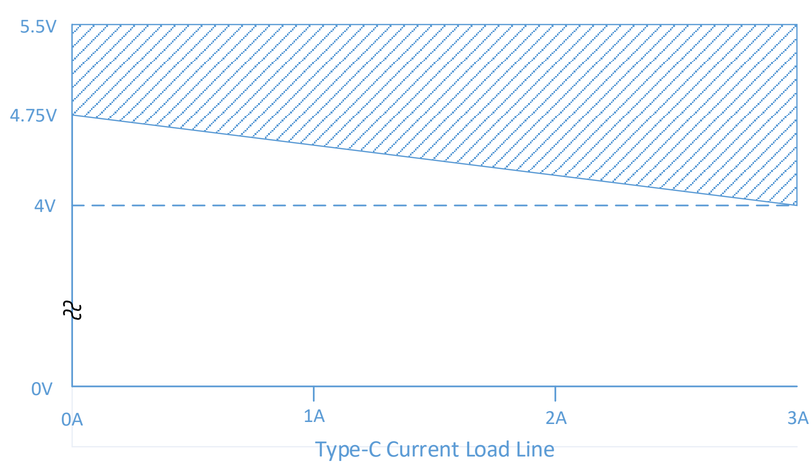
- A USB-based charger with a USB Type-C receptacle (Source) shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).

- A USB-based charger with a USB Type-C receptacle shall not advertise current exceeding 3.0 A except when it uses the *USB-PD* Discover Identity mechanism to determine the cable's actual current carrying capability and then it shall limit the advertised current accordingly.
- A USB-based charger with a USB Type-C receptacle (Source) which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A within tVBUSON of entering the Attached.SRC state and shall short D+ and D− together with a resistance less than 200 ohms. This will ensure backwards compatibility with legacy sinks which may use *USB BC 1.2* for charger detection.

4.8.1.2 USB-based Chargers with USB Type-C Captive Cables

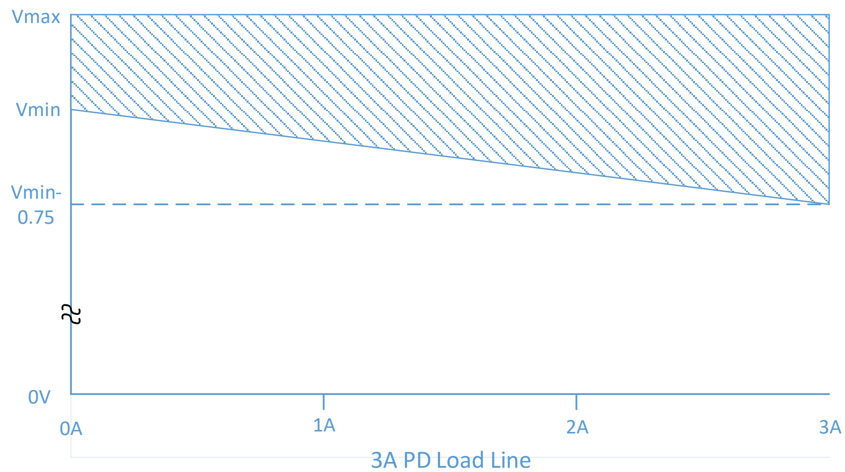
- A USB-based charger with a USB Type-C captive cable that supports USB PD shall only apply power to VBUS when it detects a Sink is attached and shall remove power from VBUS when it detects the Sink is detached (vOPEN).
- A USB-based charger with a USB Type-C captive cable that does not support USB PD may supply VBUS at any time. It is recommended that such a charger only apply power to VBUS when it detects a Sink is present and remove power from VBUS when it detects the Sink is not present (vOPEN).
- A USB-based charger with a USB Type-C captive cable shall limit its current advertisement so as not to exceed the current capability of the cable (up to 5 A).
- A USB-based charger with a USB Type-C captive cable which is not capable of data communication shall advertise USB Type-C Current of at least 1.5 A. It shall short D+ and D− together with a resistance less than 200 ohms. This will ensure backwards compatibility with legacy sinks which may use *USB BC 1.2* for charging detection.
- The voltage as measured at the plug of a USB-based charger with a USB Type-C captive cable may be up to 0.75 × I / 3 V (0 < I ≤ 3 A), or 0.75 × I / 5 V (0 < I ≤ 5 A) lower than the standard tolerance range for the chosen voltage, where I is the actual current being drawn.
    - A USB-based charger that advertises USB Type-C Current shall output a voltage in the range of 4.75 V – 5.5 V when no current is being drawn and between 4.0 V – 5.5 V at 3 A. The output voltage as a function of load up to the advertised USB Type-C Current (default, 1.5 A and 3 A) shall remain within the cross-hatched area shown in Figure 4-40.

Figure 4-40 USB Type-C Cable's Output as a Function of Load for Non-PD-based USB Type-C Charging



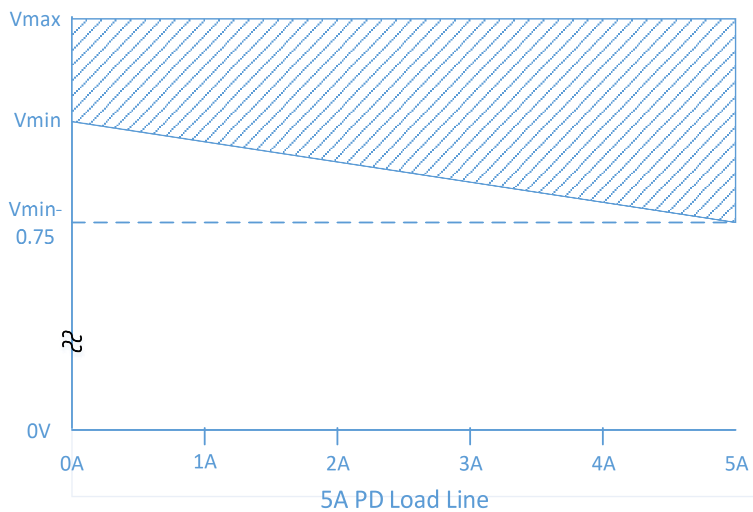
- A USB PD-based charger that has negotiated a voltage V at ≤ 3 A shall output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 3 A. Under all loads, the output voltage shall remain within the cross-hatched area shown in Figure 4-41.

Figure 4-41 0 – 3 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load



- A USB PD-based charger that has negotiated a voltage V at between 3 A and 5 A shall output a voltage in the range of Vmax (V + 5%) and Vmin (V – 5%) when no current is being drawn and Vmax and Vmin – 0.75 V at 5 A. Under all loads, the output voltage shall remain within the cross hatched area shown in Figure 4-42.

Figure 4-42 3 – 5 A USB PD-based Charger USB Type-C Cable's Output as a Function of Load



- Note: The maximum allowable cable IR drop for ground is 250 mV (see Section 4.4.1). This is to ensure the signal integrity of the CC wire when used for connection detection and *USB PD* BMC signaling.

4.8.2 Non-USB Charging Methods

A product (Source and/or Sink) with a USB Type-C connector shall only employ signaling methods defined in USB specifications to negotiate power over its USB Type-C connector(s).

4.8.3 Sinking Host

A Sinking Host is a special sub-class of a DRP that is capable of consuming power but is not capable of acting as a USB device. For example a hub's DFP or a notebook's DFP that operates as a host but not as a device.

The Sinking Host shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). The Sinking DFP shall support *USB PD* and shall support the DR_Swap command in order to get the Sink into the DFP data role.

4.8.4 Sourcing Device

A Sourcing Device is a special sub-class of a DRP that is capable of supplying power but is not capable of acting as a USB host. For example a hub's UFP or a monitor's UFP that operates as a device but not as a host.

The Sourcing Device shall follow the rules for a DRP (See Section 4.5.1.4 and Figure 4-15). It shall also follow the requirements for the Source as Power Source (See Section 4.8.1). The Sourcing Device shall support *USB PD* and shall support the DR_Swap command in order to enable the Source to assume the UFP data role.

4.8.5 Charging a System with a Dead Battery

A system that supports being charged by USB whose battery is dead shall apply Rd to both CC1 and CC2 and follow all Sink rules. When it is connected to a Source, DRP or Sourcing Device, the system will receive the default V_{BUS}. It may use any allowed method to increase the amount of power it can use to charge its battery.

Circuitry to present Rd in a dead battery case only needs to guarantee the voltage on CC is pulled within the same range as the voltage clamp implementation of Rd in order for a Source to recognize the Sink and provide V_{BUS}. For example, a 20% resistor of value Rd in series with a FET with V_{GTH}(max) < V_{CLAMP}(max) with the gate weakly pulled to CC would guarantee detection and be removable upon power up.

When the system with a dead battery has sufficient charge, it may use the *USB PD* DR_Swap message to become the DFP.

4.8.6 USB Type-C Multi-Port Chargers

A USB Type-C Multi-Port Charger is a product that exposes multiple USB Type-C Source ports for the purpose of charging multiple connected devices. A compliant USB Type-C charger may offer on each of its ports a mix of power options as defined in Section 4.6.

Multi-Port Chargers will generally fall into two categories as defined by the following.

1. Assured Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is equal to the total power delivery capacity of the charger.

2. Shared Capacity Chargers: a multi-port charger where the sum of the maximum capabilities of all of the exposed ports, as indicated to the user, is less than the total power delivery capacity of the charger.

A Multi-Port Charger may offer in a single product separate visually identifiable groupings of charging ports. In this case, each group can independently offer either one of the two charging categories, either an Assured Capacity Charger or a Shared Capacity Charger.

This section defines the requirements and provides guidelines for the operation and behavior of a USB Type-C Multi-Port Charger.

4.8.6.1 General Requirements

Individual source ports shall always comply with power negotiation and rules set forth by the USB Type-C and USB Power Delivery specifications, adjusted as needed when available resources change as other ports take more or less power.

The minimum capability of all individual USB Type-C ports of a USB Type-C Multi-Port Charger shall be 5V @ 1.5 A independent of how many of the other ports are in use.

When a USB Type-C Charger includes charging ports that are based on USB Standard-A receptacles, the following requirements shall be met.

- The USB Standard-A ports shall be implemented as an independent group, i.e. USB Standard-A ports shall not be included in a group of USB Type-C ports behaving as a Shared Capacity Charger. Any load change on a USB Type-A port shall not result in a voltage change on any of the USB Type-C ports and vice-versa.
- The minimum capability of each USB Standard-A port shall be 5V @ 500 mA independent of how many of the other ports are in use.

4.8.6.2 Multi-Port Charger Behaviors

Each Source port of Assured Capacity Chargers shall, by design, behave independently and be unaffected by the status and loading of the other ports. An exception to this behavior is allowed if the charger has to take any action necessary to meet an overall product operational safety requirement due to unexpected behavior on any port.

For Shared Capacity Chargers, the following behavioral rules shall apply:

- Each of the exposed Source Ports shall have the same power capabilities. Each port of the charger shall be capable of the same maximum capability, minimum capability, and be able to draw from the shared power equally.
- All exposed USB PD unattached Source Ports shall have the same power capabilities.
    - Ports shall have the ability to supply the available shared capacity power up to the port's maximum power.
        - A shared capacity charger's ports may offer less than this value but shall increase the offer up to the required value when the Sink sets the Capabilities Mismatch bit in its response. This may be done in multiple steps, but all ports in the Shared Capacity Group shall reach the maximum power within three seconds.
    - Whenever a power contract is made or changed on any port, the available shared capacity shall be re-computed, and the source shall send updated Source Capability messages as needed.
        - As ports of a Shared Capacity Group are connected, each remaining unattached Source Port shall be capable of advertising the lower of the Maximum Capability of the port OR the Total Shared Capacity –

the contracted power for the attached ports – (the number of unattached ports – 1) * the minimum port power.

- Ports shall offer at least 7.5 W.
- When calculating the available shared capacity for ports in a Fixed Supply power contract, the shared capacity charger shall use the Voltage times the Maximum Current in the PDO as the power the port is supplying regardless of the actual Operating Current requested in the RDO request.
- When calculating the available shared capacity for ports in a PPS power contract, the shared capacity charger shall use the Maximum Voltage times the Maximum Current in the APDO as the power the port is supplying regardless of the actual voltage and current in the RDO request.
- Ports when not in a PD contract shall follow the rules for a shared USB Type-C Current source unless there is sufficient remaining power for each port to advertise 15 W.

- All exposed USB Type-C Current ports shall have the ability to offer the same power capabilities.
  - All ports shall initially offer at least 1.5 A.
  - The total of offers across all the ports shall never exceed the capacity of the shared supply.
  - Ports that initially offer 1.5 A shall increase to 3 A after attach if they have sufficient available shared capacity within one second.
  - Ports shall never offer less than 1.5 A – e.g. shall not offer Default.

As Source ports are connected and begin providing power, the remaining Source ports will each have the same power capabilities. The maximum capability may be less than the previously connected ports due to less unused capacity of the total power delivery capacity of the charger. For example, if the total power delivery capacity of a USB Type-C two-port charger is 60 W with a port PDP of 35 W and the first connected Source port has established a 35 W power contract with its connected Sink, then the second Source port will only be able to offer a PDP of 25 W.

Each port should start by offering the minimum capability for the port and increase the offering to the Sink upon a connection. For example, if the maximum capability of a USB Type-C only Source port is 3 A, then all of the exposed Source ports will be able to offer 3 A. Each port should start by offering less than the max (such as 1.5 A) and then increase the offering to 3 A after an attach. This would happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase to 3 A offering. A sink, in this example, would see a starting advertisement of USB Type-C Current @ 1.5 A at attach and would then see the USB Type-C Current advertisement increase to 3 A. As another example, if the maximum capability of a USB Type-C Source port is to offer *USB PD* with a PDP of 35 W, then all of the exposed Source ports would also support *USB PD* 35 W. Each port would start by offering something less on initial connection, like 15 W, and then increase the offering with new Source Capabilities when it determines the Sink would like more power. If the Sink is not offered the power it requires, it will send a request with the Capability Mismatch bit set to indicate to the source it wants more power. This will happen for each port as it is connected until the unused shared capacity is exhausted, at which point no other ports would increase the power offering.

When establishing the remaining available capacity, a charger that supports policy-based power rebalancing may include the power that can be reclaimed from ports already in use:

1. by adjusting advertised source capabilities equivalent with a reduced PDP to one or more ports that are already in use; or
2. by issuing a *USB PD* GotoMin command to one or more ports already in use.

Policy-based power rebalancing should consider providing good user experience and preserving nominal USB functionality on impacted devices. Fixed rebalancing algorithms that do not factor in overall USB system policy may not be appropriate for power rebalancing implementations.

4.8.6.3 Multi-Port Charger Port Labeling

Multi-port chargers shall have OEM-designed port labeling consistent with the following rules.

- For Assured Capacity Chargers, each exposed Source port shall be labeled to indicate the PDP of the port. In this case, the user will be able to expect that each of the labeled ports will be able to meet power contracts consistent with the labeling independent of how many of the Source ports are in use.
- For Shared Capacity Chargers, each Source port shall be labeled to indicate the same PDP. Additionally, the charger shall have a label that, with a minimum of equal visual prominence, indicates the total power delivery capacity being shared across all of the ports identified as a group.

A Multi-Port Charger that offers in a single product separate groupings of charging ports, each grouping shall be clearly identified as a separate grouping and each grouping shall be individually labeled consistent with that group's behavior model, either as an Assured Capacity Charger or a Shared Capacity Charger.

Refer to the USB Implementers Forum (USB-IF) for USB Type-C Chargers certification along with further labeling guidelines.

4.8.6.4 Multi-Port Charger that include USB Data Hub Functionality

Multi-Port chargers that also incorporate USB data hub capabilities shall meet the same requirements as standalone chargers. These charging-capable hubs shall be self-powered and shall fully operate as a charger independent of the state of the USB data bus connections.

For hub-based Multi-Port Chargers that offer power to the upstream-facing port (to the host), this port may either behave as an Assured Capacity Charging port (e.g. be a dedicated charging port) or as a Shared Capacity Charging port (e.g. sharing capacity with downstream-facing ports). In either case, it should be clearly labeled consistent with its designed behavior, including identifying it as part of a group if it is sharing capacity with other ports.

When the upstream-facing port is sharing capacity with the downstream-facing ports, the PDP of the upstream-facing port can differ from the downstream-facing ports.

4.9 Electronically Marked Cables

All USB Full-Featured Type-C cables shall be electronically marked. USB 2.0 Type-C cables may be electronically marked. An eMarker is element in an Electronically Marked Cable that returns information about the cable in response to a *USB PD* Discover Identity command.

Electronically marked cables shall support *USB Power Delivery* Structured VDM Discover Identity command directed to SOP' (the eMarker). This provides a method to determine the characteristics of the cable, e.g. its current carrying capability, its performance, vendor identification, etc. This may be referred to as the USB Type-C Cable ID function.

Prior to an explicit *USB PD* contract, a Sourcing Device is allowed to use SOP' to discover the cable's identity. After an explicit *USB PD* contract has been negotiated, only the Source shall communicate with SOP' and SOP" (see Section 6.2.1).

Passive cables that include an eMarker shall follow the Cable State Machine defined in Section 4.5.2.4 and Figure 4-20.

Once VCONN is available, all electronically marked cables shall use it as the only power source. If VCONN is applied after VBUS then until VCONN is available, the cable may remain unpowered or may draw power from VBUS. Within tVCONNSwitch, the cable shall switch from VBUS to VCONN. Cables that include an eMarker shall meet the maximum power defined in Table 4-6. The only exception is an Optically Isolated Active Cable (OIAC Section 6), which can draw from both VCONN and VBUS.

Refer to Table 4-5 for the requirements of a Source to supply VCONN. When VCONN is not present, a powered cable shall not interfere with normal CC operation including Sink detection, current advertisement and *USB PD* operation.

Figure 4-43 illustrates a typical electronically marked cable. The isolation elements (Iso) shall prevent VCONN from traversing end-to-end through the cable. Ra is required in the cable to allow the Source to determine that VCONN is needed.

Figure 4-43 Electronically Marked Cable with VCONN connected through the cable

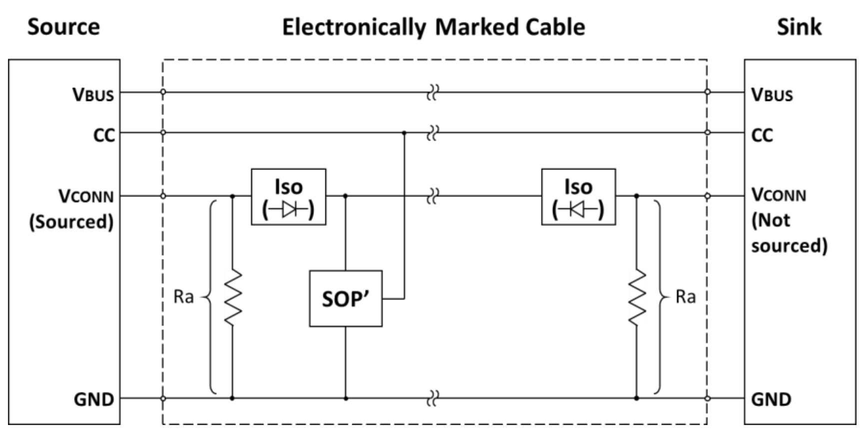
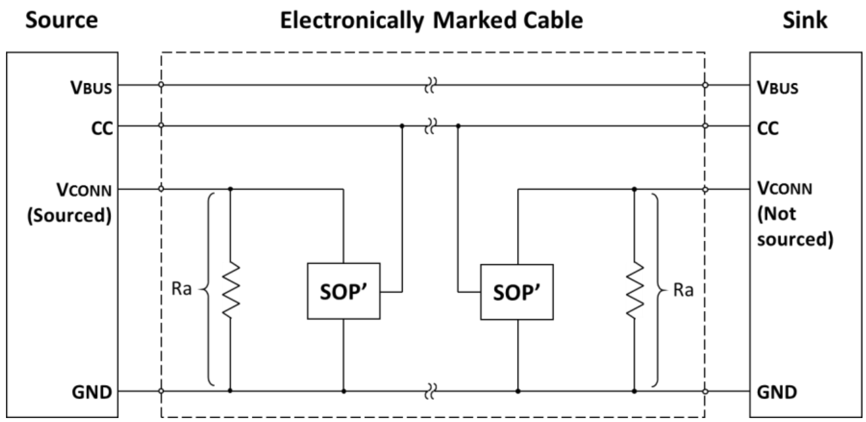


Figure 4-44 illustrates an electronically marked cable where the VCONN wire does not extend through the cable, therefore an SOP' (eMarker) element is required at each end of the cable. In this case, no isolation elements are needed.

Figure 4-44 Electronically Marked Cable with SOP' at both ends



For cables that only respond to SOP', the location of the responder is not relevant.

4.9.1 Parameter Values

Table 4-21 provides the power on timing requirements for the eMarker SOP' and SOP" to be ready to communicate.

Table 4-21 SOP' and SOP" Timing

	Maximum	Description
tVCONNStable	50 ms	The time between the application of VCONN until SOP' and SOP" shall be ready for communication.

4.9.2 Active Cables

An active cable is an electronically marked cable that incorporates data bus signal conditioning circuits, for example to allow for implementing longer cables. Active cables with data bus signal conditioning in both plugs shall implement SOP' and may implement SOP". Active cables shall meet the power requirements defined in Table 4-6.

Active cables may support either one TX/RX pair or two TX/RX pairs. The eMarker in the cable shall identify the number of TX/RX lanes supported. Active cables may or may not require configuration management. Active cable configuration management is defined in Section 5.5.4.

4.10 VCONN-Powered Accessories (VPAs) and VCONN-Powered USB Devices (VPDs)

VCONN-Powered Accessories and VCONN-Powered USB Devices are both direct-attach Sinks that can operate with just VCONN.

Both expose a maximum impedance to ground of Ra on the VCONN pin and Rd on the CC pin.

The removal of VCONN when VBUS is not present shall be treated as a detach event.

4.10.1 VCONN-Powered Accessories (VPAs)

A VCONN-Powered Accessory implements an Alternate Mode (See Appendix E).

VCONN-Powered Accessories shall comply with Table 4-7.

When operating in the Sink role and when VBUS is not present, VCONN-Powered Accessories shall treat the application of VCONN as an attach signal, and shall respond to *USB Power Delivery* messages.

When powered by only VCONN, a VCONN-Powered Accessory shall negotiate an Alternate Mode. If it fails to negotiate an Alternate Mode within tAMETimeout, its port partner removes VCONN.

When VBUS is supplied, a VCONN-Powered Accessory is subject to all of the requirements for Alternate Modes, including presenting a *USB Billboard Device Class* interface if negotiation for an Alternate Mode fails.

Should a VCONN-Powered Accessory wish to provide charge-through functionality, it must do so by negotiating voltage and current independently on both the Host and charge-through ports, and possibly re-regulating the voltage from the Source before passing it through to the Sink. The Sink is able to take the full current that is advertised to it by the VCONN-Powered Accessory.

4.10.2 VCONN-Powered USB Devices (VPDs)

A VCONN-Powered USB Device shall implement a USB UFP endpoint.

VCONN-Powered USB Devices shall comply with Table 4-8.

When VBUS is not present, VCONN-Powered USB Devices shall treat the application of VCONN as an attach signal.

A VCONN-Powered USB Device shall respond to *USB PD* messaging on SOP' and shall not respond to other USB PD messaging. A VCONN-Powered USB Device shall respond to USB PD Hard Reset and Cable Reset signaling.

A Charge-Through VCONN -Powered USB Device shall discard all *USB PD* messages while a connection is enabled between the host port CC and Charge-Through port CC.

When VBUS is supplied by the Host, the VCONN-Powered USB Device shall behave like a normal UFP Sink, but still only respond to *USB PD* messaging on SOP'. If VBUS is subsequently removed while VCONN remains applied, the VCONN-Powered USB Device shall remain connected, and use VCONN as the sole detach signal.

Since VCONN-Powered USB Devices do not respond to *USB PD* on SOP, they cannot enter Alternate Modes.

A VCONN-Powered USB Device may provide Charge-Through functionality via VPD Charge-Through. VCONN-Powered USB Devices shall not provide any data pass-through to the Charge-Through port other than the CC wire.

Since the power and CC negotiation is passed through directly, the Sink shall limit its maximum current based on the additional impedance introduced by the VCONN-Powered USB Device.

Additionally, since power can only flow from the Charge-Through port to the Host, VCONN must be provided by the host, and there is no data connection beyond the CC wire passed through to the connected source, there are limitations on what the Host can advertise and support via *USB PD*:

- The Host shall not negotiate or accept a PR_Swap or VCONN_Swap

- The Host shall not enable FR_Swap
- The Host may only negotiate a DR_Swap when using *USB PD* Revision 2.0, and only for the purpose of switching which side initiates PD communications. The Host will always remain a DFP for USB data.
- The Host shall not advertise dual-role data or dual-role power in its SourceCapability or SinkCapability messages – Host changes its advertised capabilities to UFP role/sink only role.
- The Host shall not negotiate any Alternate Modes that change the function of pins on the connector.
- The Host shall represent itself to the Charge-Through Source using *USB PD* as if it were a Sink-only, data-less device.

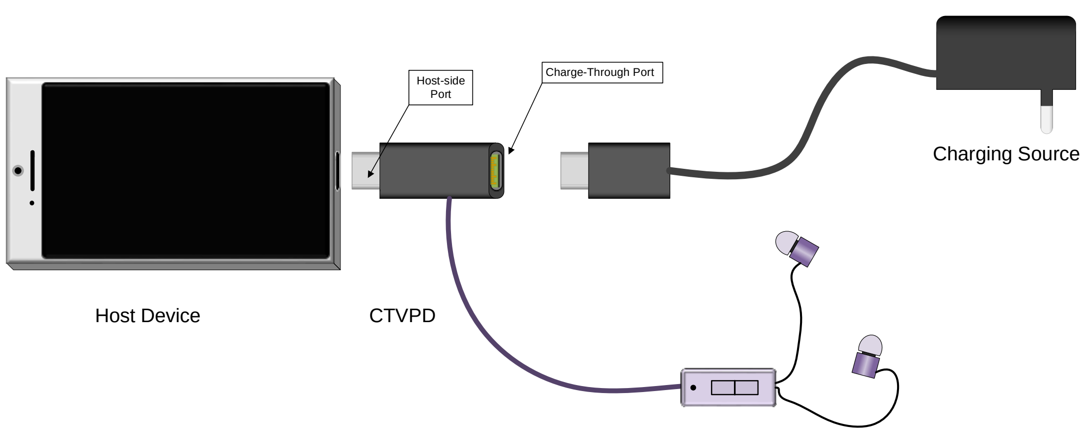
Table 4-22 Charge-Through VPD CC Impedance (RccCON) Requirements

	Minimum	Maximum	Description
RccCON		15 Ω	Impedance in the Charge-Though VPD while a connection is enabled between the host port CC and Charge-Through port CC.
	zOPEN		Impedance between the host port CC and Charge-Through CC when a connection is disabled.

Table 4-23 CTVPD Charge-Through Port VBUS Bypass Requirements

	Minimum	Maximum	Description
CCTB	1 µF	10 µF	Bypass capacitance on Charge-Through port VBUS connection to support ADP max CADP_THR

Figure 4-45 Example Charge-Through VCONN-Power USB Device Use Case



4.11 Parameter Values

4.11.1 Termination Parameters

Table 4-24 provides the values that shall be used for the Source's Rp or current source. Other pull-up voltages shall be allowed if they remain less than 5.5 V and fall within the correct voltage ranges on the Sink side – see Table 4-32, Table 4-33 and Table 4-34. Note: when two Sources are connected together, they may use different termination methods which could result in unexpected current flow.

Table 4-24 Source CC Termination (Rp) Requirements

Source Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 μA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 μA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 μA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

Notes:

1. For Rp when implemented in the USB Type-C plug on a USB Type-C to *USB 3.1* Standard-A Cable Assembly, a USB Type-C to *USB 2.0* Standard-A Cable Assembly, a USB Type-C to *USB 2.0* Micro-B Receptacle Adapter Assembly or a USB Type-C captive cable connected to a USB host, a value of 56 kΩ ± 5% shall be used, in order to provide tolerance to IR drop on VBUS and GND in the cable assembly.

The Sink may find it convenient to implement Rd in multiple ways simultaneously (a wide range Rd when unpowered and a trimmed Rd when powered). Transitions between Rd implementations that do not exceed tCCDebounce shall not be interpreted as exceeding the wider Rd range. Transitions between Rd implementations shall not allow the voltage on CC to go outside the voltage band that defines a connection. Table 4-25 provides the methods and values that shall be used for the Sink's Rd implementation.

Table 4-25 Sink CC Termination (Rd) Requirements

Rd Implementation	Nominal value	Can detect power capability?	Max voltage on pin
± 20% voltage clamp[1]	1.1 V	No	1.32 V
± 20% resistor to GND	5.1 kΩ	No	2.18 V
± 10% resistor to GND	5.1 kΩ	Yes	2.04 V

Note:

1. The clamp implementation inhibits *USB PD* communication although the system can start with the clamp and transition to the resistor once it is able to do *USB PD*.

Table 4-26 provides the impedance value to ground on VCONN in powered cables.

Table 4-26 Powered Cable Termination Requirements

	Minimum Impedance	Maximum Impedance
Ra	800 Ω[1]	1.2 kΩ

Note:
1. The minimum impedance may be less after VCONN is applied. The current consumed from VCONN shall be as specified in Table 4-6, Table 4-7, and Table 4-8 when the voltage is less than vVCONNValid. The voltage across Ra when connected to any valid Rp shall be below the Max voltage in Table 4-36 Voltage on Sink CC pins (Multiple Source Current Advertisements) for vRa.

Table 4-27 provides the minimum impedance value to ground on CC for a device (Sink or Source) to be undetected by a Source. This shall apply for ports in the Disabled state or ErrorRecovery state. This shall also apply for Sources when unpowered (for example a power brick unplugged from AC mains).

Table 4-27 CC Termination Requirements for Disabled state, ErrorRecovery state, and Unpowered Source

	Minimum Impedance to GND	Notes
zOPEN	126 kΩ	zOPEN shall only be evaluated below vCC-Clamp.

Table 4-28 provides the impedance value for an SBU to appear open.

Table 4-28 SBU Termination Requirements

	Termination	Notes
zSBUTermination	≥ 950 kΩ	Functional equivalent to an open circuit

4.11.2 Timing Parameters

Table 4-29 provides the timing values that shall be met for delivering power over VBUS and VCONN.

Table 4-29 VBUS and VCONN Timing Parameters

	Minimum	Maximum	Description
tVBUSON	0 ms	275 ms	From entry to Attached.SRC until VBUS reaches the minimum vSafe5V threshold as measured at the source's receptacle.
tVBUSOFF	0 ms	650 ms	From the time the Sink is detached until the Source removes VBUS and reaches vSafe0V (See *USB PD*).
tVCONNON	Note 1	2 ms	From the time the Source supplied VBUS in the Attached.SRC state. Measured from vSafe5V to the minimum VCONN voltage (see Table 4-5)
tVCONNON-PA	0 ms	100 ms	From the time a Sink with accessory support enters the PoweredAccessory state until the Sink sources minimum VCONN voltage (see Table 4-5)
tVCONNOFF	0 ms	35 ms	From the time that a Sink is detached or as directed until the VCONN supply is disconnected.
tSinkAdj	tRpValueChange (Min)	60 ms	Response time for a Sink to adjust its current consumption to be in the specified range due to a change in USB Type-C Current advertisement

Note:

1. VCONN may be applied prior to the application of VBUS

Figure 4-46 illustrates the timing parameters associated with the DRP toggling process. The tDRP parameter represents the overall period for a single cycle during which the port is exposed as both a Source and a Sink. The portion of the period where the DRP is exposed as a Source is established by dcSRC.DRP and the maximum transition time between the exposed states is dictated by tDRPTransition.

Figure 4-46 DRP Timing

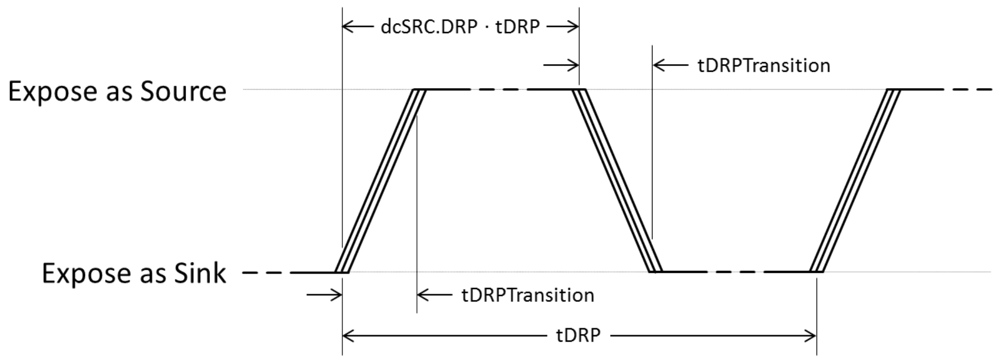


Table 4-30 provides the timing values that shall be met for DRPs. The clock used to control DRP swap should not be derived from a precision timing source such as a crystal, ceramic resonator, etc. to help minimize the probability of two DRP devices indefinitely failing to resolve into a Source-to-Sink relationship. Similarly, the percentage of time that a DRP spends advertising Source should not be derived from a precision timing source.

Table 4-30 DRP Timing Parameters

	Minimum	Maximum	Description
tDRP	50 ms	100 ms	The period a DRP shall complete a Source to Sink and back advertisement
dcSRC.DRP	30%	70%	The percent of time that a DRP shall advertise Source during tDRP
tDRPTransition	0 ms	1 ms	The time a DRP shall complete transitions between Source and Sink roles during role resolution
tDRPTry	75 ms	150 ms	Wait time associated with the Try.SRC state.
tDRPTryWait	400 ms	800 ms	Wait time associated with the Try.SNK state.
tTryTimeout	550 ms	1100 ms	Timeout for transition from Try.SRC to TryWait.SNK.
tVPDDetach	10 ms	20 ms	Time for a DRP to detect that the connected Charge-Through VCONN-Powered USB Device has been detached, after VBUS has been removed.

Table 4-31 provides the timing requirement for CC connection behaviors.

Table 4-31 CC Timing

	Minimum	Maximum	Description
tCCDebounce	100 ms	200 ms	Time a port shall wait before it can determine it is attached
tPDDebounce	10 ms	20 ms	Time a Sink port shall wait before it can determine it is detached due to the potential for *USB PD* signaling on CC as described in the state definitions.
tTryCCDebounce	10 ms	20 ms	Time a port shall wait before it can determine it is re-attached during the try-wait process.
tErrorRecovery	25 ms		Time a self-powered port shall remain in the ErrorRecovery state.
	240 ms		Time a source shall remain in the ErrorRecovery state if it was sourcing VCONN in the previous state.
tRpValueChange	10 ms	20 ms	Time a Sink port shall wait before it can determine there has been a change in Rp where CC is not BMC Idle or the port is unable to detect BMC Idle.
	0 ms	5 ms	Time a Sink port shall wait before it can determine that there has been a change in Rp when *USB PD* signaling can be detected by the port and CC line is BMC Idle.
tSRCDisconnect	0 ms	20 ms	Time a Source shall detect the SRC.Open state. The Source should detect the SRC.Open state as quickly as practical.
tNoToggleConnect	0 ms	5 ms	Time to detect connection when neither Port Partner is toggling.
tOnePortToggleConnect	0 ms	80 ms	Time to detect connection when one Port Partner is toggling (0ms … dcSRC.DRP max * tDRP max + 2 * tNoToggleConnect).
tTwoPortToggleConnect	0 ms	510 ms	Time to detect connection when both Port Partners are toggling (0ms … 5 * tDRP max + 2 * tNoToggleConnect).

	Minimum	Maximum	Description
tVPDCTDD	30 µs	5 ms	Time for a Charge-Through VCONN-Powered USB Device to detect that the Charge-Through source has disconnected from CC after VBUS has been removed, transition to CTUnattached.VPD, and re-apply its Rp termination advertising 3.0 A on the host port CC.
tVPDDisable	25 ms		Time for a Charge-Through VCONN-Powered USB Device shall remain in CTDisabled.VPD state.

4.11.3 Voltage Parameters

Table 4-32, Table 4-33 and Table 4-34 provide the CC voltage values that a Source shall use to detect what is attached based on the USB Type-C Current advertisement (Default USB, 1.5 A @ 5 V, or 3.0 A @ 5 V) that the Source is offering.

Table 4-32 CC Voltages on Source Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.15 V	0.20 V
Sink (vRd)	0.25 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 4-33 CC Voltages on Source Side – 1.5 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.35 V	0.40 V
Sink (vRd)	0.45 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 4-34 CC Voltages on Source Side – 3.0 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.75 V	0.80 V
Sink (vRd)	0.85 V	2.45 V	2.60 V
No connect (vOPEN)	2.75 V		

Table 4-35 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that does not support higher than default USB Type-C Current Source advertisements.

Table 4-35 Voltage on Sink CC Pins (Default USB Type-C Current only)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.18 V	

Table 4-36 provides the CC voltage values that shall be detected across a Sink's Rd for a Sink that implements detection of higher than default USB Type-C Current Source advertisements. This table includes consideration for the effect that the IR drop across the cable GND has on the voltage across the Sink's Rd.

Table 4-36 Voltage on Sink CC pins (Multiple Source Current Advertisements)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.04 V	
vRd-USB	0.25 V	0.61 V	0.66 V
vRd-1.5	0.70 V	1.16 V	1.23 V
vRd-3.0	1.31 V	2.04 V	

Table 4-37 provides the clamping voltage that any port (Source, Sink or DRP) may clamp its CC pin to protect from damage. The inclusion of clamping shall not impact the functionality when the CC pin is functioning as VCONN Source or Sink.

Table 4-37 CC Pin Clamping Voltage

	Minimum Voltage
vCC-Clamp	2.9 V

5 USB4 Discovery and Entry

USB4™ discovery and operational entry differs significantly from *USB 2.0* and *USB 3.2*. This chapter defines the process of discovering across a USB Type-C® connection that both port partners are *USB4*-capable (or not), having the DFP-side of the link make a decision regarding to enter *USB4* operation (or not), and how operational entry is accomplished.

5.1 Overview of the Discovery and Entry Process

The following provides an overview of the general process for discovery and entry into *USB4* operation.

1. USB Type-C CC Connection State Machines resolve Source/Sink and the initial data roles (DFP/UFP).
2. Initial VBUS and VCONN power is supplied.
3. *USB Power Delivery* protocol is used to establish a power contract between the port partners.
4. *USB PD* Discover Identity process is used by the DFP to identify port partner (SOP) capabilities.
5. *USB PD* Discover Identity process is used by the DFP to identify cable (SOP') capabilities.
6. If the cable and port partner both support USB4 operation, the DFP issues *USB PD* Enter_USB Messages to both the cable (if it is an active cable) and port partner to enter USB4 operation.
7. If both port partners are Dual-Role-Data (DRD) capable, either the DFP or UFP can optionally initiate a data-role swap in order to exchange host and device roles.

The first three steps above are the same as used for all USB connections for establishing port relationships and power between the port partners. Step 5 where the cable is queried for its capabilities may optionally occur during Step 3, this would most likely be done before if the Source needs to know if the cable supports supplying current beyond 3 A.

Depending on the resulting power source relationship after the first few steps, the use of *USB PD* DR_Swap may be necessary to establish the port partner that is closest to the host as the data role DFP. For example, a hub supplying power to a host and DR_Swap is used to correct the data roles between the hub and host.

After the port partner's capabilities are identified by the DFP, it may be appropriate based on what is discovered about the port partner to also query the port partner using the *USB PD* Alternate Mode SVID discovery process as an extension to Step 4. There are situations where a port partner supports Alternate Modes that may also be useable during *USB4* operation and this would be discovered during this additional query.

After the cable capabilities are identified by the DFP, it may be appropriate based on what is discovered about the cable to also query the cable using the *USB PD* Alternate Mode SVID discovery process as an extension to Step 5. There are situations where a cable that supports Thunderbolt™ 3 Alternate Mode may also be useable for *USB4* operation and this would be discovered during this additional query.

USB4 operation is entered using a *USB PD* USB Enter_USB Message. This message will be sent to both the cable (SOP' and also SOP" if present) and the port partner (SOP), each of which will respond with an Accept message to confirm and establish when the cable or port partner is functionally ready for *USB4* operation. If the cable to be used will be operating in

Thunderbolt 3 Alternate Mode, then the cable will be enabled using the *USB PD* Enter Mode Command instead of the *USB PD* USB Enter_USB Message (See Appendix F).

USB4 functionally enables an ability for connecting two host platforms and establishing a data channel between the hosts, this is dependent on at least one of these host platforms being capable of Dual-Role-Data operation so that a proper USB Type-C DFP-to-UFP data relationship can be established between them. In most cases, both host platforms will be DRD-capable and once USB4 operation is established, either of these host platforms can choose to initiate a change of its role in the DFP-to-UFP relationship. To accomplish this, the *USB PD* DR_Swap process is used during Step 7 listed above.

5.2 USB4 Functional Requirements

The following functional requirements are for *USB4* hosts and devices.

5.2.1 USB4 Host Functional Requirements

USB4 hosts shall meet the following functional requirements:

- *USB4* hosts with dual-role-data (DRD) support shall respond to *USB PD* Discover Identity command with both DFP and UFP VDOs.

5.2.2 USB4 Device Functional Requirements

USB4 devices shall meet the following functional requirements:

- *USB4* devices shall respond to *USB PD* Discover Identity command with UFP VDOs.
- *USB4* devices shall provide a USB interface exposing a *USB Billboard Device Class* when it cannot connect as a *USB4* device within tUSB4Timeout.
- If the *USB4* device additionally supports Alternate Modes, the device shall complete the *USB4* discovery and entry process (successful or not) before falling back to *USB 3.2* or *USB 2.0* and exposing an appropriate *USB Billboard Device Class*.

5.2.3 USB4 Alternate Mode Support

The *USB4* specification enables products to be designed to support Alternate Modes, specifically *DisplayPort™ Alt Mode* and *Thunderbolt 3 Alt Mode*. Unlike *USB 3.2* and *USB 2.0* hubs, this also includes supporting specific Alternate Modes on *USB4* hubs.

5.2.3.1 USB4 Alternate Mode Support on Hosts

For *USB4* hosts that implement DisplayPort Tunneling, *DP Alt Mode* with Multi-function support (DP_BR 1 channel signaling combined with USB 3.2 support) as defined by the *DisplayPort Alt Mode* specification shall be implemented on all of its USB Type-C DFPs.

The *USB4* host shall support the first connected DisplayPort display on any of its USB Type-C ports. Support for subsequently connected DisplayPort displays is optional.

USB4 hosts may optionally implement *TBT3* compatibility support as defined by the *USB4* specification on its USB Type-C DFPs.

5.2.3.2 USB4 Alternate Mode Support on Hubs and USB4-based Docks

USB4 hubs and *USB4*–based docks shall implement *DP Alt Mode* with Multi-function support (DP_BR 1 channel signaling combined with USB 3.2 support) as defined by the *DisplayPort Alt Mode* specification on all exposed USB Type-C DFPs.

USB4 hubs shall support the first connected DisplayPort display on any of its USB Type-C DFPs. Support for subsequently connected DisplayPort displays is optional.

USB4-based docks shall support the first connected display on any of its USB Type-C DFPs or non-USB display connectors (if present, collectively). Support for subsequently connected displays is optional.

USB4 hubs shall implement *TBT3* compatibility support as defined by the *USB4* specification on its USB Type-C DFPs. *USB4*–based docks shall implement *TBT3* compatibility support as defined by the *USB4* specification on its USB Type-C UFP and USB Type-C DFPs.

For *USB4* hubs, downstream-facing ports shall not implement Alternate Modes that do not have a USB-IF Standard ID (SID) or Accessory Modes.

5.3 USB4 Power Requirements

USB4 requires that the power connection between the port partners be established and maintained using *USB PD* prior to and through-out *USB4* operation. A *USB4* port, prior to entering *USB4* operation, shall operate as a *USB 3.2* port with regarding power (See Section 4.6). *USB4* does not use the USB device protocols defined in *USB 2.0* and *USB 3.2* for managing device power.

5.3.1 Source Power Requirements

For USB Type-C ports that support *USB4* data bus operation, the following requirements shall be met.

- *USB4* ports shall be minimally capable of supplying at least 7.5 W (i.e. 5 V @ 1.5 A) on VBUS to bus-powered *USB4* devices.
- The minimum capability for powering bus powered devices on data-capable ports shall be independently met on each USB Type-C port of a multi-port host or hub.

5.3.2 Sink Power Requirements

For *USB4* devices that rely on bus power to operate (independent of any charging needs), the following requirements shall be met.

- *USB4* devices shall draw only up to 250 mA on VBUS when the Source advertises Default USB power (see Section 4.11.1) prior to a *USB PD* power contract being made between the device and its port partner.
    - *USB4* devices may draw higher levels of power prior to a *USB PD* power contract being made if the Source advertises USB Type-C Current at either 1.5 A or 3.0 A.
- *USB4* devices shall be minimally capable of operating with a Source that only delivers up to 7.5 W (i.e. 5 V @ 1.5 A).
- *USB4* devices shall not enter into *USB4* data bus operation until after a *USB PD* power contract has been established, and while in *USB4* operation, the device shall adhere to *USB PD* power behavioral requirements at all times including appropriately responding to changes in Source capabilities.

In cases where the full functional capabilities or the highest performance of the *USB4* device requires more than the power being offered by the host, the device shall be minimally capable of providing the user with basic functionality as expected for the type and listed functions of the device. This allows for making available a higher level of operation or performance when a higher level of power is supplied, e.g. 15 W for full functionality versus 7.5 W for basic functionality. In this case, the device shall expose a Billboard that indicates functionality is limited by the available power.

5.3.3 Device Power Management Requirements

For *USB4*, device power management is enabled using a combination of *USB PD* capabilities that operate in conjunction with the *USB4* link states of the device's UFP connection.

The connection between the device's UFP and its DFP port partner can be put into a suspend state based on the value of the USB Suspend Supported Flag in the Source-Capabilities Message used in the *USB PD* explicit power contract.

When the USB Suspend Supported Flag is set by the Source, the Sink shall meet the Suspend power requirement when the *USB4* link is in the CLd state. Prior to the entry of the link into CLd state, it is expected that the host will have placed all of the device's functions into an appropriate suspend state.

Suspend power is defined based on the capabilities of the *USB4* device:

- *USB4* Device that is not capable of remote wake or has remote wake disabled: 25 mW
- *USB4* Device that supports remote wake and has remote wake enabled: 50 mW

If the Source clears the USB Suspend Supported Flag, the Sink shall follow Explicit Contract power requirements regardless of the *USB4* link state. For *USB4*, the use of *USB PD* zero negotiated current is not a valid Suspend entry method since it is not coordinated with the host operating system and the function device drivers.

5.4 USB4 Discovery and Entry Flow Requirements

This section provides the detailed requirements for *USB4* discovery and entry. Additional requirements related to *USB4* operation are in the *USB4 Specification*.

Prior to entering and during *USB4* operation, the functional requirements of Chapter 3.11.1 shall be met including all functional interface and configuration channel (CC) requirements.

5.4.1 USB Type-C Initial Connection

For a *USB4*-capable port, prior to initiating *USB4* cable and device discovery, a valid Source-to-Sink connection shall exist and the USB Type-C connection state machine of the port shall either be in the Attached.SRC or Attached.SNK state.

When two *USB4* dual-role-data (DRD) ports are connected together, e.g. two *USB4* hosts, USB Type-C connection process will establish the initial data roles between the port partners.

Once the initial data roles are established, the *USB4* DFP may immediately proceed to train the link for *USB 3.2*. If a UFP is *USB4* capable, it shall hold off exposing SuperSpeed USB terminations until the completion of the *USB4* discovery and entry process or tUSB4Timeout. Once the *USB4* discovery and entry process has completed, the UFP will enable SuperSpeed USB device terminations either via the *USB4* SuperSpeed USB tunnel or natively depending on whether the completed port connection is *USB4* or *USB 3.2*, respectively.

5.4.2 USB Power Delivery Contract

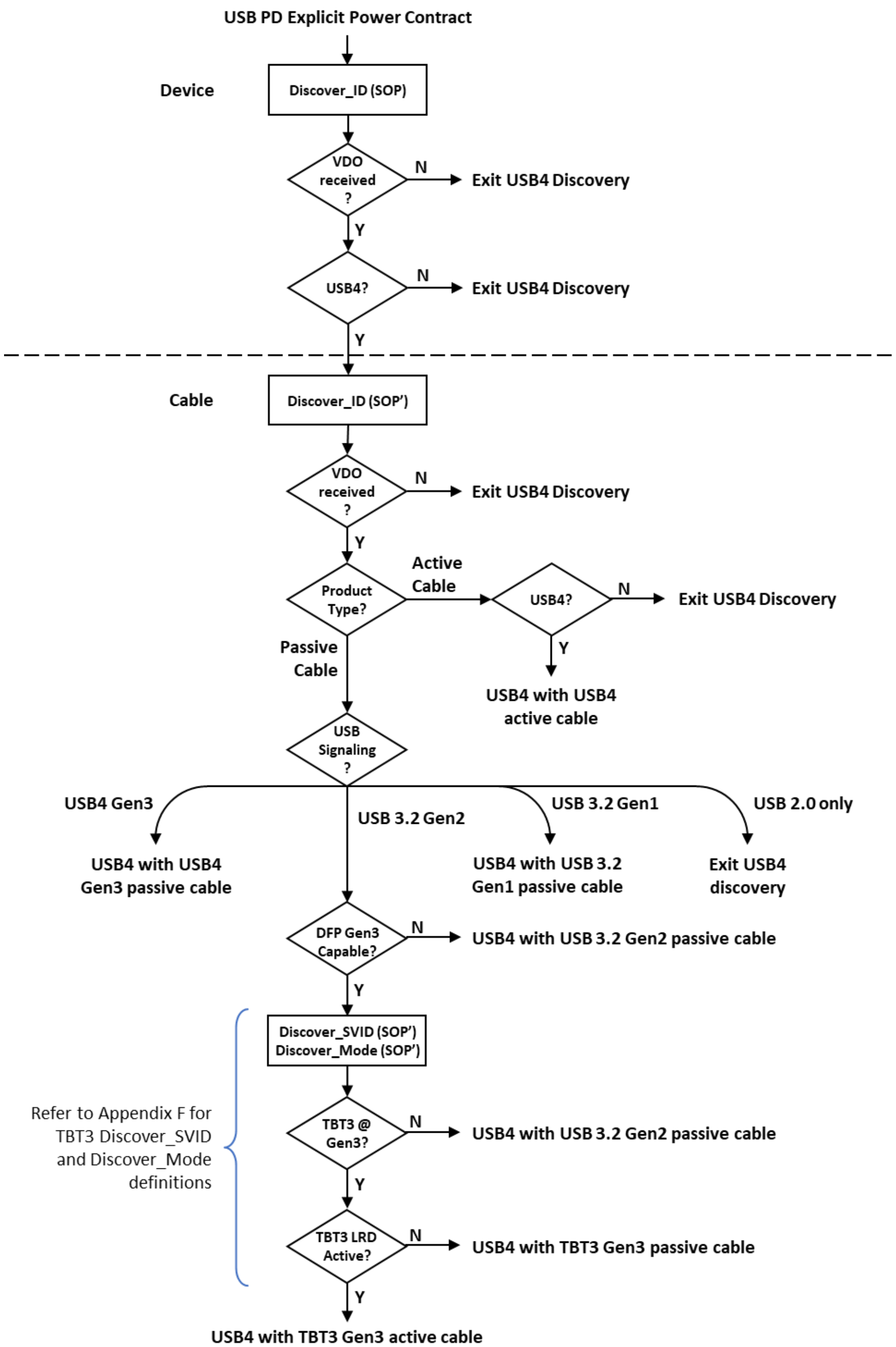
Prior to initiating *USB4* device discovery, the port partners shall negotiate a *USB PD* Explicit Contract.

During the process of establishing a stable *USB PD* Explicit Contract, the Source or Sink may have initiated power-role and VCONN swaps. Prior to moving on to USB4 discovery, the functional data role shall be properly established (e.g. a self-powered hub upstream facing port is a DRP and comes up as a Source where DR_Swap is then required to the correct data role to the hub) and the DFP shall be the source of VCONN.

5.4.3 USB4 Discovery and Entry Flow

Figure 5-1 illustrates the basic flow model for *USB4* discovery and entry.

Figure 5-1 USB4 Discovery and Entry Flow Model



5.4.3.1 USB4 Device Discovery (SOP)

USB4 device discovery shall occur only after having a negotiated *USB PD* Explicit Contract.

USB4 device discovery involves the use of the *USB PD* Discover ID process between the DFP and its port partner (SOP).

5.4.3.2 USB4 Cable Discovery (SOP')

The DFP shall determine that the attached cable is *USB4*-compatible prior to entering into *USB4* operation. In cases where the *USB4* device is directly connected or has a captive cable, the *USB4* device shall respond to *USB4* cable discovery on SOP' as a captive passive cable and indicating the appropriate USB Signaling support.

Table 5-1 summarizes the list of cables that are intended to support *USB4*-compatible operation. Regarding Active Cables, this list does not include Optically-Isolated Active Cables (OIACs) which are to be handled as a special case given that these cables do not support *USB 2.0* and power delivery over the cable (See Chapter 6).

Table 5-1 Certified Cables Where USB4-compatible Operation is Expected

	Cable Signaling	USB4 Operation	Notes
USB Type-C Full-Featured Cables (Passive)	USB 3.2 Gen1	20 Gbps	This cable will indicate support for USB 3.2 Gen1 (001b) in the USB Signaling field of its Passive Cable VDO response. Note: even though this cable isn't explicitly tested, certified or logo'ed for USB 3.2 Gen2 operation, USB4 Gen2 operation will generally work.
	USB 3.2 Gen2 (USB4 Gen2)	20 Gbps	This cable will indicate support for USB 3.2 Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	USB4 Gen3	40 Gbps	This cable will indicate support for USB4 Gen3 (011b) in the USB Signaling field of its Passive Cable VDO response.
Thunderbolt™ 3 Cables (Passive)	TBT3 Gen2	20 Gbps	This cable will indicate support for USB 3.2 Gen1 (001b) or USB 3.2 Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response.
	TBT3 Gen3	40 Gbps	In addition to indicating support for USB 3.2 Gen2 (010b) in the USB Signaling field of its Passive Cable VDO response, this cable will indicate that it supports TBT3 Gen3 in the Discover Mode VDO response.
USB Type-C Full-Featured Cables (Active)[1]	USB4 Gen2	20 Gbps	This cable will indicate support for USB4 Gen2 (010b) in the USB Signaling field of its Active Cable VDO response.
	USB4 Gen3	40 Gbps	This cable will indicate support for USB4 Gen3 (011b) in the USB Signaling field of its Active Cable VDO response.

Note:

1. SuperSpeed USB active cables do not support USB4–compatible operation.

Determining if the cable is USB4-compatible starts the use of the USB PD Discover ID process between the DFP and the attached cable (SOP'). If no response is received when the DFP issues a USB PD Discover ID command to the cable, then the USB4 discovery process shall be exited and the DFP shall proceed to establish a functional connection to its UFP port partner following traditional USB 2.0 process.

USB4-compatible support is generally determined based on the USB Signaling Support indicated in the cable VDO responses appropriate for the type of cable it is, passive or active, with compatible passive cables being those that indicate USB signaling support for Gen1 or higher and with compatible active cables being those that indicate USB signaling support for Gen2 or higher.

When a passive cable is identified as a USB 3.2 Gen2 cable and the DFP is Gen3 capable, the DFP needs to check further using USB PD Alternate Mode process to determine if the cable is a Thunderbolt 3 passive cable supporting Gen3.

Some existing Thunderbolt 3 active cables may not support *USB4* operation, discovery and use of this cable is optional. Please refer to Appendix F regarding how to discover and support these cables.

5.4.3.2.1 Discovering Passive Cables

The *USB PD* specification defines the Passive Cable VDO responses to the Discover Identity Command sent by the DFP to a *USB4*-compatible passive cable.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 011b (*USB4* Gen3), the *USB4* discovery process is complete and *USB4* operation up to as high as 40 Gbps is supported. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC4G3-3 and CC4G3-5 indicated in Table 3-1.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 000b (*USB 2.0* only), the *USB4* discovery process will be exited and the DFP shall proceed to establish a functional connection to its UFP port partner following traditional USB 2.0 process.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is either 010b (*USB 3.2* Gen2) or 001b (*USB 3.2* Gen1), the *USB4* discovery process is complete if the DFP is limited to *USB4* Gen2. In Chapter 3 of this specification, these cable assemblies are those with the following cable references: CC3G2-3, CC3G2-5, CC3G1-3, and CC3G1-3 indicated in Table 3-1. Note that *USB 3.2* Gen1 cables, while not tested and certified to be used for *USB 3.2* Gen2 operation, are expected to work for *USB4* Gen2 operation.

If the USB Signaling field [B2…0] in the Passive Cable VDO response is 010b (*USB 3.2* Gen2) but the DFP is capable of *USB4* Gen3 operation, then the DFP shall use the *USB PD* Alternate Mode process to determine if the cable also can be identified as a TBT3 Gen3 cable. Refer to Section 5.4.3.2.3 for TBT3 cable discovery process. If the Cable Speed field of the Discover Modes VDO response is set to 011b, then the *USB4* discovery process is complete and *USB4* operation up to as high as Gen3 is supported using the TBT3 passive cable (see Table F-11).

5.4.3.2.2 Discovering Active Cables

The *USB PD* specification defines the Active Cable VDO responses to the Discover Identity Command sent by the DFP to a *USB4*-compatible active cable.

If the USB Signaling Support field [B2…0] in the Active Cable VDO 1 response is 011b (USB4 Gen3), the *USB4* discovery process is complete and *USB4* operation up to as high as Gen3 is supported.

Optionally, discovery and use of existing TBT3 active cables that indicate support for rounded data rate operation is allowed if the active cable isn't explicitly identified as *USB4*-compatible.

Failure to identify that the attached active cable is *USB4*-compatible will result in exiting the *USB4* discovery process and reverting to following traditional *USB 3.2* and *USB 2.0* process.

5.4.3.2.3 Process for Discovering Thunderbolt 3 Cables

The *USB PD* specification defines the process for discovering Alternate Mode-enabled cables. The following summarizes this process specific to discovering Thunderbolt 3 cables for purposes of determining *USB4*-compatibility. Prior to performing these steps, the *USB PD* Discover Identity process will have already been used to establish if the cable is passive or active.

The following steps are used for discovering Thunderbolt 3 cables and the cable's capabilities using the *USB PD* Alternate Mode process.

1. DFP issues the Discover SVIDs command to the cable SOP'.
2. If the cable's Discover SVID response indicates 0x8087 (Intel/TBT3) as one of its SVIDs, then proceed to next step, otherwise the cable is not a Thunderbolt 3 cable (see Section F.2.4).
3. DFP issues the Discover Modes command with its SVID set to 0x8087 to the cable's SOP'.
4. If this discovery is part of the *USB4*-compatible passive cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the Cable Speed field to complete the process.
5. If this discovery is part of the *USB4*-compatible active cable discovery process, from the cable's Discover Modes VDO responses (see Section F.2.6), extract the value in the TBT_Rounded_Support field to complete the process. [Note: discovery and use of *USB4*-compatible TBT3 active cables is an optional feature that also would require use of *USB PD* Enter Mode command to enable the cable for *USB4* operation.]

5.4.3.3 USB4 Operational Entry

USB4 operational entry shall occur only after having established that the attached cable, if present, and the port partner are *USB4*-capable.

USB4 operational entry involves the use of the *USB PD* Enter_USB Message process between the DFP and both the attached *USB4*-compatible cable and the *USB4*-capable port partner – sending this message is order specific: SOP' first, SOP" second if present, and SOP third. Sending the *USB PD* Enter_USB Message to SOP' and SOP" is not needed for passive cables.

When using the *USB PD* Enter_USB Message for enabling *USB4* operation, the DFP shall indicate 010b (*USB4*) in the USB Mode field of the Enter_USB Data Object. The remaining fields shall be set appropriately by the DFP based on the capabilities of the DFP and attached cable.

5.4.4 USB4 Post-Entry Operation

5.4.4.1 During USB4 Operation

While in *USB4* operation, the following are allowed:

- The *USB PD* explicit power contract may be re-negotiated.
- Issue an *USB PD* Data_Reset command to change the mode of operation, e.g. from *USB4* to *USB 3.2* or an Alternate Mode.
- Enable Alternate Modes that do not reconfigure the port interface and operate in parallel with *USB4*.

5.4.4.2 Exiting USB4 Operation

The *USB PD* Data_Reset process causes USB data connections to be reset and Alternate Modes to be exited. This process does not change the existing power contract and data roles between the port partners. The Data_Reset process shall include the following steps:

- Issue a *USB PD* Data_Reset command to the SOP port partner to reset the data bus, reset the cable, and exit any Alternate Modes while preserving the power on VBUS.
- The tUSB4Timeout and tAMETimeout timers within the UFP shall be reset upon sending or receiving a *USB PD* Data_Reset command.
- Re-enter the *USB4* Discovery and Entry process (Section 5.4.3).

5.5 USB4 Hub Connection Requirements

USB4 hub behavior with regard to managing its DFP connections has *USB4*-specific dependencies on the connection status and capabilities of its single UFP. Additionally, hubs have *USB4*-specific responsibilities for communicating the capabilities of the *USB4* host to downstream-connected *USB4* hubs. This section provides both requirements and guidance for *USB4* hub port connection behavior.

5.5.1 USB4 Hub Port Initial Connection Requirements

The following requirements apply to all hub ports.

1. Run the USB Type-C Connection process,
2. Establish an initial *USB PD* explicit contract,
3. If desired, use PR_Swap to establish the preferred power role, and
4. Use DR_Swap to establish data role to be consistent with the port's position in the USB tree if needed.

5.5.2 USB4 Hub UFP and Host Capabilities Discovery

The *USB4* hub DFPs capabilities are ultimately based on the capabilities seen at its UFP (once it has established a connection to the host). If the *USB4* hub's UFP is connected to an upstream *USB4* hub, then the capabilities over the connection between the two hubs may not initially represent the capabilities all the way back to the host.

The following summarizes the general principles regarding how UFP and host capabilities impact DFP connections.

- The downstream connection to a device or hub that is attached to the *USB4* hub's DFP is based on the capabilities of the hub.
- Once the *USB4* hub's UFP has established a connection, the hub's capabilities are limited to the capabilities of that UFP connection.
- When the *USB4* hub's UFP connection indicates that a host is not present, once the hub is notified that a host becomes present, the hub will limit its capabilities as needed to match those of the host.
    - Any connections on the *USB4* hub's DFPs that existed prior to the host being present are adjusted to align with changes in capabilities if needed.
- Once a host becomes present in a *USB4* tree, all intermediary hubs will update their connections to align with the host capabilities as the host present status is propagated to the downstream connected *USB4* hubs.

The capabilities seen by the hub's UFP are based on one of the following:

- An *USB PD* Enter_USB message is received which indicates the USB operation (*USB4*, *USB 3.2* or *USB 2.0*) and associated characteristics supported (*USB4* PCIe-supported, *USB4* DP supported, etc.) by the upstream port partner.
- An *USB PD* Enter Mode command is received to start a supported Alternate Mode (Thunderbolt 3, DisplayPort).
- No *USB PD* Enter_USB message is received within the tUSB4Timeout or *USB PD* Enter Mode message is received within the tAMETimeout indicating only *USB 3.2* and *USB 2.0* are available.

If the *USB4* hub's UFP is connected to an upstream *USB4* hub, then the capabilities reported in the received *USB PD* Enter_USB message shall only be considered the host's capabilities if the Host Present bit is set. If the Host Present bit is reset, then the hub shall wait for a subsequent USB PD Enter_USB message to be received with the Host Present bit set. Once the Host Present bit is set, the capabilities as represented in the USB PD Enter_USB message can be used as the host's capabilities for the purpose of establishing final DFP connections.

If the USB4 hub's UFP receives an USB PD Enter_USB message which indicates the USB operation as either USB 3.2 or USB 2.0, the USB4 hub shall not wait for the completion of the tUSB4Timeout before proceeding to establish its UFP and DFP connections following USB 3.2 or USB 2.0 hub requirements, respectively.

5.5.3 Hub DFP Connection Requirements

5.5.3.1 Speculative Connections

When a device is attached to the DFP of a USB4 hub prior to the hub's UFP being connected and the host capabilities are known, the hub will speculatively connect to the attached device based on the following requirements.

- Use USB PD Discover ID and the USB PD Alternate Mode process to determine the full capabilities of the attached cable and device.
- Based on the discovered capabilities, establish the most capable connection based on the capabilities of the USB4 hub's DFP in the following priority order:
    1. USB4
    2. Thunderbolt 3 Alt Mode
    3. DP Alt Mode
    4. USB 3.2
    5. USB 2.0
- Inhibit port status notifications and data paths upstream from the USB4 hub's DFPs while waiting for the USB4 hub's UFP connection to be established.

5.5.3.2 Operational Connections

Once the USB4 hub's UFP connection is established and the host capabilities are determined (see Section 5.5.2), the hub shall evaluate each existing DFP connection based on the capabilities associated with the hub's UFP connection and perform one of the following actions.

- If the DFP connection properly aligns with the capabilities of the UFP connection, enable the status notifications and data path for that port.
- If the DFP connection does not properly align with the capabilities of the UFP connection, the DFP connection shall do one of the following:
    - If the UFP remains in USB4 and the DFP connection is with a downstream USB4 hub, send a revised USB PD Enter_USB message with the Host Present bit set.
    - If the UFP changed to USB 3.2 or USB 2.0 and the DFP connection is with a downstream USB4 hub, the DFP shall be reset the connection using USB PD Data_Reset followed by sending a revised USB PD Enter_USB message indicating USB 3.2 or USB 2.0 and the Host Present bit set.
    - Otherwise, the DFP shall enter the ErrorRecovery state to reset the connection and establish a new connection that aligns with the hub's UFP capabilities.

5.5.4 Hub Ports Connection Behavior Flow Examples

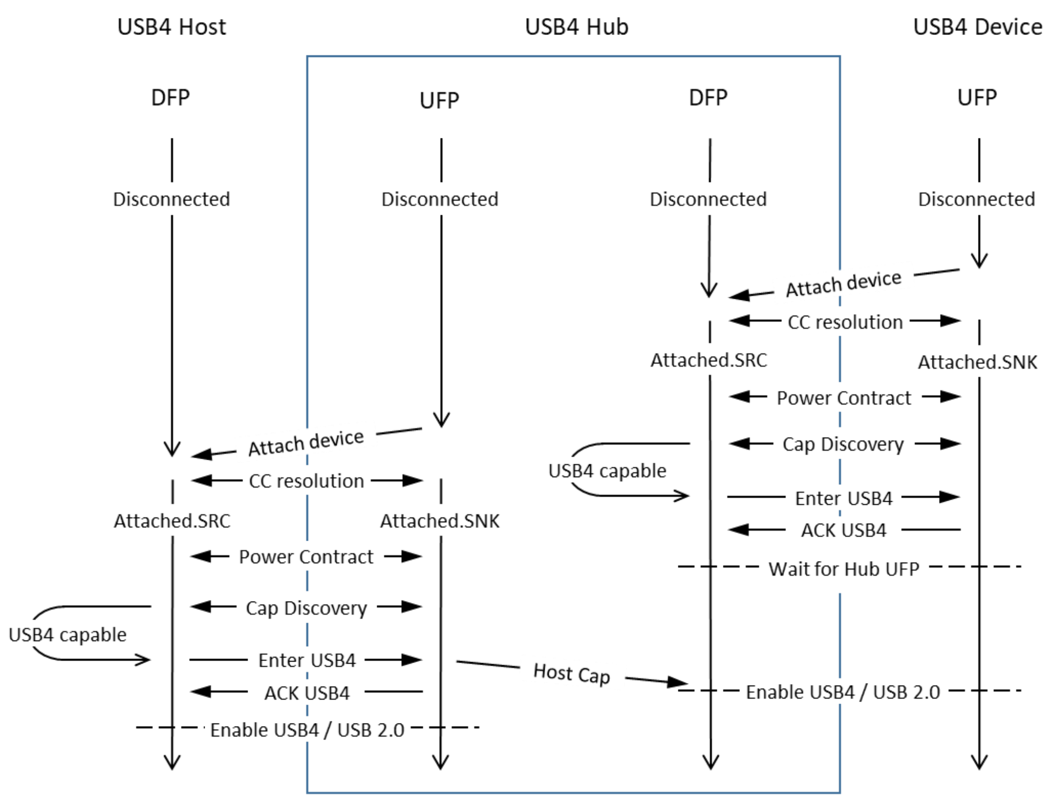
This section illustrates several example connection flows that assume that the hub's DFP connection is established prior to the hub's UFP connection. In these cases, the host capabilities are unknown at the time that the hub's DFP is connecting with the attached device. Given this, the initial connection established by the hub's DFP is speculatively based only on the hub and device's capabilities and may have to be revised once the host capabilities are known if there is a functional mismatch. When the hub's UFP connection is fully established prior to devices appearing on the hub's DFP, the connection can be established with full knowledge of the host's capabilities – flows associated with this relationship are not illustrated.

For the example flows in this section, the Source/Sink power roles remain as initially resolved by the CC connection state machine with no PR_Swap or DR_Swap activity.

All these example flows intend to minimize the total connection time for enabling the functionality of the device connected to the hub's DFP. This is accomplished by establishing the highest functional connection based on mutual capabilities between the hub and the device even as the hub's UFP capabilities are unknown or not ready for operation. If the speculatively established connection turns out to be valid once the hub's UFP capabilities are established, then the DFP's connection will be enabled as is. If the speculatively established connection turns out to be invalid, the DFP connection will be reset and a connection that aligns with the hub's UFP capabilities shall be established.

Figure 5-2 Illustrates a connection flow aligned across the combination of a *USB4* host, hub and device. The expected result is the successful enabling of end-to-end *USB4* operation.

Figure 5-2 USB4 Hub with USB4 Host and Device Connection Flow Alignment



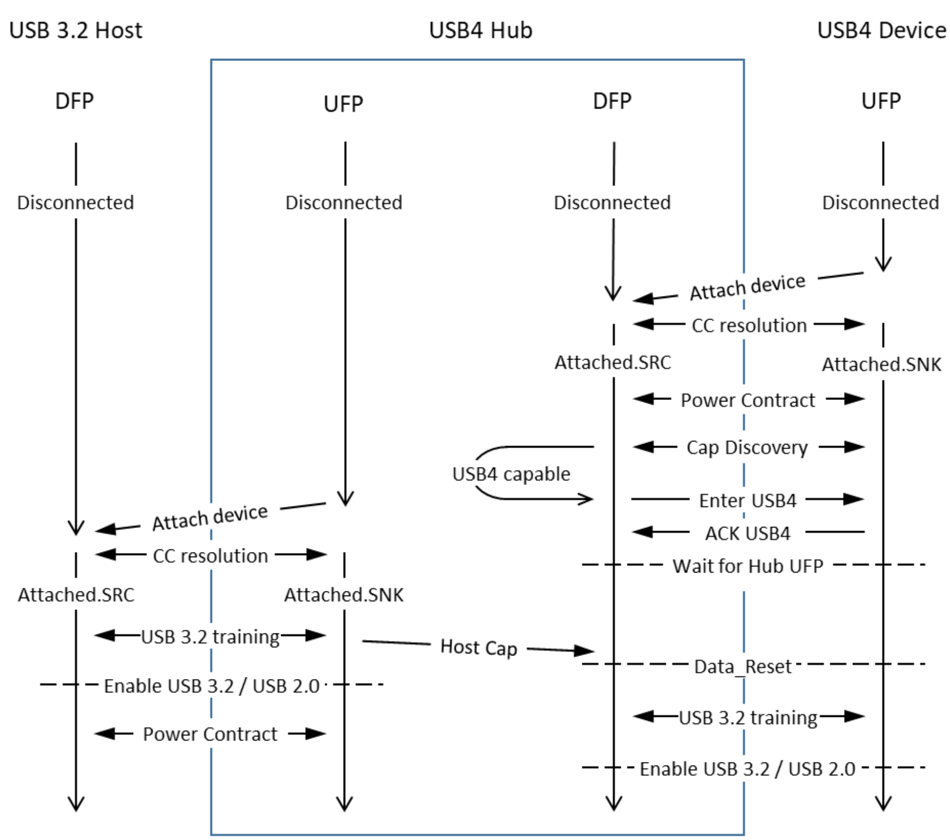
In the illustrated flow, Cap Discovery includes all USB PD message exchanges needed between the DFP and its UFP port partner to discover the UFP's USB capabilities along with TBT3-compatibility and DP Alt Mode capabilities. For the USB4 hub's DFP, Cap Discovery is done on a speculative basis whenever it does not already know of the capabilities of the host that will eventually be connected via the hub's UFP.

Upon completion of Cap Discovery between the hub's DFP and its UFP port partner, the hub DFP will establish the highest functional connection and then wait for the hub UFP to complete its connection. Once the hub's UFP connection is established, the host capabilities available is used to determine what should be done to complete the hub DFP connection to the UFP port partner.

Host Cap is based on the resulting configuration (e.g. data bus protocol and speed) of the USB4 Hub's UFP and the Host capabilities information received in the USB PD Enter_USB Message from its DFP port partner (see Section 5.5.2). The USB4 hub uses Host Cap to set the available capabilities of the hub's DFPs.

Figure 5-3 illustrates a connection flow aligned across the combination of a USB 3.2 host, a USB4 hub and a USB4 device.

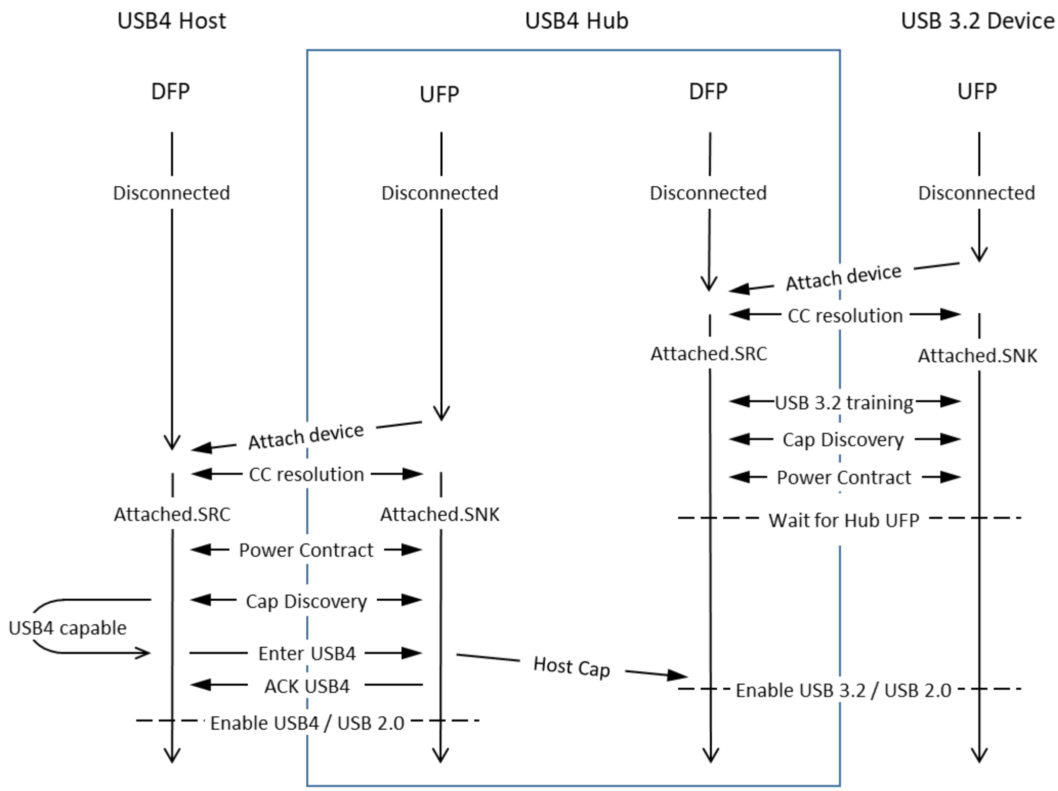
Figure 5-3 USB4 Hub with USB 3.2 Host and USB4 Device Host Connection Flow



In the flow above, once connected to a USB 3.2 host, the Host Cap reflects that the hub can only support USB 3.2 on its DFPs and the speculatively established USB4 connection on the DFP is exited with the USB4 hub now operating as a traditional USB 3.2 hub.

Figure 5-4 illustrates a connection flow aligned across the combination of a *USB4* hub with a *USB4* host and *USB 3.2* device.

Figure 5-4 USB4 Hub with USB4 Host and USB 3.2 Device Connection Flow

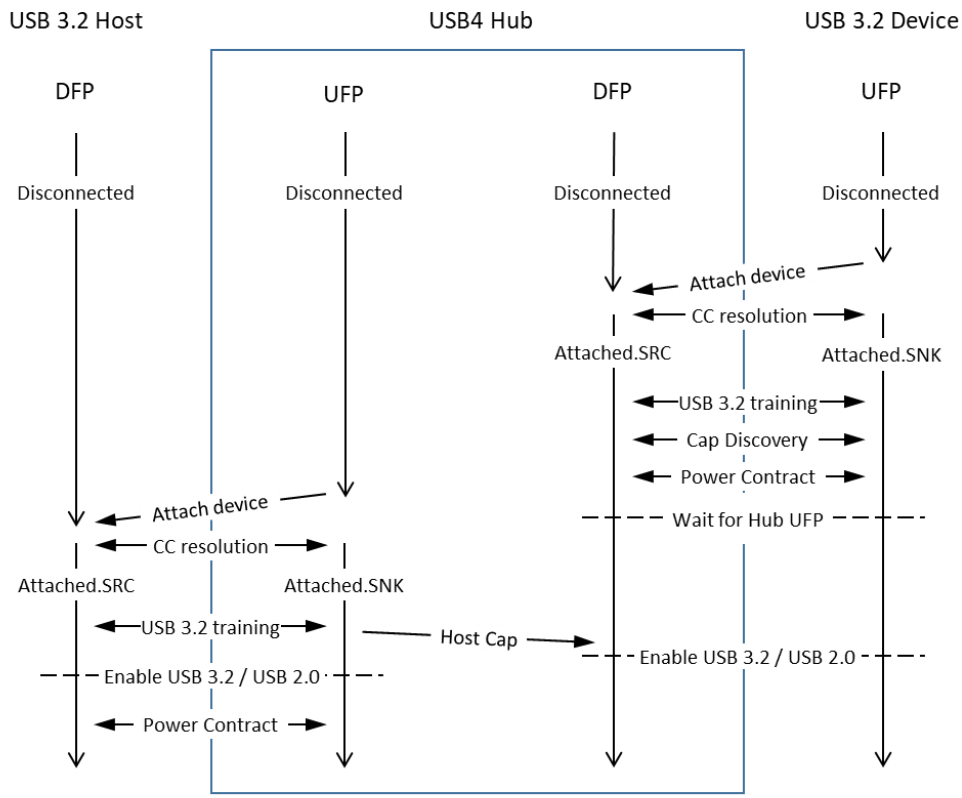


While *USB 3.2* devices won't necessarily respond to the Discover ID (SOP), the *USB4* hub's DFP will attempt to discover the capabilities of the attached device.

In the flow above, after the *USB4* connection of the hub's UFP is established, the DFP connection remains valid with the *USB 3.2* data path of the DFP being serviced by the *USB4* Enhanced SuperSpeed tunnel.

Figure 5-5 illustrates a connection flow aligned across the combination of a USB4 hub with a USB 3.2 host and device.

Figure 5-5 USB4 Hub with USB 3.2 Host and Device Connection Flow

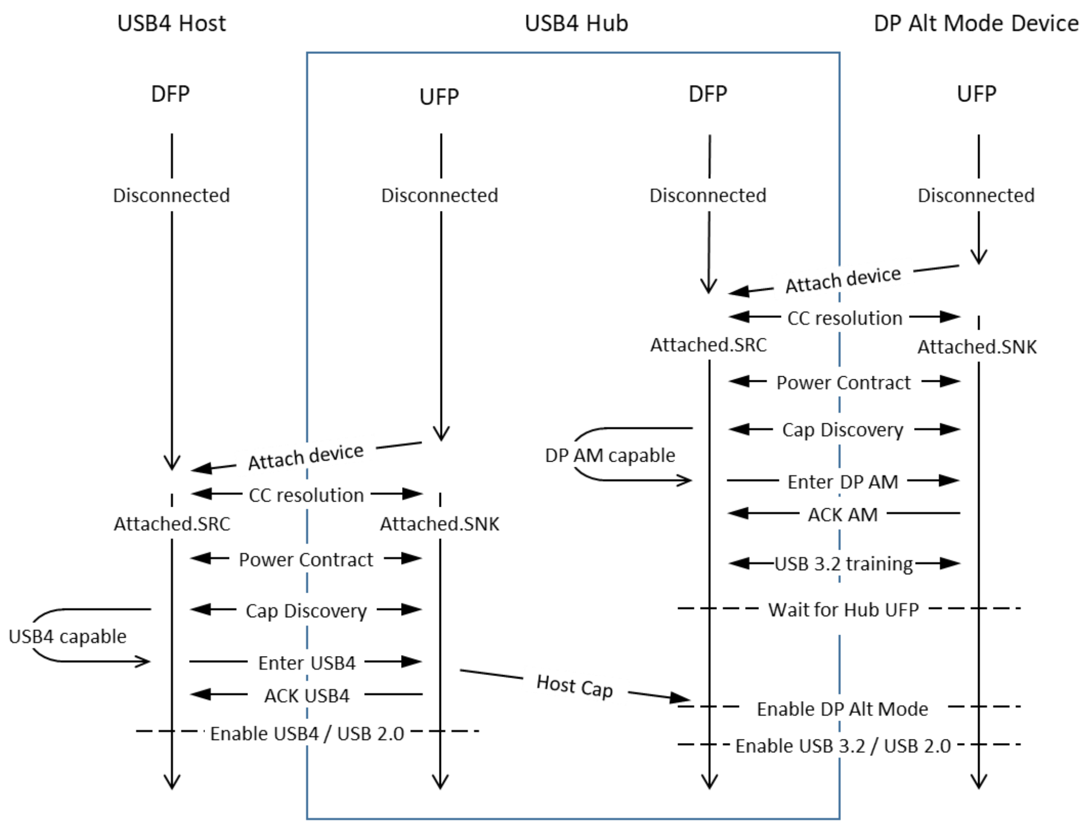


While USB 3.2 devices won't necessarily respond to the Discover ID (SOP), the USB4 hub's DFP will attempt to discover the capabilities of the attached device.

In the flow above, after the USB 3.2 connection of the hub's UFP is established, the DFP connection remains valid with the USB4 hub now operating as a traditional USB 3.2 hub.

Figure 5-6 illustrates a connection flow aligned across the combination of a USB4 host, USB4 hub and a DP Alt Mode device (operating in Multi-function mode). In this case, the expected result is the enabling of the DP Alt Mode as bridged from USB4 DisplayPort tunneling.

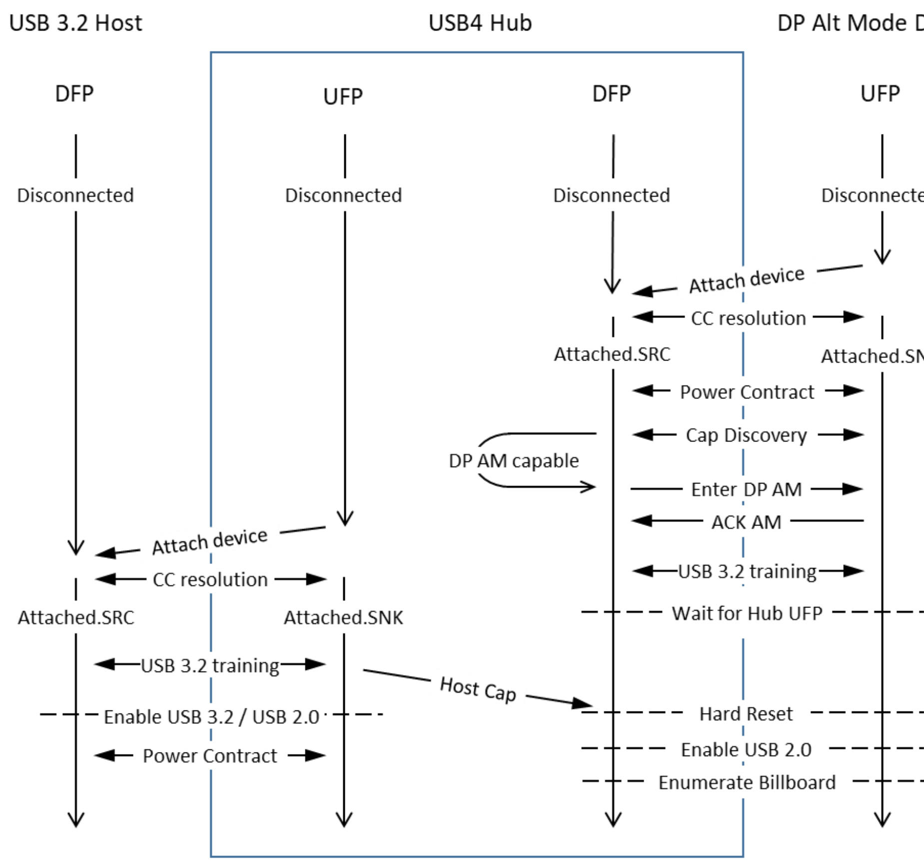
Figure 5-6 USB4 Hub with USB4 Host and DP Alt Mode Device Connection Flow



In the flow above, after the USB4 connection of the hub's UFP is established, the DFP connection remains valid with the DisplayPort and USB 3.2 data paths of the DFP being serviced by the USB4 DisplayPort and Enhanced SuperSpeed tunnels.

Figure 5-7 illustrates a connection flow aligned across the combination of a USB 3.2 host, a USB4 hub and a DP Alt Mode device (operating in Multi-function mode). The expected result in this case is that the DP Alt Mode will not be enabled and a Billboard exposed by the device since the host doesn't support USB4.

Figure 5-7 USB4 Hub with USB 3.2 Host and DP Alt Mode Device Connection Flow



In the flow above, after the USB 3.2 connection of the hub's UFP is established, the DFP connection is no longer valid with the USB4 hub now operating as a traditional USB 3.2 hub. The hub's DFP would then reset the port which will lead to a USB 2.0 connection and the exposure of the Billboard device.

5.5.5 Connecting to Downstream USB4 Hubs

When a USB4 hub is attached on its DFP to the UFP of another USB4 hub, the USB4 hub shall use the Host Present bit of the USB PD Enter_USB message to inform the downstream hub if the USB4 capabilities listed in the message reflects the host's capabilities or not. If an initial connection is made with the downstream hub with the Host Present bit reset in the USB PD Enter_USB message, the USB4 hub shall subsequently send a revised USB PD Enter_USB message with the Host Present bit set after its UFP has been fully established (see Section 5.5.2).

5.5.6 Fallback Functional Requirements for USB4 Hubs

When a USB4 hub is attached on its UFP to a non-USB4 DFP, the USB4 hub shall seamlessly fall back to functioning as and meeting the requirements for a USB 3.2 hub.

5.6 USB4 Device Connection Requirements

5.6.1 Fallback Mapping of USB4 Peripheral Functions to USB Device Class Types

USB4 peripheral devices provide functions based on data transferred over one or more of the protocol tunnels of *USB4*: Enhanced SuperSpeed USB, DisplayPort and PCI Express. For all peripheral functions that use the Enhanced SuperSpeed USB protocol tunnel, the mapping of those functions to USB device class specifications is clear but for those based on the other tunneled protocols, this mapping doesn't apply since those functions don't rely on USB device class drivers to operate.

Each function of a *USB4* device shall be mapped to an equivalent USB device class when possible. *USB4* devices that contain mapped USB device class functions shall support operation at *USB 3.2* or *USB 2.0* when connected to non-*USB4* hosts. This requirement is exempted for those functions that rely on DisplayPort or PCIe tunnels for *USB4* data transfer that don't reasonably map to an existing USB device class, e.g. a PCIe graphics adapter.

The performance of the function when mapped to a lower speed connection is expected to scale appropriately while still providing the functional equivalent of the primary capabilities of the peripheral function.

Table 5-2 lists USB Device Class types and the mapping requirements for *USB4* device peripheral functions as it relates to fallback when operating over *USB 3.2* or *USB 2.0*.

Table 5-2 Fallback Mapping USB4 Peripheral Functions to USB Device Class Types

Device Class Category	USB4 Peripheral Function Mapping	Comments
Audio	Required	
Video	Required	
Mass Storage	Required	
Comms/Networking	Required	
Printer	Required	
HID	Required	Only required when an equivalent HID subclass or report usage is defined.
Media Transfer Protocol	Required	
Smart Card	Required	
Still Image Capture	Required	
Monitor Device	Required	Only required in conjunction with providing associated display applications.

For all *USB4* peripheral functions based on DisplayPort and PCIe protocol tunneling that do not map to USB device class equivalents when operating over *USB 3.2* or *USB 2.0*, an appropriate USB Billboard Device Class shall be exposed to enable user notifications by the operating system of the host platform.

5.7 Parameter Values

5.7.1 Timing Parameters

Table 5-3 provides the timeout requirement for a device that supports *USB4* to enable a *USB Billboard Device Class* interface when the device cannot connect as a *USB4* device during the discovery and entry process (Section 5.4).

Table 5-3 USB Billboard Device Class Availability Following USB4 Device Entry Failure

	Maximum	Description
tUSB4Timeout	1000 ms	The time between (1) a Sink attach or (2) the data connection is reestablished in the *USB PD* Data Reset process until the *USB Billboard Device Class* interface is exposed when *USB4* device entry is not successful.

6 Active Cables

Active cables shall minimally support *USB 3.2* Gen 2x2. *USB4* active cables shall support all *USB 3.2* rates and *USB4*. Active cables shall support *USB PD* eMarkers and may support Alternate Modes and advertise them as defined in Section 6.6.5.

All *USB4™* active cables shall be interoperable with Thunderbolt™ 3 as defined in the *USB4* Specification (Chapter 13) and this specification (Section 6.7 and Appendices E and F).

Short active cables supporting lengths up to 5 meters shall work in both directions and orientations and should function like passive cables from the user's perspective.

Optically Isolated Active Cables (OIACs) support longer lengths up to 50 meters and provide electrical isolation between the two ends of the cable. OIACs are targeted for Industrial, Machine Vision, Remote Sensor, Pro Video, and Medical applications. OIACs do not 'just work' unlike short active cables. Long OIACs may not function correctly with Hosts, Devices, and Hubs that are not compliant to the *USB 3.2* Specification. Table 6-1 shows the limitations of OIACs with short active cables. Legacy USB3 devices may require using an adapter between the device and the OIAC. This adapter is defined in Section 6.6.4.3.1.

Since no power runs through an OIAC, they can only be used to connect a Source DRD to a Source DRD or a Source DRD to a DFP. *USB PD* Revision 3 must be supported on both port partners for an OIAC to function. Each cable plug of an OIAC is locally powered from VCONN and/or optionally from VBUS. OIACs shall function for *USB 3.2* when VCONN only is provided and may optionally use VBUS if provided. OIACs may require VBUS for Alternate Mode support. OIACs have no functionality when either cable plug is connected to a Sink/UFP only device (Sink/UFP devices are unable to provide power to the cable plug). OIACs require at least one end of the cable plug to be connected to a DRD (DRP and capable of accepting a DR_Swap to USB Device Role).

If a connection to a *USB 2.0* Device is required at the end of an OIAC, an adapter with a *USB 3.2* to *USB 2.0* transaction translator and VBUS/VCONN Source may be connected at the Device side of the cable to convert the *USB 3.2* signals to *USB 2.0* and provide power to the *USB 2.0* Device and the OIAC.

If an OIAC supports Alternate Modes that require the use of SBUs, the SBUs shall be optically isolated.

Table 6-1 Comparison of Active Cables

	USB 3.2 Short Active Cable	USB4 Short Active Cable	USB 3.2 Optically Isolated Active Cable
USB4 Support	N/A	USB4 Repeater	
USB 3.2 Support	USB 3.2 Repeater	USB 3.2 Repeater	USB 3.2 Repeater
USB 2.0 Support	Passive Connection	Passive Connection	No end-to-end electrical connection. An OIAC Legacy Adapter (Section 6.6.4.3.1) required for USB 2.0 support.
TBT3 Alt Mode Support	Optional	Required	Optional
SBU Support[1]	Passive Connection	Passive Connection	Optional normative support in Alternate Modes only
USB PD Communication	All messages supported	All messages supported	Only a subset of messages is supported.
Bus Powered Devices	Supported	Supported	Not supported unless a VBUS/VCONN Source is connected between OIAC and Bus Powered Device. An OIAC Legacy Adapter (Section 6.6.4.3.1) is an example of a VBUS/VCONN Source.
End-to-End Electrical Connection	Yes	Yes	No
End-to-End Ground and VBUS Connections	Yes	Yes	No

Note 1: SBU support for Active Cables can be either passive or active in the case of a linear re-driver-based active cable or active in the case of a re-timer-based active cable.

Table 6-2 Summary of Active Cable Features

Cable Type	Length	USB PD	VBUS	VCONN Wiring	CC	USB 2.0	USB 3.2 (All required)	USB4	Alternate Modes	SBU
USB 3.2 Short	< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	N/A	Optional	Note 3 Note 4
USB4 Short	< 5 m	SOP' Required (SOP" Optional)	3 A or 5 A	Same as passive cable	Same as passive cable	Same as passive cable	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2	Gen2 Gen3	TBT3 Note 2	Note 3 Note 5
USB 3.2 Optically Isolated	USB 3.2 Latency[1]	SOP' and SOP" Required	0 A	Local cable plug only	Optical	Not Allowed	Gen 1x1 Gen 2x1 Gen 1x2 Gen 2x2		Optional	Note 6

Note 1: Length is set by the latency requirement in USB 3.2.

Note 2: Thunderbolt™ 3 Alternate Mode support required as defined in Appendix F.

Note 3: A passive connection in USB 3.2 mode is required.

Note 4: Support for SBU is optional normative in Alternate Modes.

Note 5: SBU support for USB4 can be either passive or active in the case of a linear re-driver-based active cable or active in the case of a re-timer-based active cable.

Note 6: SBU support for USB 3.2 OIAC is optional normative in Alternate Modes only.

All active cables, regardless of length, shall be compliant with this specification, the USB 3.2 including Appendix E, and the USB 3.2 Active Cable CTS.

6.1 USB Type-C State Machine

OIAC cable plugs behave as Sinks on an initial cable connection. OIACs use USB PD Revision 3 to configure one plug as the DFP and one as the UFP as described in Section 6.2.1.

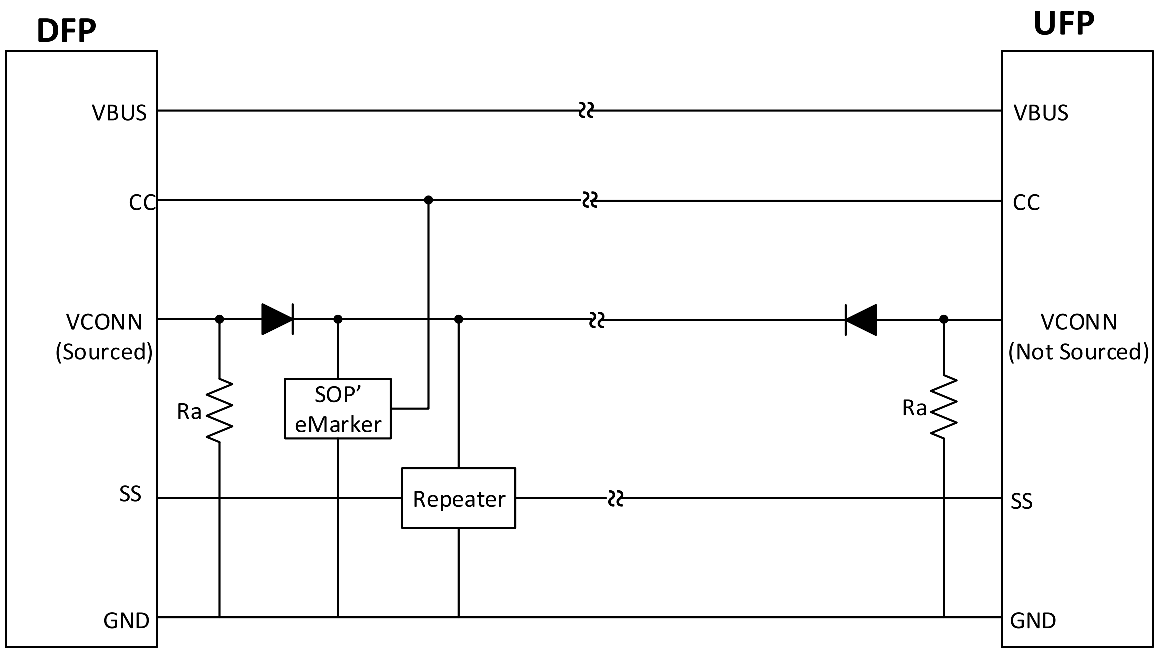
6.2 USB PD Requirements

This specification uses the USB Type-C® terminology for connection states and not the USB PD specification terminology.

Active cables shall be electronically marked and wired per Figure 6-1, Figure 6-2, or Figure 6-3.

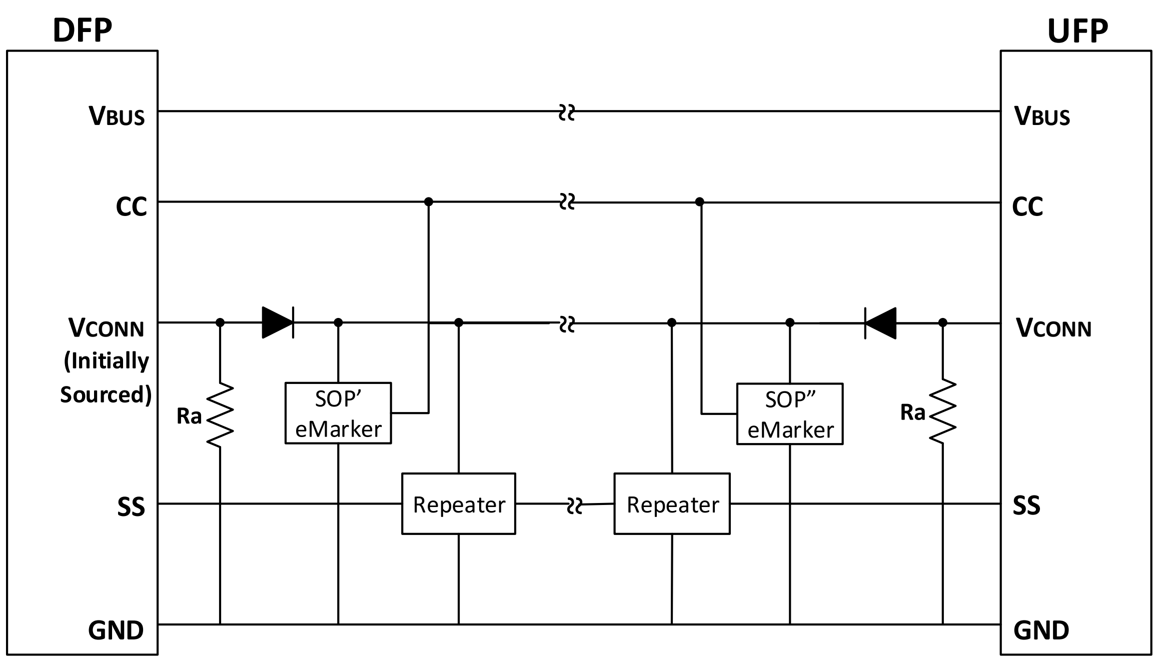
- The temperature sensor shall be co-located with the repeater for accurate thermal reporting.
- An active cable that contains two repeaters shall support both SOP' and SOP".
- An active cable that only contains one repeater internal to the active able (not in the cable plugs) shall implement SOP' and is not required to implement SOP".

Figure 6-1 Electronically Marked Short Active Cable with SOP' Only



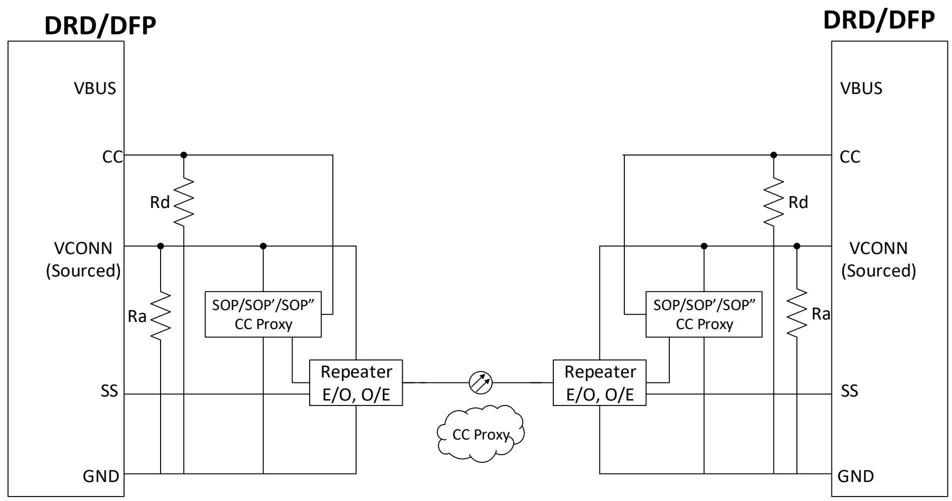
Short active cables may optionally be electronically marked on both ends of the cable as illustrated in Figure 6-2.

Figure 6-2 Electronically Marked Short Active Cable with SOP' and SOP"



Optically isolated active cables shall be electronically marked on both ends of the cable as illustrated in Figure 6-3

Figure 6-3 Electronically Marked Optically Isolated Active Cable



6.2.1 Active Cable USB PD Requirements

Active cables shall support *USB PD* Revision 3, Version 1.2 or later. Active cables shall support *USB PD* Structured VDMs.

6.2.1.1 SOP' and SOP" Requirements

Active cables shall respond to ***Discover_Identity*** and ***Get_Status*** on SOP'. When the SOP'' Controller Present bit is set in the Active Cable VDO, they shall respond ***Get_Status*** on SOP'' as well.

OIACs have a different definition for SOP". SOP" is always the far-end cable plug relative to the message initiator.

6.2.1.2 Discovering Cable Characteristics

The *USB PD* ***Discover_Identity*** Command is used to discover the characteristics of the active cable. This command shall only be sent to SOP'. All active cables shall respond to the ***Discover_Identity*** Command with Active Cable VDOs that returns information about the cable. Note the active cable shall respond using either *USB PD* Revision 2 or *USB PD* Revision 3 following the *USB PD* Interoperability rules.

Table 6-3 summarizes the *USB4* cables regarding key identity values that will be returned to *USB PD* Revision 3 ***Discover_Identity*** commands.

Table 6-3 USB4 Cable Identity Summary

USB4™ Cable	Function				SOP' Configuration (USB PD Revision 3)					
					ID Header VDO	Passive Cable VDO	Active Cable VDO 1	Active Cable VDO 2		
	USB2	USB3	TBT3	DP	Cable Plug Passive/ Active B29…27	Cable Termination Type B12…11	Cable Termination Type B12…11	Physical connection B10	Active element B9	Optical Isolated Active Cable B2
Passive[1]	Yes	Yes	Yes	Yes	011b	00b/01b	n/a	n/a	n/a	n/a
Linear Re-driver[1]	Yes	Yes	Yes	Opt.	011b	01b[2]	n/a	n/a	n/a	n/a
Re-timer[1]	Yes	Yes	Yes	Opt.	100b	n/a	10b/11b	0b	1b	0b
Hybrid Optical [1, 3]	Yes	Yes	Yes	Opt.	100b	n/a	11b	1b	0b/1b	0b
Optically Isolated	No	Yes	Opt.	No	100b	n/a	11b	1b	0b/1b	1b

Notes:

1. USB4 cables are required to support Thunderbolt™ 3 compatibility at this time. The TBT3-specific identity requirements are defined in Appendix F.
2. The Linear Re-driver active cable represents as only a Passive Cable that is discovered per Figure 5-1.
3. A Hybrid Optical cable is defined as using an intermediate optical transmission line for the high-speed signaling path (TX/RX) while retaining a copper-based solution for the rest of the defined interfaces.

Note: As indicated in Table 6-3, USB4 passive cables are required to support Thunderbolt™ 3 compatibility. The implication of this requirement is that USB4 Gen3 passive cables will properly respond to TBT3 Passive Cable Discover Identity commands with the VDOs as defined in Table F-1 and Table F-3 of Section F.2.1 in order that they will be used in a TBT3 connection at Gen3 speeds. USB4 Gen2 cables should not implement TBT3 Passive Cable Identity VDOs.

6.2.1.3 Cable Status

The USB PD ***Get_Status*** Command is used to discover the current state of the active cable. Cable status shall be reported on SOP' and shall also be reported on SOP" when the SOP'' Controller Presence bit is set in the Active Cable VDO.

6.2.2 USB PD Messages for OIAC

The following sections outline the USB PD Messages for an OIAC.

6.2.2.1 USB PD Message Handling on Initial Connection

The OIAC shall not forward USB PD messages until after determining the DFP to UFP Connection in the Active State and the Active Cable is configured (Phase 3 complete). The OIAC shall process USB PD messages locally in the USB Type-C plug as defined in Table 6-4 on an initial connection before the disconnect/reconnect and data role establishment.

Table 6-4 OIAC USB PD Message Behavior on Initial Connection

Message Type	Local Cable Plug SOP	Local Cable Plug SOP'/SOP"	Local Cable Plug SOP	Local Cable Plug SOP'	Local Cable Plug SOP"
Control Messages	**Transmitted Message**		**Received Message**		
Accept	Normative	Normative	Normative	Ignore	Ignore
DR_Swap	Normative	Not Allowed	Wait	Ignore	Ignore
FR_Swap	Not Allowed	Not Allowed	Reject	Ignore	Ignore
Get_Country_Codes	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_PPS_Status	Not Supported	Not Allowed	Not Supported	Ignore	Ignore
Get_Sink_Cap	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Get_Sink_Cap_Extended	Not Supported	Not Allowed	Not Supported	Ignore	Ignore
Get_Source_Cap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Source_Cap_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Status	Not Allowed	Not Allowed	Not Supported	Normative	Ignore
GoodCRC	Normative	Normative	Normative	Normative	Ignore
GotoMin	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Not_Supported	Normative	Normative	Normative	Normative	Normative
Ping	Not Allowed	Not Allowed	Ignore	Ignore	Ignore
PR_Swap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
PS_RDY	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Reject	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Soft_Reset	Normative	Not Allowed	Normative	Ignore	Ignore
Vconn_Swap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Wait	Normative	Not Allowed	Normative	Ignore	Ignore
Data Messages	**Transmitted Message**		**Received Message**		
Source_Capabilities	Not Allowed	Not Allowed	Normative	Ignore	Ignore
Request	Normative	Not Allowed	Not Supported	Ignore	Ignore
Get_Country_Info	Not Allowed	Not Allowed	Not Supported	Not Supported	Not Supported
BIST	Not Allowed	Not Allowed	Not Supported	Normative	Ignore
Sink_Capabilities	Normative	Not Allowed	Not Supported	Ignore	Ignore
Battery_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Alert	Not Allowed	Not Allowed	Ignore	Ignore	Ignore

Table 6-3 OIAC USB PD Message Behavior on Initial Connection, cont.

Message Type	Local Cable Plug SOP	Local Cable Plug SOP'/SOP"	Local Cable Plug SOP	Local Cable Plug SOP'	Local Cable Plug SOP"
Extended Messages	**Transmitted Message**		**Received Message**		
Battery_Capabilities	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Country_Codes	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Country_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Firmware_Update_Request	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Firmware_Update_Response	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Battery_Cap	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Battery_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Get_Manufacturer_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Manufacturer_Info	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
PPS_Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Security_Response	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Security_Request	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Sink_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Source_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Status	Not Allowed	Not Allowed	Not Supported	Ignore	Ignore
Vendor Defined Messages	**Transmitted Message**		**Received Message**		
Discover Identity	Normative	Not Allowed	NAK	Normative	NAK
Discover SVIDs	Not Allowed	Not Allowed	NAK	Conditional Normative/ NAK	NAK
Discover Modes	Not Allowed	Not Allowed	NAK	Conditional Normative/ NAK	NAK
Enter Mode	Not Allowed	Not Allowed	NAK	NAK	NAK
Exit Mode	Not Allowed	Not Allowed	NAK	NAK	NAK
Attention	Not Allowed	Not Allowed	Ignore	NAK	NAK

6.2.2.2 USB PD Message Handling in the Active State

There are some USB PD SOP and SOP" messages that invalid in an OIAC, therefore the next two sections explicitly define all USB PD messages that do not traverse the cable either because the message is targeted to SOP' or are invalid and all USB PD messages that do traverse the cable to SOP" and SOP.

6.2.2.2.1 USB PD Messages Which Do Not Traverse the Cable in the Active State

The USB PD messages which do not traverse the OIAC when Active are defined in Table 6-5. Section 6.2.2.2.2 describes the messages which traverse the OIAC in Active.

Table 6-5 OIAC USB PD Messages Which Do Not Traverse in Active State

Message Type	Cable Plug SOP	Cable Plug SOP'/SOP"	Cable Plug SOP	Cable Plug SOP'/SOP"
Control Messages	**Transmitted Message**		**Received Message**	
Accept	Normative	Normative	Normative	Ignore[1]
FR_Swap	Not Allowed	Not Allowed	Reject	Ignore[1]
Get_PPS_Status	Not Supported	Not Allowed	Not Supported	Ignore[1]
Get_Sink_Cap	Not Allowed	Not Allowed	Normative[3]	Ignore[1]
Get_Sink_Cap_Extended	Not Supported	Not Allowed	Normative[3]	Ignore[1]
Get_Source_Cap	Normative	Not Allowed	Not Supported	Ignore[1]
Get_Source_Cap_Extended	Normative	Not Allowed	Not Supported	Ignore[1]
GoodCRC	Normative	Normative	Normative	Normative[2]/ Ignore[1]
GotoMin	Not Allowed	Not Allowed	Ignore	Ignore[1]
Ping	Not Allowed	Not Allowed	Ignore	Ignore[1]
PR_Swap	Not Allowed	Not Allowed	Not Supported	Ignore[1]
PS_RDY	Not Allowed	Not Allowed	Normative	Ignore[1]
Reject	Normative	Not Allowed	Normative	Ignore[1]
Soft_Reset	Normative	Not Allowed	Normative	Ignore[1]
Vconn_Swap	Not Allowed	Not Allowed	Not Supported	Ignore[1]
Wait	Normative[4]	Not Allowed	Normative	Ignore[1]
Data Messages	**Transmitted Message**		**Received Message**	
Source_Capabilities	Not Allowed	Not Allowed	Normative	Ignore[1]
Request	Normative	Not Allowed	Not Supported	Ignore[1]
BIST	Not Allowed	Not Allowed	Not Supported	Normative[2]/ Ignore[1]
Sink_Capabilities	Normative	Not Allowed	Not Supported	Ignore[1]
Extended Messages	**Transmitted Message**		**Received Message**	
PPS_Status	Not Allowed	Not Allowed	Not Supported	Ignore[1]
Sink_Capabilities_Extended	Normative	Not Allowed	Not Supported	Ignore[1]
Source_Capabilities_Extended	Not Allowed	Not Allowed	Not Supported	Ignore[1]

Note:

1. SOP" message may be dropped and not forwarded across the cable.
2. Normative for SOP' and Ignore for SOP".
3. See Section 6.4.2.
4. See Section 6.2.2.5.

6.2.2.2.2 USB PD Messages Which Do Traverse the Cable in the Active State

All USB PD SOP messages defined in Table 6-6 are forwarded across the cable on SOP. The messages are sent by the Initiator, forwarded optically through the cable, and then driven on CC from the far side cable plug to the Receiver.

The timing of the message forwarding is defined in Table 6-7. The GoodCRC is generated locally to the cable plug and returned within tTransmit on a valid Message. The OIAC shall be able to handle messages received with a minimum spacing of tInterFrameGap.

The message Initiator expects a response within tSenderResponse and will perform error recovery if no response is received within this time unless the message is a Firmware_Update_Request/Response or a Security_Request/Response. The message Receiver responds within tReceiverResponse unless there is an error. The OIAC shall decide to respond locally or forward the message, send the message across the fiber, and drive the message on the far side plug CC pin within tForward as shown in Figure 6-4 unless the message is Firmware_Update_Request/Response or a Security_Request/Response. The *USB PD* handler shall forward the messages addressed to SOP defined in Table 6-5. The *USB PD* Handler shall only forward to the far-end plug any message addressed to SOP" which are defined below:

- Firmware_Update_Request, Firmware_Update_Response
- Security_Request, Security_Response
- Status
- Enter Mode, Exit Mode, Attention (if the Alternate Modes are supported by the OIAC)

The OIAC shall not forward *USB PD* messages until it completes Phase 3. The cable plug shall send no response if a GoodCRC is not received from the Responder.

Some implementations may implement local copies of the SOP" information on the local cable plug and use an internal mechanism to send/receive responses.

Table 6-6 OIAC USB PD Messages Addressed to SOP Which Traverse the OIAC in the Active State

Message Type	SOP
Control Messages	**Forward Message**
DR_Swap	Normative
Get_Country_Codes	Normative
Get_Status	Normative
Not_Supported	Normative
Wait	Normative
Data Messages	**Forward Message**
Get_Country_Info	Normative
Battery_Status	Normative
Alert	Normative
Extended Messages	**Forward Message**
Battery_Capabilities	Normative
Country_Codes	Normative
Country_Info	Normative
Firmware_Update_Request	Normative
Firmware_Update_Response	Normative
Get_Battery_Cap	Normative
Get_Battery_Status	Normative
Get_Manufacturer_Info	Normative
Manufacturer_Info	Normative
Security_Request	Normative
Security_Response	Normative
Status	Normative
Vendor Defined Messages	**Forward Message**
Discover Identity	Normative
Discover SVIDs	Normative
Discover Modes	Normative
Enter Mode	Normative
Exit Mode	Normative
Attention	Normative

Figure 6-4 OIAC USB PD Message Forwarding

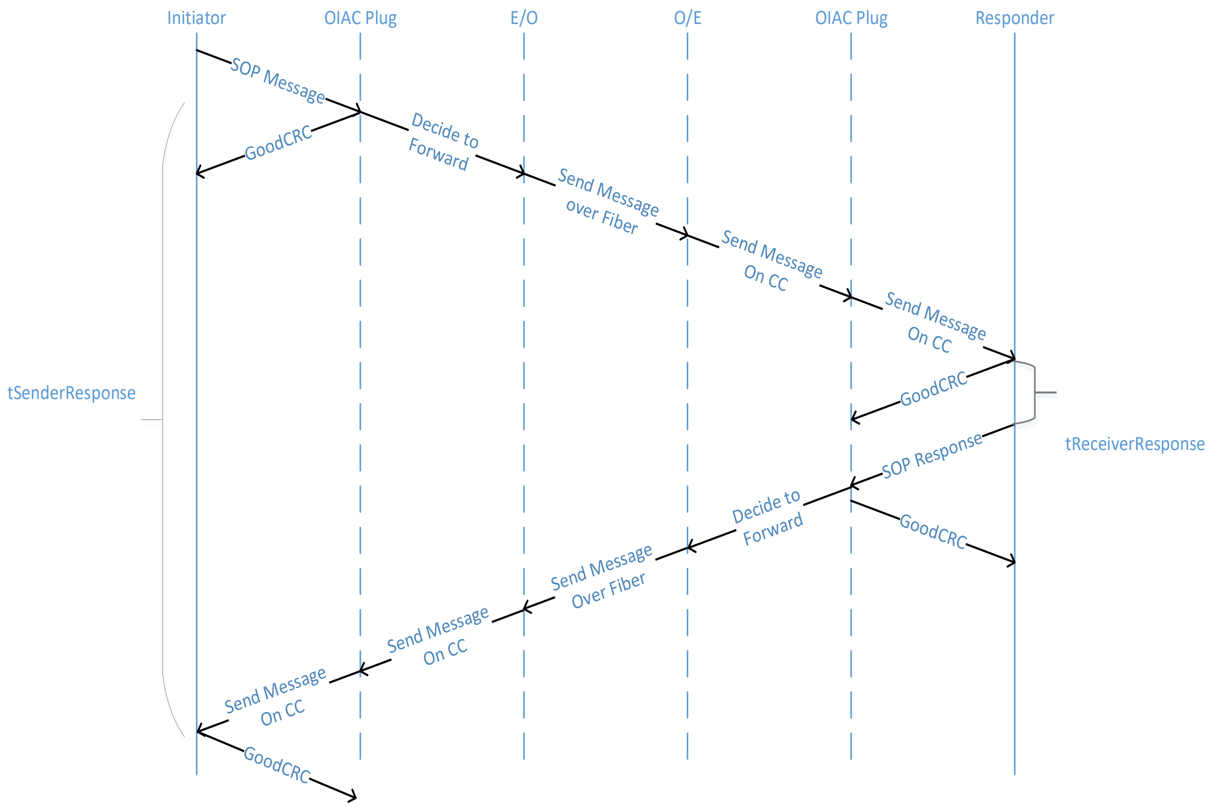


Table 6-7 OIAC USB PD Message Timing

Timer	Value (Min)	Value (Max)	Units	Reference
tDRSwapWait	100		ms	Time to wait if WAIT received before sending another DR_Swap. Defined in the *USB PD* Specification.
tForward		4	ms	Time to forward SOP Message one direction in OIAC.
tTransmit		195	µs	Time to send the GoodCRC. Defined in the *USB PD* Specification.
tInterFrameGap	25		µs	Time from the end of last bit of a Frame until the start of the first bit of the next Preamble. Defined in the *USB PD* Specification.
tReceiverResponse		15	ms	Time for SOP Receiver to respond. Defined in the *USB PD* Specification.
tSenderResponse	24	30	ms	Time for SOP Initiator to receive response. Defined in the *USB PD* Specification.
tBootupCRCHoldoff		50	ms	Hold off on GoodCRC until ready to respond with Operational RDO in Phase 3.

Note: The *USB PD* specification revision shall take precedence over this table if any discrepancies exist.

6.2.2.3 USB PD Reset Handling

The *USB PD* Reset handling by OIAC is defined in Table 6-8.

The OIAC shall:

1. Detect the Hard Reset ordered set
2. Forward it to the remote plug and remote port
3. Reset its state machine.

Table 6-8 OIAC SOP Messages Which Terminate at the Cable Plug

Ordered Sets	Note
Hard Reset	Resets port partners at each end of the cable and the cable itself
Cable Reset	OIAC shall ignore a Cable reset

A Hard Reset signal can occur at any time during normal operation of the cable and also during the cable initialization. This signal will take precedent over the initialization state machine and immediately forward the Hard Reset Message to the remote plug, using an internal cable message.

6.2.2.4 Internal Cable Messages

All SOP" and SOP messages shall be forwarded or terminated as defined in Section 6.2.2 and will not be further described in this section.

The messages defined in this section provide informative guidance on internal messages for OIACs. The actual definition and implementation of each message is left to the implementer.

In this section and Section 6.3, there is a defined Plug-A and Plug-B to support *USB PD* communication through the OIAC cable. These designations are established at the time of manufacture and are completely internal to the cable. They are used to simplify the cable initialization and internal messaging.

6.2.2.4.1 MSG_Keep_Alive

A low duty cycle message that is meant to inform the remote cable plug that the local cable plug is still operational.

A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.2.2.4.2 MSG_Keep_Alive_ACK

Acknowledgement message to the MSG_Keep_Alive.

A simple example is that only Plug-A will send MSG_Keep_Alive and Plug-B must respond with MSG_Keep_Alive_ACK. Each end will have its own timeout for MSG_Keep_Alive and MSG_Keep_Alive_ACK.

6.2.2.4.3 MSG_Port_Capabilities

This message contains all relevant local port capabilities including but not limited to:

- Chunked/Unchunked capability
- DRD/DFP/UFP capabilities

6.2.2.4.4 MSG_Cable_Config

This message contains the final cable configuration based on known system capabilities.

It will contain both relevant ports' capabilities and the final DFP/UFP roles for the system.

This message will also serve as the signal in Phase 2 for the cable plug to start the reboot process.

6.2.2.4.5 MSG_Release_Remote_SourceCap_GoodCRC

This is a synchronization message to attempt to bring up both ports at the same time.

It is used in Phase 3 and is the signal to release the GoodCRC message to the Source Capabilities message from the attached port. At the beginning of Phase 3, after each plug has been rebooted, and depending on the final DFP/UFP role, each plug should wait for MSG_Release_Remote_SourceCap_GoodCRC before it is allowed to release a GoodCRC in response to a Source_Capabilities message from the port.

6.2.2.4.6 MSG_DR_Swap_Init

Initial DR_Swap sent by Plug-A to Plug-B to perform a DR_Swap.

6.2.2.4.7 MSG_DR_Swap_Reject

Plug-B sends this message to report that the initial DR_Swap was rejected by its attached port.

This is needed by Plug-A to attempt to re-configure the cable such that the port associated to Plug-B can remain a DFP. This is part of the DR_Swap test in Phase 1, shown in the state diagram transition from M3 to M4 (or M3 to M5). It is also possible that this may be needed in Phase 3, if the port associated with Plug-B rejects the DR_Swap.

6.2.2.4.8 MSG_DR_Swap_Accept

Plug-B sends this message to report that the initial DR_Swap was accepted by its attached port.

This is needed by Plug-A to continue (M3 → M6 transition) in Phase 1 in the cable initialization.

6.2.2.4.9 MSG_Force_Detach

This message is to request the remote plug to disconnect from its attached port. The disconnect method can be done by raising the voltage on the CC line to above vRd-Connect or removing Rd.

This will cause the remote port to remove VCONN from the remote plug all the circuitry should be powered down, therefore resetting any action taken by the plug on the CC line to cause the disconnect.

6.2.2.4.10 MSG_Hard_Reset

This message is to forward a Hard_Reset signal to the remote plug and port.

An internal Hard Reset message should be responded to with an Acknowledgement.

6.2.2.4.11 MSG_Acknowledgement

This message is to acknowledge that a message was received.

This message has been explicitly defined in a few specific cases but can be used more broadly.

6.2.2.5 Data Role Swap in Active State

OIACs shall support Data Role Swaps on SOP. Each OIAC plug discovers its plug port partner and determines if it is capable of a Data Role Swap during the initialization process described in Section 6.3. OIAC cable plugs generate internal messages to communicate the DR_Swap, Accept, Reject, and Wait to the far side of the cable.

- The flow of a successful DR_Swap is shown in Figure 6-5.
- The flow of a Responder rejecting a DR_Swap is shown in Figure 6-6.
- The flow of a Responder issuing a Wait to a DR_Swap is shown in Figure 6-7. Note: The *USB PD* Wait and Retry timers shall follow all timing requirements in *USB PD*.
- The flow of an Initiator rejecting a cable plug DR_Swap due to an Accept from the Responder is shown in Figure 6-8.
- The flow of an Initiator issuing a Wait to a cable plug DR_Swap due to an Accept from the Responder is shown in Figure 6-9. Note: This does not follow the *USB PD* Wait timing, because a Hard Reset is initiated

Figure 6-5 OIAC Successful Data Role Swap

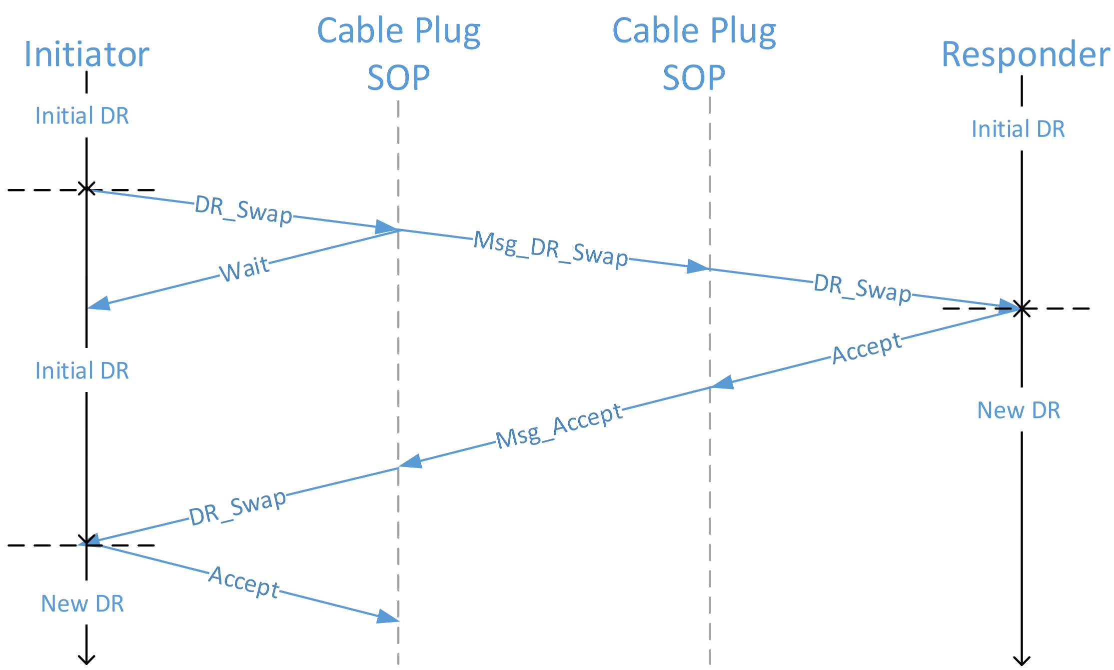


Figure 6-6 OIAC Rejected Data Role Swap

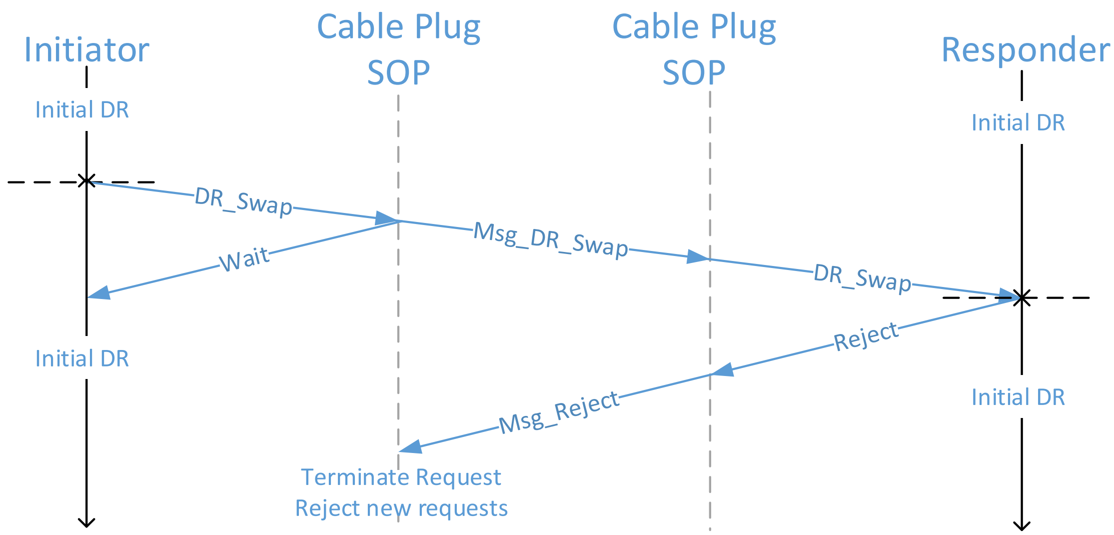


Figure 6-7 OIAC Wait Data Role Swap

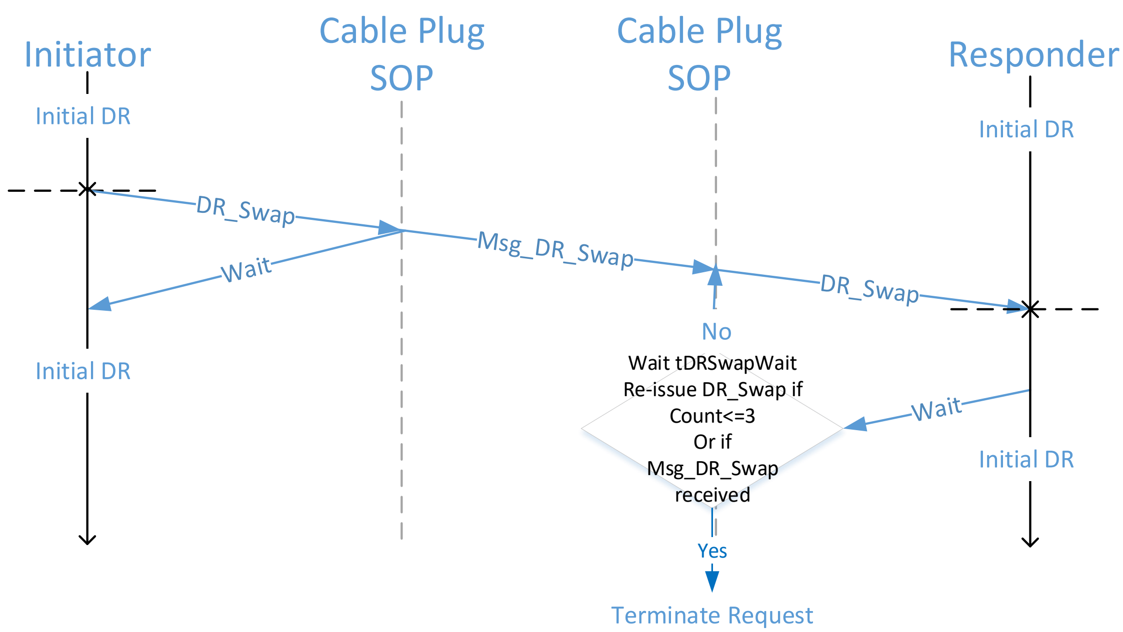


Figure 6-8 OIAC Initiator Reject Data Role Swap

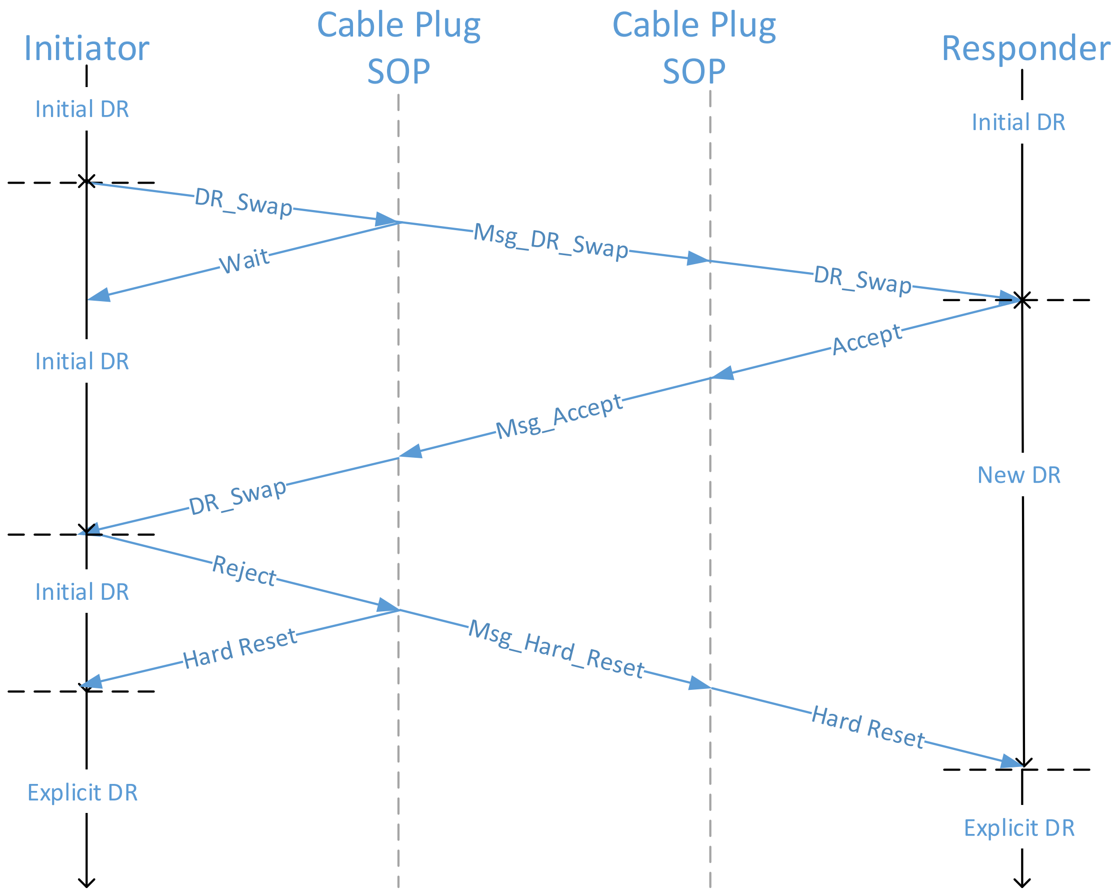
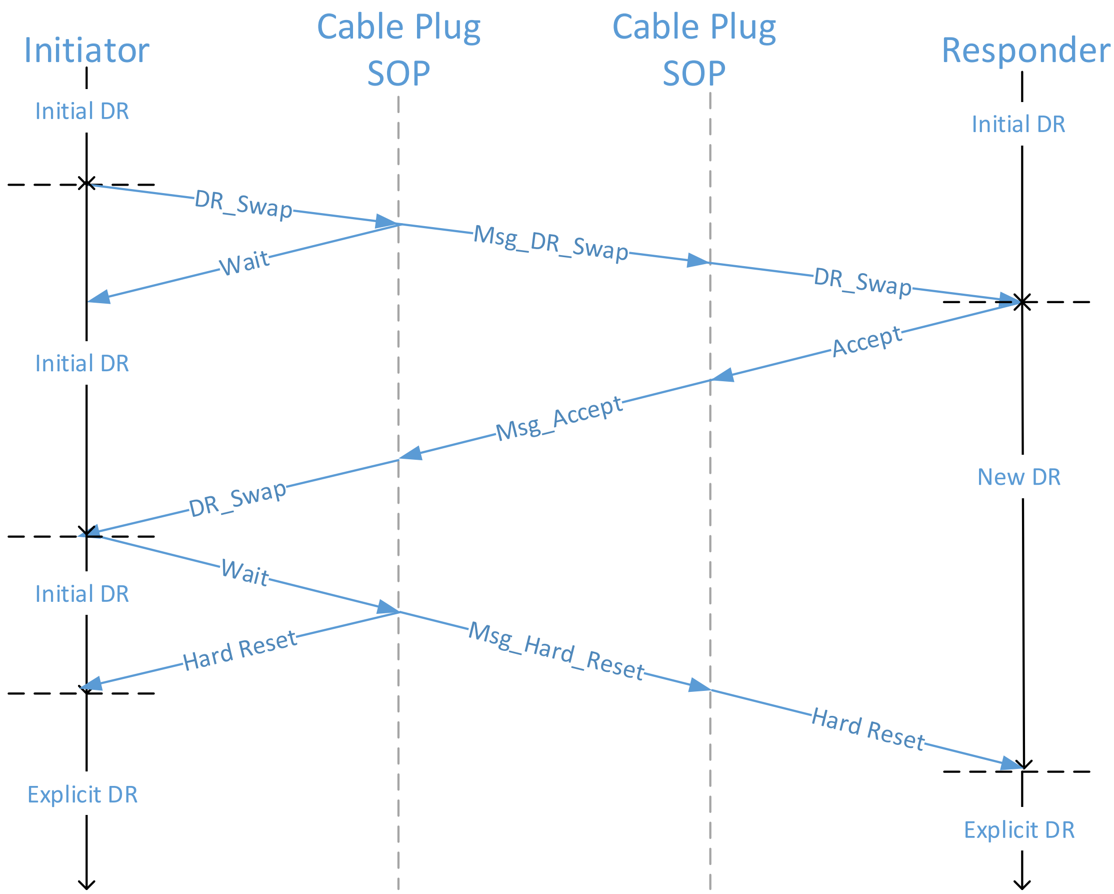


Figure 6-9 OIAC Initiator Wait Data Role Swap



6.2.3 Short Active Cable Behaviors in Response to Power Delivery Events

Each cable plug of the short active cable shall be capable of communicating on SOP' and SOP" if reported in the Discover_Identity Command.

6.2.3.1 Data Role Swap

Short active cables are transparent to the *USB PD* Data Role swap.

6.2.3.2 Power Role Swap

Short active cables shall maintain *USB 3.2* signaling during a *USB PD* Power Role swap. The source of VCONN is not affected by a Power Role Swap.

6.2.3.3 VCONN Swap

Short active cables shall maintain *USB 3.2* signaling during a *USB PD* VCONN swap. During a VCONN Swap, the original VCONN Source continues to supply VCONN for some time after the new VCONN Source begins to supply VCONN. This ensures that VCONN is never dropped.

6.2.3.4 Fast Role Swap

Short active cables will drop *USB 3.2* signaling as a side-effect of a Fast Role Swap if VCONN is not maintained during the Fast Role Swap.

6.3 OIAC Connection Flow and State Diagrams

This section defines the connection state diagrams for the OIAC.

OIAC plug defined at time of manufacture as either Plug-A or Plug-B for *USB PD* communication. This in no way indicates the plug has more or less capability, rather it allows for a consistent behavior when making the initial end to end connection.

The OIAC communicates using *USB PD* with its plug partners to determine the partner capabilities. The OIAC performs a series of connect/disconnects to establish the correct UFP/DFP data role for the cable plug. The possible combinations for ports and cable plugs is defined in Table 6-9.

The connection and establishment of data roles is performed in three phases.

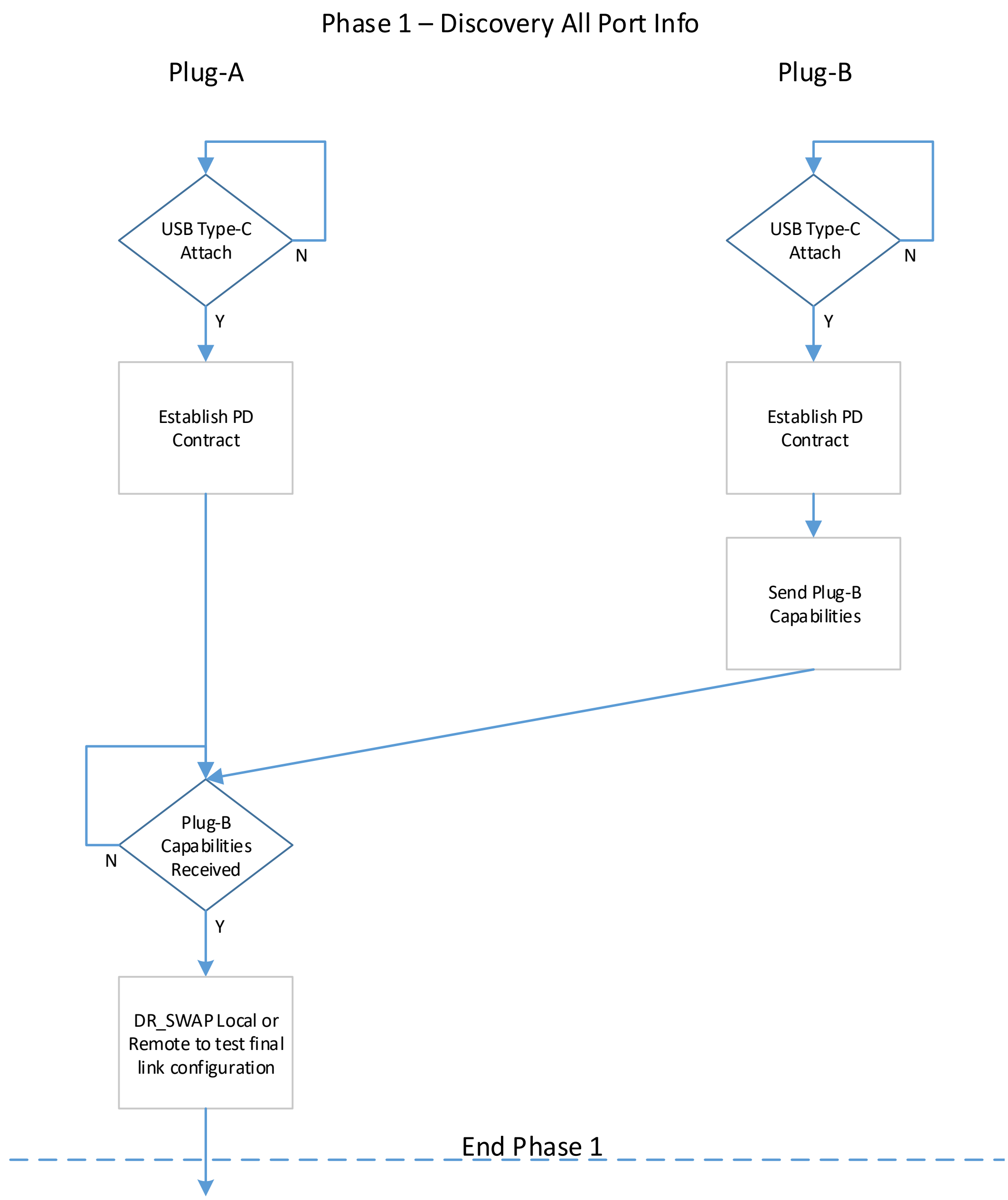
Table 6-9 Port and Plug Capabilities

Host/Device Port Capabilities	Cable Configuration		Host/Device Port Capabilities
	Plug-A Role	Plug-B Role	
DRD	DFP	UFP	DRD
DFP	UFP	DFP	DRD
DRD	DFP	UFP	DFP
DFP	Billboard		DFP
Any	Billboard if possible		UFP
UFP	Billboard if possible		Any

6.3.1 OIAC Connection Flow – Discovery – Phase 1

The OIAC cable plugs discover the capabilities of their port partners in the Discovery Phase.

Figure 6-10 OIAC Discovery – Phase 1



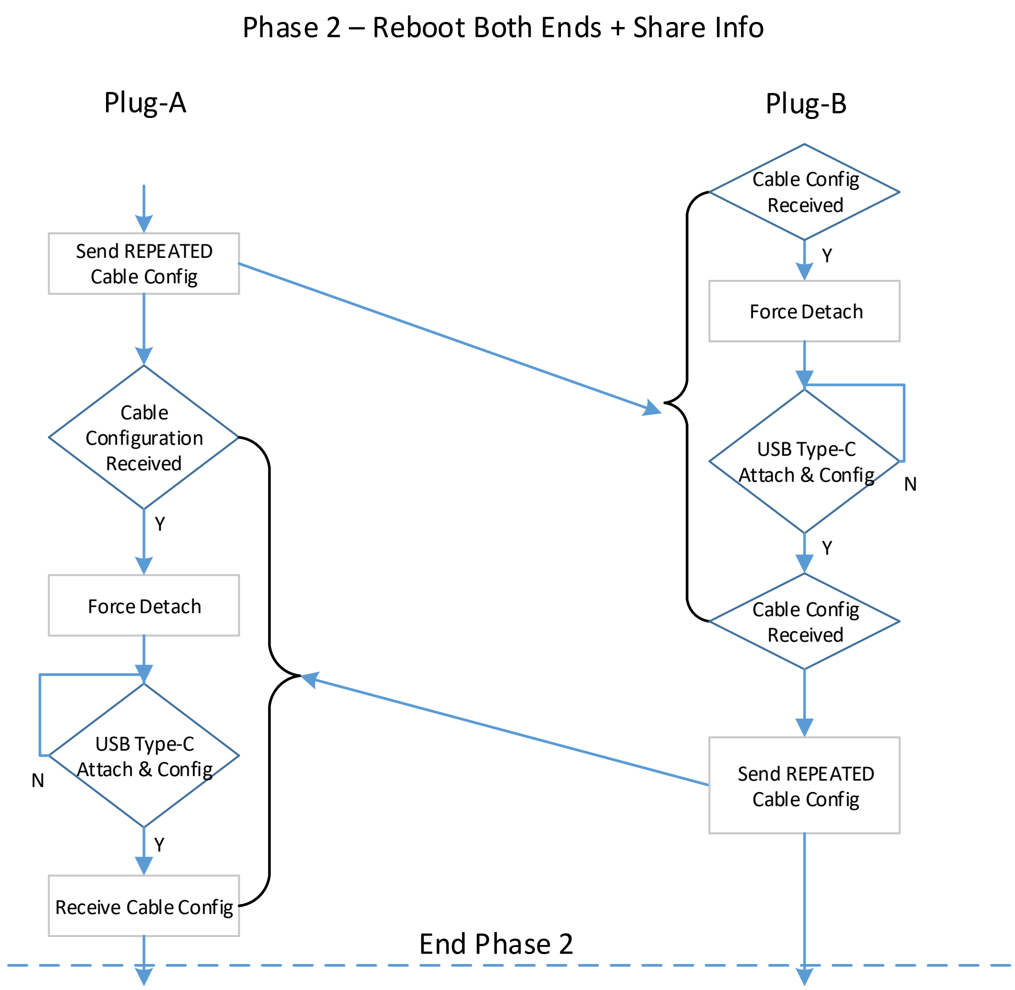
6.3.2 OIAC Connection Flow – Reboot – Phase 2

The OIAC cable plugs forward the capabilities of their plug partners and perform disconnect/reconnect.

- Plug-A will always start with repeatedly sending “MSG_Cable_Config” to Plug-B to start reboot.
- Plug-B Reboots.
- Plug-B sees “MSG_Cable_Config” and holds off on SourceCap GoodCRC until it is allowed to release it.

- Plug-B sends "MSG_Cable_Config" to the Plug-A.
- Plug-A Reboots.
- Plug-A sees "MSG_Cable_Config" and holds off on SourceCap GoodCRC until it is allowed to release it.

Figure 6-11 OIAC Reboot – Phase 2



6.3.3 OIAC Connection Flow – Configuration – Phase 3

The OIAC Plug-A determines DFP/UFP roles for Plug-A and Plug-B. Plug-A releases the PLUG to be configured as the DFP and initiates a DR_Swap. The side that issues the DR_Swap send a DR_Swap and releases the other side SourceCap GoodCRC.

Figure 6-12 OIAC Plug-A Configured as DFP – Phase 3

Host/Device Port		Cable Plug-A	Cable Plug-B		Host/Device Port
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

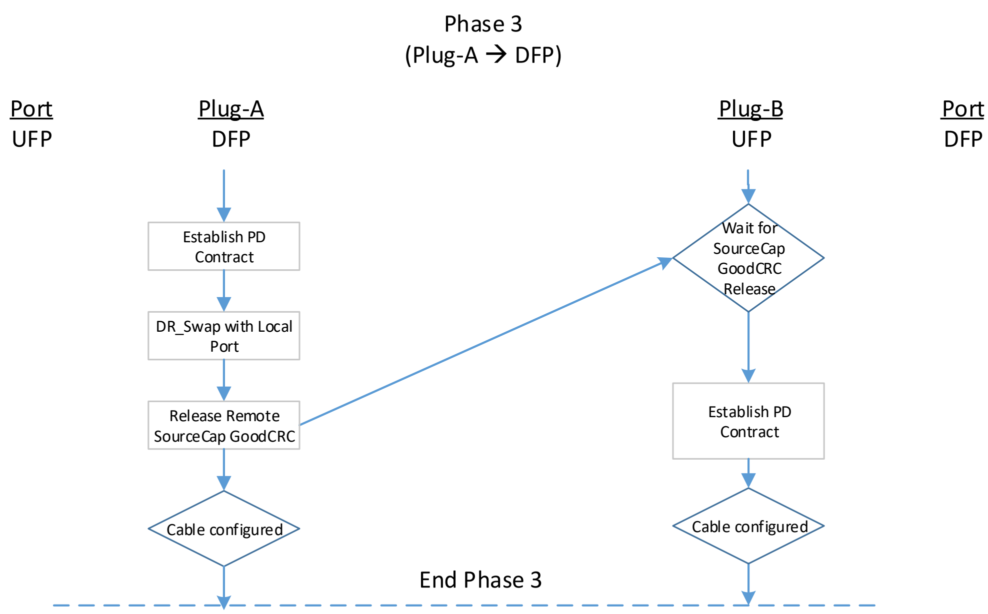


Figure 6-13 OIAC Plug-A Configured as UFP – Phase 3

Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any

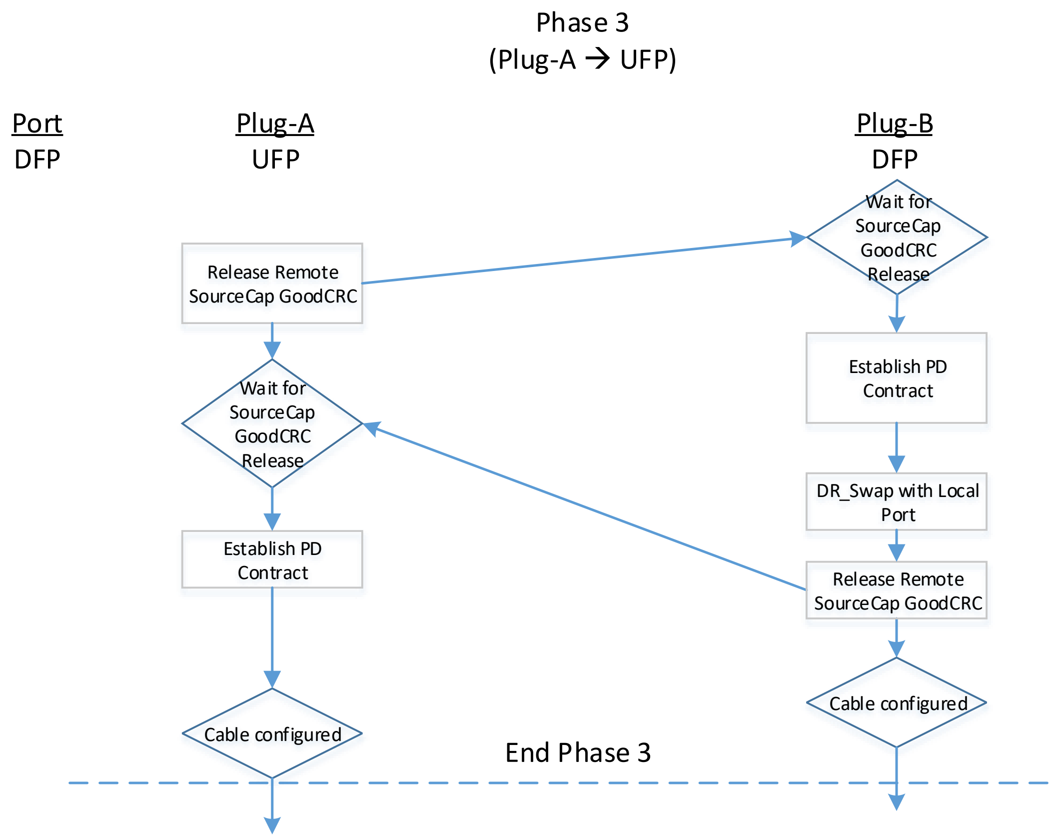
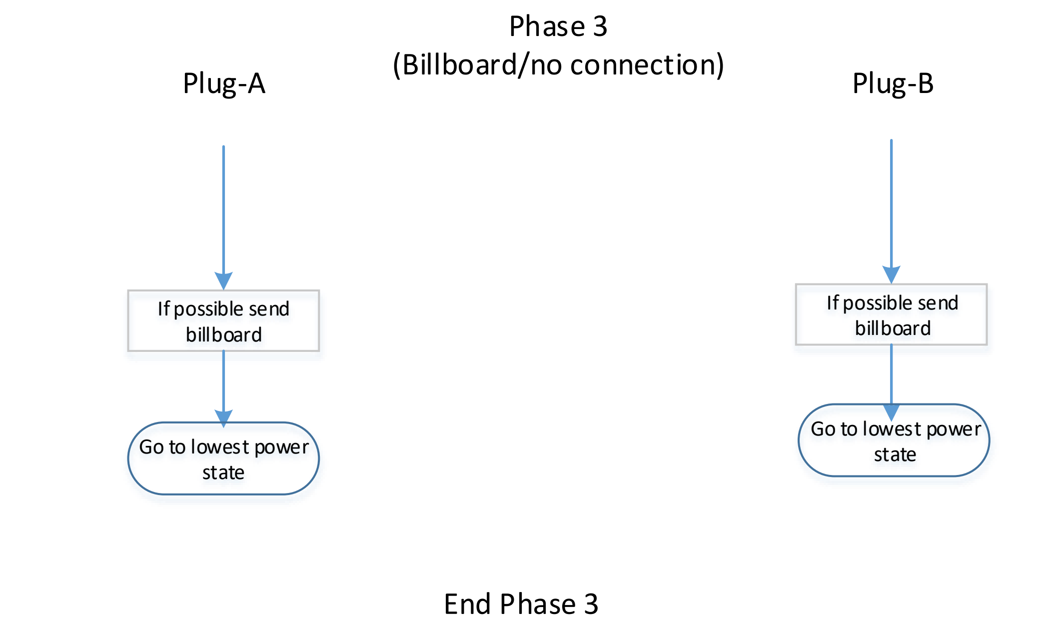


Figure 6-14 OIAC Plug-A No Connection Possible Billboard – Phase 3

Host/Device Port		Cable			Host/Device Port
		Plug-A	Plug-B		
DRD		DFP	UFP		DRD
DFP		UFP	DFP		DRD
DRD		DFP	UFP		DFP
DFP		Billboard			DFP
Any		Billboard if Possible			UFP
UFP		Billboard if Possible			Any



6.3.4 OIAC Connection State Diagram Plug-A

The following sections details a possible OIAC state diagram for Plug-A.

Figure 6-15 OIAC Plug-A State Diagram Part 1 (Phase 1 and 2)

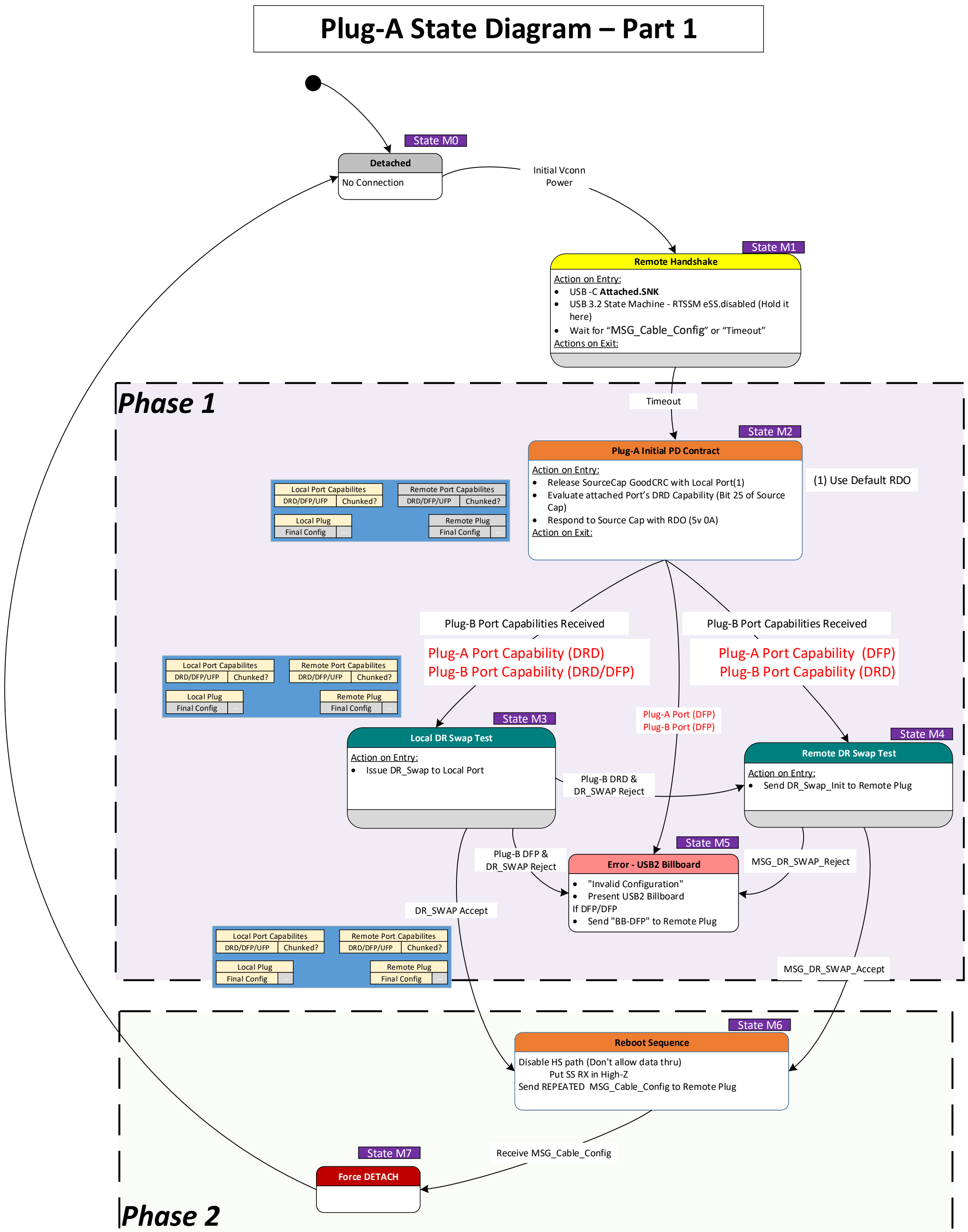
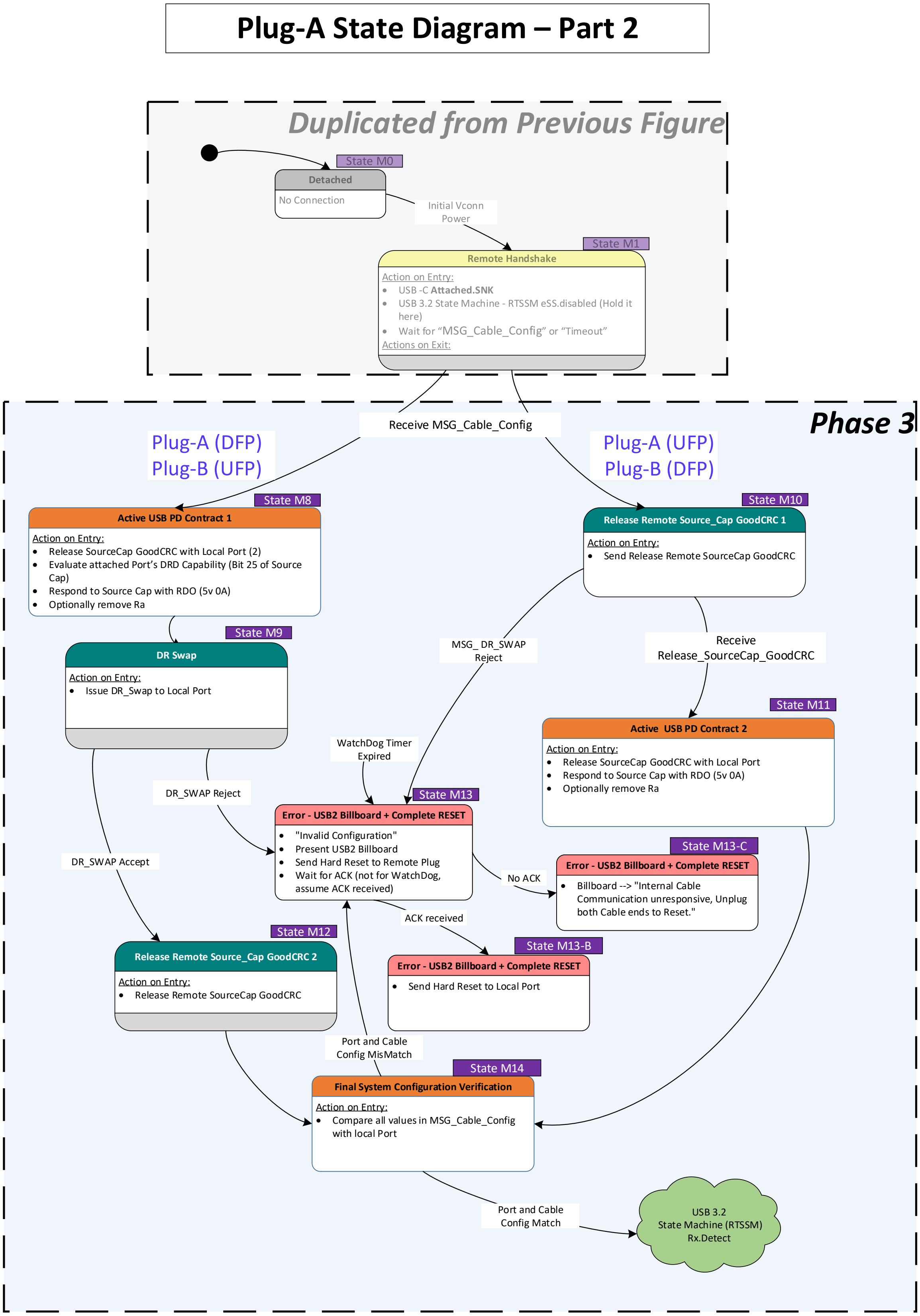


Figure 6-16 OIAC Plug-A State Diagram Part 2 (Phase 3)



6.3.4.1 Detached State (M0)

The plug is in ***Detached*** (M0) when no power is applied. The plug transitions to ***Remote Handshake*** (M1) when VCONN is applied.

6.3.4.2 Remote Handshake State (M1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from Plug-B.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of Plug-B's Repeat Port Capabilities messages and the maximum cable latency.

The plug starts in the *USB 3.2* RTSSM eSS.Disabled and remains in eSS.Disabled until cable initialization is complete at the end of Phase 3.

6.3.4.2.1 Entry to Remote Handshake

The plug enters Attached.SNK followed by entry to ***Remote Handshake*** (M1).

6.3.4.2.2 Exit from Remote Handshake

The plug transitions to:

- ***Plug-A Initial PD Contract*** (M2) when the "Timeout" timer has expired,
- ***Active USB PD Contract 1*** (M8) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a DFP and Plug-B will resolve to a UFP, or
- ***Release Remote Source_Cap GoodCRC 1*** (M10) upon receipt of a "MSG_Cable_Config" message when Plug-A resolves to a UFP and Plug-B will resolve to a DFP.

6.3.4.3 Plug-A Initial PD Contract State (M2)

When the plug is in ***Plug-A Initial PD Contract***, the plug has established an initial *USB PD* contract and evaluated its local port's DRD capability.

6.3.4.3.1 Entry to Plug-A Initial DP Contract

On Entry to ***Plug-A Initial PD Contract***, the plug shall:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port
2. Evaluate the local attached port's DRD capability (as indicated in the Source Capabilities message)
3. Respond to the Source Capabilities message with the "default" RDO specified in Table 6-11.

6.3.4.3.2 Exit from Plug-A Initial DP Contract

The OIAC plug shall transition to:

- ***Local DR Swap Test*** (M3) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DRD and the Plug-B port is either a DRD or DFP,
- ***Remote DR Swap Test*** (M4) upon receipt of a MSG_Port_Capabilities where the Plug-A port is a DFP and the Plug-B port is DRD, or

- ***Error – USB2 Billboard*** (M5) upon determination both Plug-A and Plug-B are connected to DFPs.

6.3.4.4 Local DR Swap Test State (M3)

The ***Local DR Swap Test*** is a test to ensure that the Plug-A port that is defined as a DRD will accept a DR_Swap request.

6.3.4.4.1 Entry to Local DR Swap Test

On entry to ***Local DR Swap Test***, the plug shall issue DR_Swap request to its local port.

If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.4.4.2 Exit from Local DR Swap Test

The OIAC plug shall transition to:

- ***Remote DR Swap Test*** (M4) upon receipt of a Reject and the Plug-B port reported that it is a DRD,
- ***Error – USB2 Billboard*** (M5) upon receipt of a Reject and the Plug-B port reported that it is a DFP, or
- ***Reboot Sequence*** (M6) upon receipt of an Accept.

6.3.4.5 Remote DR Swap Test State (M4)

The ***Remote DR Swap Test*** is a test to ensure that the Plug-B port that is defined as a DRD will accept a DR_Swap request.

6.3.4.5.1 Entry to Remote DR Swap Test

On entry to ***Remote DR Swap Test***, the plug shall issue a DR_Swap_Init to the remote plug.

6.3.4.5.2 Exit from Remote DR Swap Test

The OIAC plug shall transition to:

- ***Reboot Sequence*** (M6) upon receipt of a MSG_DR_Swap_Accept, or
- ***Error – USB2 Billboard*** (M5) upon receipt of a MSG_DR_Swap_Reject.

6.3.4.6 Error – USB2 Billboard (M5)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."

6.3.4.6.1 Entry to Error – USB2 Billboard

On entry ***Error – USB2 Billboard***, the plug shall issue present a Billboard message over *USB 2.0* and then power down to its lowest possible state.

6.3.4.6.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.4.7 Reboot Sequence State (M6)

When the plug is in the ***Reboot Sequence***, it will disable the High Speed Data path and start to initiate a remote plug reboot.

6.3.4.7.1 Entry to Reboot Sequence

On entry to Reboot Sequence, the plug shall:

1) Disable the HS path by changing the SS RX termination to High-Z.
2) Determine and store the final System Configuration for this link.
    a. The System Configuration will contain:
        i. Host/Device Port information
        ii. Final Plug-A/Plug-B roles
            1. If coming from State M3
                a. Plug-A → DFP (DR_Swap)
                b. Plug-B → UFP
            2. If coming from State M4
                a. Plug-A → UFP
                b. Plug-B → DFP (DR_Swap)
            3. If coming from State M9
                a. Plug-A → UFP
                b. Plug-B → DFP (DR_Swap)
3) Continuously send "MSG_Cable_Config" message to the remote plug.

6.3.4.7.2 Exit from Reboot Sequence

The OIAC plug shall transition to the ***Force Detach*** (M7) when a "MSG_Cable_Config" message is received that matches the final configuration that Plug-A sent to Plug-B.

6.3.4.8 Force Detach State (M7)

The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.

6.3.4.8.1 Entry to Force Detach

On entry to ***Force Detach***, the plug shall raise the voltage on the CC-wire above vRd-Connect.

6.3.4.8.2 Exit from Force Detach

The plug transitions to ***Detached*** upon exit from ***Force Detach***.

6.3.4.9 Active USB PD Contract 1 State (M8)

Active USB Contract 1 is where OIAC Plug-A creates at *USB PD* contract with the local port.

6.3.4.9.1 Entry to Active USB PD Contract 1

The OIAC plug shall follow the steps listed below:

1. Begin responding to *USB PD* messages from its port partner with GoodCRCs.
2. Evaluate Fixed 5V PDO in the Source Capabilities message to check if its port partner is a DRD.
3. Request for a 5 V @ 0 A power contract.
4. May remove Ra to save power.

6.3.4.9.2 Exit from Active USB PD Contract 1

The plug transitions to the ***DR Swap*** (M9) when it receives an Accept followed by a PS_RDY message from its port partner.

6.3.4.10 DR Swap State (M9)

The ***DR Swap*** is used to set the final data role of the OIAC's Plug-A and signal to the OIAC Plug-B to complete its configuration.

6.3.4.10.1 Entry to DR Swap

The OIAC plug shall issue a DR_Swap to its port partner.

If the local port responds to the DR_Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (M5).

6.3.4.10.2 Exit from DR Swap

If the DR_Swap message is responded to with:

- An Accept, it shall transition to the ***Release Remote Source_Cap GoodCRC 2 State*** (M12), or
- A Reject it shall transition to the ***Error - USB2 Billboard + Complete Reset*** (M13).

6.3.4.11 Release Remote Source_Cap GoodCRC 1 State (M10)

The OIAC is waiting to for Release_Remote_Source_Cap_GoodCRC to better synchronize the power on of the two OIAC plug ends.

6.3.4.11.1 Entry to Release Remote Source_Cap GoodCRC 1

The OIAC plug shall release the Remote SourceCap GoodCRC.

6.3.4.11.2 Exit from Release Remote Source_Cap GoodCRC 1

The OIAC plug shall transition to:

- ***Active USB PD Contract 2 State*** (M11), when a "MSG_ Release_Remote_SourceCap_GoodCRC" message is received, or
- ***Error – USB2 Billboard + Complete Reset*** (M13) upon receipt of a MSG_DR_Swap_Reject.

6.3.4.12 Active USB PD Contract 2 State (M11)

Active USB Contract 2 is where OIAC Plug-A creates at *USB PD* contract with the local port and should end with viable link.

6.3.4.12.1 Entry to Active USB PD Contract 2

The OIAC plug shall follow the steps listed below:

1. Begin responding to USB PD messages from its port partner with GoodCRCs.
2. Request a 5 V @ 0 A power contract.
3. May remove Ra to save power.

6.3.4.12.2 Exit from Active USB PD Contract 2

The plug shall transition to ***Final System Configuration Verification*** (M13) for final system verification.

6.3.4.13 Release Remote Source_Cap GoodCRC 2 State (M12)

OIAC Source Plug configuration is completed and the *USB 3.2* begins looking for a connection.

6.3.4.13.1 Entry to Release Remote Source_Cap GoodCRC 2

The OIAC plug shall release the Remote SourceCap GoodCRC.

6.3.4.13.2 Exit from Release Remote Source_Cap GoodCRC 2

The plug shall transition to ***Final System Configuration Verification*** (M13) for final system verification.

6.3.4.14 Error – USB2 Billboard + Complete Reset (M13)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."

6.3.4.14.1 Entry to Error – USB2 Billboard + Complete Reset (M13)

On entry Error – USB2 Billboard + Complete Reset, the plug shall:

1) Present a USB2 Billboard message
2) Send a MSG_Hard_Reset to the remote Plug
3) Wait for Hard Reset Ack from Remote Plug (Unless entry is from an expired WatchDog Timer, in which case, go directly to M13-B)

   Received ACK (State M13-B):

4) Send Hard Reset to the Local Port

   Did NOT receive ACK (State M13-C):

5) Present USB2 Billboard Message: "Error: Internal Cable Communication Error. Unplug both cable ends to reset."

6.3.4.14.2 Exit from Error – USB2 Billboard + Complete Reset (M13 B/C)

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power from each port.

6.3.4.14.3 WatchDog Timer Entry

A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer shall NOT be implemented including but not limited to M2, where it is possible that only a single end of the OIAC is connected and M6, where the reboot sequence can take a few seconds.

6.3.4.15 Final System Configuration Verification (M14)

Final System Configuration Verification is used to do one final check there were no unforeseen changes the local port and the final cable configuration defined by Plug-A.

6.3.4.15.1 Entry to Final System Configuration Verification

The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.

6.3.4.15.2 Exit from Final System Configuration Verification

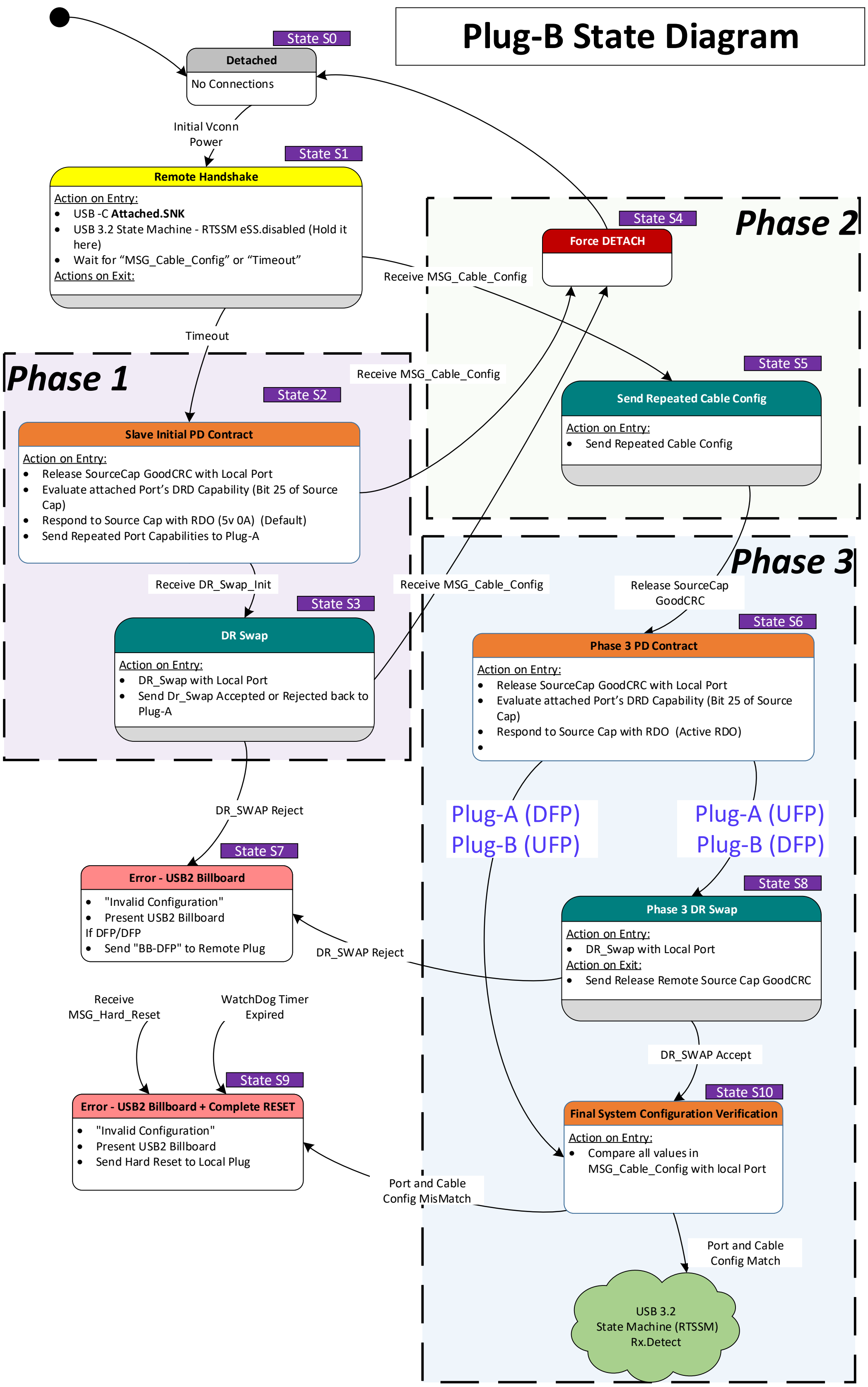
The plug shall transition to:

- ***Rx.Detect***, and start far-end receiver termination detection and the *USB 3.2* RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error - USB2 Billboard + Complete RESET*** (State M14) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

6.3.5 OIAC Connection State Diagram Plug-B

The following sections details a possible OIAC state diagram for Plug-B.

Figure 6-17 OIAC Plug-B State Diagram



6.3.5.1 Detached State (S0)

The plug is in ***Detached*** (S0) when no power is applied. The plug transitions to ***Remote Handshake*** (S1) when VCONN is applied.

6.3.5.2 Remote Handshake State (S1)

The plug is waiting for the "Timeout" timer expiration or a "MSG_Cable_Config" message from Plug-A.

Recommended Timeout time = ~100ms

The Timeout time is dependent on the duty cycle of the Plug-A's Repeat MSG_Cable_Config messages and the maximum cable latency.

6.3.5.2.1 Entry to Remote Handshake

The plug enters Attached.SNK followed by entry to ***Remote Handshake*** (S1).

The plug starts in the USB 3.2 RTSSM eSS.Disabled and remains in eSS.Disable until cable initialization is complete at the end of Phase 3.

6.3.5.2.2 Exit from Remote Handshake

The plug transitions to:

- ***Plug-B Initial PD Contract*** (S2) when the "Timeout" timer has expired, or
- ***Send Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message.

6.3.5.3 Plug-B Initial DP Contract (S2)

The plug takes the following actions in the order defined:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.
2. Evaluate the local attached port's DRD Capability (as indicated in the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) and negotiate an explicit power contract.
4. Send "MSG_Port_Capabilities" to Plug-A. The plug shall continue to send "MSG_Port_Capabilities" until it exits this state.

6.3.5.3.1 Entry to Plug-B Initial DP Contract

The plug enters ***Plug-B Initial PD Contract*** (S2) upon "Timeout" timer expiration.

6.3.5.3.2 Exit from Plug-B Initial DP Contract

The plug transitions to:

- ***DR Swap*** (S3) upon receipt of a "DR_Swap_Init" message from Plug-A, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.5.4 DR Swap (S3)

The plug determines if a DR_Swap can be performed with the local attached port or Plug-A configured itself.

6.3.5.4.1 Entry to DR Swap

Upon entry into DR Swap (S3) the plug shall:

1. Send DR_Swap message to the local attached port.
2. Send MSG_DR_Swap_Accept when the plug receives Accept message from the local attached port.
3. Send MSG_DR_Swap_Reject when the plug receives Reject message from the local attached port.

If the local port responds to the DR Swap with "Wait," then the plug shall follow the tDRSwapWait timer and retry up to 3 times, after which it will error out and transition to state ***Error – USB2 Billboard*** (S7).

6.3.5.4.2 Exit from DR Swap

The plug shall transition to:

- ***Error – USB2 Billboard*** (S7) upon rejection of the local attached port DR_Swap, or
- ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.5.5 Force Detach (S4)

The plug shall transition to SRC.Open on both CC and VCONN and maintain this state for at least tSRCDisconnect.

6.3.5.5.1 Entry to Force Detach

The plug enters ***Force Detach*** (S4) upon receipt of a "MSG_Cable_Config"" message from Plug-A.

6.3.5.5.2 Exit from Force Detach

The plug transitions to ***Detached*** (S0) upon exit from ***Force Detach***.

6.3.5.6 Send Repeated Cable Config (S5)

The plug repeatedly sends "MSG_Cable_Config" messages in this state to inform Plug-A of the configuration of the local attached port.

6.3.5.6.1 Entry to Send Repeated Cable Config

The plug enters ***Repeated Cable Config*** (S5) upon receipt of a "MSG_Cable_Config" message from Plug-A.

6.3.5.6.2 Exit from Send Repeated Cable Config

The plug transitions to ***Phase 3 PD Contract*** (S6) upon receipt of a "Release SourceCap GoodCRC" message from the Plug-A port.

6.3.5.7 Phase 3 PD Contract (S6)

The plug performs the following actions in this state:

1. Send a GoodCRC in response to a Source Capabilities message from the local attached port.
2. Evaluate the attached local attached port's DRD Capability (as indicated in the Source Capabilities message).
3. Send the initial RDO (5 V/0 A) in response to the Source Capabilities message and negotiate an explicit power contract.

6.3.5.7.1 Entry to Phase 3 PD Contract

The plug enters ***Phase 3 PD Contract*** upon receipt of a "Release SourceCap GoodCRC" message from Plug-A.

6.3.5.7.2 Exit from Phase 3 PD Contract

The plug transitions to:

- ***Final System Configuration Verification*** (S10) for final system verification upon determination Plug-A is acting as a DFP and it is acting as a UFP, or
- ***Phase 3 DR Swap*** (S8) upon determination Plug-A is acting as a UFP and it is acting as a DFP.

6.3.5.8 Error – USB2 Billboard (S7)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: A DFP only device connected to one of the plugs."

6.3.5.8.1 Entry to Error – USB2 Billboard

The plug transitions to this state upon rejection of a DR_Swap by the local attached port.

6.3.5.8.2 Exit from Error – USB2 Billboard

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.5.9 Phase 3 DR Swap State (S8)

The plug issues a DR_Swap with its local attached port in this state.

6.3.5.9.1 Entry to Phase 3 DR Swap

The plug enters ***Phase 3 DR Swap*** upon determination Plug-A is connected as a UFP and Plug-B should connect as a DFP.

6.3.5.9.2 Exit from Phase 3 DR Swap

The plug shall transition to:

- ***Final System Configuration Verification*** (S10) for final system verification after successful completion of the DR_Swap with the local attached port, or
- ***Error – USB2 Billboard*** (S7) after unsuccessful completion of the DR_Swap with the local attached port.

6.3.5.10 Error – USB2 Billboard + Complete RESET (S9)

The plug presents a Billboard indicating an Invalid Configuration is present. For example: "Error: An invalid configuration occurred. Full link will be reset."

6.3.5.10.1 Entry to Error – USB2 Billboard + Complete RESET

On entry ***Error – USB2 Billboard + Complete RESET***, the plug shall:

1. Present a USB2 Billboard message.
2. Send Hard_Reset to the Local Plug.

6.3.5.10.2 Exit from Error – USB2 Billboard + Complete RESET

The only means of exiting this Error state, is either from a Reset that disconnects VCONN power or a disconnect event which also disconnects VCONN power.

6.3.5.10.3 WatchDog Timer Entry

A watchdog timer should be implemented for internal cable messages that require a response. The watchdog timer will also provide an entry to an ***Error State*** (M13) if the far end plug is unresponsive for any reason.

There are a few states where the watchdog timer shall NOT be implemented including but not limited to S5, where the reboot sequence can take a few seconds.

6.3.5.11 Final System Configuration Verification (S10)

The ***Final System Configuration Verification*** is used to one final check there were no unforeseen changes the local port and the final cable configuration defined by Plug-A.

6.3.5.11.1 Entry to Final System Configuration Verification

The OIAC plug shall check all values in the MSG_Cable_Config match that of the current local port's configuration.

6.3.5.11.2 Exit from Final System Configuration Verification

The plug shall transition to:

- ***Rx.Detect***, and start far-end receiver termination detection and the *USB 3.2* RTSSM State Machine after a successful match of the MSG_Cable_Config and the local port's configuration, or
- ***Error – USB2 Billboard + Complete RESET*** (State S9) after unsuccessful match of the MSG_Cable_Config and the local port's configuration.

6.4 Active Cable Power Requirements

6.4.1 VBUS Requirements

Short active cables shall meet the limits of the IR Drop on VBUS and ground defined in Section 4.4.1.

Short active cables shall provide VBUS and support at least 3 A and optionally 5 A current.

6.4.2 OIAC VBUS Requirements

The OIAC cable plugs have two power contracts. The first contract is defined at first connection of the cable. The second contract is after the data role establishment in the Active state.

6.4.2.1 OIAC VBUS Requirements on Initial Connection

The OIAC cable plugs shall negotiate a power contract with their plug partners as defined in this section on Initial Connection. The *USB PD* Sink Capabilities PDO presented by the OIAC cable plug (SOP) on Initial Connection is defined in Table 6-10. The Sink RDO (SOP) before data role establishment is defined in Table 6-11.

The OIAC cable plug (SOP) shall wait tTypeCSinkWaitCap after VBUS is presented before issuing a Hard Reset to restart sending of the Source_Capabilities.

Table 6-10 OIAC Sink_Capabilities PDO (SOP) on Initial Connection

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	X	USB Communications Capable – Don't care
B25	X	Dual-Role Data – Don't care
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	0001100100b	5V in 50mV units
B9..0	Design defined	Operational current in 10mA units

Table 6-11 OIAC Sink_Capabilities_Extended PDO (SOP) on Initial Connection

Offset	Field	Size	Value	Description
0	VID	2	Numeric	Vendor ID (assigned by the USB-IF)
2	PID	2	Numeric	Product ID (assigned by the manufacturer)
4	XID	4	Numeric	Value provided by the USB-IF assigned to the product
8	FW Version	1	Numeric	Firmware version number
9	HW Version	1	Numeric	Hardware version number
10	SKEDB Version	1	Numeric	SKEDB Version (not the specification Version): Version 1.0 = 1 Values 0 and 2-255 are Reserved and shall not be used.
11	Load Step	1	Bit Field	0x00
12	Sink Load Characteristics	2	Bit field	0x00
14	Compliance	1	Bit Field	0x00
15	Touch Temp	1	Value	0
16	Battery Info	1	Byte	0x00
17	Sink Modes	1	Bit field	0x00
18	Sink Minimum PDP	1	Byte	0x00
19	Sink Operational PDP	1	Byte	0x00
20	Sink Maximum PDP	1	Byte	0x00

Table 6-12 OIAC Sink RDO (SOP) on Initial Connection

Bit(s)	Value	Parameter
B31	0b	Reserved
B20..28	001b	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	No USB Suspend
B23	0b	Unchunked Extended Messages Not Supported
B22..20	000b	Reserved
B19..10	0	Operating Current in 10 mA units
B9..0	0	Maximum current in 10 mA units

6.4.3 USB PD Rules in Active State

The OIAC cable plugs shall negotiate a power contract with their plug partners as defined in this section in the Active State. The OIAC shall follow the message applicability rules defined in Table 6-4 until entry to the Active State.

The minimum USB PD Sink Capabilities PDO presented by the OIAC cable plug (SOP) is defined in Table 6-13. The OIAC may request additional Sink Capabilities (higher voltages and currents) for performance optimization. The minimum Sink RDO is provided as an example in Table 6-14. The OIAC shall function when receiving the minimum Source PDO.

The OIAC cable plug (SOP) shall wait tTypeCSinkWaitCap after VBUS is presented before issuing a Hard Reset to restart sending of the Source_Capabilities

Table 6-13 OIAC Active Sink RDO (SOP)

Bit(s)	Value	Parameter
B31	0b	Reserved
B20..28	As required	Object Position
B27	0b	No GiveBack flag
B26	0b	No Capabilities Mismatch
B25	1b	USB Communication Capable
B24	1b	USB Suspend
B23	As reported from remote end	Unchunked Extended Messages
B22..20	000b	Reserved
B19..10	Design Defined	Operating Current in 10 mA units[1]
B9..0	Design Defined	Maximum current in 10 mA units[1]

Note 1: Thermal design must be considered.

Table 6-14 OIAC Sink_Capabilities PDO (SOP) in Active

Bit(s)	Value	Parameter
B31..30	00b	Fixed Supply
B29	0b	Not Dual-Role Power
B28	0b	Not higher capability
B27	0b	Not unconstrained power
B26	1b	USB Communications Capable
B25	As reported from Remote End	Dual-Role Data[1]
B24..23	00b	Fast Role Swap not supported
B22..20	000b	Reserved
B19..10	0001100100b	5 V in 50 mV units
B9..0	Design defined	Operational current in 10 mA units[2]

Notes: 1. Reflection of far side connection; 2. Thermal design must be considered.

6.4.4 VCONN Requirements

Active Cables shall:

- Meet the VCONN sink requirement defined in Table 4-6, Table 6-20 and Table 6-30.
- Connect VCONN as shown in Figure 6-1, Figure 6-2 or Figure 6-3.

Active cables shall meet the VCONN requirements specified in Section 4.9.

6.5 Mechanical

All active cables shall meet the mechanical requirements defined in the Section 3.8.

6.5.1 Thermal

6.5.1.1 Thermal Shutdown

All active cables shall implement a temperature sensor and place the *USB 3.2* signals in the eSS.Disabled state when the plug skin temperature reaches the maximum defined in Table 6-15. Active cables shall indicate they are in thermal shutdown if queried via the *USB PD* ***Get_Status*** command.

OIACs shall billboard in shutdown. For example: "Error: The Optical Cable has experienced a thermal shutdown."

The Thermal Shutdown is cleared by the following events:

- Disconnect
- *USB PD* Hard Reset

6.5.1.2 Maximum Skin Temperature

Active cable plug's skin temperature shall not exceed a maximum operating temperature of 30 °C above the ambient temperature for a plastic/rubber housing and 15 °C for a metal housing in any operating mode.

6.5.1.3 Thermal Reporting

Active cables shall implement reporting their maximum internal operating temperature in the *USB PD* ***Discover_ID*** Command. Active cables shall implement reporting their current internal operating temperature in the *USB PD* ***Get_Status*** Command on SOP' and SOP" when supported. Active cables shall update their reported Internal Temperature at least every 500 ms.

The plug's Internal Temperature is reported in °C and shall be monotonic. It is not the plug's skin temperature, but cable manufacturers shall correlate the maximum internal operating temperature with the maximum plug skin temperature to ensure shutdown when the maximum plug skin temperature is reached.

Sources and/or Sinks may take action to reduce VBUS current to reduce the cable plug internal operating temperature to below the reported maximum operating temperature. It is recommended Sources and/or Sinks poll the plug's Internal Temperature every 2 seconds.

Table 6-15 Cable Temperature Requirements

Temperature Requirements	
Maximum Internal to Skin Temperature Offset	Design Specific
Maximum Internal Operating Temperature	Design Specific
Maximum Skin Temperature Plastic/Rubber[1]	80 °C
Maximum Skin Temperature Metal[1]	55 °C

Note 1: IEC 60950-1 reduced by 5 °C

6.5.2 Plug Spacing

Active cables will support the USB Type-C vertical and horizontal spacing defined Section 3.10.2 when functioning in *USB 3.2* x1 operation. However, this spacing may impose thermal constraints. Appendix D provides system design guidance to minimize the thermal impact due to connector spacing. It is recommended that products designed for *USB 3.2* x2 operation with multiple adjacent USB Type-C connectors follow the design guidance in Appendix D to minimize the likelihood the active cable will go into thermal shutdown.

6.6 Electrical Requirements

6.6.1 Shielding Effectiveness Requirement

All active cables shall meet the shielding effectiveness requirement defined in Section 3.7.7 and Figure 3-65.

6.6.2 Low Speed Signal Requirement

6.6.2.1 CC Channel Requirements

Active cables shall meet the Low-Speed Signal Requirements in Section 3.7.2.4.

6.6.2.2 SBU Requirements

6.6.2.2.1 Short Active Cables

Short active cables SBU wires shall meet the requirements defined in Table 6-16 and shall meet the crosstalk requirements both near-end and far-end between the low speed signals as defined in Section 3.7.2.4.

SBUs have no guaranteed performance when Vconn is not provided to the cable. The Host or Device shall not provide any signal beyond what is defined in Table 6-16 when VCONN has not been provided.

Table 6-16 Summary of Active Cable Features

Name	Description	Min	Max	Units
zCable_SBU	Cable characteristic impedance on the SBU wires	32	53	Ω
tCableDelay_SBU	Cable propagation delay on the SBU wire		26	ns
rCable_SBU	DC resistance of SBU wires in the cable in USB		40	Ω
vCable_SBU	Cable voltage swing on SBU wires	−0.3	4.0	V
Insertion Loss[1]	Cable insertion Loss		5 @ 0.5 MHz 7 @ 1 MHz 12 @ 10 MHz 13 @ 25 MHz 15 @ 50 MHz 16 @ 100 MHz	dB
iCableSBU	Maximum end-to-end current	−25	+25	mA

Note 1: Measurement referenced to 50 Ohms.

6.6.2.2.2 Optically Isolated Cables

OIACs are not required to support SBU1/2 for *USB 3.2* support. SBUs are not usable until the cable has entered an Alternate Mode. OIACs which choose to support SBU signals shall meet the requirements of the Alternate Mode(s) they support. Definition of the SBU requirements for Alternate Modes is outside the scope of this document.

6.6.3 USB 2.0

The *USB 2.0* support depends on the type of active cable.

6.6.3.1 Short Active Cables

Short active cables shall meet the *USB 2.0* requirements defined in Section 3.7.2.4 and 3.7.2.7.

Note: Active Cables greater than 5m report the number of hub hops consumed in the Active Cable VDOs.

6.6.3.2 Optically Isolated Active Cables

OIACs forward *USB 3.2* and do not forward *USB 2.0*. The OIAC will take action to reset the link when the USB Device drops from *USB 3.2* to *USB 2.0*.

During the initial connection the OIAC shall present as a *USB 2.0* DFP and provide a 15K Ohm pull down on the D+/D− pins on both ends of the cable. The cable plug shall not issue a *USB 2.0* Reset in this state.

The OIAC cable plug shall issue a *USB 2.0* Reset upon detecting a *USB 2.0* connection on D+/D− (LS, FS, or HS *USB 2.0* connection). The cable plug shall issue a *USB 2.0* Bus Reset by pulling D+ and D− low for at least 50 ms.

The OIAC shall implement a tDisableCount counter to determine how many times the cable has transitioned from *USB 3.2* to *USB 2.0*. The tDisableCount counter shall be reset to zero on either condition:

- Power on Reset of the OIAC, or
- Successful transition to *USB 3.2* U0.

The OIAC shall present and latch a USB 2.0 billboard when tDisableCount counter reaches three.

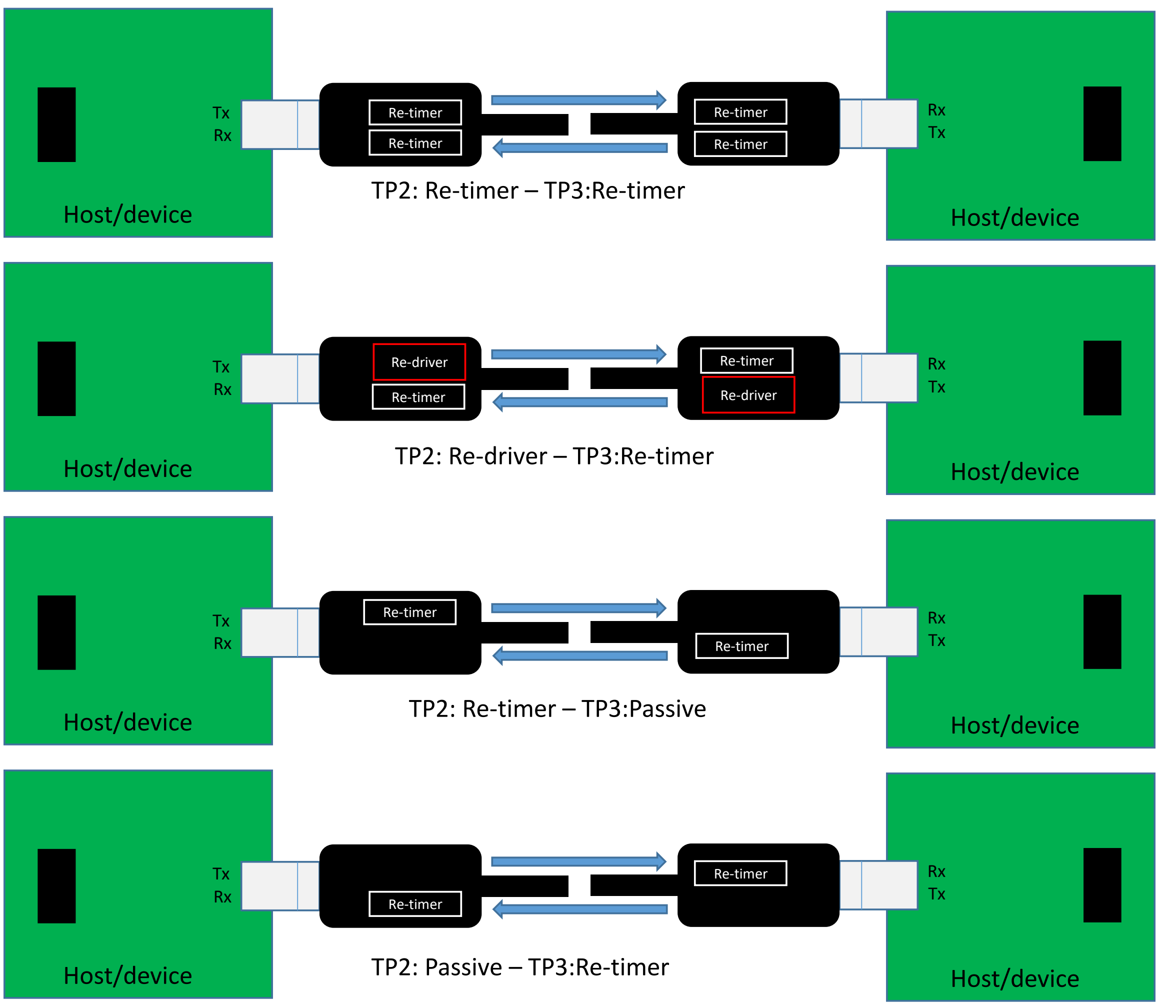
6.6.4 USB 3.2

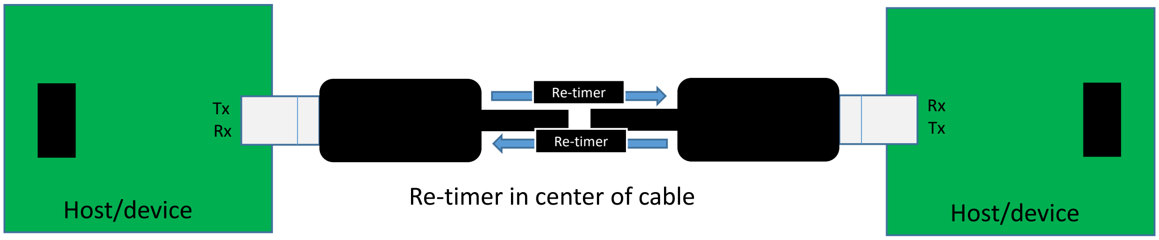
Active cables shall meet the requirements in this section regardless of length. Active cables shall incorporate AC-coupling from the plug to repeater on both the USB 3.2 TX and RX signals. Active cables shall provide a discharge path for discharging the AC-coupling capacitors in the cable on unplug per USB 3.2.

6.6.4.1 USB 3.2 Active Cable Architectures

Active cables may have the combinations of re-timers and re-drivers as illustrated in Figure 6-18. Active cables without at least one re-timer are out of scope. Active cables without re-timers connected to TP3 are out of scope. Active cables shall support the features defined in Table 6-2.

Figure 6-18 Active Cable Topologies





6.6.4.2 USB 3.2 Power-on and Rx.Detect

Active cables shall present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ when not powered. Active cables shall present a high impedance to ground of $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ at initial power-on. The active cable shall perform far-end receiver termination detection on both cable ends upon receiving V_{CONN}. Upon detecting a far-end low-impedance receiver termination ($R_{RX\text{-}DC}$), the active cable shall enable its low-impedance receiver termination ($R_{RX\text{-}DC}$) to mirror the presence of the Host/Device. The active cable shall perform far-end receiver termination detection for Repeaters per *USB 3.2* including in low power states U2/U3.

An active cable shall complete power-on and far-end receiver termination detection through the cable within $t_{FWD\_RX.DETECT}$.

Table 6-17 Active Cable Power-on Requirements

Name	Minimum	Maximum	Units
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$	Per *USB 3.2*	Per *USB 3.2*	
$R_{RX\text{-}DC}$	Per *USB 3.2*	Per *USB 3.2*	
$t_{FWD\_RX.DETECT}$		42[1]	Ms

Note 1: 84 ms – (2 * 12 ms + 18 ms) worst case.

Active cables including OIACs shall reflect the receiver terminations across the cable to replicate the behavior of a passive cable.

6.6.4.3 USB 3.2 U0 Delay

All active cables shall meet the *USB 3.2* delay defined in Table 6-18.

Table 6-18 OIAC Maximum USB 3.2 U0 Delay

USB 3.2 Gen	Cable Maximum U0 Delay	Description
Gen1	3000 ns	Active cables with USB 3.2 Gen1 latency larger than 125 ns may not function correctly when used in conjunction with host, devices, and hubs which do not support the extended timers required in the USB 3.1 Specification Revision 1.0 (July 26, 2013) and USB 3.1 Pending_HP_Timer ECN.
Gen2	3000 ns	Active cables with USB 3.2 Gen2 latency larger than 305 ns may not function correctly when used in conjunction with host, devices, and hubs which do not support the extended timers required in the USB 3.1 Specification Revision 1.0 (July 26, 2013) and USB 3.1 Pending_HP_Timer ECN.

6.6.4.3.1 OIAC Legacy Adapter

Table 6-19 defines the all scenarios in which an OIAC will not function without an OIAC legacy adapter between the OIAC and the Legacy Device, Hub, or Host.

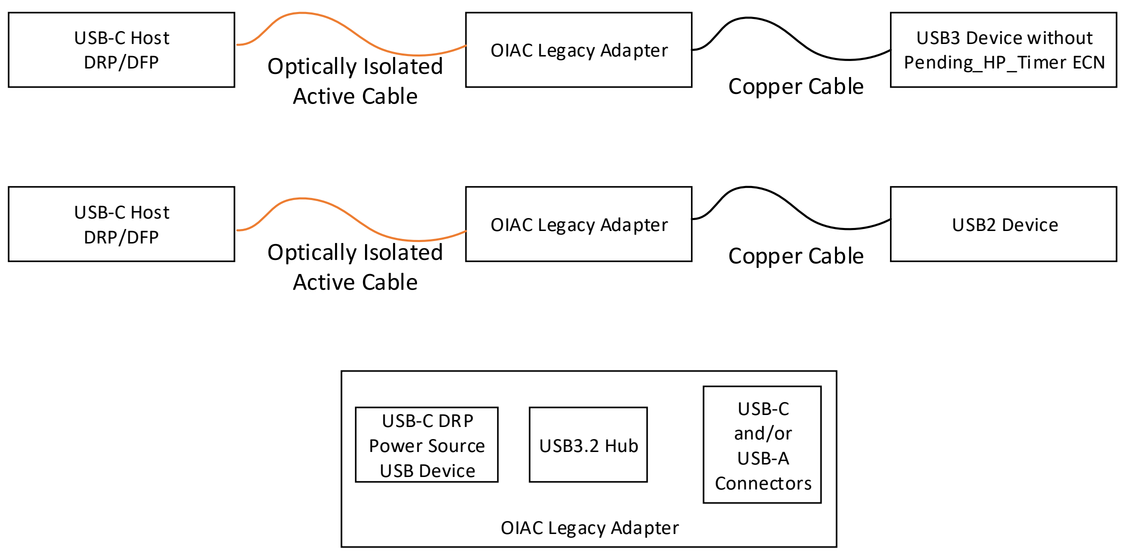
The OIAC Adapter requires the following capabilities:

1. USB Type-C DRP/Source on the upward facing port connected to the OIAC,
2. USB PD on the upward facing port connected to the OIAC,
3. USB 3.2 Hub incorporating the Pending_HP_Timer ECN, and
4. Optional: USB 2.0 to USB 3.2 transaction translator on the downstream facing port (only needed if connecting to USB 2.0-only devices, hubs, or hosts).

Table 6-19 Usages for OIAC That Require an Adapter or Hub

USB Device, Hub, or Host Scenarios which require an OIAC Adapter					
Connector	**Power Role**	**Data Role**	**USB PD**	**USB 3.2 Generation**	**USB 2.0**
USB Type-C	Sink only	–	–	–	–
	–	UFP only	–	–	–
	DRP	UFP only DRD	No USB PD	–	–
			USB PD R2/R3	USB 3.2 without the Pending_HP_Timer ECN	–
			–	–	USB 2.0 only
Any non-USB Type-C	–	–	–	–	–

Figure 6-19 Illustrations of Usages for OIAC That Require an Adapter or Hub



6.6.4.4 USB 3.2 U-State Power Requirements

Active cables shall meet the VCONN power requirements for USB 3.2 operation in Table 6-20. These requirements are for the entire cable not just a cable plug.

Table 6-20 USB 3.2 U-State Requirements

State	Maximum Power Consumption VCONN	Power Consumption Notes
U0	1.0 W single-lane 1.5 W dual-lane	Applies to POLLING.LFPS, TRAINING, and RECOVERY states.
U1	≤ U0 power	Forwarding LFPS is required
U2	≤ U1 power	Forwarding LFPS is required
U3	20 mW	Steady state power. eMarker in sleep.
Rx.Detect	20 mW	Rx.Detect period may be lengthened when no USB 3.2 terminations have been detected. eMarker in sleep.
eSS.Disabled	20 mW	USB 3.2 is disabled. eMarker in sleep.

Note: U3, Rx.Detect, and eSS.Disabled Power requirements are not applicable to OIAC cables.

6.6.4.5 USB 3.2 U-State Exit Latency

Active cables shall meet the U-state exit latency defined in USB 3.2 Appendix E.

6.6.4.6 USB 3.2 Signal Swing

An active cable transmitter only has to drive 8.5 dB insertion loss at 5 GHz to the Host/Device controller receiver for USB 3.2 Gen2, if the transmitter is located in the cable plug next to the receiving port.

A Host/Device controller transmitter must drive a total loss of 23 dB at 5 GHz to the far side for USB 3.2 Gen2. The difference in loss budget allows the active cable transmitter swing to be reduced. An active cable receiver can assume a larger receiver swing than in the Host/Device for the same reason.

Figure 6-20 defines the SuperSpeed electrical test points and is copied from the USB 3.2 specification. Figure 6-21 indicates the test points and test equipment connections.

Figure 6-20 SuperSpeed USB Electrical Test Points

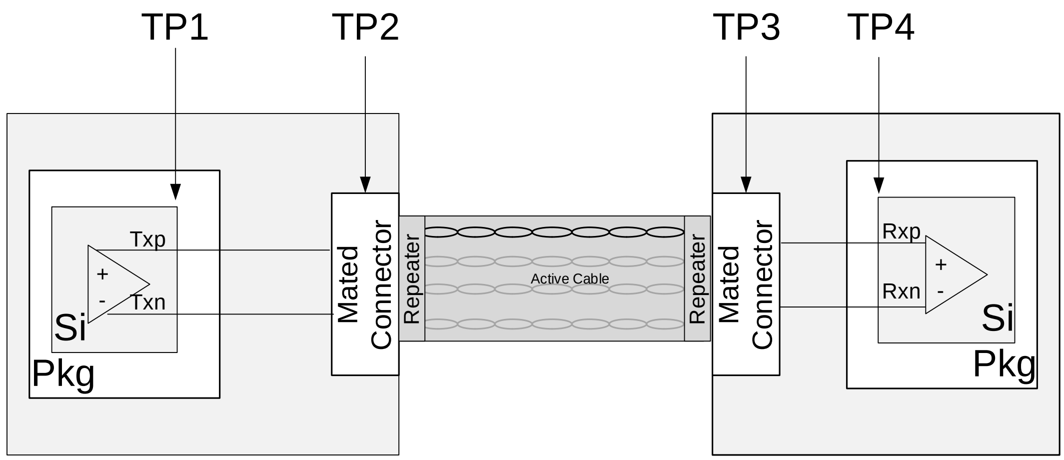
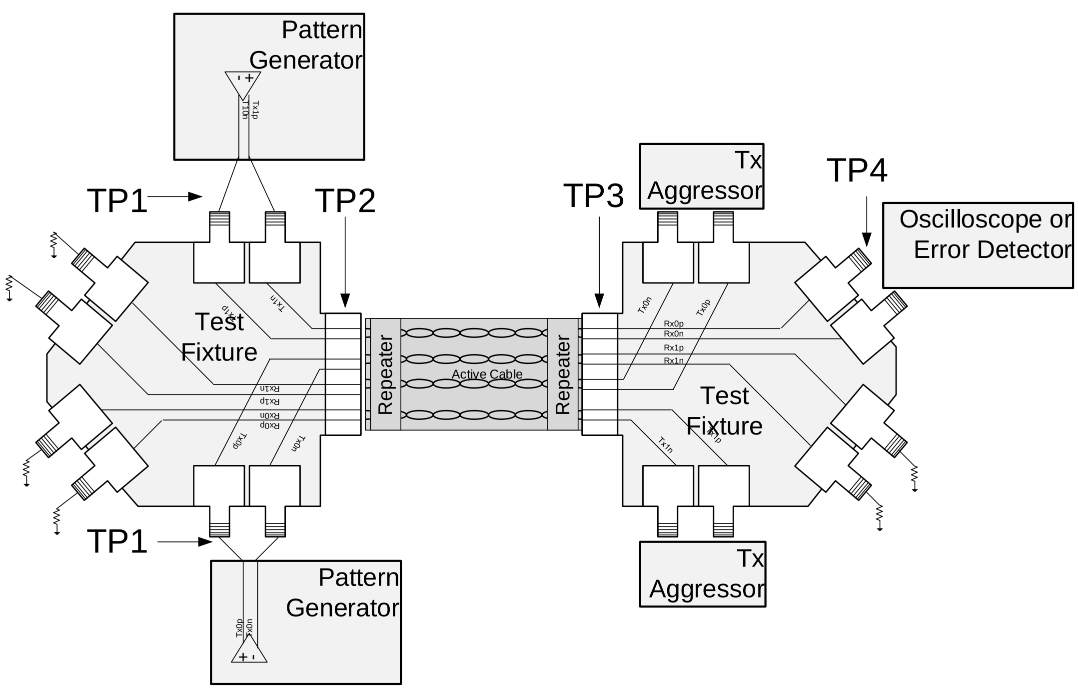


Figure 6-21 SuperSpeed USB Compliance Test Setup



6.6.4.6.1 TP1 – Active Cable Input Stressed Source

The active cable input stressed source is generated at TP1 per Table 6-21 for amplitude and per Table 6-22 for jitter. SSC shall be present in the stressed signal at TP1. Table 6-21 is a subset of the USB 3.2 Table 6-18. Table 6-22 is a subset of USB 3.2 Table 6-28. If any discrepancy exists between this specification and the USB 3.2 specification, the USB 3.2 specification shall take precedence.

The maximum swing with the maximum de-emphasis and pre-shoot shall be tested with the minimum loss compliance test board. The minimum swing with the minimum de-emphasis and pre-shoot shall be tested with the maximum loss compliance test board. The input jitter composition is the same for both the minimum and maximum swing stressed sources.

The active cable shall function over the range of parameter in USB 3.2 Table 6-17 and Table 6-21.

Table 6-21 Active Cable USB 3.2 Stressed Source Swing, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX-DIFF-PP}$	Differential p-p TX voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DE-RATIO}$	TX de-emphasis	USB 3.2 Table 6-17	−3.1 ± 1.0	dB	Nominal is 3.5 dB for Gen1 operation. Gen2 transmitter equalization requirements are described in USB 3.2 Section 6.7.5.2.
$V_{PRESHOOT}$	TX Preshoot	USB 3.2 Table 6-17	2.2 ± 1.0	dB	Gen2 transmitter equalization requirements are described in USB 3.2 Section 6.7.5.2.

Table 6-22 Active Cable USB 3.2 Stressed Source Jitter, TP1

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms	1
J_{Rj_p-p}	Random Jitter peak-peak at 10^{-12}	0.17	0.14	UI p-p	1,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1Mhz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3

Notes:

1. All parameters measured at TP1. The test point is shown in Figure 6-20 and Figure 6-21.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the RX is required to tolerate Pj at all frequencies between the compliance test points.
3. During the RX tolerance test, SSC is generated by test equipment and present at all times. Each JPj source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the RX tolerance test.
5. The JTOL specs for Gen2 comprehend jitter peaking with re-timers in the system and has a 25 dB/decade slope.

6.6.4.6.2 TP2 – Active Cable Input (Informative)

The values in Table 6-23 indicate the informative input signal swings at TP2 for an active cable. Table 6-23 is included to provide guidance beyond the normative requirements of Table 6-21 and Table 6-22. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-23. Similarly, an active cable that meets all the values in Table 6-23, is not guaranteed to be in fully compliance with the normative part of this specification.

Table 6-23 Active Cable USB 3.2 Input Swing at TP2 (Informative)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential p-p TX voltage swing	250 (min) 1000 (max)	250 (min) 850 (max)	mV	Nominal is 550 mV p-p
$V_{TX\text{-}DE\text{-}RATIO}$	TX de-emphasis	0 (min) 4.0 (max)	2.1 (min) 4.1 (max)	dB	There is no de-emphasis requirement for Gen1.
$V_{PRESHOOT}$	TX Preshoot	NA	1.2 (min) 3.2 (max)	dB	Applicable to USB 3.2 Gen2 operation only.

6.6.4.6.3 TP3 – Active Cable Output (Informative)

The values in Table 6-24 indicate the informative output signal swings at TP3 for an active cable. Table 6-24 is included to provide guidance beyond the normative requirements of Table 6-21 and Table 6-22. An active cable can be fully compliant with the normative requirements of this specification and not meet all the values in Table 6-24. Similarly, an active cable that meets all the values in Table 6-24, is not guaranteed to be in full compliance with the normative part of this specification.

Table 6-24 Active Cable USB 3.2 Output Swing at TP3 (Informative)

Symbol	Parameter	Gen1 (5.0 GT/s)	Gen2 (10 GT/s)	Units	Comments
$V_{TX\text{-}DIFF\text{-}PP}$	Differential RX peak-to-peak voltage	300 (min) 850 (max)	300 (min) 850 (max)	mV	Measured after the RX EQ function Nominal is 0.5 V p-p
$V_{TX\text{-}DE\text{-}RATIO\text{-}GEN1}$	TX de-emphasis	0 (min) 4.0 (max)	NA	dB	No pre-shoot allowed
$V_{TX\text{-}DE\text{-}RATIO}$ + $V_{PRESHOOT\text{-}GEN2}$	TX de-emphasis + TX Preshoot	NA	0 (min) 3.0 (max)	dB	Sum of the de-emphasis and pre-shoot. There is no de-emphasis and pre-shoot requirement.

6.6.4.6.4 TP4 – Active Cable Output

The active cable transmitter output is defined at TP4 for both high and low loss channels. The requirements for TP4 are defined in the USB 3.2 specification Table 6-20. The input signal for the test shall be applied at TP1 as defined in the USB 3.2 specification.

The low loss test board shall be used to test the maximum output swing. The maximum loss test board shall be used to test the minimum output swing. Jitter must be met with both test boards.

The active cable bit-error-rate shall be tested at TP4 and meet or exceed a BER of 10^{-12}. The error detector used shall have the ability to remove SKP ordered sets.

6.6.5 USB4

This section describes the electrical requirements and compliance testing for *USB4* active cables. The compliance testing is defined to ensure interoperability in terms of data integrity and electrical specifications enabling the active cable to reliably receive an input signal and output a valid signal at its other end.

The *USB4* active cable types are:

1. Re-timer-based active cable (this section covers re-timer based cable for *USB4* only, *USB 3.2* re-timer cable is defined in Section 6.6.4)
2. Linear re-driver-based (LRD-based) active cable (*USB 3.2* and *USB4*)
3. Linear optical active cable
   (electrical spec not defined yet)

6.6.5.1 Electrical Requirements That Apply to All Active Cable Types

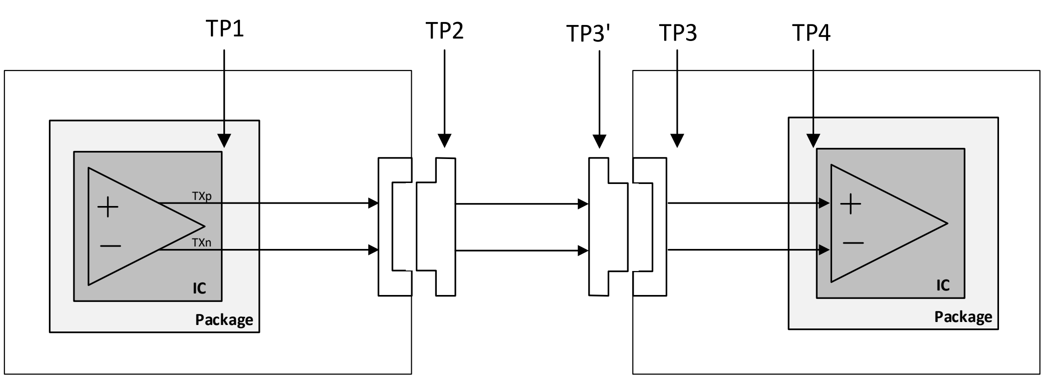
6.6.5.1.1 System Compliance Test Point Definition

All measurements shall be referenced to the following compliance points. Calibration shall be applied in cases where direct measurement is not feasible.

Table 6-25 Compliance Points Definition

Test Point	Description	Comments
TP1	Transmitter IC output	Not used for electrical testing
TP2	Transmitter port connector output	Measured at the plug side of the connector
TP3	Receiver port connector output	Measured at the receptacle side of the connector. All the measurements at this point shall be done while applying reference equalization function
TP3'	Receiver port connector input	Measured at the plug side of the connector
TP4	Receiver IC input	Not used for electrical testing

Figure 6-22 Compliance Points Definition



6.6.5.1.2 Compliance Receptacle Test Boards

The USB Type-C high speed test fixture shall be used to enable cable compliance testing. The fixture shall be comprised of a high-quality USB Type-C receptacle and a short PCB trace that may be connected to coaxial cable with SMA/SMP connector at its end. Because TP2 and TP3' reference points are located on the USB Type-C plug side of the connector, the loss and distortion of the receptacle fixture shall be calibrated such that all the measured values correspond to the standard reference points. The reference point TP3 is defined such that the insertion-loss from the connector pads to the compliance point is 0.5 dB ± 0.25 dB at 5GHz and 1 dB ± 0.25 dB at 10 GHz. Extra loss and distortion elements shall be compensated by physical and/or mathematical means.

The target impedance of the fixture shall be 85 Ω. AC coupling capacitors shall be placed on the receptacle test fixture following the Router Assembly requirements as specified in *USB4* specification and CTS.

6.6.5.1.3 AC Coupling Capacitors

Active cables shall include AC-coupling capacitance between 135 nF and 265 nF inside their plugs placed at the output transmit path and between 300 nF and 363 nF at the input receive path. Discharge resistors between 200 KΩ and 242 KΩ shall be placed at the input receive path. See Figure 3-3 in the *USB4* specification for a diagram of the AC-coupling capacitors and discharge resistors.

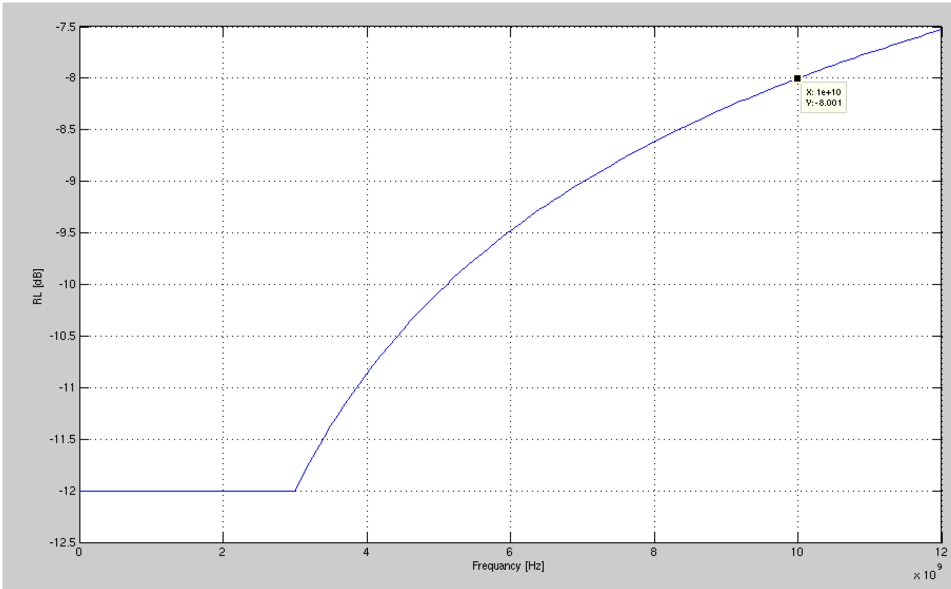
Active cable designs need to consider that a change of current consumption from VBUS as allowed by *USB Power Delivery* can add a considerable amount of common mode offset that may not be handled by the AC-coupling in this spec.

6.6.5.1.4 Differential Return-Loss Mask (Informative)

Re-timer and re-driver cable input and output return-loss measurements shall be referenced to a differential impedance of 85 Ω. When measured at TP3' and TP1 (respectively), the differential mode return loss recommended to not exceed the limits given in the following equation:

$$SDD22(f), SDD11(f) = \begin{cases} -12 & 0.05 < f_{GHz} \leq 3 \\ -7.5 + 7.5 \cdot \log 10\left(\frac{f_{GHz}}{12}\right) & 3 < f_{GHz} \leq 12 \end{cases}$$

Figure 6-23 RX Differential Return-Loss Mask



6.6.5.2 Re-timer-based Active Cable Electrical Specifications

This section describes the electrical requirements and compliance testing for *USB4* re-timer-based active cables.

6.6.5.2.1 Output Equalization

A *USB4* active cable shall implement tunable 3-tap finite-impulse-response (FIR) equalization at its output. The transmit equalization shall support 16 preset configurations with different de-emphasis and pre-shoot settings as specified in the *USB4* specification, and shall be measured at TP3'.

6.6.5.2.2 High-Speed Specifications

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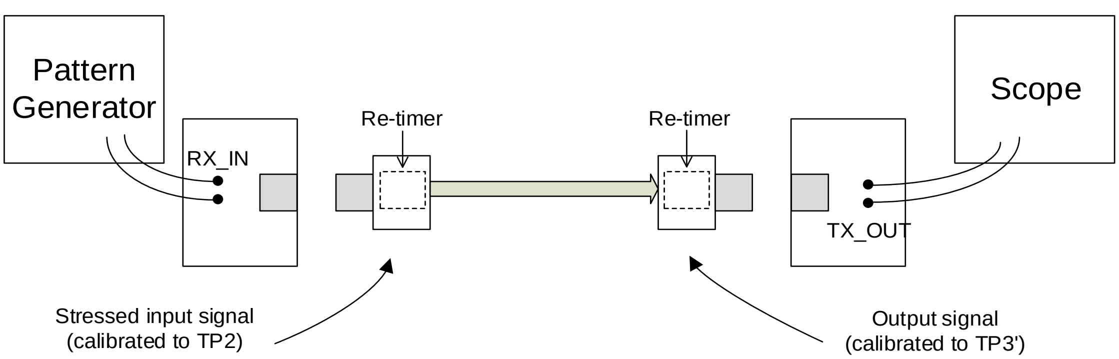
Figure 6-24 Active Cable Compliance Test Setup



6.6.5.2.3 Cable Compliance Testing

Table 6-26 defines the USB4 Active Cable specifications for Gen2 and Gen3 systems at TP3'. These parameters shall be measured at the Active Cable's output while applying a stressed signal at the input as specified in Table 6-27.

A USB4 active cable shall be tested by injecting several different periodic jitter components, one at a time. The test shall include sinusoidal jitter frequencies of 1 MHz, 2 MHz, 10 MHz, 50 MHz, and 100 MHz. In all cases, the incoming signal shall include SSC modulation on top of the sinusoidal jitter component at the range of 300ppm to −5300ppm. PRBS31 pattern shall be used for USB4 active cable compliance testing. However, calibration of the stressed signal source may be performed with a periodic pattern shorter than PRBS31. AC common-mode noise shall be added at the pattern generator output to ensure worst-case transmitter characteristics. The total common-mode noise shall be 100 mV peak-to-peak at TP2, where the added noise profile shall be sinewave at frequency not smaller than 400 MHz. All the specified jitter values shall be calibrated while applying the reference CDR defined in the USB4 specification.

A USB4 active cable receiver may configure its Link Partner's TX equalizer during the Link establishment. The pattern generator shall support tunable 3-tap FIR at its output, which may be adjusted during the test by the receiver under test through out-of-band software channel.

Table 6-26 Re-timer-based USB4 Active Cable Output Specifications Applied for All Speeds (at TP3')

Name	Description	Min	Max	Units	Comments
CABLE_BER	End to End bit error rate		1E−12		See Note 1
AC_CM	Output AC Common Mode Voltage		100	mV pp	
LANE_TO_LANE_SKEW	Cable's Input-to-Output Skew between lanes		18	ns	
NRL	Noise Contributed by Integrated Return Loss				See 6.6.5.2.5
JTF_BW	Jitter tracking (forwarding) 3dB bandwidth from cable input to output		0.5	MHz	See Note 2
JTF_PEAKING	Jitter amplification from cable input to output		0.3	dB	Measured from 0 to 0.5 MHz. See Note 2
SSC_VARIATION	SSC output to input down-spread variation	−0.3	+0.3	dB	See Note 2
SSC_SLEW_RATE	SSC frequency slew rate (df/dt) during steady-state		1250	ppm/µs	See Note 3
INIT_FREQ_VARIATION	Non-modulated transmit frequency accuracy during the initial stages of the training period	−300	+300	ppm	See Notes 4 and 5
DELTA_FREQ_200ns	Transmit frequency variation over 200 ns measurement windows following the switching from local to recovered clock		1400	ppm	See Notes 4 and 5

Name	Description	Min	Max	Units	Comments
DELTA_FREQ_1000ns	Transmit frequency variation over 1 µs measurement windows following the switching from local to recovered clock		2200	ppm	See Notes 4 and 5
V_OUTPUT_DC_AC_CONN	Instantaneous DC+AC voltages at the cable output side of the AC coupling capacitors	−0.5 (min1) −0.3 (min2)	+1.0	V	See Note 6
TJ	Total Jitter		0.32	UI pp	See Notes 7 and 9
UDJ	Deterministic jitter that is uncorrelated to the transmitted data		0.13	UI pp	
UDJ_LF	Low Frequency Uncorrelated Deterministic Jitter		0.06	UI pp	See Note 10
DCD	Deterministic Jitter Associated by Duty-Cycle-Distortion		0.03	UI pp	
Y1	Eye inner height at TP3' (one-sided voltage opening of the differential signal)	200		mV	Measured for 1E6 UI. See Notes 8 and 9, and *USB4* specification.
Y2	Eye outer height at TP3' (one-sided voltage opening of the differential signal)		650	mV	Measured for 1E6 UI. See Notes 8 and 9, and *USB4* specification.

Notes:

1. The cable BER requirement is referred to the raw data, without applying forward error correction nor pre -coding.
2. JTF_BW and JTF_PEAKING characterizes the corresponding input-to-output low-pass Jitter Transfer Function bandwidth and peaking. In addition, it is required that the cable will not change the SSC modulation depth by more than specified. For verifying that, the SSC down-spreading depth of the cable input and output shall be compared.
3. The SSC slew rate shall be extracted from the transmitted signal over measurement intervals of 0.5 µs. The SSC slew-rate shall be extracted from the transmitter phase after applying a 2nd order low-pass filter with 3 dB point at 5 MHz. Steady-state clocking shall be applied from the point that SLOS training pattern is forwarded by the transmitter.
4. As shown in Figure 6-25, the initial transmit frequency is not modulated. The transmit frequency variation following the switching from local to recovered clock shall be measured over time intervals of 200 ns and 1 µs.
5. Measurement shall be performed over the transmitted signal. The signal phase shall be extracted while applying 2nd order low-pass filter with 3 dB point at 5 MHz.
6. The absolute single-ended voltage seen by the receiver. This requirement applies to all link states and during power-on, and power-off. (min1, max) is measured with a 200 KΩ receiver load, and (min2, max) is measured with a 50 Ω receiver load. The ground offset between the cable output and UFP is not included in V_OUTPUT_DC_AC_CONN.
7. TJ is defined as the sum of all "deterministic" components plus 14.7 times the RJ RMS (the transmitter RJ RMS multiplier corresponds to the target BER with some margin on top).
8. The output voltage is differential.
9. Transmit jitter shall be measured while applying the reference CDR described in the *USB4* Specification. Note that the measured jitter includes residual SSC jitter passing the reference CDR.
10. UDJ_LF is the uncorrelated deterministic jitter measured after applying 2nd order Low-Pass-Filter with 3 dB cut-off at 0.5 MHz on the measured jitter. This filter needs to be applied on top of the reference CDR rejection function. The measurement shall be performed while applying input stress signal with periodic jitter component of 100 MHz.

Figure 6-25 Example for Transmitter Frequency Variation During Clock Switching

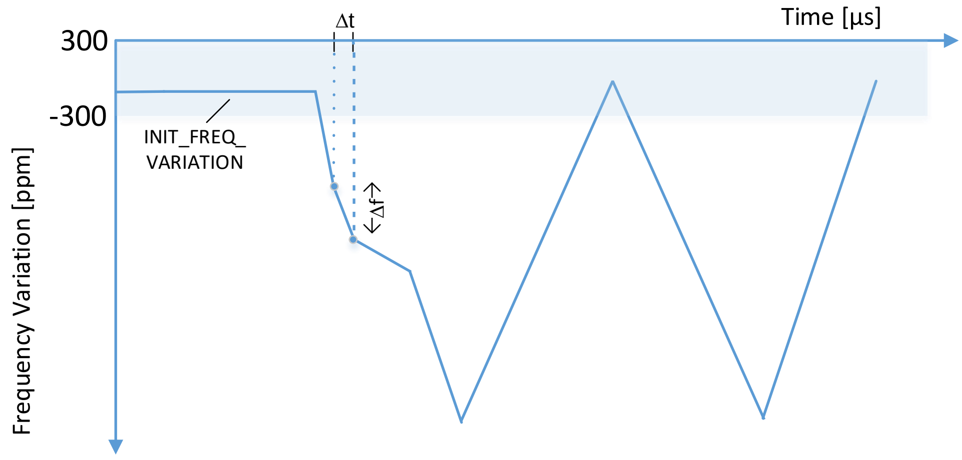
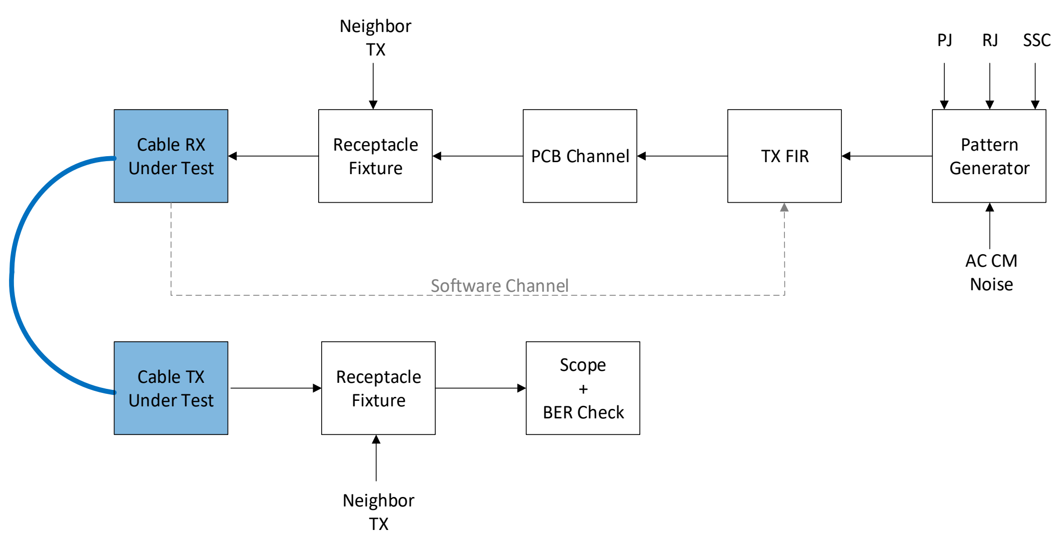


Table 6-27 Stressed Received Conditions for USB4 Gen2 and Gen3 Cable Compliance Testing (at TP2)

USB4 Gen	Inner eye Voltage [mV peak]	Data Dependent Jitter (DDJ) [UI peak-to-peak]	Random Jitter [UI peak-to-peak]	Periodic Jitter [UI peak-to-peak]	Total Jitter [UI peak-to-peak]
Gen2	140	0.12	0.14	0.17	0.43
Gen3	120	0.15	0.14	0.17	0.46

Figure 6-26 Active Cable Functional Test Setup



6.6.5.2.4 Cable Error-Bursts Testing

In order to facilitate proper FEC operation, an active cable receiver shall take steps to limit the probability that a burst of errors is restarted immediately after receiving one or more correct bits (see USB4 specification). The cable receiver under test shall trigger on bit-errors and shall capture error events that follow.

The test setup shall be initialized with the same configuration used for testing the uncoded BER with periodic jitter component of 100 MHz. As part of this setup, PRBS31 pattern is assumed and neither forward-error-correction nor pre-coding are applied. After initialization, the periodic jitter magnitude shall be increased to the point where uncoded BER of 1E−8 is observed. The receiver under test shall trigger on bit-error and shall capture error events that follow. An error event is defined as a mismatch between the received data and the reference PRBS31 pattern. At least 32 consecutive bits shall be examined for errors starting from the initial trigger. The probability for burst renewal shall be 5E−7 or less (i.e. one error burst restart per 2 million error captures).

The following is an example analysis:

No burst restart: captured_data[31:0]=00000000000000000000001111111111

Burst restart: captured_data[31:0]=00000000000000000000111001111111

where '1' represents a bit error and '0' represents a correct bit, as expected from "exclusive or" (XOR) operation between the received bits and the synchronized reference PRBS31 pattern. Captured_data[0] corresponds to the error event trigger.

Note: A burst of errors contains 1 or more consecutive bit errors.

6.6.5.2.5 Noise Contributed by Integrated Return Loss (NRL)

This section will be added in a future ECN.

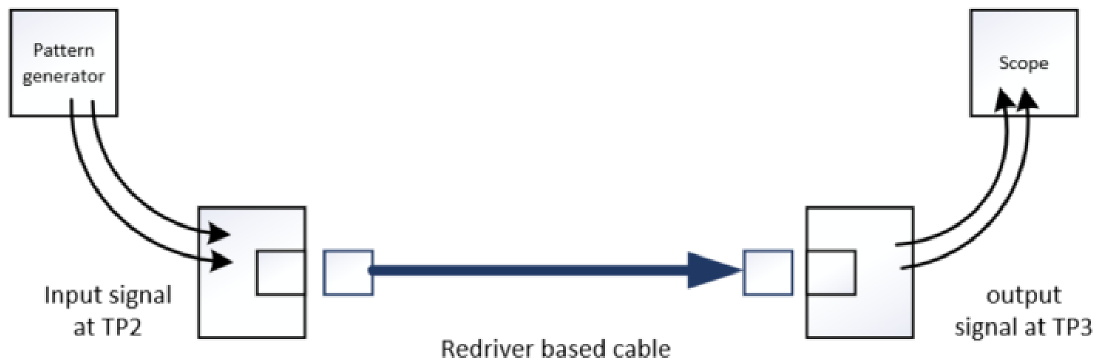
6.6.5.3 Linear Re-driver-based Active Cable Electrical Requirements

Linear re-driver-based (LRD-based) active cables shall be tested as a complete component for compliance.

An LRD-based active cable is expected to receive a reference signal (referenced to TP2) defined in this specification and output a signal at the other end with electrical characterization that meets the requirements (referenced to TP3).

As shown in Figure 6-27, a compliant USB Type-C receptacle shall be connected to both ends of the active cable for injecting and measuring the signal to the corresponding TP2 and TP3 reference points. Details of the Compliance Receptacle and boards can be found in Section 3.3.6 of USB4 Specification.

Figure 6-27 Linear Re-driver-based Active Cable Compliance Setup



Note: The internal placement of the re-driver ICs is purposely not specified to allow full flexibility to the manufacture to develop various re-driver-based solutions.

6.6.5.3.1 General Implementation Notes

This specification was developed considering electrical interoperability with legacy systems, as the LRD-based Active Cables were added to the USB ecosystem in a late phase when a lot of devices were already in the field.

The USB Type-C interconnect ecosystem assumes the worst case 1 m/2 m/0.8 m passive cable is the worst-case connection (for *USB 3.2*, *USB4* Gen2 and *USB4* Gen3 respectively).

The intent is to align the LRD-based Active-Cable specifications to the existing passive cable specifications defined in Chapter 3 of this specification, such that the LRD-based active cable characteristics will be equal or better than those of the worst-case passive cable. The worst-case passive cable is defined in the *USB 3.2* and *USB4* Compliance Test Specification (CTS). This specification will define the electrical characteristics of the LRD-based cable that shall meet this requirement.

The LRD-based active cable specification assumes no change is needed to the existing TX/RX specification of the endpoint PHYs so that compatibility to existing certified *USB 3.2* and *USB4* devices is maintained.

Given this background, the following are assumptions regarding the LRD-based active cable implementation:

1. LRD-based active cable is assumed to have no clock mechanism in its datapath (such as CDR).

2. LRD-based active cable is assumed to not have a dynamic amplitude control (such as AGC) to avoid masking the txffe training from the receiver.

3. LRD-based active cable is assumed to not use the training patterns to train itself, especially it is assumed to not block the output data during any phase of the training period.

4. Receiver systems rely on the low-pass-filter nature of the cable and having an over-equalized cable (i.e. weak LPF characteristic) can lead to interoperability issues. Therefore, it is recommended that when developing an LRD-based active cable, the

cable should be built and tuned in a way that will make it the most passive-cable-like as opposed to most equalized cable.

6.6.5.3.2 USB4 Linear Re-driver-based Active Cable Compliance Testing

Table 6-28 defines the USB4 linear re-driver-based active cable specifications for USB 3.2 and for USB4 Gen2 and Gen3 systems at TP3.

These parameters shall be measured at the LRD-based active cable's output while applying a reference signal at the input as specified in Table 6-29.

An LRD-based active cable shall be tested by injecting several patterns, calibrated to TP2.

Table 6-28 Linear Re-driver-based Active Cable Output Parameters

Symbol	Description	Min	Max	Units	Conditions
$ILfitatDC$	Defining the ILfit mask for the cable response. Note: The main intention is to keep the cable with LPF characteristic similar to the passive cable.	ILfitatNq+1.5	0	dB	See 6.6.5.3.4
$ILfitatf1$		$ILfitatNq$	$ILfitatDC$	dB	See 6.6.5.3.4
$ILfitatNq$		USB 3.2: −6 USB4 Gen2: −12 USB4 Gen3: −7.5	ILfitatDC − 1.5	dB	See 6.6.5.3.4
$ILfitatf2$		$ILfitatNq - 3$	$ILfitatNq$	dB	See 6.6.5.3.4
$ILfitatf3$		$ILfitatf2 - 4$	$ILfitatf2$	dB	See 6.6.5.3.4
$ILfitatWB$	Max gain of the cable in the range of DC to f_N		0	dB	See 6.6.5.3.4
OUTPUT_NOISE	Standard deviation of the cable output noise. Combination of all noises beside the non-linearity noise.	See 6.6.5.3.5		mV	See 6.6.5.3.5
SIGMA_E	Standard deviation of the Non-linearity noise measured in the cable output		15	mV	See 6.6.5.3.6
Operating margin	Receiver margin evaluation	3		dB	See 6.6.5.3.9 normative only for USB4-Gen3
Eye mask	Eye mask in the cable output				See 6.6.5.3.10
CM_NOISE	Common mode noise		100	mV pp	See 6.6.5.3.12
IRL	Integrated Return Loss				See 6.6.5.3.7
IMR	Integrated multi-reflection (integration of ILD (Insertion loss deviation))				See 6.6.5.3.8
OUTPUT_ISI	Managing the response of the cable to be in a certain regular limit				See 6.6.5.3.11

Table 6-29 Input Signal at TP2 for Compliance Testing

Pattern (defined in USB4 Specification 8.3.2.1.1)	Swing (reference to TP2)	Added Jitter	TX Equalization	SSC	Minimum Measurement Time	Usage
PRBS15	800 mV p-p	No	No EQ	No	20 µs	Cable gain, non-linearity noise
PRBS15	USB4: 1300 mV p-p USB 3.2: 1200 mV p-p	No	No EQ	No	20 µs	Non-linearity noise
SQ512	300 mV p-p	No	NoEQ	No	20 µs	Output noise
PRBS31	As defined in USB4 Specification and CTS					Eye mask at TP3

6.6.5.3.3 Measurement Methods

The compliance testing of an LRD-based active cable to this specification will be done based on measurements from both time and frequency domains.

For all time domain specification items, the measured LRD-based active cable parameters will be compared to the worst-case passive cable supported in each technology (with nominal cable length of 1 m for USB 3.2, 2 m for USB4 Gen2 and 0.8 m for USB4 Gen3) measured in the exact same setup to reduce testing complexity.

The worst-case passive cable is defined in the active cable CTS.

More details on the measurement methods can be found in the active cable CTS.

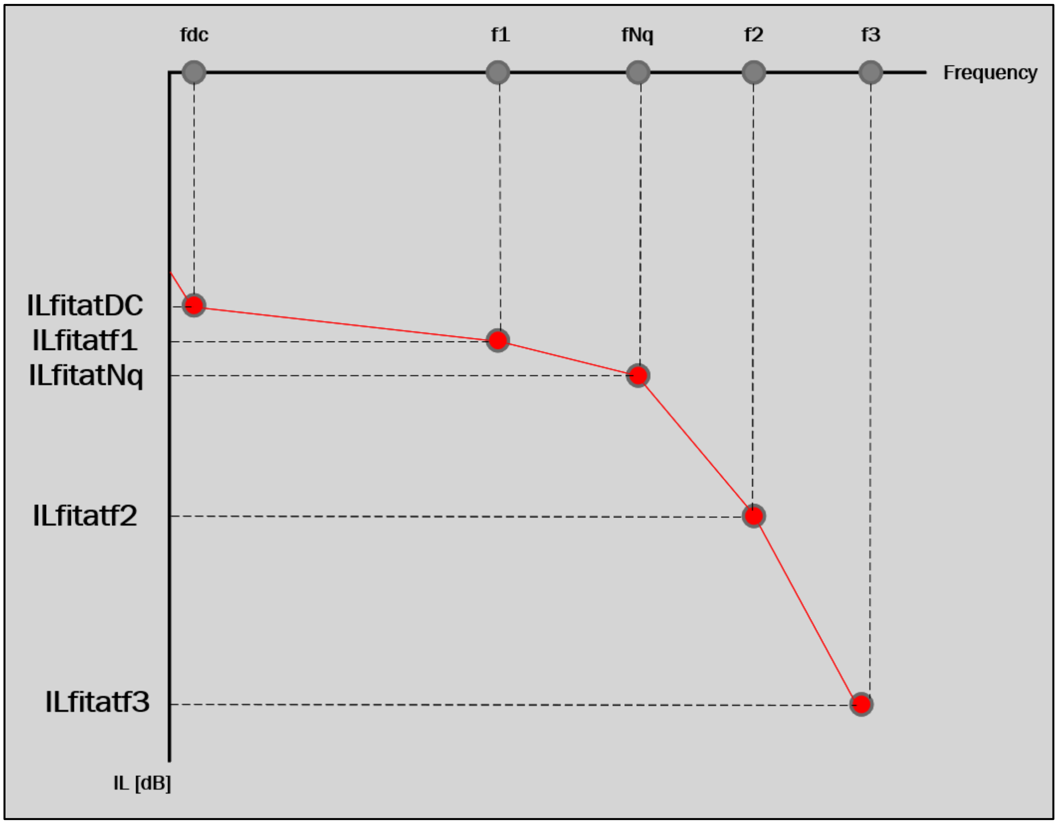
6.6.5.3.4 Cable ILfit Mask (DC/f1/Nq/f2/f3/WB)

Based on the pulse response extraction from the time domain measurements, $(h(n))$ Fourier Transform is used to extract the impulse frequency response $H_{impulse}(f)$. For the specification parameters calculation, a fitted version of $H_{impulse}(f)$ shall be used. The pulse extraction and fitting methods are detailed in the active cable CTS and in Appendix G of this document.

$$ILfitatDC = 20 * \log_{10}(ILfit(DC))$$
$$ILfitatf_1 = 20 * \log_{10}(ILfit(f_1))$$
$$ILfitatf_N = 20 * \log_{10}(ILfit(f_N))$$
$$ILfitatf_2 = 20 * \log_{10}(ILfit(f_2))$$
$$ILfitatf_3 = 20 * \log_{10}(ILfit(f_3))$$
$$ILfitat\text{WB} = \max\left(20 \cdot \log_{10}\left(ILfit(f_0)\right)\right), where\ f_0\ is\ in\ the\ range\ of\ DC\ to\ f_N$$

$$DC = 100\ MHz$$
$$f_1 = f_N * 0.7$$
$$f_2 = f_N * 1.25$$
$$f_3 = f_N * 1.5$$
$$f_N\ for\ USB3.2{:}\ 5\ GHz$$
$$f_N\ for\ USB4\ Gen2{:}\ 5\ GHz$$
$$f_N\ for\ USB4\ Gen3{:}\ 10\ GHz$$

Figure 6-28 Gain Parameters Specified for the Linear Re-driver Active Cable



6.6.5.3.5 OUTPUT_NOISE (σ_n)

σ_n is the standard deviation of the uncorrelated additive noise added to the output signal of the linear re-driver-based active cable.

To achieve an accurate measurement, the calculation will be done based on a low frequency signal (SQ512 pattern) applied to the cable input, with 0.3 Vpp amplitude.

Since the noise calculation is referred to the receiver input, a 2nd order Butterworth LPF filter with −2 dB @ Nq shall be applied on the captured wave to account for the receiver BW and device side platform.

The limit of OUTPUT_NOISE is defined as function of the IL at Nyquist frequency. This allows a degree of freedom to the cable developer to trade between the cable's gain and noise.

The limit is defined as:

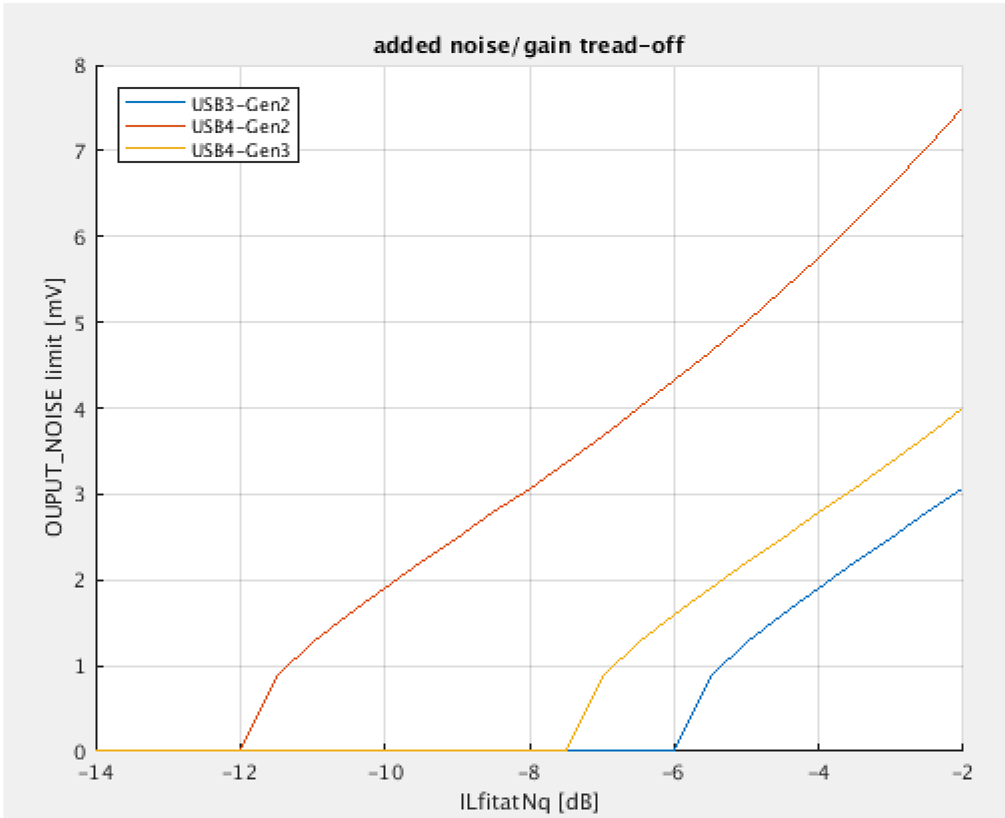
$$\sigma_{cable} \le \sqrt{\frac{\sigma_1^2}{10^{\frac{H(f_N)_{PC}-H(f_N)_{RC}}{10}}} - \sigma_1^2 \cdot \frac{1}{\alpha}}$$

Using the following parameters:

σ_1	2 mV
α	0.9
$H_{PC}(f_N)$	USB 3.2: −6 dB USB4 Gen2: −12 dB USB4 Gen3: −7.5 dB

Figure 6-29 shows a graph of this function for the given parameters.

Figure 6-29 OUTPUT_NOISE Limit Versus *ILfitatNq*



6.6.5.3.6 SIGMA_E (σ_e)

σ_e is the standard deviation of the non-linearity related noise added by the linear re-driver-based active cable.

This measurement shall be performed twice: once with minimum input swing and once with maximum input swing.

Then, $\sigma_e = \max\left(\sigma_{e\,\max swing}, \sigma_{e\,\min swing}\right)$.

where:

$\text{maximum input } swing = 1300mVpp\ (USB4)\ or\ 1200mVpp\ (USB3.2)$
$\text{Minimum } input\ swing = 800mVpp$
$(compatible\ with\ USB\ 3.2/USB4\ specification\ \max swing\ definition)$

More details on the calculation of the non-linearity noise can be found in the Active Cable CTS and in Appendix G of this document.

6.6.5.3.7 Integrated Return-Loss (IRL)

The IRL term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.1.

The IRL limit is different for LRD-based active cables and is given by the following functions:

Mode:	IRL Limit:
USB 3.2 Gen2	$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$
USB4 Gen2	$IRL \leq 0.046 \cdot ILfitatNq^2 + 1.812 \cdot ILfitatNq - 8.784$
USB4 Gen2	$if(-4dB \leq ILfit@Nq):\ IRL \leq -13dB$ $if(ILfit@Nq < -4dB):\ IRL \leq ILfit@Nq - 9$

6.6.5.3.8 Integrated Multi-Reflection (IMR)

The IMR term for an LRD-based active cable is calculated similarly to the passive cable, see 3.7.2.3.2.

The IMR limit is different for LRD-based active cables and is given by the following functions:

Mode:	IRL Limit:
USB 3.2 Gen2	$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 20.392$
USB4 Gen2	$IMR \leq 0.126 \cdot ILfitatNq^2 + 3.024 \cdot ILfitatNq - 20.392$
USB4 Gen2	$if(-4dB \leq ILfit@Nq):\ IMR \leq -29dB$ $if(ILfit@Nq < -4dB):\ IMR \leq 1.741 \cdot ILfit@Nq - 22.143$

6.6.5.3.9 Evaluating Channel Operation Margin (COM)

Channel operating margin (COM) shall be calculated for LRD-based active cables supporting USB4 Gen3, for evaluating a reference receiver margin based on the cable's measured S parameters.

The measurements of the cable and the setting of the associated COM tool is defined in the Active Cable CTS.

6.6.5.3.10 Cable Output Eye Mask

An LRD-based active cable shall meet eye mask limits at its output.

The test setup shall be identical to the USB 3.2 and USB4 calibrated receiver test which includes worst case passive cable.

During the test, a reference CTLE, DFE and TXFFE settings shall be tuned according to the USB 3.2 /USB4 spec for obtaining the optimal eye.

1. USB 3.2 have fixed TXFFE setting according to the USB 3.2 Gen2 TX specification.

2. USB4 can tune the TXFFE according to the TXFFE preset table in USB4 Specification Table 3-5.

After obtaining the optimal eye with the passive cable, repeat the same measurement with the LRD cable under test, and compare the extracted eyes.

The optimal LRD cable eye shall meet these criteria:

$$LRD\ cable\ eye\ area \geq Passive\ cable\ eye\ area$$
AND
$$LRD\ cable\ eye\ width > 0.9 * \ Passive\ cable\ eye\ width$$

Note that the maximum eye height is constrained by the spec item *ILfitatWB* that prevent active amplification over the entire frequency range.

6.6.5.3.11 Cable OUTPUT_ISI

To limit irregularity in the LRD-based active cable due to additional components (IC package etc.), an ISI-Margin test is used to evaluate the regularity of the cable's output. ISI-margin is calculating both pre-cursor and post-cursor side of the pulse and output single value. An optimal reference equalization (TXFFE, CTLE, DFE) is applied on the raw captured output signal to distinguish between equalizeable and un-equalizeable ISI.

The following steps shall be applied for calculating OUTPUT_ISI:

1. Using the extracted un-equalized pulse response $h(n)$ described in section 6.6.5.3.4 and mathematically applying the reference TX equalizer, RX CTLE and DFE as defined in the relevant specification (*USB 3.2* and *USB4*).

   The transmit and receiver equalization shall be selected such that the OUTPUT_ISI is maximized.

2. Using the equalized pulse response $h^e(n)$ to calculate OUTPUT_ISI as the ratio between the signal and the sum of the absolute values of the pre-cursor taps and the post cursor taps from tap 2 and above.

$$OUTPUT\_ISI = 20 \cdot log_{10}\left(\frac{\sum_{n_{pk}-0.5\cdot M}^{n_{pk}+0.5\cdot M-1} h^e(n)}{\sum_{0}^{n_{pk}-0.5\cdot M-1} |h^e(n)| + \sum_{n_{pk}+1.5\cdot M}^{n_{max}} |h^e(n)|}\right)$$

   where,

   $h^e(n)$ is the equalized pulse response with M samples per UI

   n_{pk} is the equalized pulse response peak index

   n_{max} is the last index to be included in the ISI summation, such that

$$\{n_{max}\colon |h^e(n)| < \frac{h^e(n_{pk})}{100} \quad \forall\, n > n_{max}\}$$

To simplify the measurement and avoid de-embedding the cable from the setup, the limit for OUTPUT_ISI is defined to be equal to or higher than a worst-case cable measured on the same setup.

6.6.5.3.12 Cable CM_NOISE

CM_NOISE is defined as the maximum peak value of the signal captured in the cable output with common mode setting on the scope (p+n) and prbs15 data pattern.

The CM_NOISE shall not exceed 100mV.

6.6.5.4 USB4 CL-State Power Requirements

Active cables shall meet the VCONN power requirements for *USB4* operation in Table 6-30. These requirements are for the entire cable not just a cable plug.

Table 6-30 USB4 CL-State Requirements

State	Maximum Power Consumption VCONN	Power Consumption Notes
CL0	1.5 W	Applies to training states and CL0.
CL0s	≤ CL0 power	
CL1	≤ CL0 power	
CL2	≤ CL1 power	
CLd	20 mW	Steady state power.

Note: CLd Power requirements are not applicable to OIAC cables.

6.6.6 Return Loss

Return loss is defined in the *USB 3.2* specification.

6.7 Active Cables That Support Alternate Modes

Active cables may support Alternate Modes. Active cables that support Alternate Modes shall be discoverable via *USB PD*. They shall use the standard *USB PD* mechanisms to discover, enter and exit Alternate Modes.

6.7.1 Discover SVIDs

Active cables that support an Alternate Mode shall report support for SVIDs on SOP' only.

6.7.2 Discover Modes

Active cables that support an Alternate Mode shall report support for Modes on SOP' only.

6.7.3 Enter/Exit Modes

Enter and ***Exit*** mode shall be communicated on SOP' and on SOP'' when the SOP'' Controller Present bit is set in the Active Cable. It is recommended that ***Enter Mode*** be sent initially to SOP' and then SOP" if supported and then SOP. It is recommended ***Exit Mode*** be sent initially to SOP and then to SOP" if supported and then SOP'.

6.7.4 Power in Alternate Modes

The power dissipation in an active cable's Alternate Mode shall maintain the plug's Maximum Skin Temperature below the requirement defined in Table 6-15.

Alternate Modes should reduce power in active cables in sleep states for best user experience.

A Audio Adapter Accessory Mode

A.1 Overview

Analog audio headsets are supported by multiplexing four analog audio signals onto pins on the USB Type-C® connector when in the Audio Adapter Accessory Mode. The four analog audio signals are the same as those used by a traditional 3.5 mm headset jack. This makes it possible to use existing analog headsets with a 3.5 mm to USB Type-C adapter. The audio adapter architecture allows for an audio peripheral to provide up to 500 mA back to the system for charging.

An analog audio adapter could be a very basic USB Type-C adapter that only has a 3.5 mm jack, or it could be an analog audio adapter with a 3.5 mm jack and a USB Type-C receptacle to enable charge-through. The analog audio headset shall not use a USB Type-C plug to replace the 3.5 mm plug.

A USB host that implements support for USB Type-C Analog Audio Adapter Accessory mode shall also support USB Type-C Digital Audio (TCDA) with nominally equivalent functionality and performance. A USB device that implements support for USB Type-C Analog Audio Adapter Accessory mode should also support TCDA with nominally equivalent audio functionality and performance.

A.2 Detail

An analog audio adapter shall use a captive cable with a USB Type-C plug or include an integrated USB Type-C plug.

The analog audio adapter shall identify itself by presenting a resistance to GND of ≤ Ra on both A5 (CC) and B5 (VCONN) of the USB Type-C plug. If pins A5 and B5 are shorted together, the effective resistance to GND shall be less than Ra/2.

A DFP that supports analog audio adapters shall detect the presence of an analog audio adapter by detecting a resistance to GND of less than Ra on both A5 (CC) and B5 (VCONN).

Table A-1 shows the pin assignments at the USB Type-C plug that shall be used to support analog audio.

Table A-1 USB Type-C Analog Audio Pin Assignments

Plug Pin	USB Name	Analog Audio Function	Location on 3.5 mm Jack	Notes
A5	CC			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
B5	VCONN			Connected to digital GND with resistance ≤ Ra. System uses for presence detect.
A6/B6	Dp	Right	Ring 1	Analog audio right channel A6 and B6 shall be shorted together in the adapter.
A7/B7	Dn	Left	Tip	Analog audio left channel A7 and B7 shall be shorted together in the adapter.
A8	SBU1	Mic/AGND	Ring 2	Analog audio microphone (OMTP & YD/T) or Audio GND (CTIA).
B8	SBU2	AGND/Mic	Sleeve	Audio GND (OMTP & YD/T or analog audio microphone (CTIA).
A1/A12 B1/B12	GND			Digital GND (DGND) used as the ground reference and current return for CC1, CC2, and VBUS.
A4/A9 B4/B9	VBUS			Not connected unless the audio adapter uses this connection to provide 5 V @ 500 mA for charging the system's battery.
Others				Other pins shall not be connected.

The analog audio signaling presented by the headset on the 3.5 mm jack is expected to comply with at least one of the following:

- The traditional American headset jack pin assignment, with the jack sleeve used for the microphone signal, supported by CTIA-The Wireless Association
- "Local Connectivity: Wired Analogue Audio" from the Open Mobile Terminal Forum (OMTP) forum
- "Technical Requirements and Test Methods for Wired Headset Interface of Mobile Communication Terminal" (YT/D 1885-2009) from the China Communications Standards Association

When in the Audio Adapter Accessory Mode, the system shall not provide VCONN power on either CC1 or CC2. Failure to do this may result in VCONN being shorted to GND when an analog audio peripheral is present.

The system shall connect A6/B6, A7/B7, A8 and B8 to an appropriate audio codec upon entry into the Audio Adapter Accessory Mode. The connections for A8 (SBU1) and B8 (SBU2) pins are dependent on the adapter's orientation. Depending on the orientation, the microphone and analog ground pins may be swapped. These pins are already reversed between the two major standards for headset jacks and support for this is built into the headset connection of many codecs or can be implemented using an autonomous audio headset switch. The system shall work correctly with either configuration.

A.3 Electrical Requirements

The maximum ratings for pin voltages are referenced to GND (pins A1, A12, B1, and B12). The non-GND pins on the plug shall be isolated from GND on the USB Type-C connector and shall be isolated from the USB plug shell. To minimize the possibility of ground loops between systems, AGND shall be connected to GND only within the system containing the USB Type-C receptacle. Both the system and audio device implementations shall be able to tolerate the Right, Left, Mic, and AGND signals being shorted to GND. The current provided by the amplifier driving the Right and Left signals shall not exceed ±150 mA per audio channel, even when driving a 0 Ω load.

Table A-2 shows allowable voltage ranges on the pins in the USB Type-C plug that shall be met.

Table A-2 USB Type-C Analog Audio Pin Electrical Parameter Ratings

Plug Pin	USB Name	Analog Audio Function	Min	Max	Units	Notes
A6/B6	Dp	Right	−3.0	3.0	V	A6 and B6 shall be shorted together in the analog audio adapter
A7/B7	Dn	Left	−3.0	3.0	V	A7 and B7 shall be shorted together in the analog audio adapter
A8	SBU1	Mic/AGND	−0.4	3.3	V	
B8	SBU2	AGND/Mic	−0.4	3.3	V	

The maximum voltage ratings for Left and Right signals are selected to encompass a 2 Vrms sine wave (2.828 Vp = 5.657 Vpp = 6 dBV) which is a common full-scale voltage for headset audio output.

Headset microphones operate on a positive bias voltage provided by the system's audio codec and AC-couple the audio signal onto it. Some headsets may produce an audio signal level up to 0.5 Vrms (0.707 Vp = 1.414 Vpp = -6 dBV) but this is biased so that the voltage does not swing below GND. The bias voltage during operation is typically around 1.25 V but it varies quite a bit depending on the specifics of the manufacturer's design, therefore the maximum voltage rating for the SBU pins is selected to allow a variety of existing solutions.

While one SBU pin carries the Mic signal, the other SBU pin serves as AGND carrying the return current for Left, Right, and Mic. If we assume a worst-case headset speaker impedance of 16 Ω per speaker, then the worst-case return current for the speakers is ± 0.2 A. If we assume that the worst-case resistance from the AGND pin to GND within the USB Type-C system is 1 Ω (due to FET R_{ON} within the signal multiplexer, contact, and trace resistances), then the voltage of the AGND pin with respect to USB Type-C GND can vary between ± 0.2 V. The minimum voltage rating for the SBU pins has been selected to allow for this scenario with some additional margin to account for Mic signal return current and tolerances.

The system shall exhibit no more than -48 dB linear crosstalk between the Left and Right audio channels and exhibit no more than -51 dB linear crosstalk from the Left or Right channel to the Mic channel. Crosstalk measurements shall be made using a measurement adapter plug that supports USB Type-C analog audio connections according to Table A-1. In the measurement adapter, the Left and Right channels are terminated with 32 Ω resistors to AGND, the Mic channel is terminated with 2k Ω resistor to AGND; AGND is connected to USB Type-C Plug Pin A8, and the Mic channel is connected to USB Type-C Plug Pin B8.

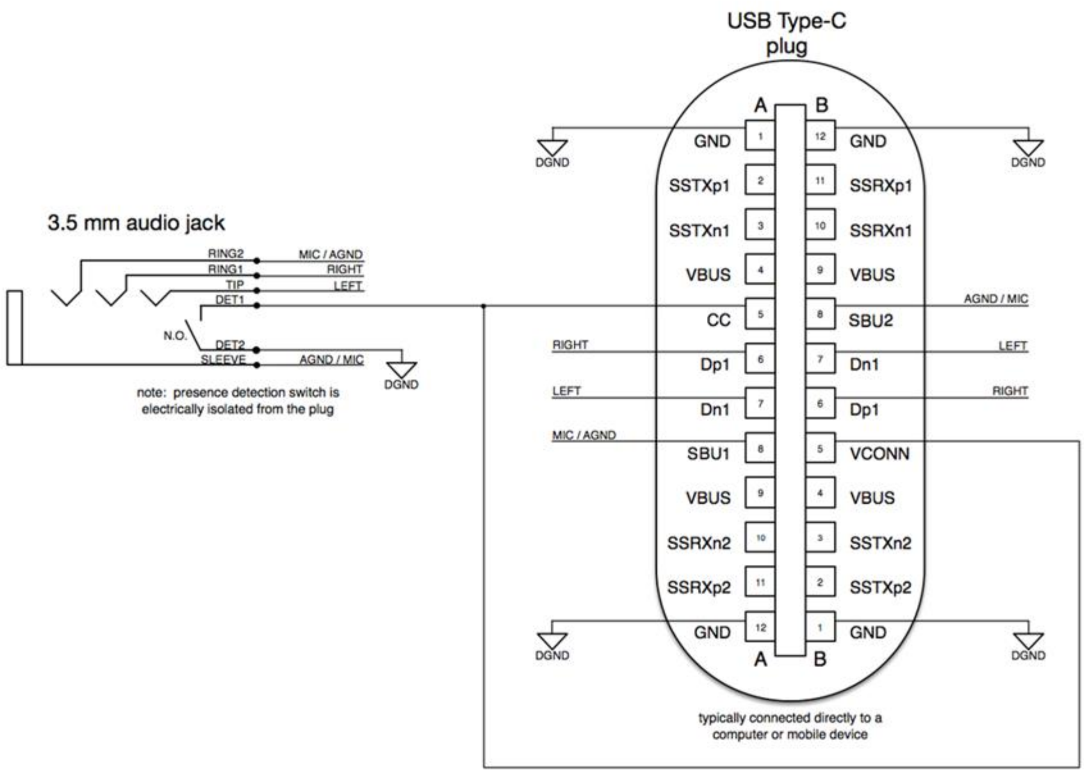
Crosstalk shall be measured by using the system to drive a sine wave signal to the Left output channel and zero signal to the Right output channel. The system shall configure the Mic channel according to the default Mic operating mode supported by the system. AC voltage levels at the Left, Right and Mic channels are measured across the corresponding termination resistors using a third-octave filter at the sine signal frequency. Left – Right crosstalk is reported as ratio of the Right channel voltage to the Left channel voltage expressed in decibels. Similarly, the Left – Mic crosstalk is reported. The measurements shall be conducted at 31.5, 63, 125, 250, 500, 1000, 2000, 4000, 8000 and 16000 Hz frequencies. The measurements shall be repeated so that the sine wave signal is driven to the Right channel and Right – Left and Right – Mic crosstalk results are obtained. Both USB Type-C plug orientations shall be measured."

A.4 Example Implementations

A.4.1 Passive 3.5 mm to USB Type-C Adapter – Single Pole Detection Switch

Figure A-1 illustrates how a simple 3.5 mm analog audio adapter can be made. In this design, there is an audio plug that contains a single-pole detection switch that is used to completely disconnect the CC and VCONN pins from digital GND when no 3.5 mm plug is inserted. This has the effect of triggering the USB Type-C presence detect logic upon insertion or removal of either the 3.5 mm plug or the audio adapter itself.

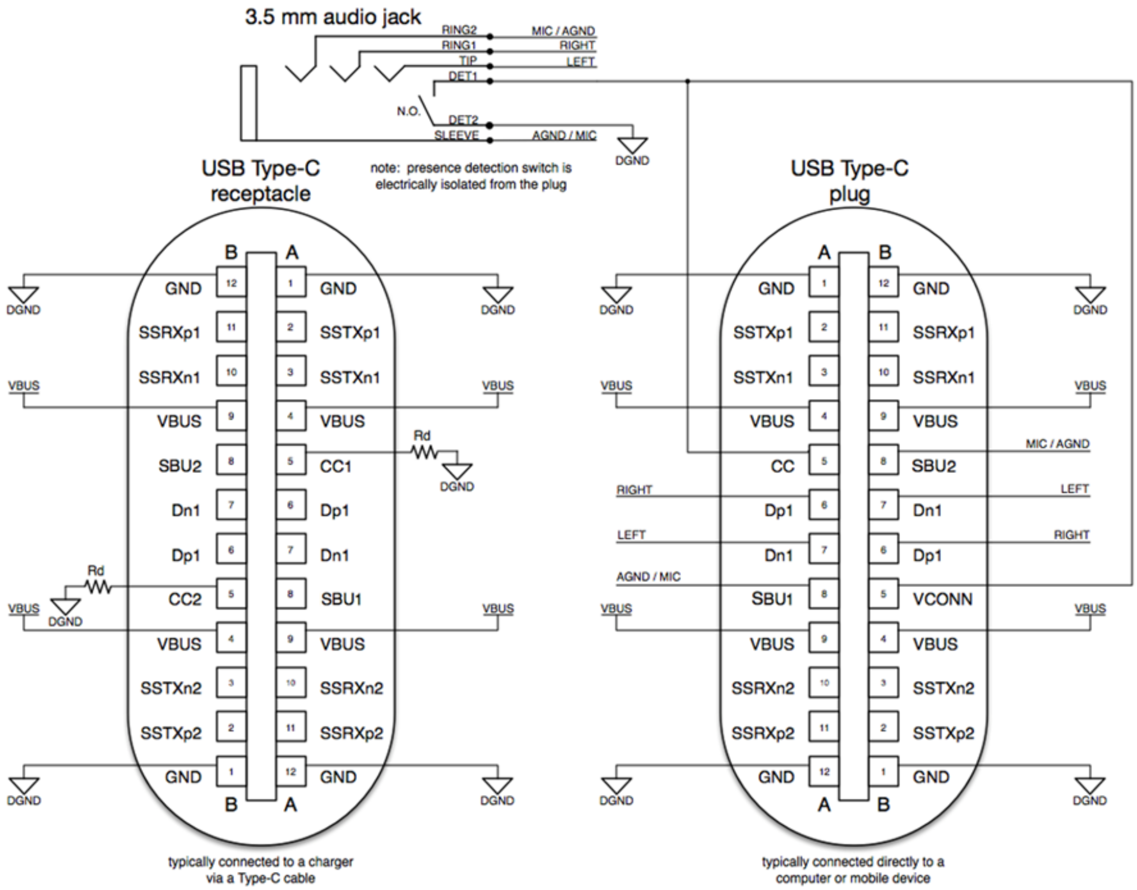
Figure A-1 Example Passive 3.5 mm to USB Type-C Adapter



A.4.2 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through

Figure A-2 illustrates a 3.5 mm analog audio adapter that supports charge-through operation. Charging power comes into the adapter through a USB Type-C receptacle and is routed directly to the adapter's USB Type-C plug, which is plugged into the device being charged. This design is limited to providing 500 mA of charge-through current since it has no way to advertise greater current-sourcing capability. The USB Type-C receptacle presents Rd on both of its CC pins because a CC pull-down must be present for the receptacle to indicate that it wants to consume VBUS current. USB Type-C systems that support analog audio should ensure that charging is not interrupted by insertion or removal of the 3.5 mm audio plug and that audio is not interrupted by insertion or removal of the cable connected to the audio adapter's USB Type-C receptacle by using the system's presence detection logic monitoring the states of both the CC1 and CC2 pins and VBUS.

Figure A-2 Example 3.5 mm to USB Type-C Adapter Supporting 500 mA Charge-Through



B Debug Accessory Mode

B.1 Overview

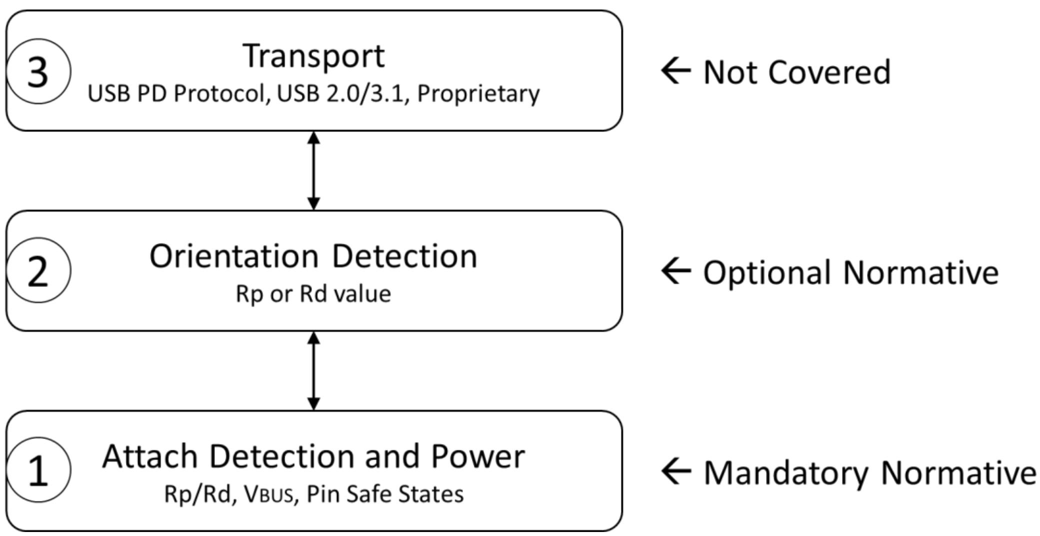
This appendix covers the functional requirements for the USB Type-C® Debug Accessory Mode (DAM), Debug and Test System (DTS), and Target System (TS). The USB Type-C connector is ideal for debug of closed-chassis, form-factor devices. Debug covers many areas, ranging from detailed JTAG Test Access Port (TAP)-level debug in a lab to high-level debug of software applications in production. Lab debug requires early debug access to hardware registers soon after reset, whereas software debug uses kernel debuggers, etc. to access software state. Debug Accessory Mode in USB Type-C enables debug of closed-chassis, form-factor devices by re-defining the USB Type-C ports for debug purposes.

Basic debug requirements are defined as a standard feature, and additional debug features may be added as per vendor specifications.

B.2 Functional

The USB Type-C Debug Accessory Mode follows a layered structure as shown in Figure B-1, defining the minimum physical layer for Attach, Detection and Power. Orientation detection is optional normative. The transport layer is left proprietary and is not covered in this document.

Figure B-1 USB Type-C Debug Accessory Layered Behavior



B.2.1 Signal Summary

Figure B-2 shows the pin assignments of the DTS plug that are used to support DAM. The pins highlighted in yellow are those available to be configured for debug signals. Both CC1 and CC2 are used for current advertisement and optional orientation detection.

Figure B-2 DTS Plug Interface

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC1	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	CC2	D+	D-	SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The DTS and TS must follow the USB Safe State as defined in the *USB PD* specification at all times (whether in DAM or not).

B.2.2 Port Interoperability

Table B-1 summarizes the expected results when interconnecting a DTS Source, Sink or DRP port to a TS Source, Sink or DRP port.

Table B-1 DTS to TS Port Interoperability

	DTS Source	DTS Sink	DTS DRP
TS Sink	Functional	Non-functional[1]	Functional
TS Sink w/ Accessory Support	Functional	Non-functional[1]	Functional
TS DRP	Functional	Functional	Functional
TS Source	Non-functional[1]	Functional	Functional

1. In the cases where no function results, neither port shall be harmed by this connection. Following the USB Safe State ensures this.

B.2.3 Debug Accessory Mode Entry

The typical flow for the configuration of the interface in the general case of a DTS to a TS is as follows:

1. Detect a valid connection between the DTS (Source, Sink, or DRP) and TS (Source, Sink, or DRP)
2. Optionally determine orientation of the plug in the receptacle
3. Optionally establish *USB PD* communication over CC for advanced power delivery negotiation and Alternate Modes. *USB PD* communication is allowed only if the optional orientation of the plug is determined.
4. Establish test access connections with the available USB Type-C signals

The DTS DRP will connect as either a Source or a Sink, but its state diagram gives preference to the Source role.

B.2.3.1 Detecting a Valid DTS-to-TS Connection

The general concept for setting up a valid connection between a DTS and TS is based on being able to detect the typical USB Type-C termination resistances. However, detecting a Debug Accessory Mode connection requires that both CC pins must detect a pull-up (Rp) or pull-down (Rd) termination. A USB Type-C Cable does not pass both CC wires so a receptacle to receptacle Debug Accessory Mode connection cannot be detected.

A DTS is only allowed to connect to a TS that is presenting either Rp/Rp or Rd/Rd. Otherwise, the TS does not support Debug Accessory Mode.

To detect either an Rp/Rp or Rd/Rd, the DTS must be a captive cable or a direct-attach device with a USB Type-C plug and the TS must have a USB Type-C receptacle.

B.2.4 Connection State Diagrams

This section provides reference connection state diagrams for CC-based behaviors of the DTS. The TS connection state diagrams are found in Section 4.5.2.

Refer to Section B.2.4.1 for the specific state transition requirements related to each state shown in the diagrams.

Refer to Section B.2.4.3 for a description of which states are mandatory for each port type and a list of states where *USB PD* communication is permitted.

Figure B-3 illustrates a connection state diagram for a DTS Source.

Figure B-3 Connection State Diagram: DTS Source

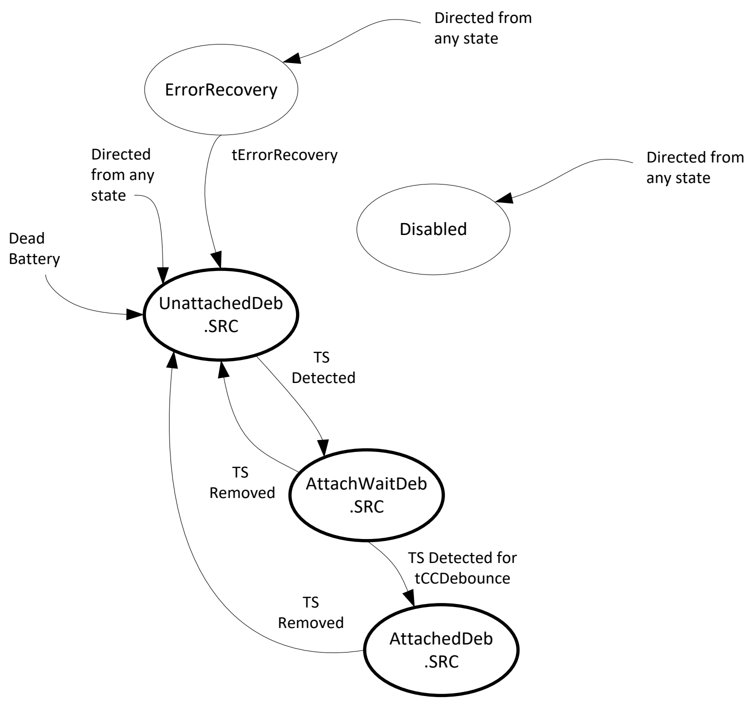


Figure B-4 illustrates a connection state diagram for a simple DTS Sink.

Figure B-4 Connection State Diagram: DTS Sink

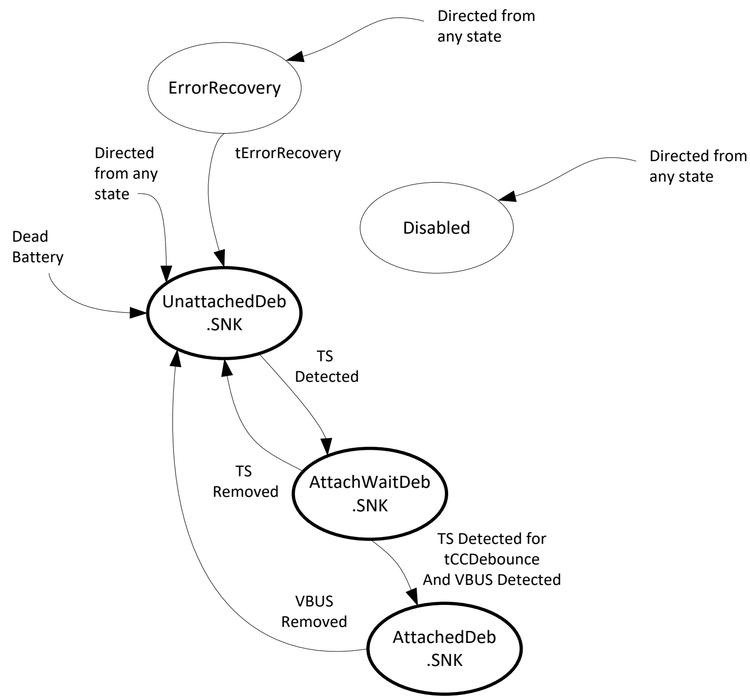
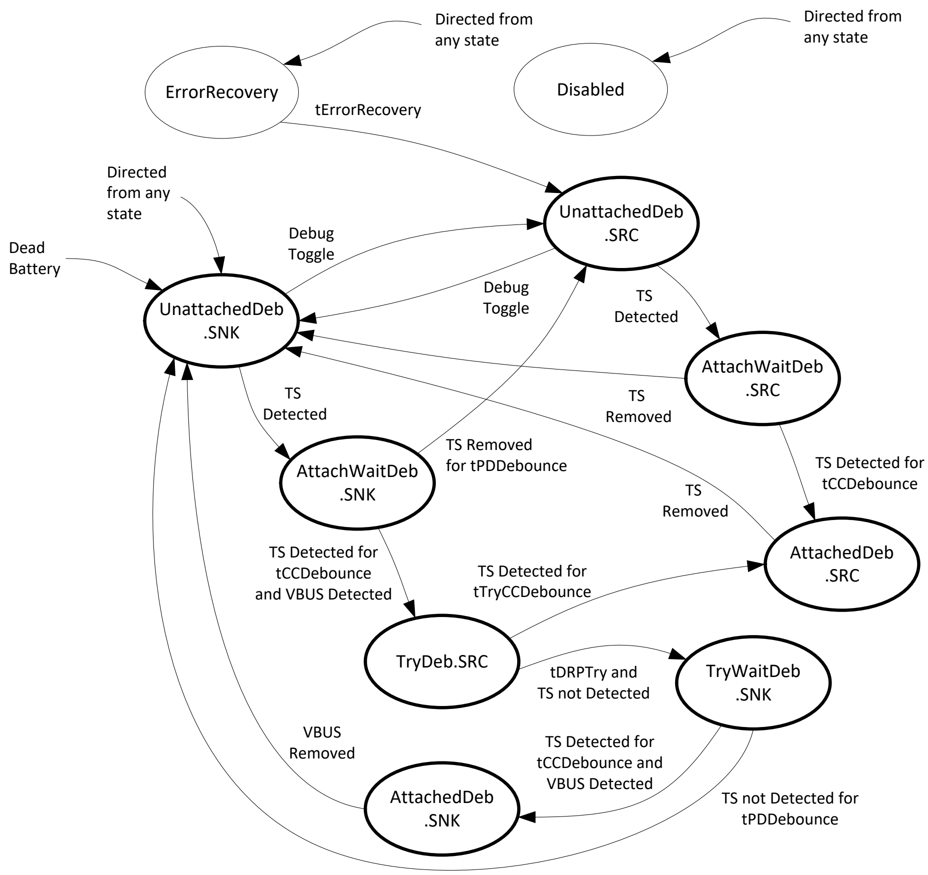


Figure B-5 illustrates a connection state diagram for a DTS DRP.

Figure B-5 Connection State Diagram: DTS DRP



B.2.4.1 Connection State Machine Requirements

The DTS state machine requirements follow those outlined in Section 4.5.2.2 for the general USB Type-C state machines with the additional following states defined.

Note, VCONN shall not be driven by any DTS or TS port in any state.

B.2.4.1.1 Exiting from ErrorRecovery State

This state appears in Figure B-3, Figure B-4, and Figure B-5.

The ErrorRecovery state is where the DTS cycles its connection by removing all terminations from the CC pins for tErrorRecovery followed by transitioning to the appropriate UnattachedDeb.SNK or UnattachedDeb.SRC state based on DTS type.

The DTS should transition to the ErrorRecovery state from any other state when directed.

A DTS may choose not to support the ErrorRecovery state. If the ErrorRecovery state is not supported, the DTS shall be directed to the Disabled state if supported. If the Disabled state is not supported, the DTS shall be directed to either the UnattachedDeb.SNK or UnattachedDeb.SRC states.

A DTS Sink shall transition to UnattachedDeb.SNK after tErrorRecovery.

A DTS Source shall transition to UnattachedDeb.SRC after tErrorRecovery.

A DTS DRP shall transition to UnattachedDeb.SRC after tErrorRecovery.

B.2.4.1.2 UnattachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the UnattachedDeb.SNK state, the DTS is waiting to detect the presence of a TS Source.

A DTS with a dead battery shall enter this state while unpowered.

B.2.4.1.2.1 UnattachedDeb.SNK Requirements

The DTS shall not drive VBUS.

Both CC pins shall be independently terminated to ground through Rd.

B.2.4.1.2.2 Exiting from UnattachedDeb.SNK State

The DTS shall transition to AttachWaitDeb.SNK when a TS Source connection is detected, as indicated by the SNK.Rp state on both of its CC pins.

A DTS DRP shall transition to UnattachedDeb.SRC within tDRPTransition after the state of one or both CC pins is SNK.Open for tDRP – dcSRC.DRP · tDRP, or if directed.

B.2.4.1.3 AttachWaitDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the AttachWaitDeb.SNK state, the DTS has detected the SNK.Rp state on both CC pins and is waiting for VBUS.

B.2.4.1.3.1 AttachWaitDeb.SNK Requirements

The requirements for this state are identical to UnattachedDeb.SNK.

B.2.4.1.3.2 Exiting from AttachWaitDeb.SNK State

A DTS Sink shall transition to UnattachedDeb.SNK when the state of one or both CC pins is SNK.Open for at least tPDDebounce.

A DTS DRP shall transition to UnattachedDeb.SRC when the state of one or both CC pins is SNK.Open for at least tPDDebounce.

A DTS Sink shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

A DTS DRP shall transition to TryDeb.SRC when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

B.2.4.1.4 AttachedDeb.SNK State

This state appears in Figure B-4 and Figure B-5.

When in the AttachedDeb.SNK state, the DTS is attached and operating as a DTS Sink.

B.2.4.1.4.1 AttachedDeb.SNK Requirements

This mode is for debug only

The port shall not drive VBUS.

The port shall provide an Rd as specified in Table 4-15 on both CC pins if orientation is not needed. See Section B.2.6 for orientation detection.

The port shall monitor to detect when VBUS is removed.

If the DTS needs to establish a *USB PD* communications, it shall do so only after entry to this state. In this state, the DTS takes on the initial *USB PD* role of UFP/Sink.

The DTS shall connect the debug signals for Debug Accessory Mode operation only after entry to this state.

The DTS may follow the DAM Sink Power Sub-State behavior specified in Section 4.5.2.3.

B.2.4.1.4.2 Exiting from AttachedDeb.SNK State

A DTS shall transition to UnattachedDeb.SNK when VBUS is no longer present

B.2.4.1.5 UnattachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the UnattachedDeb.SRC state, the DTS is waiting to detect the presence of a TS Sink

B.2.4.1.5.1 UnattachedDeb.SRC Requirements

The DTS shall not drive VBUS.

The DTS shall source current on both CC pins independently.

The DTS shall provide a unique Rp value on each CC pin as specified in Section 4.5.2.3.

B.2.4.1.5.2 Exiting from UnattachedDeb.SRC State

The DTS shall transition to AttachWaitDeb.SRC when the SRC.Rd state is detected on both CC pins.

A DTS DRP shall transition to UnattachedDeb.SNK within tDRPTransition after dcSRC.DRP · tDRP, or if directed.

B.2.4.1.6 AttachWaitDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

The AttachWaitDeb.SRC state is used to ensure that the state of both of the CC pins is stable after a TS Sink is connected.

B.2.4.1.6.1 AttachWaitDeb.SRC Requirements

The requirements for this state are identical to UnattachedDeb.SRC.

B.2.4.1.6.2 Exiting from AttachWaitDeb.SRC State

The DTS shall transition to AttachedDeb.SRC when VBUS is at vSafe0V and the SRC.Rd state is detected on both of the CC pins for at least tCCDebounce.

A DTS Source shall transition to UnattachedDeb.SRC and a DTS DRP to UnattachedDeb.SNK when the SRC.Open state is detected on either of the CC pins.

B.2.4.1.7 AttachedDeb.SRC State

This state appears in Figure B-3 and Figure B-5.

When in the AttachedDeb.SRC state, the DTS is attached and operating as a DTS Source.

B.2.4.1.7.1 AttachedDeb.SRC Requirements

The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.

The DTS shall supply VBUS current at the level it advertises. See Section B.2.6.1.1 for advertising current level.

The DTS shall supply VBUS within tVBUSON of entering this state, and for as long as it is operating as a power source.

If the DTS needs to establish *USB PD* communications, it shall do so only after entry to this state. The DTS shall not initiate any *USB PD* communications until VBUS reaches vSafe5V. In this state, the DTS takes on the initial *USB PD* role of DFP/Source.

The DTS shall connect the debug signals for Debug Accessory Mode operation only after entry to this state.

B.2.4.1.7.2 Exiting from AttachedDeb.SRC State

A DTS Source shall transition to UnattachedDeb.SRC when the SRC.Open state is detected on either CC pin.

A DTS DRP shall transition to UnattachedDeb.SNK when SRC.Open is detected on either CC pin.

A DTS shall cease to supply VBUS within tVBUSOFF of exiting AttachedDeb.SRC.

B.2.4.1.8 TryDeb.SRC State

This state appears in Figure B-5.

When in the TryDeb.SRC state, the DTS DRP is querying to determine if the TS is also a DRP, to favor the DTS taking the Source role.

B.2.4.1.8.1 TryDeb.SRC Requirements

The DTS shall not drive VBUS.

The DTS shall source current on both CC pins independently.

The DTS shall provide a unique Rp value on each CC pin as specified in Section B.2.4.2.

B.2.4.1.8.2 Exiting from TryDeb.SRC State

The DTS shall transition to AttachedDeb.SRC when the SRC.Rd state is detected on both CC pins for at least tTryCCDebounce.

The DTS shall transition to TryWaitDeb.SNK after tDRPTry if the state of both CC pins is not SRC.Rd.

B.2.4.1.9 TryWaitDeb.SNK State

This state appears in Figure B-5.

When in the TryWaitDeb.SNK state, the DTS has failed to become a DTS Source and is waiting to attach as a DTS Sink.

B.2.4.1.9.1 TryWaitDeb.SNK Requirements

The DTS shall not drive VBUS.

Both CC pins shall be independently terminated to ground through Rd.

B.2.4.1.9.2 Exiting from TryWaitDeb.SNK State

The DTS shall transition to AttachedDeb.SNK when neither CC pin is SNK.Open after tCCDebounce and VBUS is detected.

The DTS shall transition to UnattachedDeb.SNK when the state of one of the CC pins is SNK.Open for at least tPDDebounce or if VBUS is not detected within tPDDebounce.

B.2.4.2 Power Sub-State Requirements

B.2.4.2.1 TS Sink Power Sub-State Requirements

When in the DebugAccessory.SNK state and the DTS Source is supplying default VBUS, the TS Sink shall operate in one of the sub-states shown in Figure B-6. The initial TS Sink Power Sub-State is PowerDefaultDeb.SNK. Subsequently, the TS Sink Power Sub-State is determined by the DTS Source's USB Type-C current advertisement determined by the Rp value on each CC pin as shown in Table B-2. The TS Sink in the attached state shall remain within the TS Sink Power Sub-States until either VBUS is removed or a *USB PD* contract is established with the Source.

The TS Sink is only required to implement TS Sink Power Sub-State transitions if the TS Sink wants to consume more than default USB current.

Note, a TS Source will not use the values in Table B-2. A TS Source will present the same Rp on each CC pin using the standard Rp value for the desired current advertisement.

Figure B-6 TS Sink Power Sub-States

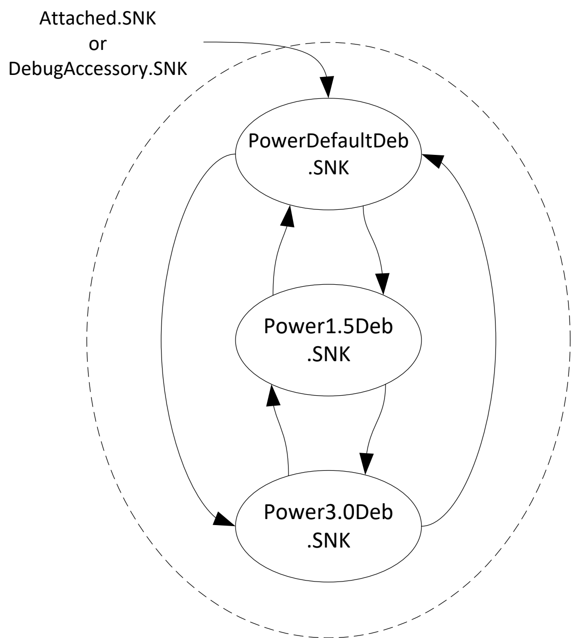


Table B-2 Rp/Rp Charging Current Values for a DTS Source

Mode of Operation	CC1	CC2
Default USB Power	Rp for 3 A	Rp for 1.5 A
USB Type-C Current @ 1.5 A	Rp for 1.5 A	Rp for Default
USB Type-C Current @ 3 A	Rp for 3 A	Rp for Default

B.2.4.2.2 PowerDefaultDeb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the lowest range (default) of Source-supplied current.

B.2.4.2.2.1 PowerDefaultDeb.SNK Requirements

The port shall draw no more than the default USB power from VBUS. See Section 4.6.2.1.

If the DTS Sink wants to consume more than the default USB power, it shall monitor vRd on both CC pins to determine if more current is available from the Source.

B.2.4.2.2.2 Exiting from PowerDefaultDeb.SNK

For any change on CC indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on each CC pin have been stable for at least tRpValueChange.

For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power1.5Deb.SNK Sub-State.

For vRd voltages on the CC pins indicating 3 A mode, the DAM Sink shall transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.3 Power1.5Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within the two lower ranges (default and 1.5 A) of DAM Source-supplied current.

B.2.4.2.3.1 Power1.5Deb.SNK Requirements

The DAM Sink shall draw no more than 1.5 A from VBUS.

The DAM Sink shall monitor both vRd voltages while it is in this sub-state.

B.2.4.2.3.2 Exiting from Power1.5Deb.SNK

For any change on the CC pins indicating a change in allowable power, the DAM Sink shall not transition until the new vRd voltages on both CC pins have been stable for at least tRpValueChange.

For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For vRd voltages on the CC pins indicating 3 A mode, the port shall transition to the Power3.0Deb.SNK Sub-State.

B.2.4.2.4 Power3.0Deb.SNK Sub-State

This sub-state supports DAM Sinks consuming current within all three ranges (default, 1.5 A and 3.0 A) of DAM Source-supplied current.

B.2.4.2.4.1 Power3.0Deb.SNK Requirements

The port shall draw no more than 3.0 A from VBUS.

The port shall monitor both vRd voltages while it is in this sub-state.

B.2.4.2.4.2 Exiting from Power3.0Deb.SNK

For any change on the CC pins indicating a change in allowable power, the port shall not transition until the new vRd voltages on both CC pins have been stable for at least tRpValueChange.

For vRd voltages on the CC pins indicating Default USB Power mode, the port shall transition to the PowerDefaultDeb.SNK Sub-State and reduce its power consumption to the new range within tSinkAdj.

For vRd voltages on the CC pins indicating 1.5 A mode, the DAM Sink shall transition to the Power1.5Deb.SNK Sub-State.

B.2.4.2.5 DTS Sink Power Sub-State Requirements

A DTS Sink follows the same power sub-states defined in Section 4.5.2.2.22. The TS Source will be advertising current with a standard Rp value that is the same for each CC pin. If optional orientation detection is performed, the DTS Sink will only be able to determine the Rp value from the CC pin that is set for *USB PD* communication.

B.2.4.3 Connection States Summary

Table B-3 defines the mandatory and optional states for each type of port. For states allowing *USB PD* communication, DAM connections requiring *USB PD* communication shall determine orientation by the steps described in Section B.2.6.

Table B-3 Mandatory and Optional States

	DTS Source	DTS SINK	DTS DRP	USB PD Communication and/or Debug Signal Activity
UnattachedDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachWaitDeb.SNK	N/A	Mandatory	Mandatory	Not Permitted
AttachedDeb.SNK	N/A	Mandatory	Mandatory	Permitted
UnattachedDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachWaitDeb.SRC	Mandatory	N/A	Mandatory	Not Permitted
AttachedDeb.SRC	Mandatory	N/A	Mandatory	Permitted
TryDeb.SRC	N/A	N/A	Mandatory	Not Permitted
TryWaitDeb.SNK	N/A	N/A	Mandatory	Not Permitted

B.2.5 DTS Port Interoperability Behavior

This section describes interoperability behavior between DTS ports and TS ports.

B.2.5.1 DTS Port to TS Port Interoperability Behaviors

The following sub-sections describe typical port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks and DRPs as presented in Table B-1.

B.2.5.1.1 DTS Source to TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a TS Sink.

1. DTS Source and TS Sink in the unattached state
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
    - DTS Source detects the TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
    - DTS Source turns on VBUS
3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
    - TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK
4. While the DTS Source and TS Sink are in the attached state:
    - DTS Source adjusts both Rp values as needed for offered current

- TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
- DTS Source monitors both CC pins for detach and when detected on either pin, enters UnattachedDeb.SRC
- TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.2 DTS Source to TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a TS DRP.

1. DTS Source and TS DRP in the unattached state
   - TS DRP alternates between Unattached.SRC and Unattached.SNK
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the TS DRP's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. TS DRP transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
   - TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters DebugAccessory.SNK
4. While the DTS Source and TS DRP are in their respective attached states:
   - DTS Source adjusts both Rp values as needed for offered current
   - TS DRP detects and monitors vRd on both CC pins for available current on VBUS and performs any orientation required
   - DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
   - TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK (and resumes toggling between Unattached.SNK and Unattached.SRC)

B.2.5.1.3 DTS Sink to TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a TS Source.

1. TS Source and DTS Sink in the unattached state
2. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC. After tCCDebounce, it enters UnorientedDebugAccessory.SRC.
   - TS Source turns on VBUS
3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.
   - DTS Sink in UnattachedDeb.SNK detects the TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK.
   - DTS Sink in AttachWaitDeb.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters AttachedDeb.SNK
   - DTS sink determines advertised current from vRd on either CC pin.

4. If orientation supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.
5. If orientation supported, TS Source detects change in vRd of one of the CC pins and transitions from UnorientedDebugAccessory.SRC to OrientedDebugAccessory.SRC and performs any orientation required.
6. While the TS Source and DTS Sink are in the attached state:
    - If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
    - TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
    - DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.1.4 DTS Sink to TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a TS DRP.

1. DTS Sink and TS DRP in the unattached state
    - TS DRP alternates between Unattached.SRC and Unattached.SNK
2. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
    - TS DRP in Unattached.SRC detects both CC pull-downs of DTS Sink in UnattachedDeb.SNK and enters AttachWait.SRC
    - TS DRP in AttachWait.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters UnorientedDebugAccessory.SRC and turns on VBUS
3. DTS Sink transitions from UnattachedDeb.SNK to AttachedDeb.SNK through AttachWaitDeb.SNK.
    - DTS Sink in UnattachedDeb.SNK detects the TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK. After that state persists for tCCDebounce and it detects VBUS, it enters AttachedDeb.SNK
    - DTS sink determines advertised current from vRd on either CC pin.
7. If orientation is supported, DTS Sink adjusts Rd on the non-CC communication pin as needed for orientation detection.
8. If orientation supported, TS DRP detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.
9. While the TS DRP and DTS Sink are in the attached state:
    - If orientation is supported, DTS sink determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
    - TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK
    - DTS Sink monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.1.5 DTS DRP to TS Sink Behavior

The following describes the behavior when a DTS DRP is connected to a TS Sink.

1. DTS DRP and TS Sink in the unattached state

- DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK

2. DTS DRP transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS DRP in UnattachedDeb.SRC detects both of the CC pull-downs of TS Sink enters AttachWaitDeb.SRC
   - DTS DRP in AttachWaitDeb.SRC detects that the pull-downs on both CC pins persist for tCCDebounce. It then enters AttachedDeb.SRC
   - DTS DRP turns on VBUS
3. TS Sink transitions from Unattached.SNK to DebugAccessory.SNK through AttachWait.SNK
   - TS Sink in Unattached.SNK detects the DTS DRP's pull-ups on both CC pins and enters AttachWait.SNK
   - TS Sink in AttachWait.SNK detects that the pull-ups on both CC pins persist for tCCDebounce and it detects VBUS. It enters DebugAccessory.SNK
4. While the DTS DRP and TS Sink are in their respective attached states:
   - DTS DRP adjusts Rp as needed for offered current
   - TS Sink detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
   - DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK
   - TS Sink monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.6 DTS DRP to TS DRP Behavior

The following describes the behavior when a DTS DRP is connected to TS DRP.

Case #1:

1. Both DRPs in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS DRP alternate between Unattached.SRC and Unattached.SNK
2. DTS DRP transitions from UnattachedDeb.SRC to AttachWaitDeb.SRC
   - DTS DRP in UnattachedDeb.SRC detects both CC pull-downs of TS DRP in Unattached.SNK and enters AttachWaitDeb.SRC
3. TS DRP transitions from Unattached.SNK to AttachWait.SNK
   - TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK
4. DTS DRP transitions from AttachWaitDeb.SRC to AttachedDeb.SRC
   - DTS DRP in AttachWaitDeb.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters AttachedDeb.SRC and turns on VBUS
5. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK
   - TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK
   - TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
6. While the TS DRP and DTS DRP are in the attached state:

- TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK
- DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK

Case #2:

1. Both DRPs in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - TS DRP alternate between Unattached.SRC and Unattached.SNK
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects both CC pull-ups of TS DRP in Unattached.SRC and enters AttachWaitDeb.SNK
3. TS DRP transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
   - TS DRP in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC
   - TS DRP in AttachWait.SRC continues to see both CC pull-downs of TS DRP for tCCDebounce, enters UnorientedDebugAccessory.SRC and turns on VBUS
4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC
   - DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC
5. TS DRP transitions from UnorientedDebugAccessory.SRC to Unattached.SNK
   - TS DRP in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SNK
6. TS DRP transitions from Unattached.SNK to AttachWait.SNK
   - TS DRP in Unattached.SNK detects both CC pull-ups of DTS DRP and enters AttachWait.SNK
7. DTS DRP transitions from TryDeb.SRC to AttachedDeb.SRC
   - DTS DRP in TryDeb.SRC detects both CC pull-downs of TS DRP for tTryCCDebounce and enters AttachedDeb.SRC
   - DTS DRP turns on VBUS
8. TS DRP transitions from AttachWait.SNK to DebugAccessory.SNK
   - TS DRP detects DTS DRP's pull-ups on both CC pins for tCCDebounce and detects VBUS and enters DebugAccessory.SNK
9. While the DTS DRP and TS DRP are in their respective attached states:
   - DTS DRP adjusts Rp as needed for offered current
   - TS DRP detects and monitors vRd on the CC pins for available current on VBUS and performs any orientation required
   - DTS DRP monitors both CC pins for detach and when detected, enters UnattachedDeb.SNK
   - TS DRP monitors VBUS for detach and when detected, enters Unattached.SNK

B.2.5.1.7 DTS DRP to TS Source Behavior

The following describes the behavior when a DTS DRP is connected to TS Source.

1. DTS DRP and TS Source in the unattached state
    - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
    - TS Source in Unattached.SRC
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
    - DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK
3. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC through AttachWait.SRC
    - TS Source in Unattached.SRC detects both CC pull-downs of DTS DRP and enters AttachWait.SRC
    - TS Source in AttachWait.SRC continues to see both CC pull-downs of DTS DRP for tCCDebounce, enters UnorientedDebugAccessory.SRC and turns on VBUS
4. DTS DRP transitions from AttachWaitDeb.SNK to TryDeb.SRC
    - DTS DRP in AttachWaitDeb.SNK continues to see both CC pull-ups of TS DRP for tCCDebounce and detects VBUS, enters TryDeb.SRC
5. TS Source transitions from UnorientedDebugAccessory.SRC to Unattached.SRC
    - TS Source in UnorientedDebugAccessory.SRC detects the removal of both CC pull-downs of DTS DRP and enters Unattached.SRC
6. DTS DRP transitions from TryDeb.SRC to TryWaitDeb.SNK
    - After tDRPTry, DTS DRP does not see pull-downs on both CC pin and enters TryWaitDeb.SNK
7. TS Source transitions from Unattached.SRC to UnorientedDebugAccessory.SRC
    - TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC
    - TS Source continues to detect pull-downs on both CC pins for tCCDebounce and enters UnorientedDebugAccessory.SRC and outputs VBUS
8. DTS DRP transitions from TryWaitDeb.SNK to AttachedDeb.SNK
    - DTS DRP sees pull-ups on both CC pins for tCCDebounce and detects VBUS and enters AttachedDeb.SNK
    - If orientation required, DTS DRP adjusts Rd on the non-CC communication pin as needed for orientation detection
9. If orientation supported, TS Source detects change in vRd on one of the CC pins and transitions to OrientedDebugAccessory.SRC and performs the required orientation.
10. While the TS Source and DTS DRP are in the attached state:
    - If orientation is supported, DTS DRP determines any change in advertised current from vRd of the CC pin that has been set as the CC communication pin.
    - TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
    - DTS DRP monitors VBUS for detach and when detected, enters UnattachedDeb.SNK

B.2.5.2 DTS Port to non-DAM TS Port Interoperability Behaviors

The following sub-sections describe the non-functional port-to-port interoperability behaviors for the various combinations of DTS and TS Sources, Sinks, and DRPs that do not support DAM.

B.2.5.2.1 DTS Source to non-DAM TS Sink Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS Sink.

1. DTS Source and TS Sink in the unattached state
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. Non-DAM TS Sink transitions from Unattached.SNK to AttachWait.SNK.
   - Non-DAM TS Sink in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.
   - Non-DAM TS Sink continues to detect pull-ups on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)
4. While the DTS Source and non-DAM TS Sink are in their final state:
   - DTS Source adjusts Rp as needed for offered current
   - Non-DAM TS Sink may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM
   - DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
   - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK

B.2.5.2.2 DTS Source to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Source is connected to a non-DAM TS DRP.

1. DTS Source and non-DAM TS DRP in the unattached state
   - Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK
2. DTS Source transitions from UnattachedDeb.SRC to AttachedDeb.SRC through AttachWaitDeb.SRC
   - DTS Source detects the non-DAM TS Sink's pull-downs on both CC pins and enters AttachWaitDeb.SRC. After tCCDebounce it then enters AttachedDeb.SRC
   - DTS Source turns on VBUS
3. Non-DAM TS DRP transitions from Unattached.SNK to AttachWait.SNK.
   - Non-DAM TS DRP in Unattached.SNK detects the DTS Source's pull-ups on both CC pins and enters AttachWait.SNK.
   - Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SNK because it does not support DAM (will not enter Attached.SNK because it does not detect SNK.Open on either pin)
4. While the DTS Source and non-DAM TS DRP are in their final state:

- DTS Source adjusts Rp as needed for offered current
- Non-DAM TS DRP may draw USB default current from DTS Source as permitted by Section 4.5.2.2 but will not enter DAM
- DTS Source monitors both CC pins for detach and when detected, enters UnattachedDeb.SRC
- Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SRC

B.2.5.2.3 DTS Sink to non-DAM TS Source Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS Source.

1. Non-DAM TS Source and DTS Sink in the unattached state
2. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC
    - Non-DAM TS Source detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.
    - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
    - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Source's pull-ups on both CC pins and enters AttachWaitDeb.SNK
    - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS Source and DTS Sink are in their final state:
    - Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
    - DTS Sink monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SNK when both CC pins go to SNK.Open

B.2.5.2.4 DTS Sink to non-DAM TS DRP Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM TS DRP.

1. DTS Sink and non-DAM TS DRP in the unattached state
    - Non-DAM TS DRP alternates between Unattached.SRC and Unattached.SNK
    - DTS Sink in UnattachedDeb.SNK
2. Non-DAM TS DRP transitions from Unattached.SRC to AttachWait.SRC
    - Non-DAM TS DRP detects the DTS Sink's pull-downs on both CC pins and enters AttachWait.SRC.
    - Non-DAM TS DRP continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
    - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS DRP's pull-ups on both CC pins and enters AttachWaitDeb.SNK
    - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS DRP and DTS Sink are in their final state:

- Non-DAM TS DRP monitors both CC pins for detach and when detected, enters Unattached.SNK
- DTS Sink monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SNK when both CC pin go to SNK.Open

B.2.5.2.5 DTS DRP to non-DAM TS Sink Behavior

The DTS DRP to non-DAM TS Sink behavior follows the flow in Section B.2.5.2.1.

B.2.5.2.6 DTS DRP to non-DAM TS DRP Behavior

The DTS DRP to non-DAM TS DRP behavior follows the flows in Section B.2.5.2.2 and Section B.2.5.2.4 depending on the role forced by the non-DAM TS DRP

B.2.5.2.7 DTS DRP to non-DAM TS Source Behavior

The following describes the behavior when a DTS DRP is connected to non-DAM TS Source.

1. DTS DRP and non-DAM TS Source in the unattached state
   - DTS DRP alternates between UnattachedDeb.SRC and UnattachedDeb.SNK
   - Non-DAM TS Source in Unattached.SRC
2. DTS DRP transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK
   - DTS DRP in UnattachedDeb.SNK detects pull-ups on both CC pins and enters AttachWaitDeb.SNK
3. Non-DAM TS Source transitions from Unattached.SRC to AttachWait.SRC
   - Non-DAM TS Source in Unattached.SRC detects pull-downs on both CC pins and enters AttachWait.SRC
   - Non-DAM TS Source continues to detect pull-downs on both CC pins and stays in AttachWait.SRC because it does not support DAM (will not enter Attached.SRC because it does not detect SRC.Rd on only one CC pin)
   - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
5. While the non-DAM TS Source and DTS DRP are in their final state:
   - Non-DAM TS Source monitors both CC pins for detach and when detected, enters Unattached.SRC
   - DTS DRP monitors VBUS for attach and both CC pins for detach and enters UnattachedDeb.SRC when both CC pin go to SNK.Open

B.2.5.2.8 DTS Sink to non-DAM TS Sink with Accessory Support Behavior

The following describes the behavior when a DTS Sink is connected to a non-DAM USB Type-C TS Sink with Accessory Support.

1. DTS Sink and non-DAM TS Sink with Accessory Support (“non-DAM TS Sink” for the remainder of this flow) in the unattached state
   - Non-DAM TS Sink alternates between Unattached.SNK and Unattached.Accessory
   - DTS Sink in UnattachedDeb.SNK
2. Non-DAM TS Sink transitions from Unattached.Accessory to AttachWait.Accessory
   - Non-DAM TS Sink detects the DTS Sink’s pull-downs on both CC pins and enters AttachWait.Accessory

- Non-DAM TS Sink continues to detect pull-downs on both CC pins and enters USB Type-C Debug Accessory Mode

3. DTS Sink transitions from UnattachedDeb.SNK to AttachWaitDeb.SNK.
    - DTS Sink in UnattachedDeb.SNK detects the non-DAM TS Sinks pull-ups on both CC pins and enters AttachWaitDeb.SNK
    - DTS Sink remains in AttachWaitDeb.SNK because it does not detect VBUS
4. While the non-DAM TS DRP and DTS Sink are in their final state:
    - Non-DAM TS Sink monitors both CC pins for detach and when detected, enters Unattached.SNK
    - DTS Sink monitors both CC pins for detach and enters UnattachedDeb.SNK when both CC pins go to SNK.Open

B.2.6 Orientation Detection

Orientation detection is optional normative. A USB Type-C port supporting Debug Accessory Mode is not required to perform orientation detection. If orientation detection is required, this method shall be followed.

B.2.6.1 Orientation Detection using Rd and/or Rp Values

In this optional normative flow, the DTS shall always initiate an orientation detection sequence, independent of its role as Source, Sink, or DRP. This means that the TS must detect this orientation sequence and perform multiplexing to orient and connect the port signals to the proper channels as well as determine the proper CC pin for *USB-PD* communication.

B.2.6.1.1 Orientation Detection with DTS as a Source

When the DTS is presenting an Rp, it shall present asymmetric Rp values (Rp1/Rp2) on CC1/CC2 to indicate orientation to the TS. The DTS as a source shall indicate a weaker resistive value on CC2. Table B-2 shows the values of Rp resistance on each CC pin to indicate orientation and advertise the USB Type-C current available on VBUS. See Table 4-24 for the Rp resistance ranges.

Once the TS sink enters the DebugAccessory.SNK state, after the vRd on both CC pins is stable for tRpValueChange, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the *USB-PD* CC communication wire. The TS Sink cannot perform *USB-PD* communication or connect any orientation-sensitive debug signals until orientation is determined.

B.2.6.1.2 Orientation Detection with DTS as a Sink

When the DTS is a sink, it shall follow a two-step approach.

1. The DTS sink shall present Rd/Rd on the CC pins of the debug accessory plug. This will put the system into debug accessory mode
2. Once the DTS sink enters AttachedDeb.SNK state, it shall present a resistance to GND of ≤ Ra on B5 (CC2)

The asymmetric signaling is detected by the TS Source in the UnorientedDebugAccessory.SRC state. Once Detected, the TS Source will move to the OrientedDebugAccessory.SRC. Once the TS source enters the OrientedDebugAccessory.SRC state, after the SRC.Ra level is detected on one of the CC pins, it will orient its signal multiplexor based on the detected orientation indicated by the relative voltages of the CC pins. The CC pin with the greater voltage is the plug CC pin, which establishes the orientation of the DTS plug in the TS receptacle and also indicates the *USB-PD* CC communication wire. The TS Source cannot perform *USB-PD* communication or connect any orientation-sensitive debug signals until orientation is determined.

B.3 Security/Privacy Requirements:

Debug port(s) typically provide system access beyond the normal operation of USB hardware and protocol. Additional protection against unintended use is needed. The design must incorporate appropriate measures to prohibit unauthorized access or modification of the unit under test and to prevent exposure of private user data on the unit under test. The method of protection is not explicitly defined in this specification.

The vendor shall assert as part of USB compliance certification that:

- The device has met the requirement to protect the system's security and user's privacy in its vendor-specific implementation of the port, and
- The device requires the user to take an explicit action to authorize access to or modification of the unit.

C USB Type-C Digital Audio

C.1 Overview

One of the goals of USB Type-C® is to help reduce the number of I/O connectors on a host platform. One connector type that could be eliminated is the legacy 3.5 mm audio device jack. While USB Type-C does include definition of an analog audio adapter accessory (see Appendix A), that solution requires a separate adapter that can be readily lost and the host implementation in support of analog audio is technically challenging. To best serve the user experience, a simplified USB Type-C digital audio solution based on native USB protocol is simpler/more interoperable with both the host platform and audio device being connected directly without the need for adapters and operates seamlessly through existing USB topologies (e.g. through hubs and docks).

This appendix is for the optional normative definition of digital audio support on USB Type-C-based products. Any USB Audio Class product, having either a USB Type-C plug or receptacle, and whether it is a host system, typically an audio source, and an audio device, typically an audio sink, shall meet the requirements of this appendix in addition to all other applicable USB specification requirements.

C.2 USB Type-C Digital Audio Specifications

USB Type-C Digital Audio (TCDA), when implemented per this specification, shall be compliant with either the USB Audio Device Class 1.0, 2.0 or 3.0 specifications as listed below. While allowed, basing a TCDA on USB Audio Device Class 1.0 is not recommended. Given the number of benefits in terms of audio profile support, simplified enumeration and configuration, and improved low-power operation, use of the USB Audio Device Class 3.0 is *strongly recommended*.

USB Audio Device Class 1.0 including:

- USB Device Class Definition for Audio Devices, Release 1.0
- USB Device Class Definition for Audio Data Formats, Release 1.0
- USB Device Class Definition for Audio Terminal Types, Release 1.0

USB Audio Device Class 2.0 including:

- USB Device Class Definition for Audio Devices, Release 2.0
- USB Device Class Definition for Audio Data Formats, Release 2.0
- USB Device Class Definition for Audio Terminal Types, Release 2.0

USB Audio Device Class 3.0 including:

- USB Device Class Definition for Audio Devices, Revision 3.0
- USB Device Class Definition for Audio Data Formats, Release 3.0
- USB Device Class Definition for Audio Terminal Types, Release 3.0
- USB Device Class Definition for Basic Audio Functions, Release 3.0

USB Audio Device Class 3.0 specifications now include the definition of basic audio function profiles (Basic Audio Device Definition, BADD). TCDA devices based on USB Audio Device Class 3.0 will implement one of the defined profiles. TCDA-capable hosts based on USB Audio Device Class 3.0 will recognize and typically implement all of the profiles that are relevant to the capabilities and usage models for the host.

TCDA devices shall fall into one of the following two configurations:

- a traditional VBUS-powered USB device that has a USB Type-C receptacle for use with a standard USB Type-C cable, or
- a VCONN-Powered USB Device (VPD) that has a captive cable with a USB Type-C plug (including thumb drive style products).

USB Type-C plug-based TCDA devices shall not be implemented as a variant of the USB Type-C Analog Audio Adapter Accessory (Appendix A).

D Thermal Design Considerations for Active Cables

D.1 Introduction

USB Type C® active cables use active circuitry to realize a longer link than passive cables and to maintain the electrical performance at high speed data transmission (*USB 3.2* Gen2 single-lane or *USB 3.2* Gen1 or Gen2 dual-lane). The additional power dissipation due to active components in the plug over-mold, creates a thermal challenge to passively dissipate power from its active components off limited outer surface area of cable over-mold. Furthermore, the VBUS current, up to 5 A for power delivery, generates joule heat from the conductors along VBUS and GND lines, including copper wires, solder joints, contact pins insides connectors and copper traces on paddle board.

This appendix provides some case studies to show the thermal impacts of certain factors affecting the maximum over-mold surface temperature TS such as IC power inside over-mold (PO), thermal boundary, VBUS current level, and port to port spacing. The case study provided is for a specific mechanical design of the cable. When a different mechanical design (geometry or material, etc.) are used, these impacts need further investigation. The methodology of the study is thermal modelling. The modeling results has been validated for some cases (1.5 W PO and 5A VBUS) with lab test results within ± 3 °C, but not for all cases. Note that this appendix is not a full factorial or complete Design of Experiment (DOE) study and whether there is interaction among any of these factors are not covered here.

To meet thermal requirements specified in Section 5.2.4.1, as well as the junction temperature T_J requirement of any active components, an active cable should be carefully designed to facilitate the desired heat flow paths. A desirable thermal resistance between powered IC to over-mold surface is achieved when neither T_S nor T_J exceeds their specifications. This appendix focuses solely on T_S as output of the study, as the T_J requirement varies depending on the IC requirements.

It is recommended that system integrator such as host or device designer should take into consideration the heat transferred to or from an active cable in the system level thermal analysis.

Nomenclature used in this appendix:

- T_A = ambient temperature (°C)
- T_J = junction temperature (°C)
- T_S = plug over-mold outer surface maximum temperature (°C)
- T_{MB} = motherboard/thermal boundary temperature (°C)
- P_O = active component power (W) inside the over-mold that directly plugged in the host or device at each end of cable.

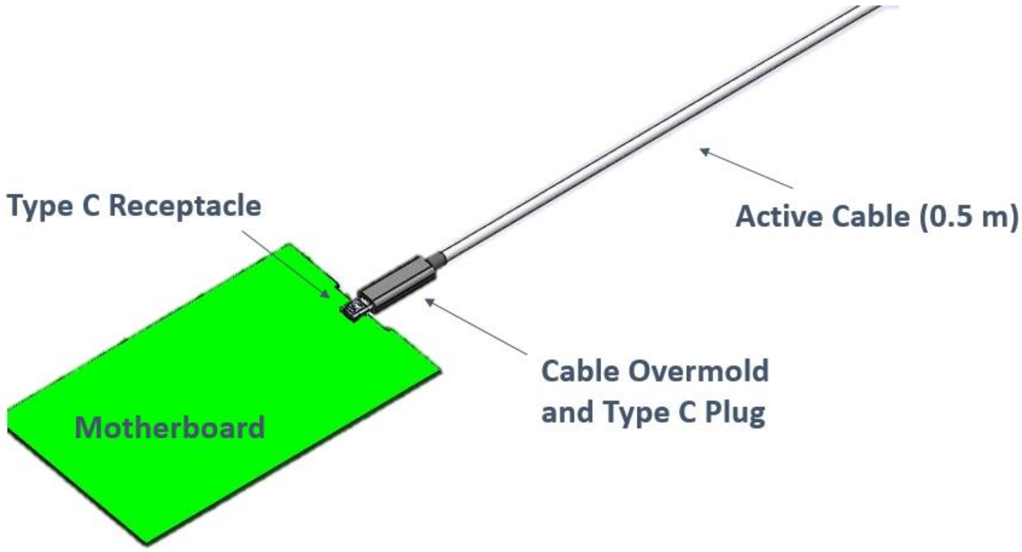
D.2 Model

D.2.1 Assumptions

A system model was built which includes a half active cable with one over-mold on the end, a mated pair of connectors (plug and receptacle) and a motherboard as its host or device side thermal boundary. The model assumes the cable is symmetric with VCONN power to be equally divided and each end of cable consumes half of VCONN power for the active components.

It is a Computational Fluid Dynamics (CFD) model with heat transfer of conduction, natural convection and radiation. Emissivity of the plug over-mold and cable jacket is assumed to be 0.92 and the connector metal surfaces is assumed to be 0.05.

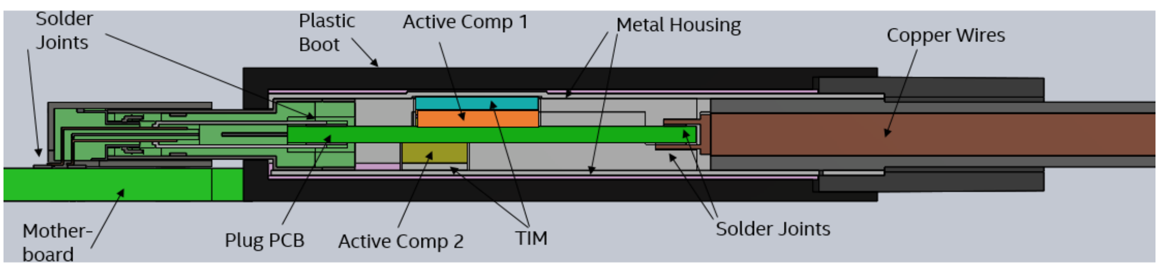
Figure D-1 Active Cable Model (Single Port, Top Mount Receptacle)



D.2.2 Model Architecture

The specific system and cable architecture used in the model is shown below.

Figure D-2 Model Architecture



The simplified cable model uses a pure copper cable, representing a typical short active cable, with total cross section of the copper conductors being about 3.8 mm^2.

The cable model incorporates a plastic boot for the over-mold which allows a higher surface temperature threshold than some other materials such as metal or glass. The over-mold length in the study was 35 mm.

In this specific cable design, two active components are surface mounted on plug PCB (or paddle board). Thermal Interface Material (TIM) are placed between "hot components" and "heat spreading material" such as metal housings to reduce thermal resistance between component junctions to ambient. Metal shells help to reduce T_S by spreading heat across the over-mold surface and avoid hot spots.

The plug PCB and motherboard are assumed to be FR4 based material. The motherboard is a bulk model assumed to be at a constant temperature without a point heat source on it. The receptacle is top mounted on the motherboard in single port and horizontal stacked cases, Figure D-6; and is vertically mounted in vertical stack up cases, Figure D-4 and Figure D-5.

D.2.3 Heat Sources

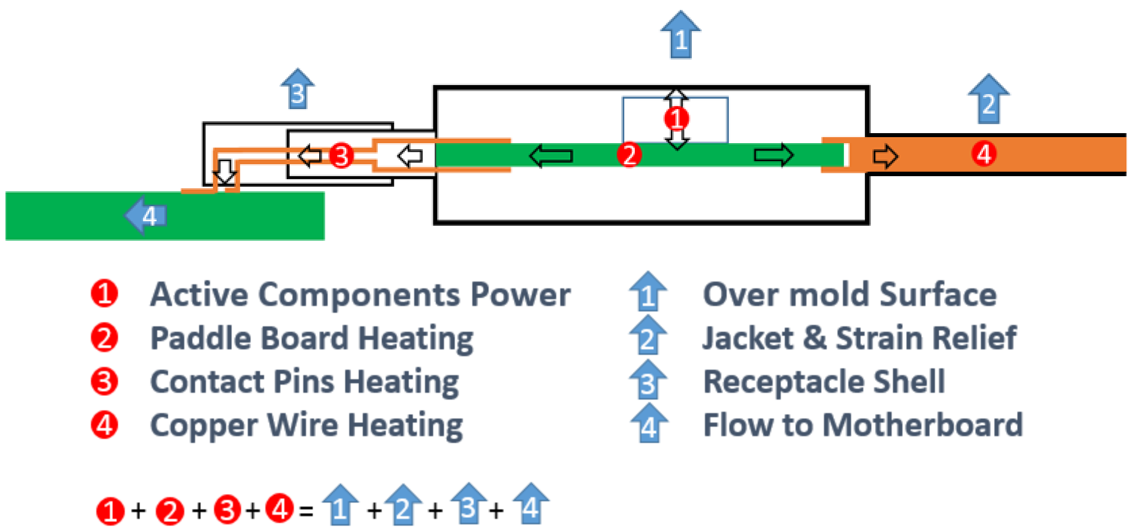
Main heat sources include:

- Active component power such as re-timer, voltage regulator, etc.; the overall power inside over-mold is P_O, which is about half of VCONN power consumed by the full cable.
- Joule heat from the any conductor that carries high current, e.g. raw cable VBUS and GND copper wire, the plug PCB copper traces, contact pins of connectors, etc.

D.2.4 Heat Flow

The main power sources and heat flow paths are illustrated in Figure D-3. The overall heat generated from the cable is mainly dissipated from over-mold surfaces, cable jacket and path to motherboard. The higher thermal resistance of one heat path, the more heat it will "push off" to other heat paths and the more risk that active component junction is overheated. Since heat flow to motherboard is not a desired path from the perspective of system design, cable and over-mold design are critical to achieve balanced heat dissipation paths so not to violate either T_S or T_J requirements.

Figure D-3 Heat Sources and Heat Flow Paths



The overall heat generated from the cable should be consistent with the overall power dissipated by the cable. An example of half a 1.0 m active cable consuming 1.5 W and sourcing 5 A VBUS is shown below:

Table D-1 Heat Sources and Heat Dissipation Example (1.5 W cable and 5 A)

(a) Heat Sources

Index	Heat Source	Power (W)
1	Active Components	0.750
2	Pin Heating	0.330
3	PCB Heating	0.135
4	Cable Heating	0.805
	Total Power Generation:	2.020

(b) Heat Dissipation

Index	Heat Source	Power (W)
1	Plug Surface	0.500
2	Cable & SR	1.120
3	Receptacle	0.050
4	Flow to Motherboard	0.350
	Total Power Dissipation:	2.020

D.3 USB 3.2 Single Lane Active Cable

Based on the assumption that VCONN power consumption is equally split between two ends of the cable and the 1 W maximum VCONN power dissipation in the USB Type-C active cable (See Table 4-5), active component power in each end or over-mold power (P_O) can go up to 0.5 W in a *USB 3.2* active cable.

D.3.1 USB 3.2 Single-Lane Active Cable Design Considerations

The active cable designer should design for T_S less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 5.5.4.

D.3.1.1 USB 3.2 Single-Lane Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-2 shows that when P_O is 0.5 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below the requirement, at both 3 A and 5 A VBUS, assuming the motherboard temperature is no higher than (T_A +25) °C.

Table D-2 USB 3.2 Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Single Lane)

	3 A VBUS	5 A VBUS
T_S (°C)	57	60

D.3.1.2 USB 3.2 Single-Lane Active Cable in a Multiple Port Configuration

When multi-port connector spacing is small, there is heat transfer between cables resulting in heat dissipation through natural convection being less effective than in the single port case. Radiation is also less effective due to the proximity of hot surfaces. This section lists a few typical 3-port configurations to show the impacts of receptacle spacing to the thermal performance of an active cable. For Figure D-4 and Figure D-5 minimum spacing center to center is 7 mm; for Figure D-6 it is 12.85 mm.

Figure D-4 Vertically Stacked Horizontal Connectors 3x1 Configuration (VERT)

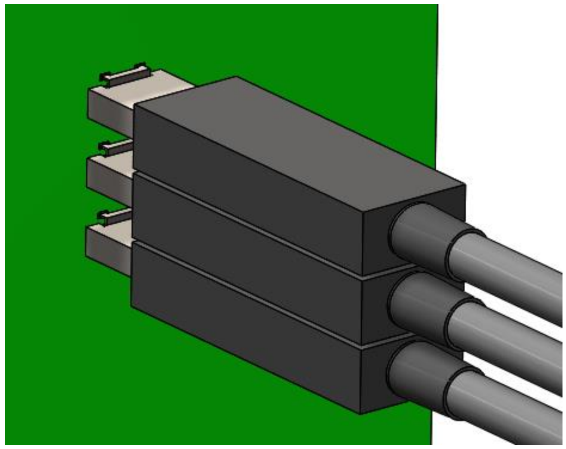


Figure D-5 Horizontally Stacked Vertical Connectors 1x3 Configuration (HZ90)

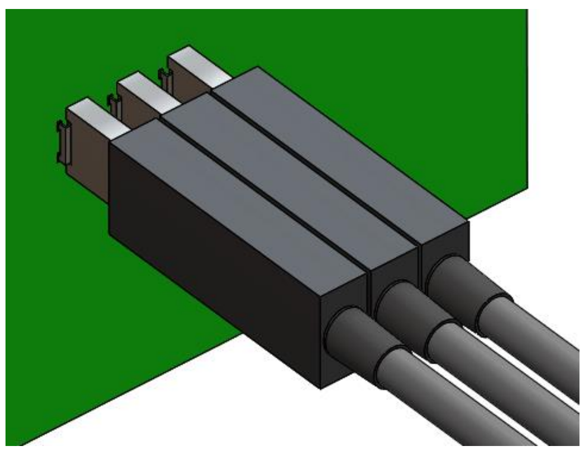
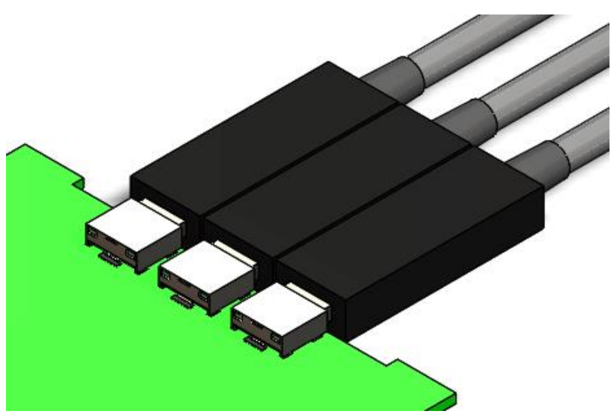


Figure D-6 Horizontally Stacked Horizontal Connector 1x3 Configuration (HORZ)

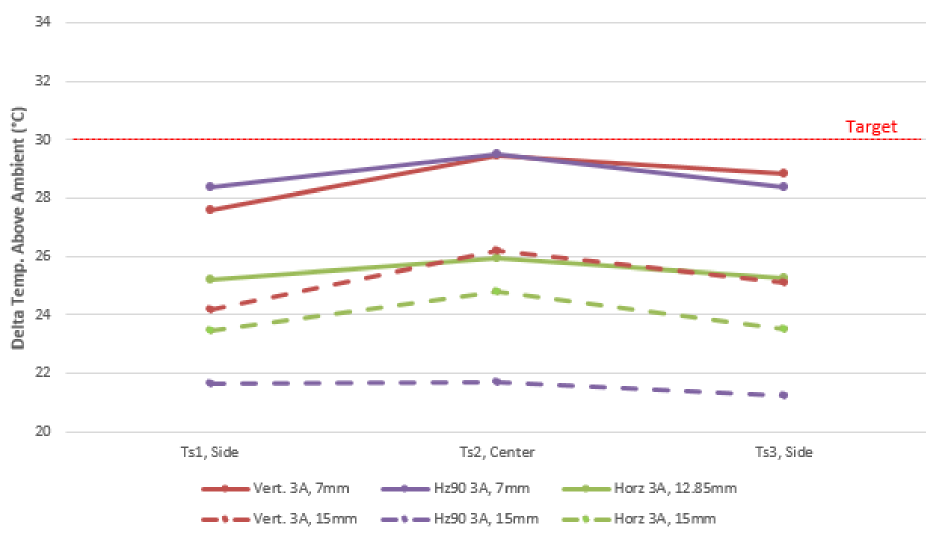


D.3.1.2.1 USB 3.2 Single-Lane 3A Active Cable in a 3-Port Configuration

When three active cables are stacked up, the port in the center position is usually in the worst situation for heat transfer. Figure D-7 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three *USB 3.2* 3A cables are plugged on a 60 °C motherboard in 35°C ambient.

In all 3-port configurations shown in Figure D-4, Figure D-5, and Figure D-6, it is achievable to keep the all three plug over-mold surface temperature T_S below the requirement, at 3 A VBUS, assuming the motherboard temperature is no higher than (T_A +25) °C. Specific cable design should be tested and validated because the margin of center port in VERT and HZ90 is less than 1 °C at minimum port spacing in thermal modeling.

Figure D-7 USB 3.2 Single-Lane 3A Active Cable in a 3-Port Configuration



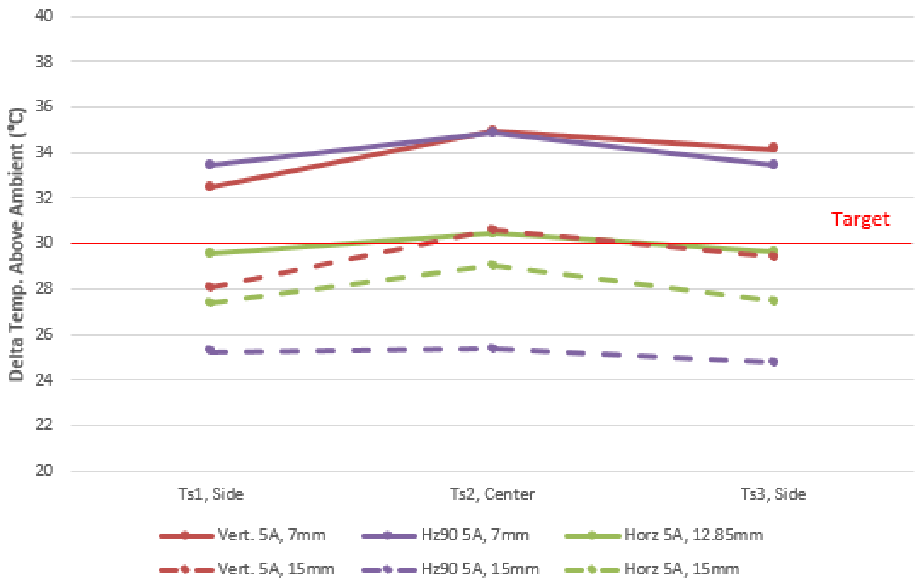
D.3.1.2.2 USB 3.2 Single-Lane 5A Active Cable in a 3-Port Configuration

Figure D-8 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three *USB 3.2* 5A cables are plugged on a 60 °C motherboard in 35 °C ambient.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. Three 5A cables at VERT and HZ90 configurations at minimum spacing could exceed the (T_A +30 °C) specification by up to 5 °C. HORZ configuration marginally meet spec on side ports but failed on center port.

Enlarging spacing between ports greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 8 °C.

Figure D-8 USB 3.2 Single-Lane 5A Active Cable in a 3-Port Configuration



D.4 Dual-Lane Active Cables

USB 3.2 defines two lanes of SuperSpeed USB data and in dual-lane operation typically has higher active component power consumption than USB 3.2 single-lane Gen2 active cables. Higher power could heat up the over-mold and raise T_S above user comfort zone when plugging or unplugging the cable.

USB 3.2 dual-lane active cable may consume up to 1.5 W of power from VCONN. This compares with the 1 W allowed for USB 3.2 single-lane active cables.

Section D.4.1 shows T_S resulting from 0.75 W over-mold power P_O in a 1.5 W dual-lane USB 3.2 active cable for a certain design, in both single-port and multiple-port configurations. Results reveals that thermal solution is necessary to meeting cable design requirements especially in multiple-port configuration.

Both over-mold power P_O and thermal boundary of the cable T_{MB} have impacts on T_S. The correlation of three are studied in Section D.4.1.2 which helps system and cable designer to take both factors into consideration.

D.4.1 USB 3.2 Dual-Lane Active Cable Design Considerations

The cable designer should design for T_S of the over-mold less than 30 °C above T_A in the condition where thermal boundary T_{MB} is of 25 °C above T_A per Section 5.5.4.

D.4.1.1 USB 3.2 Dual-Lane Active Cable in a Single Port Configuration

An active cable connected to a single port in a host or device can take full advantage of the overall plug surface area for heat dissipation. Table D-3 shows that when P_O is 0.75 W, it is achievable to keep the plug over-mold surface temperature T_S of a single cable below (T_A +30) °C at both 3 A and 5 A VBUS, assuming the motherboard temperature is no higher than (T_A +25) °C.

Table D-3 USB 3.2 Active Cable Design Single Port Case Study at 35 °C Ambient and 60 °C Thermal Boundary (Dual Lane)

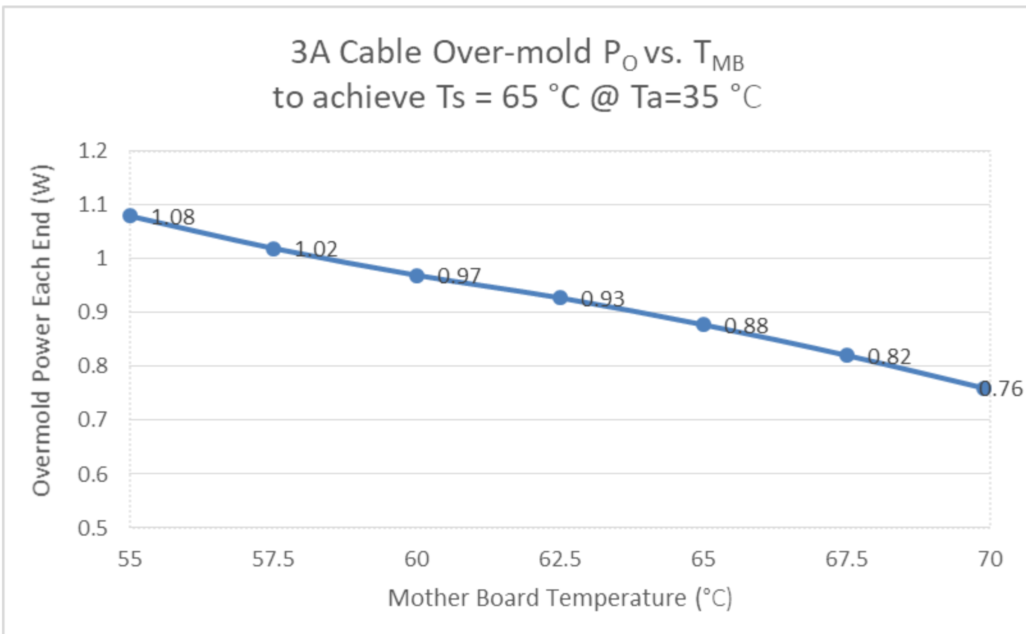
	3 A VBUS	5 A VBUS
T_S (°C)	61	64

In 5 A VBUS case, T_S is much closer to specified limit than 3 A VBUS case (Section D.3.1.1), so test and verification of thermal design is highly recommended.

D.4.1.2 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB}

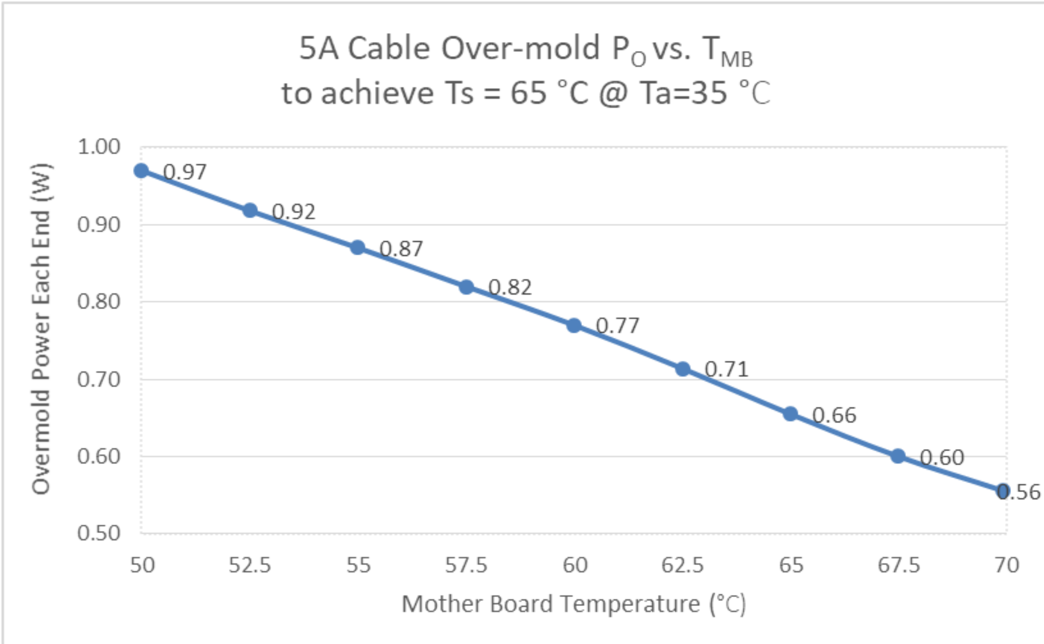
In Figure D-9, the area under graph indicate the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve $T_S < (T_A + 30)$ °C in a single port configuration in a 3 A VBUS application.

Figure D-9 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB} at 3 A VBUS in a Single Port Configuration



In Figure D-10, the area under graph indicate the combination of over-mold power P_O and thermal boundary temperature T_{MB} that can achieve $T_S < (T_A + 30)$ °C in a single port configuration in a 5 A VBUS application.

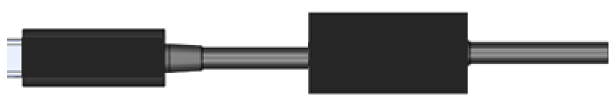
Figure D-10 Impact of Over-mold Power P_O and Thermal Boundary Temperature T_{MB} at 5 A VBUS in a Single Port Configuration



D.4.1.3 Dongle Cable

When overall active component power is higher than the maximum over-mold power P_O that could meet T_S requirement, cable may be re-designed to move the thermal load away from the USB Type-C plug over-mold such as in a dongle cable as illustrated in Figure D-11.

Figure D-11 USB 3.2 Active Cable Dongle Design (One End Shown)



The cable should be designed so that the over-mold directly plugged in the host or device dissipates no more than maximum P_O and extra heat is migrated to another part of the cable such as a dongle, so neither extra heat will flow into host and device, nor over-mold surface temperature is too hot for users to touch.

D.4.2 USB 3.2 Dual-Lane Active Cable in a Multi-Port Configuration

Multi-port connector spacing results in less effective heat dissipation by natural convection and radiation. This section lists a few typical 3-port configurations to show the impacts of receptacle spacing to the thermal performance of *USB 3.2* active cables. Naming of configurations used in this section are the same as in Section D.3.1.2.

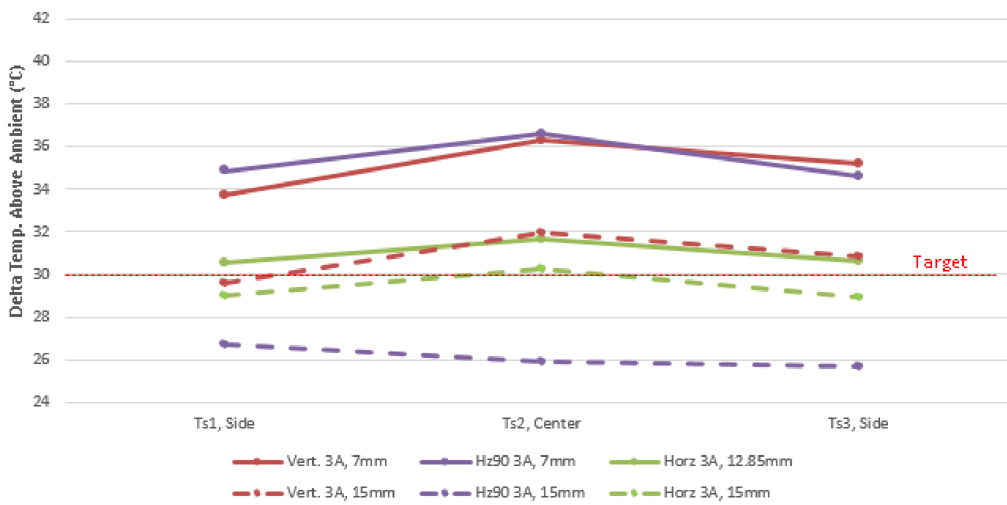
D.4.2.1 USB 3.2 Dual-Lane 3A Active Cable in a 3-Port Configuration

Figure D-12 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three *USB 3.2* dual-lane 3A VBUS and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The port in the center position is usually in the worst situation for heat transfer.

All solid lines indicate the minimum spacing cases and dash lines the enlarged spacing cases. Center port is the worst case in all configurations. T_S of center port in VERT and HZ90 configurations at minimum spacing could be more than 6 °C over the (T_A +30 °C) specification and in HORZ configuration about 2 °C over specification.

Enlarging spacing between ports could greatly reduce T_S. Especially in HZ90 configuration, spacing from 7 mm to 15 mm reduced T_S by about 11 °C, which help to reduce T_S to meet specification.

Figure D-12 USB 3.2 Dual-Lane 3A Active Cable in a 3-Port Configuration



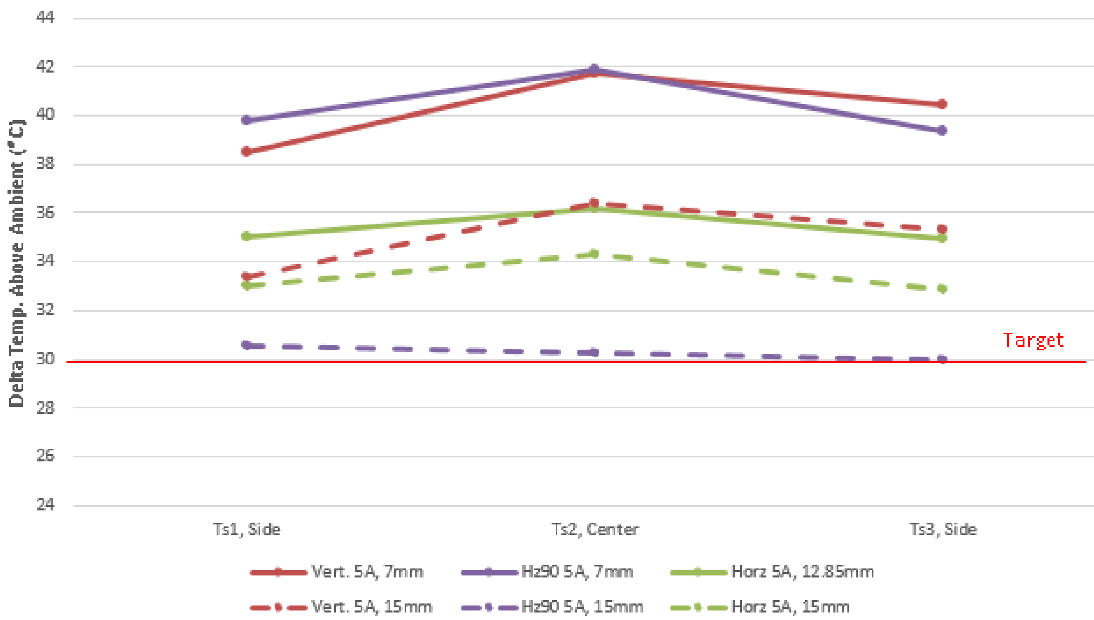
D.4.2.2 USB 3.2 Dual-Lane 5A Active Cable in a 3-Port Configuration

Figure D-13 shows the temperature difference between maximum over-mold surface temperature T_S of three ports and the ambient temperature T_A when three USB 3.2 dual-lane 5 A VBUS and 1.5 W cables are plugged on a 60 °C motherboard in 35 °C ambient. The T_S port in the center position is still the highest of all three in all cases.

In all 3-port configurations listed in Figure D-4, Figure D-5, and Figure D-6, plug over-mold surface temperature T_S of all three ports have exceeded the requirement, at 5 A VBUS, assuming the motherboard temperature is at (T_A +25) °C. T_S of center port in VERT and HZ90 configurations at minimum spacing are the highest, near 12 °C over the (T_A +30 °C) specification and in HORZ configuration about 6 °C over specification.

Enlarging spacing between ports could help reduce T_S. The largest reduction is seen in HZ90 configuration, which is near 12 °C and it brings T_S back close to target, when spacing is enlarged from 7 mm to 15 mm. However, when port spacing is not sufficient to bring T_S down to desired range, further design options in cable and host/device should be investigated.

Figure D-13 USB 3.2 Dual-Lane 5A Active Cable in a 3-Port Configuration



D.5 USB 3.2 Host and Device Design Considerations

Multi-port *USB 3.2* systems should follow the connector minimum spacing requirement defined in Section 3.10.2.

From heat flow schematics (Section D.2.4), when flow path 1 (over-mold surface dissipation) is less effective due to the limited spacing between cables, more heat would flow to motherboard and cable. It is recommended that system designer evaluate the heat flow to the system in a system level thermal analysis and provide a heat solution at the system level to reduce the motherboard temperature at these ports if necessary.

D.5.1 Heat Spreading or Heat Sinking from Host or Device

Proper thermal solutions may be needed on host or device to meet cable thermal requirements. Below are examples of placement of thermal interface material on host or device USB Type-C receptacle connector to spread heat or conduct heat away from chassis. This is to help either direct heat away from active components inside cable plug or limit amount of heat from flowing from host or device into the cable plug. Both would prevent the increased junction temperature of active components and increased cable plug surface temperature over the finger touch temperature limit. The heat management solution shown below are not limited to certain type or size.

Figure D-14 Example: Additional Heat Spreader on Receptacle in Host or Device

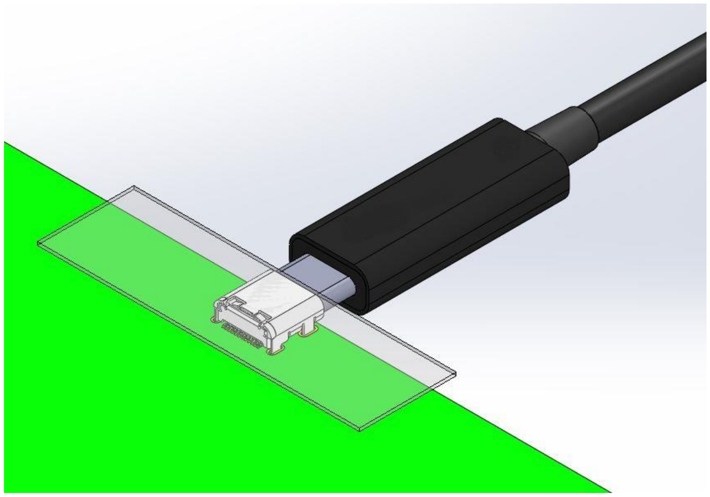
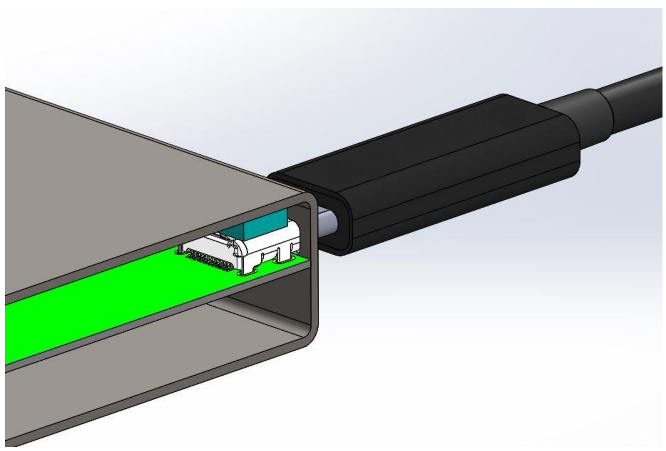


Figure D-15 Example: Heat Sinking by Chassis of Host or Device



D.5.2 Motherboard Temperature Control

Motherboard as a thermal boundary for the cable, could impact the thermal performance of cable greatly. Lowered mother temperature especially the area local around the receptacles could help reduce plug surface temperature T_S and component junction temperature T_J. See more discussion in Section D.4.1.1.

D.5.3 Wider Port Spacing for Multi-Port Applications

Wider spacing between receptacle connectors, especially when no additional heat sinking is available, is recommended for multiport application. Section D.3.1.2.1 and section D.3.1.2.2 show the impact from adjustment of port spacing.

D.5.4 Power Policies

To be added in a future update.

E Alternate Modes

All hosts and devices (except chargers and clearly marked charge-through ports) using a USB Type-C® receptacle shall expose a USB interface (minimally *USB 2.0*). In the case where the host or device optionally supports Alternate Modes:

- The host and device shall use *USB Power Delivery* Structured Vendor Defined Messages (Structured VDMs) to discover, configure and enter/exit modes to enable Alternate Modes.
- The device is strongly encouraged to provide equivalent USB functionality where such exists for best user experience.
- Where no equivalent USB functionality is implemented, the device shall provide a USB interface exposing a *USB Billboard Device Class* used to provide information needed to identify the device. A device is not required to provide a USB interface exposing a *USB Billboard Device Class* for non-user facing modes (e.g., diagnostic modes).

As Alternate Modes do not traverse the USB hub topology, they shall only be used between a host connected directly to a device.

There are Alternate Mode devices that look like a USB hub – the downstream facing ports of such devices are USB Type-C receptacles that support Alternate Modes. These devices are referred to as Alternate Mode expanders:

- The Alternate Mode port expander's downstream facing USB Type-C receptacles shall expose a USB 2.0 interface.

An Alternate Mode port expander with the capability to pass SuperSpeed USB through its upstream facing port should expose SuperSpeed USB on its downstream facing USB Type-C receptacles.

E.1 Alternate Mode Architecture

The *USB Power Delivery* Structured VDMs are defined to extend the functionality a device exposes. Only Structured VDMs shall be used to alter the USB functionality or reconfigure the pins the USB Type-C Connector exposes. Structured VDMs provide a standard method to identify the modes a device supports and to command the device to enter and exit a mode. The use of Structured VDMs are in addition to the normal *USB PD* messages used to manage power. Structured VDMs may be interspersed within the normal *USB PD* messaging stream, however they shall not be inserted in the middle of an ongoing PD power negotiation.

The Structured VDMs consist of a request followed by a response. The response is either a successful completion of the request (ACK), an indication that the device needs time before it can service a request (BUSY), or a rejection of the request (NAK). A host and device do not enter a mode when either a NAK or BUSY is returned.

Multiple modes may exist and/or function concurrently. For example, a Structured VDM may be used to manage an active cable at the same time that another Structured VDM is used to manage the device so that both the cable and device are operating in a compatible mode.

E.2 Alternate Mode Requirements

The host and device shall negotiate a *USB PD* Explicit Contract before Structured VDMs may be used to discover or enter an Alternate Mode.

The ACK shall be sent after switching to the Alternate Mode has been completed by the UFP for Enter Mode and Exit Mode requests. See Section 6.4.4 in the *USB Power Delivery Specification*.

If a device fails to successfully enter an Alternate Mode within tAMETimeout then the device shall minimally expose a *USB 2.0* interface (*USB Billboard Device Class*) that is powered by VBUS. If the device additionally supports *USB4*, then the device should defer exposing a *USB 2.0* interface (*USB Billboard Device Class*) due to an Alternate Mode timeout until the *USB4* discovery and entry process has completed (See Section 5.2.2).

When a device offers multiple modes, especially where multiple Alternate Mode definitions are needed in order to be compatible with multiple host-side implementations, successfully entering an Alternate Mode may be predicated on only one of the available modes being successfully recognized by a host. In this case, the device is not required to expose but may still expose a *USB Billboard Device Class* interface to indicate to the host the availability and status of the modes it supports.

The host may send an Enter Mode after tAMETimeout. If the device enters the mode, it shall respond with an ACK and discontinue exposing the *USB Billboard Device Class* interface. The device may expose the *USB Billboard Device Class* interface again with updated capabilities.

The current supplied over VCONN may be redefined by a specific Alternate Mode but the power shall not exceed the current rating of the pin (See Section 3.7.8.4).

E.2.1 Alternate Mode Pin Reassignment

Figure E-1 illustrates the only pins that shall be available for functional reconfiguration in a full-featured cable. The pins highlighted in yellow are the only pins that shall be reconfigured.

Figure E-1 Pins Available for Reconfiguration over the Full-Featured Cable

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	**RX2+**	**RX2−**	VBUS	**SBU1**	D−	D+	CC	VBUS	**TX1−**	**TX1+**	GND
GND	**TX2+**	**TX2−**	VBUS	VCONN			**SBU2**	VBUS	**RX1−**	**RX1+**	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Figure E-2 illustrates the only pins that shall be available for functional reconfiguration in direct connect applications such as a cradle dock, captive cable or a detachable notebook. The pins highlighted in yellow are the only pins that shall be reconfigured. Five additional pins are available because this configuration is not limited by the cable wiring.

Figure E-2 Pins Available for Reconfiguration for Direct Connect Applications

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	**RX2+**	**RX2−**	VBUS	**SBU1**	**D−**	**D+**	CC	VBUS	**TX1−**	**TX1+**	GND
GND	**TX2+**	**TX2−**	VBUS	**VCONN**			**SBU2**	VBUS	**RX1−**	**RX1+**	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

The *USB 2.0* data pins (A6, A7) shall remain connected to the USB host controller during entry, while in and during exit of an Alternate Mode except in the case of a direct connect application that remaps A6 and A7. Direct connect applications that remap A6 and A7 through the use of an Alternate Mode shall provide a USB Billboard Class device that is presented if the remapped Alternate Mode is not entered within tAMETimeout.

E.2.2 Alternate Mode Electrical Requirements

Signaling during the use of Alternate Modes shall comply with all relevant cable assembly, adapter assembly and electrical requirements of Chapter 3.

Several requirements are specified in order to minimize risk of damage to the SuperSpeed USB transmitters and receivers in a USB host or device when operating in an Alternate Mode:

- If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a captive cable, they shall be AC coupled either before or in the USB Type-C plug.
- If pin pairs B11, B10 (RX1) and A11, A10 (RX2) are used on a USB Type-C receptacle, they may be AC coupled and discharged per *USB 3.2* before the receptacle.
- AC coupling on pin pairs A2, A3 (TX1) and B2, B3 (TX2) as defined for SuperSpeed USB signaling per *USB 3.2* shall be used for Alternate Mode signaling.
- Signals being received at the USB Type-C receptacle shall not exceed the value specified for $V_{TX\text{-}DIFF\text{-}PP}$ in Table 6-18 of the *USB 3.2* specification.
- Direct Connect applications that remap pins A6 and A7 shall place pins A6 and A7 in a hi-Z state before transmitting the *USB PD* Enter_Mode command to the Sink. The Source shall not enable the alternate use of the A6 and A7 pins until an ACK has been received by the Source. In the event of a failure to enter the Alternate Mode after transmission of the *USB PD* Enter_Mode command, the Source shall restore pins A6 and A7 to the normative *USB 2.0* operation.

Direct connect applications shall ensure that any stubs introduced by repurposing the extra D+/D− pair do not interfere with USB communication with compliant hosts that short the pairs of pins together on the receptacle. This can be ensured by placing the Alternate Mode switch close to the plug, by adding inductors to eliminate the stubs at *USB 2.0* frequencies, by AC-terminating the long stubs to remove reflections at the cost of attenuated signal, or by other means.

When in an Alternate Mode, activity on the SBU lines shall not interfere with *USB PD* BMC communications or interfere with detach detection.

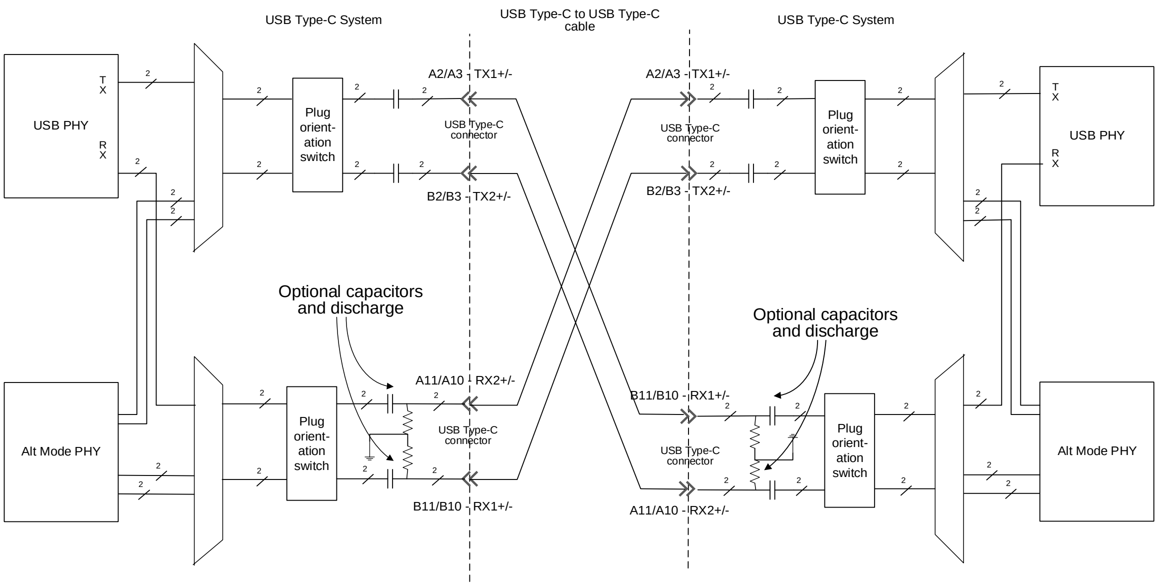
The AC coupling requirement are the same as defined in the *USB 3.2* specification. The TX signals shall be AC coupled within the system before the physical connector. The RX signals may be DC coupled or AC coupled and discharged within the system.

It should be noted that the AC coupling capacitor is placed in the system next to the USB Type-C receptacle, so that the system components (the orientation switch, the Alternate Mode selection multiplexer, and other system components) operate within the common mode limits set by the local PHY. This applies, in the SuperSpeed USB operation, to both the transmit path and the receive path within the local system. The receive path is isolated from the common mode of the port partner by the AC coupling capacitors that are implemented on the TX path in the port partner.

Figure E-3 shows the key components in a typical Alternate Mode implementation using a USB Type-C to USB Type-C full featured cable. This implementation meets the AC coupling requirements, as the capacitors required to be in or before the USB Type-C plug are implemented behind the TX pins in the port partner.

It should be noted that the AC coupling capacitor is placed in the system next to the USB Type-C receptacle, so that the system components (the orientation switch, the Alternate Mode selection multiplexer, and other system components) operate within the common mode limits set by the local PHY. This applies, in the SuperSpeed USB operation, to both the transmit path and the receive path within the local system. The receive path is isolated from the common mode of the port partner by the AC coupling capacitors that are implemented on the TX path in the port partner.

Figure E-3 Alternate Mode Implementation using a USB Type-C to USB Type-C Cable

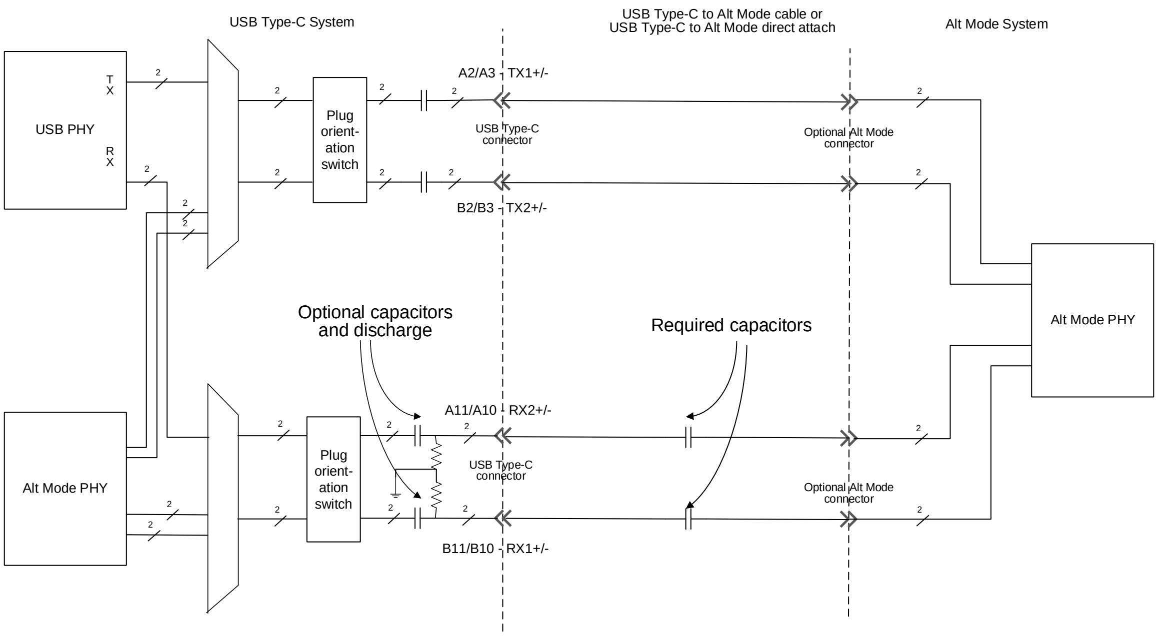


In the case where the Alternate Mode System is required to implement DC blocking capacitors within the system between active system components and the Alternate Mode connector, then this provides the necessary isolation and further capacitors in the USB Type-C to Alternate Mode adapter cable are not necessary, and may indeed impair signal integrity.

Figure E-4 shows the key components in a typical Alternate Mode implementation using either a USB Type-C to Alternate Mode connector cable, or a USB Type-C Alternate Mode Direct Attach device. In both cases it is necessary that the system path behind the RX pins on the USB receptacle be isolated from external common mode. This requirement is met by incorporating capacitors in or behind the USB Type-C plug on the Alternate Mode cable or Alternate Mode device.

In the case where the Alternate Mode System is required to implement DC blocking capacitors within the system between active system components and the Alternate Mode connector, then this provides the necessary isolation and further capacitors in the USB Type-C to Alternate Mode adapter cable are not necessary, and may indeed impair signal integrity.

Figure E-4 Alternate Mode Implementation using a USB Type-C to Alternate Mode Cable or Device



The USB Safe State is defined by the *USB PD* specification. The USB Safe State defines an electrical state for the SBU1/2 and TX/RX for DFPs, UFPs, and Active Cables when transitioning between USB and an Alternate Mode. SBU1/2 and TX/RX must transition to the USB Safe State before entering to or exiting from an Alternate Mode. Table E-1 defines the electrical requirements for the USB Safe State. See the *USB-PD* Specification for more detail on entry/exit mechanisms to the USB Safe State.

Table E-1 USB Safe State Electrical Requirements

	SBU1/2	TX[1,2]	RX[2]	A6/A7/B6/B7[4]
Common-mode voltage	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V	0 to 1.5 V
Impedance to ground[3]	< 4 MΩ	< 4 MΩ	25 KΩ – 4 MΩ	< 4 MΩ

Notes:

1. TX common-mode voltage is defined on the integrated circuit side of the AC coupling capacitors.
2. Unused TX and RX signals should transition to USB Safe State if wired to the connector but not used.
3. The DFP and UFP shall provide a discharge path to ground in USB Safe State when a connection to the USB Type-C receptacle is present.
4. Applies to docking solutions/direct connect applications that redefine pins A6, A7, B6 and B7.

E.3 Parameter Values

Table E-2 provides the timeout requirement for a device that supports Alternate Modes to enable a *USB Billboard Device Class* interface when none of the modes supported by the device are successfully recognized and configured by the DFP to which the device is attached.

Table E-2 USB Billboard Device Class Availability Following Alternate Mode Entry Failure

	Maximum	Description
tAMETimeout	1000 ms	The time between a Sink attach until a *USB Billboard Device Class* interface is exposed when an Alternate Mode is not successfully entered

While operating in an Alternate Mode, the signaling shall not cause noise ingression onto USB signals operating concurrently that exceeds the Vnoise parameters given in Table E-3.

Table E-3 Alternate Mode Signal Noise Ingression Requirements

	Limit	Bandwidth
Vnoise on BMC during BMC Active	30 mV	100 ns time constant filter
Vnoise on BMC during BMC Idle	100 mV	100 ns time constant filter
Vnoise on D+/D− (Single-ended)	40 mV	500 MHz
Vnoise on D+/D− (Differential)	10 mV	500 MHz

Note: Each Vnoise parameter is the max noise ingression level allowed onto the respective interface that is due to two SBU aggressors from the Alternate Mode signaling, under respective worse case scenarios. The coupling between SBU_A/SBU_B and CC within a USB Type-C cable shall meet the requirement described in Section 3.7.2.6.4. The coupling between SBU_A/SBU_B and USB D+/D− within a USB Type-C cable shall meet the requirement described in Section 3.7.2.6.5.

E.4 Example Alternate Mode – USB DisplayPort™ Dock

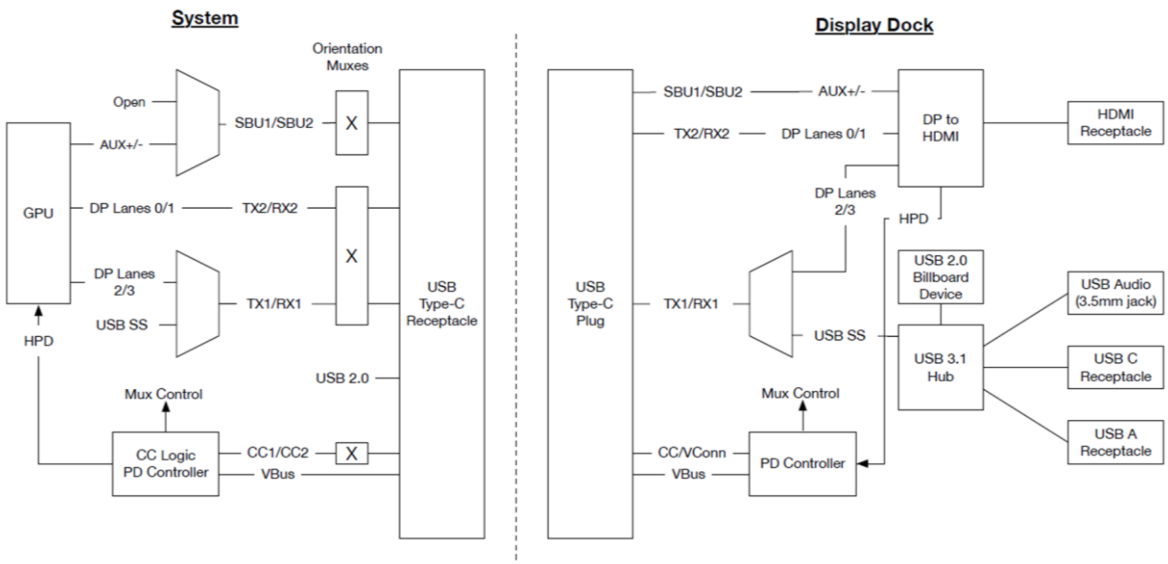
This example illustrates the use of Structured VDMs to expose and access functionality beyond the basic functionality defined by the USB Type-C Connector. The device uses its USB Type-C connector to make connection when placed in a cradle dock. This example only illustrates the functional connections.

E.4.1 USB DisplayPort™ Dock Example

- The cradle dock provides mechanical alignment and attachment in addition to those provided by the USB Type C connector allowing for only one orientation eliminating the need for an orientation MUX in the dock.
- The dock and system use *USB PD* to manage charging and power.
- The dock uses DisplayPort to drive a DisplayPort-to-HDMI adapter to support connecting an HDMI monitor.
- The dock has a USB hub that exposes two external USB ports and attached internal USB Devices, e.g. a USB audio Device (a 3.5 mm audio jack), and a USB Billboard Device.

Figure E-5 illustrates the USB DisplayPort Dock example in a block diagram form.

Figure E-5 USB DisplayPort Dock Example



The system uses USB PD Structured VDMs to communicate with the dock to discover that it supports a compatible Alternate Mode. The system then uses a Structured VDM to enter the dock mode. Since USB PD is used, it may also be used to negotiate power for the system and dock. In this example, the SuperSpeed USB signals allow the dock to work as a USB-only dock when attached to a system that does not fully support the dock or even USB PD.

E.4.2 Functional Overview

The following summarizes the behavior resulting from attaching the example USB DisplayPort Dock for three likely host system cases.

1. Host system does not support USB PD or supports USB PD without Structured VDMs
    - The host does not support USB PD, or supports USB PD but not Structured VDMs, so it will not look for SVIDs using the Structured VDM method.
    - The host will discover the USB hub and operates as it would when connected to any USB hub.
    - Since the host will not send an Enter Mode command, after tAMETimeout the dock will expose a USB Billboard Device Class interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the USB Billboard Device Class information.
2. Host system supports USB PD and Structured VDMs but does not support this specific USB DisplayPort Dock
    - The host discovers the USB hub and operates as it would when connected to any USB hub.
    - The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock may or may not be recognized by the Host.
    - If that VID is recognized by the Host, the Host then requests the modes associated with this VID. The mode associated with this USB DisplayPort Dock is not recognized by the Host.

- Since the host does not recognize the mode as being supported hence will not send the Enter Mode command, after tAMETimeout the dock will expose a *USB Billboard Device Class* interface that the host will enumerate. The host then reports to the user that an unsupported Device has been connected, identifying the type of Device from the *USB Billboard Device Class* information.

3. Host system supports this specific USB DisplayPort Dock
   - The Host looks for SVIDs that it recognizes. The VID associated with this USB DisplayPort Dock is recognized by the Host.
   - The Host then requests the modes associated with this VID. The mode associated with this USB/Display Dock is recognized by the Host.
   - Since this mode is recognized as supported, the Host uses the Enter Mode command to reconfigure the USB Type-C receptacle and enter the USB DisplayPort Dock mode.
   - The USB DisplayPort Dock may optionally expose the *USB Billboard Device Class* interface to provide additional information to the OS.

E.4.3 Operational Summary

The following summarizes the basic process of discovery through configuration when the USB DisplayPort Dock is attached to the Host.

1. Host detects presence of a device (CC pins) and connector orientation
2. Host applies default VBUS
3. Host applies VCONN because the dock presents Ra
4. Host uses *USB PD* to make power contract with the USB DisplayPort Dock
5. Host runs the Discover Identify process
   a. Sends Discover Identity message
   b. Receives an ACK message with information identifying the cable
6. Host runs the Discover SVIDs process
   a. Sends Discover SVID message
   b. Receives an ACK message with list of SVIDs for which the Dock device has modes
7. Host runs the Discover Modes process
   a. Sends Discover Modes VDM for the VIDs previously discovered
   b. Receives an ACK message with a list of modes associated with each VID
   c. If USB DisplayPort Dock mode not found, dock will timeout and present the *USB Billboard Device Class* interface and the OS will inform the user of the error - done
   d. Else
8. Host runs the Enter Mode process
   a. Sends Enter Mode VDM with VID and USB DisplayPort Dock mode
   b. Receives an ACK message – Host is now attached to the USB DisplayPort Dock and supports DisplayPort signaling to interface additional functions in combination with USB signaling

9. Host stays in the USB DisplayPort Dock mode until
    a. Explicitly exited by an Exit Mode VDM
    b. System physically disconnected from the USB DisplayPort Dock
    c. Hard Reset on *USB PD*
    d. VBUS is removed

F Thunderbolt 3 Compatibility Discovery and Entry

The *USB4™* specification includes defined support for compatibility between *USB4* products that are designed to interoperate with existing Thunderbolt™ 3 (TBT3) products. This appendix documents the normative methodology to discover and enter into TBT3 between two port partners – this methodology relies on Alternate Mode protocol as defined in Appendix E of this specification and the USB Power Delivery specification.

Thunderbolt 3 technology is organized into two primary product categories: hosts and devices. Most TBT3 devices include at least one upstream and one downstream port although a TBT3 device may include more than one downstream port in a manner similar to a hub or no downstream ports in a manner similar to a peripheral.

F.1 TBT3 Compatibility Mode Functional Requirements

In order to successfully interoperate with existing TBT3 products, the functional requirements in the following subsections must be met.

F.1.1 TBT3-Compatible Power Requirements

Before two TBT3-compatible port partners can enter TBT3 mode, a *USB PD* explicit power contract shall be established.

F.1.2 TBT3-Compatible Host Requirements

All TBT3-compatible host ports shall meet the following requirements.

- Support DRP operation
- If resolved to a UFP, use *USB PD* DR_Swap to attempt to switch into the DFP data role when DFP is preferred
- If resolved to a DFP, do not accept *USB PD* DR_Swap to remain in the DFP data role when DFP is preferred

F.1.3 TBT3-Compatible Device Upstream Requirements

F.1.3.1 Self-Powered Device

The TBT3-compatible upstream port of a self-powered device shall meet the following requirements.

- Support DRP operation
- Prefer Sink/UFP through the implementation and use of Try.SNK as needed
- If resolved to a DFP, accept *USB PD* DR_Swap to switch into the UFP data role

F.1.3.2 Bus-Powered Device

The TBT3-compatible upstream port of a bus-powered device shall meet the following requirements.

- Support Sink/UFP operation
- Reject *USB PD* DR_Swap to remain in the UFP data role

F.1.4 TBT3-Compatible Device Downstream Requirements

F.1.4.1 Self-Powered Device

The TBT3-compatible downstream stream port of a self-powered device shall meet the following requirements.

- Support DRP operation

- Prefer Source/DFP through the implementation and use of Try.SRC as needed
- If resolved to a DFP, do not accept *USB PD* DR_Swap and remain in the DFP data role

F.1.4.2 Bus-Powered Device

The TBT3-compatible downstream port of a bus-powered device shall meet the following requirements.

- Support Sink

F.1.5 TBT3-Compatible Self-Powered Device Without Predefined Upstream Port Rules

A TBT3-compatible device port may behave as either a downstream or upstream port based on its connection state to a TBT3-compatible host as described below.

- When no TBT3-compatible host is connected, the USB Type-C® ports shall:
    - Prefer to be configured as a UFP
    - Implement and use Try.SNK as needed to get into the UFP state
    - If resolved to a DFP, initiate or accept *USB PD* DR_Swap to switch to the UFP data role
    - Accept *USB PD* DR_Swap to switch to the DFP data role
    - When resolved to a UFP, identify this port as being connected to the host
        - Put the remaining downstream ports into the ErrorRecovery state.
- After a TBT3-compatible host is initially connected, the remaining downstream USB Type-C ports shall:
    - Implement and use Try.SRC as needed to get into the DFP state
    - Issue a Hard Reset if a *USB PD* DR_Swap is received when both a connection is present, and an Alternate Mode is in place
    - Issue a *USB PD* DR_Swap to switch to the DFP data role if a connection is present but no Alternate Mode has been entered (this includes performing a disconnect/reconnect on the port)
    - Accept *USB PD* DR_Swap to switch to the DFP data role if a connection is present but no Alternate Mode has been entered (this includes performing a disconnect/reconnect on the port)
- When a TBT3-compatible host that was identified as a host is disconnected, the downstream USB Type-C ports shall:
    - Enter the ErrorRecovery state
    - Behave as if no host is connected

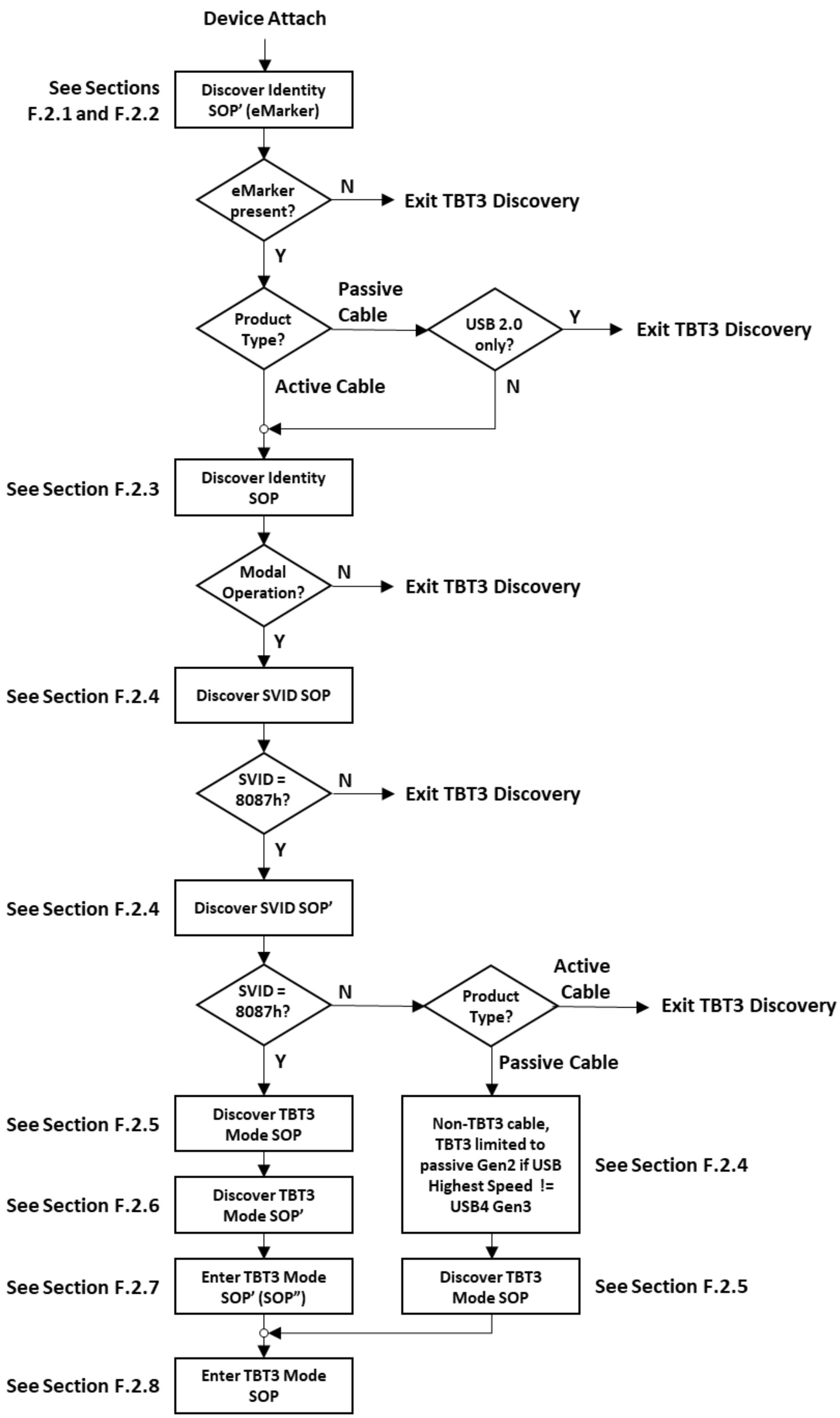
F.1.6 TBT3-Compatible Devices with a Captive Cable

TBT3-compatible devices with a captive cable shall respond to *USB PD* messages both SOP and SOP’.

F.2 TBT3 Discovery and Entry Flow

Figure F-1 describes the flow for a TBT3-compatible DFP port to discover and enter into the TBT3 Compatibility Mode of USB4 with a connected UFP. For each functional block, refer to the sub-sections identified for additional details.

Figure F-1 TBT3 Discovery Flow



F.2.1 TBT3 Passive Cable Discover Identity Responses

Table F-1, along with Table F-2 and Table F-3, defines the expected Discover Identity VDO responses for a TBT3 passive cable. In fields where multiple values are listed, cable responses may vary to match the specific connected cable's capabilities.

Table F-1 TBT3 Passive Cable Discover Identity VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	**Value**	**Parameter**
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	011b = Passive Cable	Product Type (Cable Plug)
B26	1 = Modal Operation	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Passive Cable VDO		
Depending on USB PD Specification Revision: See Table F-2 for USB PD Revision 2.0 or Table F-3 for USB PD Revision 3.0		

Table F-2 TBT3 Passive Cable VDO for USB PD Revision 2.0, Version 1.3

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed	SSTX2 Directionality Support
B8	0 = Fixed	SSRX1 Directionality Support
B7	0 = Fixed	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No	SOP" controller present
B2…0	010b = [USB 3.1] Gen1 and Gen2	SuperSpeed USB Signaling Support

Table F-3 TBT3 Passive Cable VDO for USB PD Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	000b = Version 1.0	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m) 0010b – 10ns to 20ns (~2m)	Cable Latency
B12…11	00b = VCONN not required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8…7	00b	***Reserved***
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4…3	00b	***Reserved***
B2…0	010b = [USB 3.2] Gen1 and Gen2	SuperSpeed USB Signaling Support

F.2.2 TBT3 Active Cable Discover Identity Responses

Table F-4, along with Table F-5, Table F-6 and Table F-7, defines the expected Discover Identity VDO responses for a TBT3 active cable. In fields where multiple values are listed, cable responses may vary to match the specific connected cable's capabilities.

Table F-4 TBT3 Active Cable Discover Identity VDO Responses

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	5…6	0…7	1 = Cable Plug		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	**Value**	**Parameter**
ID Header VDO		
B31	0	USB Communications Capable as USB Host
B30	0	USB Communications Capable as a USB Device
B29…27	100b = Active Cable	Product Type (Cable Plug)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	000b	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice
Active Cable VDO 1		
Depending on USB PD Specification Revision: See Table F-5 for USB PD Revision 2.0 or Table F-6 for USB PD Revision 3.0		
Active Cable VDO 2		
Applicable only for USB PD Revision 3.0 – See Table F-7		

Table F-5 TBT3 Active Cable VDO for USB PD Revision 2.0, Version 1.3

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	0001b – <10ns (~1m)	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10	0 = Fixed	SSTX1 Directionality Support
B9	0 = Fixed 1= Configurable	SSTX2 Directionality Support
B8	0 = Fixed 1 = Configurable	SSRX1 Directionality Support
B7	0 = Fixed 1 = Configurable	SSRX2 Directionality Support
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	1 = Yes	VBUS through cable
B3	0 = No 1 = Yes	SOP' controller present
B2…0	010b = [USB 3.1] Gen1 and Gen2	SuperSpeed USB Signaling Support

Table F-6 TBT3 Active Cable VDO 1 for USB PD Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…28	0000b…1111b	HW Version
B27…24	0000b…1111b	Firmware Version
B23…21	010b = Version 1.2	VDO Version
B20	0	***Reserved***
B19…18	10b = USB Type-C	USB Type-C plug to USB Type-C/Captive
B17	0	***Reserved***
B16…13	xxxxb (e.g., 0010b – 10ns to 20ns (~2m))	Cable Latency
B12…11	11b = Both ends Active, VCONN required	Cable Termination Type
B10…9	00b = 20V	Maximum VBUS Voltage
B8	1 = Yes	SBU Supported
B7	0 = Passive 1 = Active	SBU Type
B6…5	01b = 3A 10b = 5A	VBUS Current Handling Capacity
B4	0 = No 1 = Yes	VBUS through cable
B3	0 = No 1= Yes	SOP' controller present
B2…0	010b = [USB 3.2] Gen1 and Gen2	SuperSpeed USB Signaling Support

Table F-7 TBT3 Active Cable VDO 2 for USB PD Revision 3.0, Version 1.2

Bit(s)	Value	Parameter
B31…24	xxxxxxxxb (e.g., 10101010b = 170 °C)	Maximum Operating Temperature
B23…16	xxxxxxxxb (e.g., 11010010b = 210 °C)	Shutdown Temperature
B15	0	***Reserved***
B14…12	000b ≥ 10 mW	U3 Power
B11	0	U3 to U0 Transition mode
B10…8	000b	***Reserved***
B7…6	00b	USB 2.0 Hub Hops Consumed
B5	0 = Supported	USB 2.0 Supported
B4	0 = Supported	SuperSpeed Supported
B3	1 = two lanes	SuperSpeed Lanes Supported
B2	0	***Reserved***
B1…0	00b = Gen1 01b = Gen2	SuperSpeed Signaling

F.2.3 TBT3 Device Discover Identity Responses

Table F-8 defines the expected Discover Identity VDO responses for a TBT3 device. In fields where multiple values are listed, device responses may vary to match the specific connected device's capabilities.

Table F-8 TBT3 Device Discover Identity VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	4	0…7	0 = UFP	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00001b

Bit(s)	Value	Parameter
ID Header VDO		
B31	0 or 1	USB Communications Capable as USB Host
B30	0 or 1	USB Communications Capable as a USB Device
B29…27	001b = PDUSB Hub 010b = PDUSB Peripheral 101b = Alternate Mode Adapter (AMA) 110b = VCONN-Powered USB Device (VPD)	Product Type (UFP)
B26	1 = Modal Operation Supported	Modal Operation Supported
B25…23	001b = PDUSB Hub 010b = PDUSB Host 100b = Alternate Mode Controller (AMC)	Product Type (DFP)
B22…16	0	***Reserved***
B15…0	Per vendor	USB Vendor ID
Cert Stat VDO		
B31…0	0x00000000…0xFFFFFFFF	XID assigned by USB-IF
Product VDO		
B31…16	0x0000…0xFFFF	USB Product ID
B15…0	0x0000…0xFFFF	bcdDevice

F.2.4 TBT3 Discover SVID Responses

Table F-9 defines the expected Discover SVID VDO responses for a TBT3 device or cable.

Table F-9 TBT3 Discover SVID VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	3	0…7	0 = UFP	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0xFF00	1	01b	0	000b	001b	0	00010b

Bit(s)	Value	Parameter
VDO 1		
B31…16	0x8087 = Intel/TBT3	SVID 0
B15…0	0xFF01 = VESA DP (if supported)	SVID 1
VDO 2		
B31…16	0x0000 – 0xFFFF (normally the cable manufacturer VID)	SVID 2
B15…0	0x0000 (normally)	SVID 3

If the Intel/TBT3 SVID of 0x8087 is not returned in response to the Discover SVID command, a cable is a Non-TBT3 cable.

If a Non-TBT3 cable's Product Type is Active Cable, it shall be regarded as not compatible with TBT3, and TBT3 Discovery shall exit.

If a Non-TBT3 cable's Product Type is Passive Cable, the USB Highest Speed field in the cable's Passive Cable VDO shall determine TBT3 functionality and speed. If USB Highest speed is "USB4 Gen3", the cable shall be regarded as a TBT3 capable cable at Gen3 performance. If USB Highest speed is "USB 3.2 Gen1" or "USB 3.2/USB4 Gen2", it shall be regarded as a TBT3 capable cable limited to passive Gen2 performance. If USB Highest Speed indicates "USB 2.0-only, No SuperSpeed", TBT3 Discovery shall exit.

Note: Legacy TBT3 platforms may not recognize USB4 Gen3 passive cables that don't also include the TBT3 Passive Cable Discover Identity VDOs. When this happens, the USB4 Gen3 passive cable will still function but will only be used at Gen2 speeds.

F.2.5 TBT3 Device Discover Mode Responses

Table F-10 defines the expected Discover Mode VDO responses for a TBT3 device. In fields where multiple values are listed, device responses may vary to match the specific connected device's capabilities.

Table F-10 TBT3 Device Discover Mode VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
TBT3 SOP VDO		
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25…17	000000000b	***Reserved***
B16	0 = TBT3 Adapter 1 = TBT2 Legacy Adapter	TBT Adapter
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

F.2.6 TBT3 Cable Discover Mode Responses

Table F-11 defines the expected Discover Mode VDO responses for a TBT3 cable. In fields where multiple values are listed, cable responses may vary to match the specific connected cable's capabilities.

Table F-11 TBT3 Cable Discover Mode VDO Responses

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	1 = Cable Plug	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	001b	0	00011b

Bit(s)	Value	Parameter
TBT3 SOP' VDO		
B31…26	00000000b	***Reserved***
B25	0 = Passive cable 1 = Active cable	Active_Passive
B24	0b	***Reserved***
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Plug Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0 = Non-Optical 1 = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = Reserved	TBT_Rounded_Support
B18…16	000b = Reserved 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (USB 3.2 Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = Reserved	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Notes:

1. LSRX in TBT3 is the same communication channel as SBRX in USB4.

F.2.7 TBT3 Cable Enter Mode Command

Table F-12 defines the Enter Mode Command that shall be sent to the SOP' (and if needed the SOP") of an active TBT3 cable to enable the cable for TBT3 operation.

Table F-12 TBT3 Cable Enter Mode Command

Message Header						
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**	**Spec Revision**	**Rsvd**	**Message Type**
0	1	0…7	1 = Cable Plug	10b or 01b	0	1111b

VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

F.2.8 TBT3 Device Enter Mode Command

Table F-13 defines the Enter Mode Command that shall be sent to the SOP of a TBT3 device to enable the device for TBT3 operation.

Table F-13 TBT3 Device Enter Mode Command

Message Header							
Rsvd	**Number of Objects**	**Message ID**	**Cable Plug**		**Spec Revision**	**Rsvd**	**Message Type**
0	2	0…7	0 = UFP		10b or 01b	0	1111b
VDM Header							
SVID	**VDM Type**	**VDM Version**	**Rsvd**	**Object Position**	**Command Type**	**Rsvd**	**Command**
0x8087	1	01b	0	000b	000b	0	00100b

Bit(s)	Value	Parameter
TBT3 SOP VDO		
B31	0 = Not supported 1 = Supported	Vendor specific B1
B30	0 = Not supported 1 = Supported	Vendor specific B0
B29…27	000b	***Reserved***
B26	0 = Not supported 1 = Supported	Intel specific B0
B25	0 = Passive cable 1= Active cable	Active_Passive
B24	0 = TBT3 Adapter 1 = TBT2 Legacy Adapter	TBT Adapter
B23	0 = Active with bi-directional LSRX[1] communication or when Passive 1 = Active with uni-directional LSRX[1] communication	Active Cable Link Training
B22	0 = Not re-timer 1 = Re-timer	Re-timer
B21	0 = Non-Optical 1 = Optical	Cable Type
B20…19	00b = 3rd Gen Non-Rounded TBT 01b = 3rd & 4th Gen Rounded and Non-Rounded TBT 10b…11b = Reserved	TBT_Rounded_Support
B18…16	000b = Reserved 001b = USB3.1 Gen1 Cable (10 Gbps TBT support) 010b = 10 Gbps (USB 3.2 Gen1 and Gen2 passive cables) 011b = 10 Gbps and 20 Gbps (TBT 3rd Gen active cables and 20 Gbps passive cables) 100b…111b = Reserved	Cable Speed
B15…0	0x0001 = TBT Mode	TBT Alternate Mode

Notes:

1. LSRX in TBT3 is the same communication channel as SBRX in USB4.

The values to be used when sending the TBT3 Device Enter Mode command to the SOP of a TBT3 device are determined based on information retained from earlier in the discovery flow as follows:

- B31 and B30: return the values received in the B31 and B30 fields of the TBT3 Device Discover Mode Response.
- B26: return the value received in the B26 field of the TBT3 Device Discover Mode Response.
- B25: return the value received in the B25 field of the TBT3 Device Discover Mode Response.
- B23: if using a TBT3 cable, return the value received in the B23 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.
- B22: if using a TBT3 cable, return the value received in the B22 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.
- B21: if using a TBT3 cable, return the value received in the B21 field of the TBT3 Cable Discover Mode Response, otherwise set to 0.
- B20…19: if using a TBT3 cable, return the value received in the B20…19 field of the TBT3 Cable Discover Mode Response, otherwise set to 00b.
- B18…16: if using a TBT3 cable, return the value received in the B18…16 field of the TBT3 Cable Discover Mode Response, otherwise set to 010b.

F.2.9 TBT3 Cable Functional Difference Summary

Table F-14 provides a summary of existing TBT3 cables and the unique functional differences between them.

Table F-14 TBT3 Cable Functional Difference Summary

Cable	Function					SOP' Configuration					
						ID Header VDO	Discover Mode (8087)				
	USB2	USB3	TBT3 Limitations	USB4	DP	Passive/ Active B29…27	Re-timer B22	Passive/ Active B25	Uni/Bi Directional LSRX[1] B23	Rounded/none B20…19	Optical/none B21
Passive	Yes	Yes		Yes	Yes	011b	0b	0b	N/A (0b)	N/A (0b)	0b
TBT3 Re-timer	Yes	No	TBT3 Legacy[3]	No	No	100b	1b	0b	0b	00b	0b
USB4 Re-Timer (with TBT3)	Yes	Yes		Yes	Optional	100b	1b	0b/1b	1b	01b	0b
USB4 Re-Driver (with TBT3)	Yes	Yes		Yes	Optional	011b[2]	0b	1b	1b	01b	0b
TBT3 Limit Optical	No	No	No CLx No CC[4]	No	No	100b	0b	0b	1b	00b	1b
Linear Optical Re-Driver	No	Yes		Yes	No	100b	0b	1b	1b	01b	1b

Notes:

1. LSRX in TBT3 is the same communication channel as SBRX in *USB4*.
2. This cable is an active cable, however, to support backward combability with TBT3 legacy devices, B29…27 should be set to 011b.
3. Per *USB4* Chapter 13 definition.
4. This cable does not support end-to-end USB PD communication.

Notes:

1. TBT3 Re-timer cables only support TBT3 and does not support USB4 operation.
2. All other re-timer cables are as defined in Chapter 6.
3. Limit Optical cables are as defined in Chapter 6 as optically-isolated active cables.

G Extracting Pulse Response from Sampled Data and Calculating Non-Linearity Noise

The following procedure is used to determine the linear fit pulse response and error for Linear Re-Driver (LRD) based cables.

1. The transmitter shall be configured to transmit PRBS15 pattern (as defined in *USB4* Specification section 4.2.1.3.4).

2. Extract the linear fit pulse from the measured waveform using the parameters specified in Table G-1.

3. Define an input pattern x(n) to be a single PRBS period of length Nseq and an output signal to be the captured waveform y(n), sampled at M times the signal baud rate.

4. Average the captured waveform at intervals of 2 PRBS repetitions (2·N·M samples) for filtering out uncorrelated noise.

5. Correlate the averaged waveform and the reference input pattern for extracting output signal y1(n) aligned to the input pattern x(n) (N·M samples).

6. Concatenate the post-cursor input pattern corresponding to the first waveform sample at the left of the input vector x(n), and the pre-cursor input pattern corresponding to the last waveform sample at the right of the input vector as following:

   $x_1[n]$ = [{x(N-Npost+1), x(N-Npost+2), …, x(N)}, {x(1), x(2), …, x(N)}, {x(1), x(2), …, x(Npre)}]

7. Zero pad x1(n) to yield xz(n) such that M-1 zeros are inserted between each adjacent entry, before the first entry and after the last entry of x1(n).

8. Present the output signal y1(n) as the convolution of xz(n) and FIR filter h(n) containing Ntaps·M coefficients:

   $$y_1(n) = \sum_{k=0}^{N_{taps} \cdot M} x_z(n-k) \cdot h(k)$$

   and in matrix representation:

   $$y_1^{[(N_{seq} \cdot M)\ x\ 1]} = X_z^{[(N_{seq} \cdot M)\ x\ (N_{taps} \cdot M)]} \cdot h^{[(N_{taps} \cdot M)\ x\ 1]}$$

   $$X_z = \begin{bmatrix} x_z(N_{taps} \cdot M) & x_z(N_{taps} \cdot M - 1) & \dots & x_z(3) & x_z(2) & x_z(1) \\ x_z(N_{taps} \cdot M + 1) & x_z(N_{taps} \cdot M) & \dots & x_z(4) & x_z(3) & x_z(2) \\ x_z(N_{taps} \cdot M + 2) & x_z(N_{taps} \cdot M + 1) & \dots & x_z(5) & x_z(4) & x_z(3) \\ & \vdots & & & \vdots & \\ x_z(N_{seq} \cdot M) & x_z(N_{seq} \cdot M - 1) & \dots & \multicolumn{3}{c}{x_z(N_{seq} \cdot M - N_{taps} \cdot M + 1)} \end{bmatrix}$$

9. Extract the filter h coefficients by applying least-squares fitting:

   $$h = [X_z{}^T \cdot X_z]^{-1} \cdot X_z{}^T \cdot y_1$$

   where the superscript "T" denotes the matrix transpose operation.

10. Extract the linear fitting error waveform:

    $e = y_1 - X_z \cdot h$

11. Since e has M phases, need to calculate e for each phase.

    a. Align the e vector to be in length of M*N

    b. Create a matrix $E^{[NxM]}$ such as $E = \begin{bmatrix} e_1 & e_2 & \cdots & e_M \\ e_{M+1} & e_{M+2} & \cdots & e_{2M} \\ e_{2M+1} & e_{2M+2} & \cdots & e_{3M} \\ \vdots & & & \vdots \\ e_{NM+1} & e_{NM+2} & \cdots & e_{NM+M} \end{bmatrix}$

    c. Calculate the standard deviation of each phase. $e_{std} = std(E)$

    d. $\sigma_e = \max(e_{std})$

    e. The value should be normalized to the input swing: $\sigma_e = \frac{0.4}{TX_{amp}} \cdot \sigma_e$

The following parameters shall be used in the linear fit pulse calculation:

Table G-1 Linear Fit Pulse Extraction Parameters

Parameter	Value
Ntaps	100
Npost	Ntaps – Npre – 1
Npre	5
M	8

H USB PD High-Voltage Design Considerations

This appendix considers the impact of having higher voltages across the USB Type-C interface. It addresses contact lifetime and product safety when the USB Type-C cable gets unplugged while high-voltage operation is still enabled. It is applicable for the *USB Power Delivery* defined Extended Power Range (EPR) voltages (28 V – 48 V) and the Standard Power Range (SPR) at 20 V when supply current is high.

H.1 Potential for Arcing Damage During Cable Withdrawal

Arcing can occur when the connector is unplugged if the voltage differential across the gap between the plug and receptacle VBUS contacts is greater than 12 volts. Figure H-1 shows examples of the damage that could result from arcing.

Figure H-1 Arcing Damage to USB Type-C VBUS Contacts

The following conditions can result in arcing when the cable is withdrawn:

1. Source
    - Voltage regulation when the load is suddenly removed.
2. Sink
    - Length of time for the Sink to hold the voltage on its VBUS contact.
3. Cable
    - The inductive kick on VBUS occurring in sub-100 ns.
    - Ringing on VBUS occurring in microseconds.
    - The loss of IR voltage drop from the source to the plug due to load removal occurring in 0.1 to 1 µs.

An arc can be formed when the voltage difference between the Source and Sink across the gap between connector contacts is as low as 12 volts. The arcing voltage of 12 volts only applies within a gap distance of less than 7.5 – 10 µm at normal atmospheric pressures. Above this gap distance, the arcing voltage increases significantly. Assuming 12 volts across the entire range provides significant margin for analysis and application.

H.2 Arcing During USB Type-C Cable Withdrawal

There are two separate mechanisms that can create the voltage differential necessary to arc and with enough current can potentially damage contacts through excessive heating.

1. Inductive kickback
2. Sink discharge

Even before either of these mechanisms occur, there is initial heating because of all the current being channeled through a very small contact point where the power density creates enough heat to potentially melt metal.

Inductive Kickback

The first arcing mechanism is due to inductive kickback which can readily create a voltage delta of 12 volts or more. This event starts at contact break and lasts less than approximately 100 ns. Inductive kickback induced arcing occurs at any VBUS voltage – it happens regardless of the starting DC voltage on VBUS. This arcing has not been seen to cause long term damage to USB Type-C cables in the past as the current is likely too low to super heat the metal (beyond forming a temporary micron-sized molten bridge) to a point where it is permanently destructive. Calculating the energy of the inductive arc as ½ Li^2 results in approximately 5 µjoules which is too low of an energy to damage the metal and correlates well with observation over the lifetime of USB Type-C connections in practice.

Sink Discharge

The second mechanism creating a voltage differential that can result in arcing is due to the discharge of the voltage at the Sink-side VBUS contact while the Source-side VBUS contact remains high. This arcing mechanism is the one with the most potential to create and sustain an arc at high enough current to heat and damage the connector contacts.

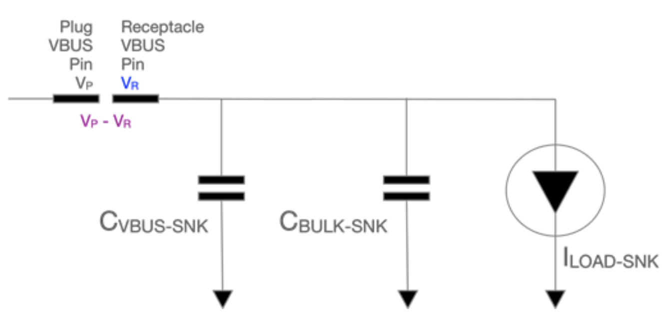
This analysis will assume that the disconnect occurs at the Sink end of a cable, but a disconnect at the Source end has the same effect.

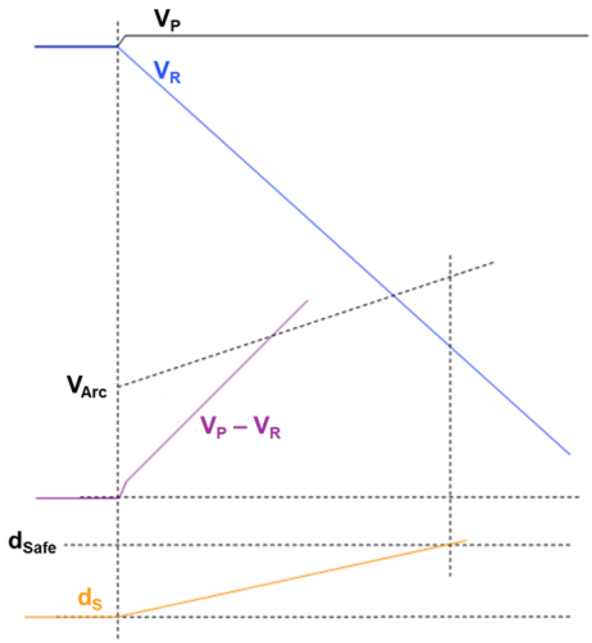
When the disconnect occurs, the Source will continue to supply power until it detects that the Sink has been disconnected which may take up to 650 ms (tVBUSOFF). The VBUS contact voltage on the Source-side may quickly (~1 µs) step up in voltage due to load regulation and the elimination of any IR voltage drop through the cable. At the same time, the Sink-side contact voltage will discharge due to the load current until the Sink detects the disconnect and removes the load. This creates a voltage difference that is increasing in time.

The withdrawal velocity is a factor in whether an arc will occur or not. If it is fast enough, then there is insufficient time to reach the voltage differential needed to form an arc. In practice, the withdrawal rate may not always be fast enough to keep the differential voltage below the threshold of arcing. In essence, there is a race between the contacts reaching a safe distance such that arcing will not occur at the voltages within the USB Type-C range and the voltage differential between the pins reaching the arcing voltage of 12 V.

Figure H-2 shows the potential for arcing due to Sink Discharge. At disconnect, the Source-side plug contact voltage V_P increases in voltage while the Sink-side receptacle contact starts decreasing in voltage, thus the differential voltage across the contact gap begins increasing. Note, the discharge rate of the Sink-side contact voltage is determined by the Sink load current and the Sink VBUS and USB PD bulk capacitance (***cSnkBulkPd***).

Figure H-2 Arcing Due to Discharge





In Figure H-2, the graph shows the voltage difference V_P–V_R reaching the potential arcing voltage V_{Arc} before the contact separation d_S reaches the safe distance d_{Safe}. This would result in an arc forming and damaging the pins if the current is sufficient.

The calculated energy of this event if V_{Arc} is 15 Volts for example for 1 ms would result in 75 milli-joules which will boil the surface of the contacts resulting in significant damage.

H.3 Mitigating Arcing Damage During Cable Withdrawal Due to Sink Discharge

The goal of arcing mitigation is not necessarily to entirely prevent arcing but to prevent damage to the connector pins due to arcing that may still occur. An arc may occur without damaging the connector pins if the energy of the arcing is sufficiently low. Experimental data suggests that arcing with a current less than 1 A does not generate enough heat to damage the connector pins.

To mitigate arcing damage due to Sink discharge, the voltage between the disconnected contacts must not reach the arcing voltage of 12 volts until the distance between the contacts reaches a safe distance or the current sinking capability of the Sink must be sufficiently low at the time of arcing. The actual arcing voltage increases significantly as the gap distance increases and is not constant and has been seen to range from 12 volts at 0 µm gap distance to as high as 300 volts with a gap distance of 7.5 – 10 µm. Assuming the minimum of 12 volts throughout gives margin and is a practical design target. Likewise, the safe distance is somewhere between 7.5 – 10 µm therefore assuming 20 µm for the following analyses gives plenty of margin.

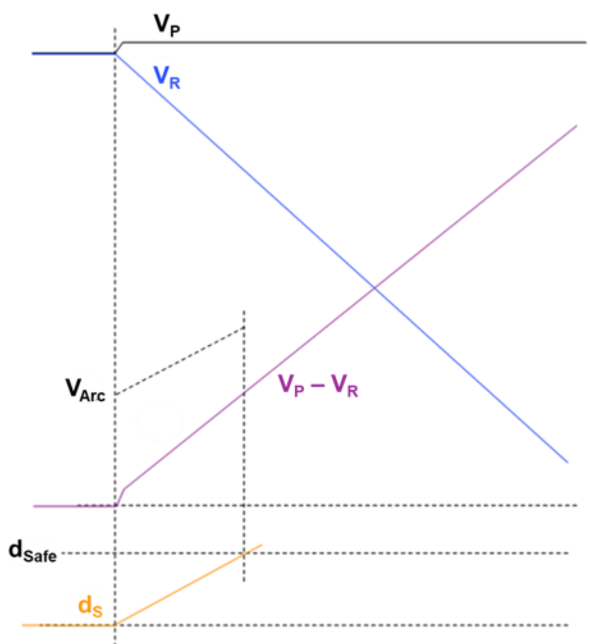
To help mitigate arcing due to Sink discharge, the Sink should manage the discharge slew rate in combination with detecting the disconnection and internally disconnecting its load. Given that it is practical, a Sink design could solely focus on limiting the slew rate to a safe level versus designing with a functional balance between the load capacitance and the time needed to detect the disconnect and remove the device's primary load. However, unplug speed and resulting distance by a human is statistical. This means that the extraction speed has a statistical chance to be very slow relative to the discharge time and has a statistical chance to stop at an unsafe distance. This means that there will always be observed arcing with enough unplug events.

The best approach is to limit the Sink discharge rate so that an arcing voltage will not be reached. While limiting the discharge speed in the Sink does mitigate the chance of an arc by itself, it should be used in conjunction with removing the load current. Both approaches are discussed in the follow examples.

H.3.1 Limiting Sink Discharge Rate

Figure H-3 shows that arcing is prevented when the discharge rate of the Sink VBUS is slow enough such that the voltage difference $V_P–V_R$ between the contacts does not reach the arcing voltage V_{Arc} before the contact distance dS reaches the safe distance d_{Safe}.

Figure H-3 Arcing Prevention During Sink Discharge by Limiting Slew Rate



The slew rate of the Sink VBUS discharge is set by the max load current in the Sink and the bulk capacitance on VBUS in the Sink. Increasing the bulk capacitance slows the discharge rate. With some limited testing, the disconnect velocity of a properly designed USB Type-C connector with retention springs has been observed to be as slow as 90 mm/s. It is assumed that there will be little degradation over lifetime due to the required minimum breaking force of the connector. The time to reach the safe distance d_S of 20 µm with a breaking velocity of 90 mm/s is 220 µs. For the timing requirement in Section 4.6.2.6, 250 µs is specified therefore in this analysis, the Sink must not discharge at a rate such that 12 V is reached before 250 µs after disconnect.

Note, the plug VBUS voltage will increase immediately at disconnect when there is load current. It must be assumed that the plug VBUS voltage may increase from being at the minimum Sink VBUS voltage for the *USB PD* contract at disconnect to the maximum Sink VBUS voltage of the *USB PD* contract minus the 750 mV defined in vSinkPD_min. This means that at disconnect, as the discharge of the Sink VBUS begins, the differential voltage may start anywhere between VSinkPD_max – VSinkPD_min.

A. Example of preventing arcing by slew rate limitation for a 20 Volt USB PD fixed contract with a max 5 A load current:

d_S = 20 µm = Safe distance to precent arcing.

V_E = 90 mm/s = Minimum contact breaking velocity.

V_{Arc} = 12 V = Minimum Arcing Voltage.

VSinkPD_max = 20 V x 1.05 = 21 V = Maximum Sink voltage at disconnect.

VSinkPD_min = 20 V x 0.95 – 750mV = 18.25V = Minimum Sink voltage at disconnect.

VDis = VSinkPD_max – VSinkPD_min = 2.75V = Maximum voltage between the contacts at disconnect.

I_{Load} = 5 A.

tSafe = d_S/ V_E = 250 µs = Time to reach the safe distance.

dV max = V_{Arc} – V_{Dis} = 12 V – 2.75 V = 9.25 V = Maximum discharge voltage before reaching V_{Arc}.

dV / dt = dV max / t_{Safe} = 9.25 V / 250 µs = 37 mV / µs = Maximum slew rate.

C_{Bulk} = I_{Load} / (dV / dT) = 5 A / 37 mV/µs = 135 µF.

In this first example, the Sink Bulk Capacitance to prevent the arcing voltage from being reached before the contacts are at a safe distance is 135 µF.

B. Example of preventing arcing by slew rate limitation for a USB PD EPR 48V contract operating at 48 V with a max 5 A load current:

In this example, the analysis is essentially the same as the first example but using the highest voltage request for the given EPR voltage range, in this case 48 volts.

With all other parameters and assumptions remaining the same, the follow adjustments are made:

VSinkPD_max = 48 V x 1.05 = 50.4 V.

VSinkPD_min = 48 V x 0.95 – 750mV = 44.85 V.

V_{Dis} = VSinkPD_max – VSinkPD_min = 5.55 V.

dV max = V_{Arc} – V_{Dis} = 12 V – 5.55 V = 6.45 V

dV / dt = dV max / t_{Safe} = 6.45 V / 250 µs = 25.8 mV / µs.

C_{Bulk} = I_{Load} / (dV / dT) = 5 A / 25.8 mV/µs = 194 µF.

In this second example, the Sink Bulk Capacitance to prevent the arcing voltage from being reached before the contacts are at a safe distance is 194 µF.

Note, due to the nature of *USB PD* contracts, the starting differential voltage between the contacts V_{Dis} at disconnect increases with increasing nominal or variable contract. This results in the dV max being lower as contract voltage gets higher. Thus, higher contract voltages will need to slow down the slew rate with higher C_{Bulk} or lower I_{Load}.

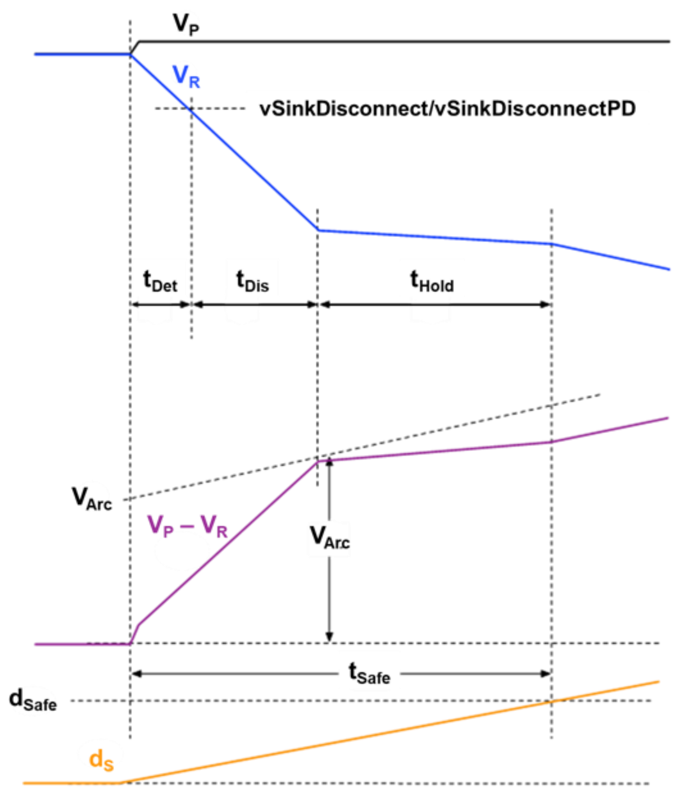
H.3.2 Load Removal

Quickly detecting the disconnect and reducing the Sink's primary load is an alternative to simply relying on managing the slew rate via adjusting the load capacitance. Based on the Sink requirements given in Section 4.6.2.6, the method analysis that follows is for detecting disconnect by the Sink based on monitoring the VBUS voltage for a drop to below the defined value for vSinkDisconnectPD and disconnecting the Sink's primary load to reduce the current that flows through the arc if an arc occurs.

Note: As a secondary method and in addition to monitoring the VBUS voltage for disconnect, monitoring the CC voltage may give the earliest indication of disconnection – this is due to the CC contacts separating before the VBUS contacts in the connector design. The amount of time between VBUS and CC contact breaks depends upon the relative distance between the VBUS contact and the CC contact in the receptacle and the extraction speed. To make CC detection of the unplug most effective, a receptacle with a distance of at least 0.3 mm should be used (see Figure 3-1). For example, a system with at least 100 µF operational capacitance that only transmits mandatory *USB PD* messages (durations < 1.6 ms) and debounces the CC pin for no more than 200 µs will detect the detach before the VBUS contact breaks if it uses a 0.3 mm receptacle.

Figure H-4 shows an alternative to increasing the capacitance relative to the load current. In this example, the Sink detects the disconnect using vSinkDisconnect or vSinkDisconnectPD depending on the contract type to disconnect the load before V_{Arc} is reached.

Figure H-4 Arcing Prevention During Sink Discharge by Load Removal



In this example, three timings are introduced. t_{Det} is the time from disconnect to reaching the minimum detection voltage. t_{Dis} is the remaining time for the Sink VBUS to discharge after reaching the minimum detection voltage t_{Det}. The sink must remove the load current within t_{Dis} to stop the discharge before the differential voltage between the contacts reaches V_{Arc}. tHold is the remaining time the discharge of VBUS must be halted or reduced such that V_{Arc} is not reached until t_{Safe} is has expired.

A. Example of preventing arcing by load removal for a 20 Volt USB PD fixed contract with a max 5 A load current:

In this analysis, some values are identical to the Limiting Sink Discharge example.

d_S = 20 µm.

V_E = 90 mm/s.

V_{Arc} = 12 V.

VSinkPD_max = 21 V.

VSinkPD_min = 18.25 V.

V_{Dis} = 2.75 V.

I_{Load} = 5 A.

t_{Safe} = 250 µs.

dV max = 9.25 V – 1 V = Maximum discharge voltage with 1 V margin before reaching V_{Arc}.

In this case, 1 V margin as been added to ensure that the sink disconnects before reaching V_{Arc}.

C_{Bulk} = 20 µF = Bulk capacitance in Sink.

In this case, C_{Bulk} is chosen to be lower than the previously calculated minimum bulk capacitance to prevent arcing by slow discharge.

dV / dt = I_{Load} / C_{Bulk} = 5 A / 20 µF = 250 mV/µs = Maximum slew rate.

Based on this maximum slew rate, the sum of (t_{Det} + t_{Dis}) can be calculated. The voltage detector and load disconnect switch can vary by implementation but the sum of these two processes need to occur within this calculated total.

(t_{Det} + t_{Dis}) = dV max / (dV / dt) = 8.25 V / 250 mV/µs = 33 µs = time from contact disconnect to removing the load.

t_{Hold} = t_{Safe} – (t_{Det} + t_{Dis}) = 250 µs – 33 µs = 217 µs.

In this example, to prevent arcing when the bulk capacitance is 20 µF, which is not enough to keep the differential voltage between the contacts from reaching the arcing voltage V_{Arc} before the contacts reach a safe distance, the load must be removed within 33 µs after VBUS contacts start to disconnect and must be held from reaching the arcing voltage for another 217 µs.

B. Example of preventing arcing by load removal for a USB PD EPR 48V contract operating at 48 V with a max 5 A load current:

In this example, the analysis is essentially the same as the first example but using the highest voltage request for the given EPR voltage range, in this case 48 volts. In this example, the bulk capacitance used has been increased to better illustrate balancing the mitigation approach between limiting Sink discharge rate and Sink load removal.

With all other parameters and assumptions remaining the same, the follow adjustments are made:

VSinkPD_max = 48 V x 1.05 = 50.4 V.

VSinkPD_min = 48 V x 0.95 – 750mV = 44.85 V.

V_{Dis} = VSinkPD_max – VSinkPD_min = 5.55 V.

dV max = V_{Arc} – V_{Dis} – 1 V = 12 V – 5.55 V – 1 V= 5.45 V (includes the 1 V margin)

C_{Bulk} = 100 µF = Bulk capacitance in Sink.

dV / dt = I_{Load} / C_{Bulk} = 5 A / 100 µF = 50 mV/µs

(t_{Det} + t_{Dis}) = dV max / (dV / dt) = 5.45 V / 50 mV/µs = 109.0 µs

t_{Hold} = t_{Safe} – (t_{Det} + t_{Dis}) = 250 µs – 109.0 µs = 141.0 µs.

The slew rate in this example assumes the bulk capacitance is 100 µF resulting in the load removal to be completed within 109.0 µs and the needed hold time of 141.0 µs.

If the bulk capacitance were to be increased to 194 µF as calculated in the limiting Sink discharge rate Example B in Section H.3.1, the slew rate would decrease to 25.8 mV/µs resulting in the load removal needing to be completed within 211.2 µs and the hold time decreased to 38.8 µs.

H.3.3 Limiting Source Current Capability

To further aid in mitigating the chance of damage from an arc, the Source should monitor for disconnect and remove the sourcing capability as well as source bulk capacitance as quickly as possible. Since the source does not have a mechanism to see the sink-side voltage, it has no direct way to determine when it should have the source and bulk capacitance disconnected from VBUS. The faster the removal of the source and bulk capacitance, the less chance there is for damage from an arc.

The simplest mechanism for detecting the disconnect is the defined monitoring of the CC voltage. Note, when the source is transmitting *USB PD* traffic, it cannot detect the disconnect with the CC voltage until the transmitted packet is finished. *USB PD* transmission from the source should be a relatively low percentage of connect time resulting in a statistically low chance of hitting this scenario. Combined with the Sink properly removing the load current for arc mitigation further reduces the chance. Another mechanism for detecting disconnect would be to monitor the load drop on VBUS. A disconnect load drop is much faster than the allowed load step from a sink defined in *USB PD*. Detection circuity can be added that distinguishes the faster load drop such that the disconnect can be detected during *USB PD* traffic transmission.