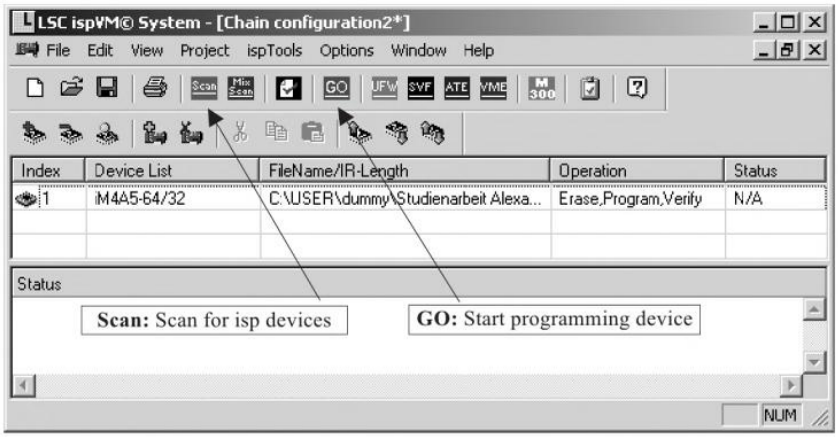

Fig. 29.2.44. ispVM-System

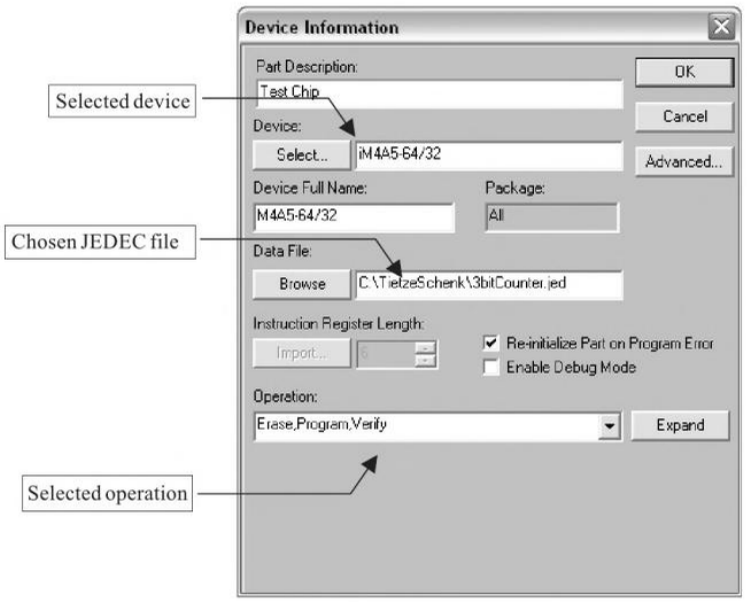

Fig. 29.2.45. JTAG Part Properties

the JTAG connection the download cable has a 10-pin socket like those commonly used on interface cables for PC mainboards. The matching 10-pin plug is located on the printed board of the PLD to be programmed. The names and meaning of the signals in the JTAG interface are listed in Fig. 29.2.43. As seen in our example, the TRST and the ENABLE signals are not required in many PLDs.

To program a device start the program ispVM (Fig 29.2.44).

- At first install the download-cable, insert the PLD and switch the power on for the board.
- Press the "Scan" button in Fig. 29.2.44. Now all PLDs in the chain of the circuit are scanned and displayed in the right order.
- Double click on the Device in the list to be changed. Insert in the dialog the information on the Device by choosing Select (resulting in the menu in Fig. 29.2.46), the Data File (JEDEC-file) and programming operation as seen in Fig. 29.2.45.

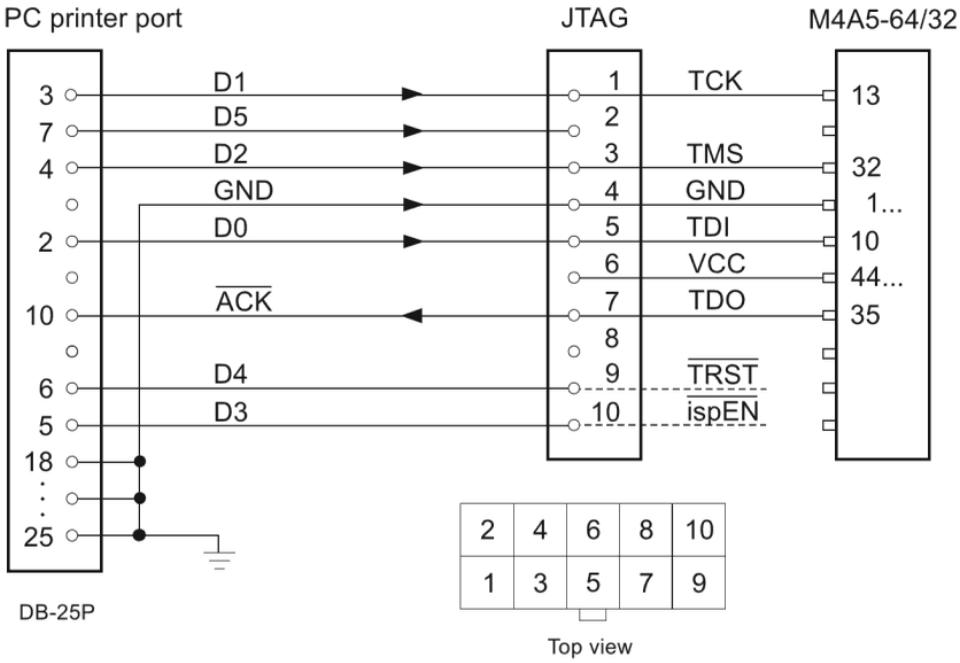

Fig. 29.2.42. Passive JTAG download cable with connections according to Lattice

as is the case with the chip from the ispM4A family used in our example. Programming is done via the standardised JTAG interface[1] which is also used to test the circuits.

To program the component all you need is a download program to transfer the JEDEC file to the chip via a download cable. The download program for Lattice-products is named ispVM. ispLEVER software contains the download program ispVM which uses the parallel port (printer interface). The necessary connections are shown in Fig. 26.2.42.

A download cable can be ordered from Lattice under the order number HW-DL-3C and is used to connect the PC parallel interface to the standardised JTAG plug on the printed board of the PLD. As an extra measure, the Lattice cable also features integrated drivers (74VHC244) to guarantee the correct levels at the PLD even in unfavourable conditions. In most cases a simple passive cable like the one shown in Fig. 29.2.42 is sufficient. For

JTAG pin	Signal name	Meaning
1	TCK	Test clock
2		not used
3	TMS	Test mode select
4	GND	Ground
5	TDI	Test data in
6	VCC	Interface supply
7	TDO	Test data out
8		not used
9	TRST	Test reset
10	ispEN	Enable programming

Fig. 29.2.43. Signals in the JTAG connector

[1] IEEE 1149.1 Boundary Scan Test Interface from the Joint Test Action Group (JTAG)