The standard shipping condition for both the D-Flash and P-Flash memory is erased with security disabled. However it is recommended that each block or sector is erased before factory programming to ensure that the full data retention capability is achieved. Data retention time is measured from the last erase operation.

**Table A-20. NVM Reliability Characteristics**

| Conditions are shown in Table A-4 unless otherwise noted | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| | | **P-Flash Arrays** | | | | | |
| 1 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[1] after up to 10,000 program/erase cycles | $t_{PNVMRET}$ | 15 | 100[2] | — | Years |
| 2 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[3] after less than 100 program/erase cycles | $t_{PNVMRET}$ | 20 | 100[2] | — | Years |
| 3 | C | P-Flash number of program/erase cycles (-40°C ≤ tj ≤ 150°C) | $n_{PFLPE}$ | 10K | 100K[3] | — | Cycles |
| | | **D-Flash Array** | | | | | |
| 4 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[3] after up to 50,000 program/erase cycles | $t_{DNVMRET}$ | 5 | 100[2] | — | Years |
| 5 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[3] after less than 10,000 program/erase cycles | $t_{DNVMRET}$ | 10 | 100[2] | — | Years |
| 6 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[3] after less than 100 program/erase cycles | $t_{DNVMRET}$ | 20 | 100[2] | — | Years |
| 7 | C | D-Flash number of program/erase cycles (-40°C ≤ tj ≤ 150°C) | $n_{DFLPE}$ | 50K | 500K[3] | — | Cycles |
| | | **Emulated EEPROM** | | | | | |
| 8 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[1] after spec. program/erase cycles | $t_{EENVMRET}$ | 5[4] | 100[2] | — | Years |
| 9 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[3] after less than 20% spec.program/erase cycles. (e.g. after <20,000 cycles / Spec 100,000 cycles) | $t_{EENVMRET}$ | 10 | 100[2] | — | Years |
| 10 | C | Data retention at an average junction temperature of $T_{Javg}$ = 85°C[3] after less than 0.2% spec. program/erase cycles (e.g. after < 200 cycles / Spec 100,000 cycles) | $t_{EENVMRET}$ | 20 | 100[2] | — | Years |
| 11 | C | EEPROM number of program/erase cycles with a ratio of EEE_NVM to EEE_RAM = 8 (-40°C ≤ tj ≤ 150°C) | $n_{EEPE}$ | 100K[4] | 1M[5] | — | Cycles |
| 12 | C | EEPROM number of program/erase cycles with a ratio of EEE_NVM to EEE_RAM = 128 (-40°C ≤ tj ≤ 150°C) | $n_{EEPE}$ | 3M[4] | 30M[5] | — | Cycles |
| 13 | C | EEPROM number of program/erase cycles with a ratio of EEE_NVM to EEE_RAM = 16384[6] (-40°C ≤ tj ≤ 150°C) | $n_{EEPE}$ | 325M[4] | 3.2G[5] | — | Cycles |

1. $T_{Javg}$ does not exceed 85°C in a typical temperature profile over the lifetime of a consumer, industrial or automotive application.
2. Typical data retention values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines Typical Data Retention, please refer to Engineering Bulletin EB618
3. $T_{Javg}$ does not exceed 85°C in a typical temperature profile over the lifetime of a consumer, industrial or automotive application.
4. This represents the number of writes of updated data words to the EEE_RAM partition. Minimum specification (endurance and data retention) of the Emulated EEPROM array is based on the minimum specification of the D-Flash array per item 6.

5. This represents the number of writes of updated data words to the EEE_RAM partition. Typical endurance performance for the Emulated EEPROM array is based on typical endurance performance and the EEE algorithm implemented on this product family. Spec. table quotes typical endurance evaluated at 25°C for this product family.
6. This is equivalent to using a single byte or aligned word in the EEE_RAM with 32K D-Flash allocated for EEEPROM

The number of program/erase cycles for the EEPROM/D-Flash depends upon the partitioning of D-Flash used for EEPROM Emulation. Defining RAM size allocated for EEE as EEE-RAM and D-Flash partition allocated to EEE as EEE_NVM, the minimum number of program/erase cycles is specified depending upon the ratio of EEE_NVM/EEE_RAM. The minimum ratio EEE_NVM/EEE_RAM =8.

**Figure A-2. Program/Erase Dependency on D-Flash Partitioning**