Paralleling of IGBTs

AND9100/D

Introduction

High power systems require the paralleling of IGBTs to handle loads well into the 10's and sometimes the 100's of kilowatts. Paralleled devices can be discrete packaged devices, or bare die assembled within a module. This is done for reasons of obtaining higher current ratings, thermal improvements, and sometimes for redundancy. Part-to-part process variations as well as layout variations, affect the static and dynamic current sharing of paralleled devices. It is important for the system design engineer to understand these issues so that a reliable system design can be achieved.

This paper will examine the types of variations due to process and temperature, and how they affect the power sharing of IGBTs. It will look at some empirical data and the implications on power sharing. The differences between IGBT modules and the paralleling of individually packaged IGBTs will also be examined.

The ability to share losses equally, is the primary goal in an application that requires paralleled IGBTs. If losses are not equally shared, the thermal differences between the devices will lead to other problems and the possible failure of the transistors. The imbalances come from two sources. Those internal to the IGBT are dealt with by selecting an appropriate device and those external to the IGBT are handled by good system design. This paper will address both of those sources.

Static Variations

There are two parameters that are important to understand from a static consideration of the IGBT. These are, the variation in $V_{CE(SAT)}$ and the variation in the transconductance during first quadrant operation (see Figures 2 and 3).

$V_{CE(SAT)}$ is an important parameter as it controls the conduction losses of the IGBT which are a significant contribution to the overall losses and therefore the heat dissipation of the device. $V_{CE(SAT)}$ is normally specified at 25°C, the rated junction temperature and sometimes a third temperature. In general, typical and maximum values are given at 25°C and a typical value only, at other temperatures.

The transconductance also varies from device-to-device. This parameter is defined as the change in collector current for the change in gate voltage. It is by no means a constant and a typical curve is normally shown in the data sheet. It can be seen from the graph in Figure 1 that it also varies with temperature. Variations in transconductance equate to variations in $V_{CE(SAT)}$.

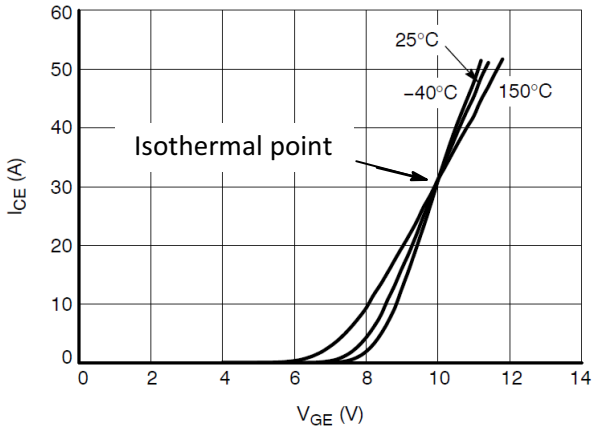

Figure 1. Typical IGBT Transfer Characteristics V_{GE} = 20 V

The $V_{CE(SAT)}$ of the IGBT is the primary static parameter to use when calculating static variations as it directly relates to the conduction loss of the transistor. The transconductance is generally specified as a typical value only, so no information is available regarding the part-to-part variation. The $V_{CE(SAT)}$ however, is normally specified over a range of temperatures, and part variation data is available also. Most manufacturers give only the typical and maximum values at 25°C; however, **onsemi** specifies minimum and maximum values on IGBTs that are normally used in parallel applications. While the minimum $V_{CE(SAT)}$ is not of great importance for single devices, it is extremely useful when paralleling devices as this allows this loss to be analyzed in detail with specific limits.

Although the temperature coefficient has not yet been discussed, it should be noted that since non punch through IGBTs have a positive temperature coefficient, differences in $V_{CE(SAT)}$ will be minimized when a temperature imbalance occurs due to the heating of the IGBT with the lower saturation voltage.

The other static variation is the forward drop of the anti-parallel rectifier. In most hard-switching applications diodes are necessary to conduct third quadrant current.

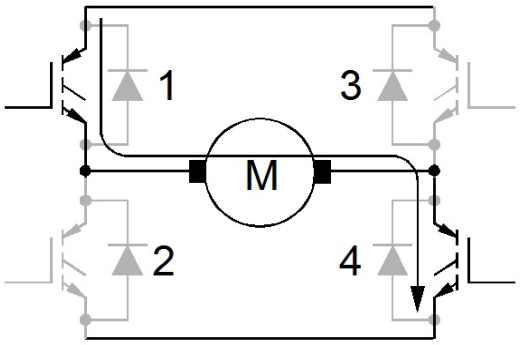

Figure 2. First Quadrant Conduction of IGBTs

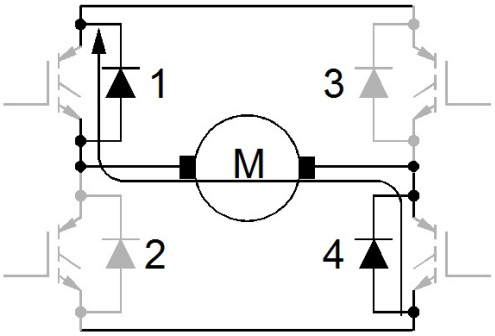

Figure 3. Third Quadrant Conduction of Diodes

The anti-parallel diodes are normally co-packaged with the IGBT although in some cases they can be separately packaged. The forward characteristics of the diode are given on the data sheet for the IGBT if it is a co-packaged device. The amount of information concerning the variation will vary from device to device. Often typical and maximum values are given in the electrical characteristics section with a set of curves over temperature in the typical characteristics section.

Dynamic Variations

The dynamic components of the losses are, turn-on losses, turn-off losses and diode reverse recovery losses. The turn-on and turn-off losses can be controlled to some degree by the gate drive circuit. The gate voltage and drive impedance are both system parameters that can be varied to adjust these losses.

Collector rise times are normally in the range of 10 – 50 ns while fall times are typically 3 to 8 times slower than the rise time. The rise and fall times are influenced by the gate drive level and impedance, so matching the signals to all paralleled devices is an important parameter in the minimization of differences in the switching speeds.

In order to match the switching speeds of the paralleled devices as much as possible, proper layout techniques are essential. To achieve this, the layout should be as symmetrical as possible to match the parasitic inductances as closely as possible. Minimizing the impedance and impedance mismatch in the emitter path to ground is very important. If a current sense transformer is used, it should be connected in the collector path. Current sense resistors, when used, are generally by necessity connected in the emitter path and this shouldn't cause problems as long as they are non-inductive resistors and the layout remains balanced.

Proper layout also requires that the thermal path for each device be as closely matched as possible e.g. don't place one device on the edge of a heat sink with another in the center, but rather, put them at symmetrical locations on the heat sink when possible.

The variations in dynamic losses come from several parameters. There are intrinsic differences in switching speeds between devices on a die-to-die basis as well as from wafer-to-wafer. In addition there are differences in the transconductance that cause the rise and fall times to vary. This could also be considered a difference in Vth, since the gate voltage is on one axis of the transconductance curve.

Any variations in gate inductance and resistance will cause an imbalance in the gate signals, in addition to variations in the emitter inductance previously discussed.

Thermal Coefficient

The thermal coefficient is an important parameter when paralleling IGBTs. It must be a positive coefficient to allow current sharing. This is the area above the isothermal point in Figure 1. A high, positive thermal coefficient forces more equal current sharing but also increases losses at high currents since the $V_{CE(SAT)}$ increases with temperature.

A negative thermal coefficient is unsafe. If one of paralleled devices gets hotter than any of the others, it will become more conductive and with more current passing through it, it will become even hotter and so forth. At best there will be a large thermal imbalance and at worst the devices may fail.

The specific transconductance curve is fixed by the particular device selected; however, the temperature coefficient can be varied by adjusting the gate drive voltage which can move the operation point closer or further from the isothermal point. Of course, varying the gate drive voltage also affects the $V_{CE(sat)}$ and switching speeds.

A high temperature coefficient will force better current sharing during the conduction period, but the tradeoff is that it will increase the power dissipation at high power levels. A positive temperature coefficient is necessary for safe parallel operation.

The transconductance (or transfer characteristics) curve, on the data sheet gives information on the change in collector current for a given gate drive signal. Figure 4 shows the transconductance curves for the NGTB15N60S1ETG IGBT.

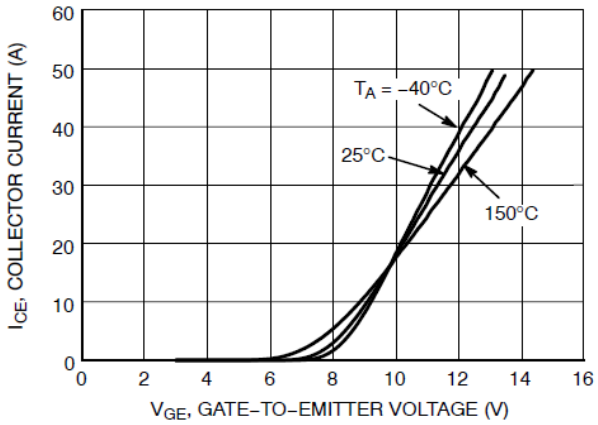

Figure 4. Temperature Coefficient from Transconductance Curves

By graphically determining the currents at gate voltages of 9 V, 9.8 V, 11 V and 12 V, the graph of Figure 5 can be generated. 9.8 V was chosen since it is the isothermal point at which the temperature coefficient is zero.

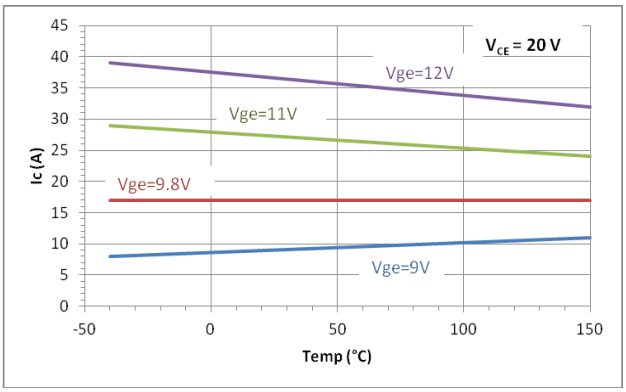

Figure 5. Collector Current Temperature Coefficient for the NGTB15N60S1ETG

At this point it should be understood that a positive temperature coefficient is desirable from the impedance or $V_{CE(SAT)}$ parameters. The above curve is for the change in current and a negative coefficient is required for this parameter. A negative coefficient here, indicates that for a forced collector-emitter voltage, the current reduces with increasing temperature, which is what is required for good current sharing.

From Figure 5 we can see that for gate drive voltages above 9.8 V the current temperature coefficient increases in slope as the gate voltage increases, offering better current sharing.

Another way to look at the temperature coefficient is to plot the collector-emitter voltage vs. temperature for a fixed gate voltage. The IGBT data sheet normally contains families of curves of the collector current vs. collector emitter voltage for various gate drive voltages at high, room and low temperature extremes.

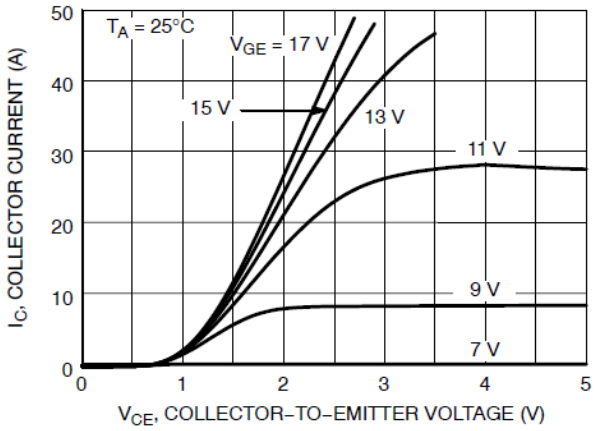

Figure 6. IGBT Output Characteristics for the NGTB15N60S1ETG

Figure 6 is one of those curves from the NGTB15N60S1ETG IGBT. This curve is for a temperature of 25°C.

Using data from these three curves, a plot of $V_{CE(sat)}$ over temperature for varying gate voltages can be generated (Figure 7). This plot shows the positive temperature coefficient at gate drive voltages greater than 9.8 V, and also that the slope increases with a higher gate voltage.

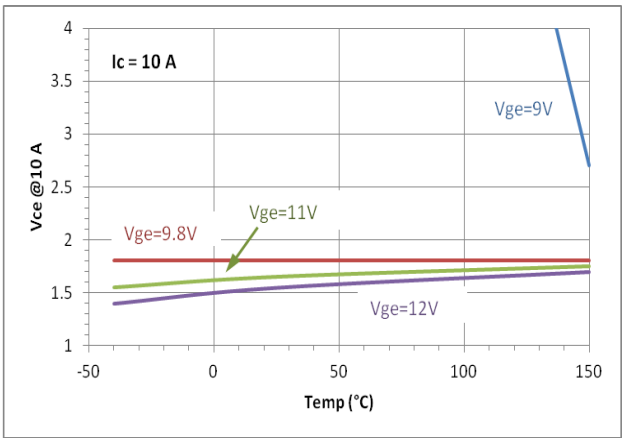

Figure 7. V_{CE} Temperature Coefficient for the NGTB15N60S1ETG

From this simplified analysis, it should be apparent that it essential to keep the gate drive voltage well above the isothermal point. The higher the gate voltage, the more even the current sharing.

Gate Resistors

Much has been written about matching the impedances around the gate drive and return path. It is well known that the more closely the impedances are matched, the better the sharing of the power and current in the IGBTs.

Most discussions of this issue suggest that separate gate drive resistors must be used. Providing a gate resistor for

each IGBT reduces the possibility of oscillations between the paralleled devices; however, it also increases the differences in the turn-on and turn-off times and profiles of the devices.

If a common gate resistor can be used, without causing oscillations, the current waveforms will be more closely matched since both gates will be at the same potential at the same time.

Figures 8 and 9 show two IGBTs in parallel operation with separate and common gate resistors.

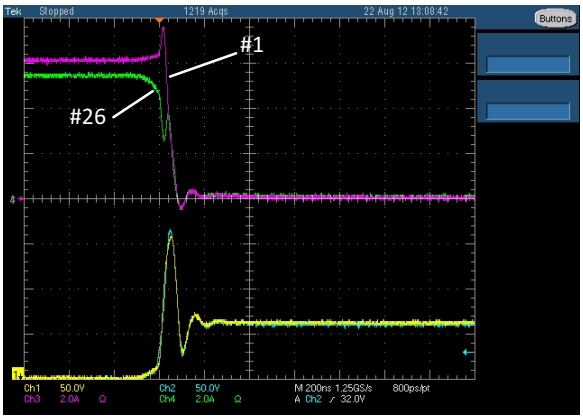

Figure 8. Turn-off Waveforms for Separate Gate Resistors

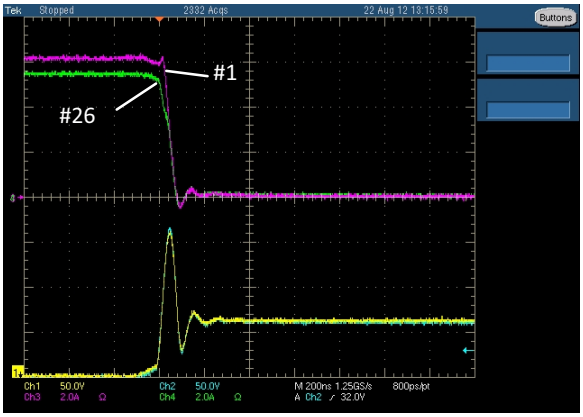

Figure 9. Turn-off Waveforms for a Common Gate Resistor

The IGBTs chosen for this test were intentionally picked for their dissimilar characteristics so that the differences could be seen when mismatched parts were used.See the Empirical Data section below for more information on the IGBT testing used.

The upper waveforms that are labeled with the IGBT numbers are the collector currents and the lower traces are the collector voltages.

For this test, two 22 Ω resistors were used for the drive with separate gate resistors and a single 11 Ω resistor was used for the drive with a common gate resistor. The IGBTs were 40 A, 600 V, NGTB40N60IHL devices.

It can be seen from the scope shots that even though a common gate resistor does not have an impact on the current sharing, it does greatly improve the matching of the switching waveforms.

If oscillations occur between the devices, it will be necessary to use separate resistors for each IGBT; however, even in this case it is possible to use a common resistor in series with the separate resistors.

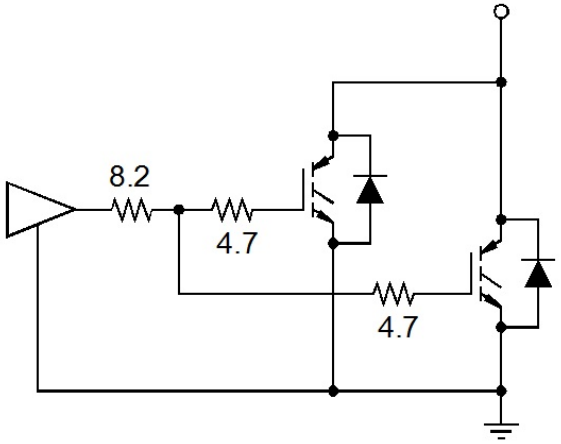

Figure 10. Combined Common and Separate Gate Resistors

The circuit shown in Figure 10, uses a combination of common and separate gate resistors. The values can be easily adjusted between either extreme once the unit is built to match the switching characteristics as closely as possible while still eliminating oscillations between the two IGBTs.

Empirical Data

A group of NGTB40N60IHL IGBTs was serialized and tested for conduction and switching losses. Those data were then plotted based on conduction losses and total switching losses. Two sets of devices were chosen. Units 1 and 26 were used for testing of dissimilar devices and units 2 and 27 were used for testing of similar devices.

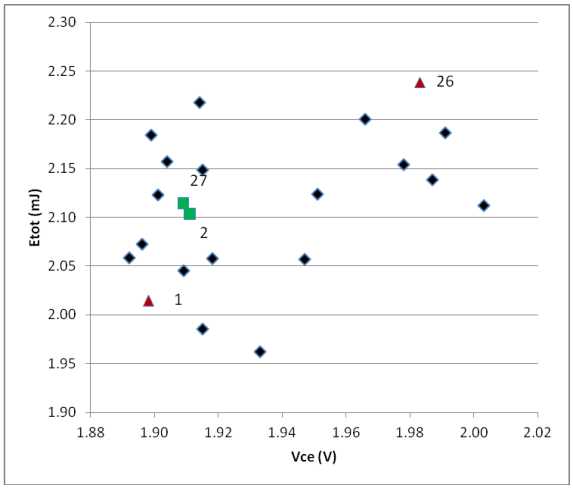

Figure 11. Scatter Plot of NGTB40N60IHL IGBT Sample

The following three scope traces show the collector-emitter voltage and collector current of the two best matched devices (#2, 26).

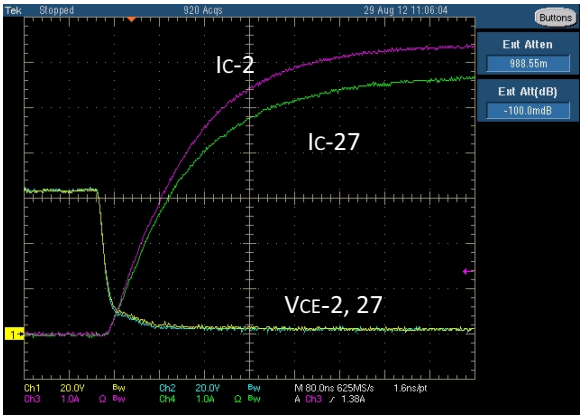

Figure 12. Turn-on Waveform for Matched Devices

Even though the two devices are closely matched, there is a difference in the currents at turn on. This imbalance; however, does not last long and the steady-state currents are essentially equal due to the matching of the $V_{CE(sat)}$ parameter.

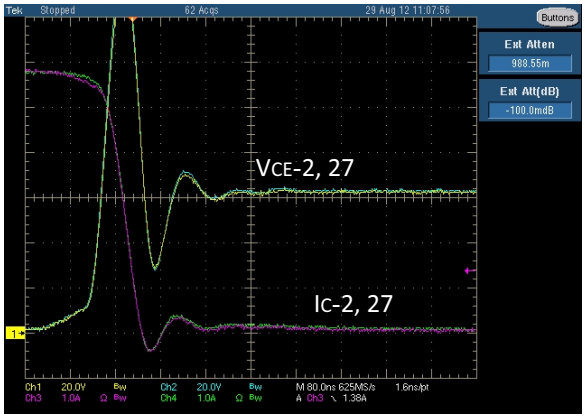

Figure 13. Turn-off Waveform for Matched Devices

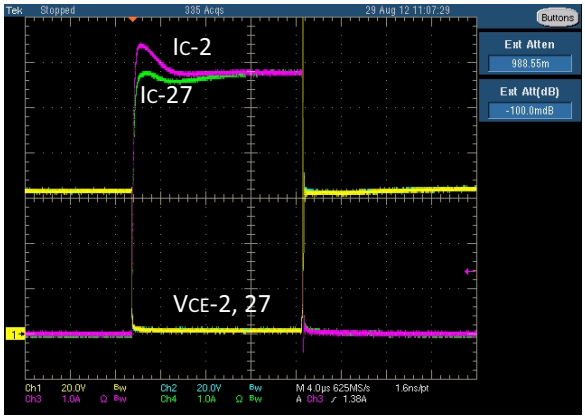

Figure 14. Pulse Waveform for Matched Devices

From the above waveforms it can be seen that even though the turn on does not track equally between the two parts, the currents come in to alignment and the turn off waveforms are identical. Figure 14 was repeated with individual gate drive resistors with no change to the waveform.

It should also be noted that the IGBTs were matched based on their total switching losses, so the individual turn-on and turn-off losses may not be exactly matched.

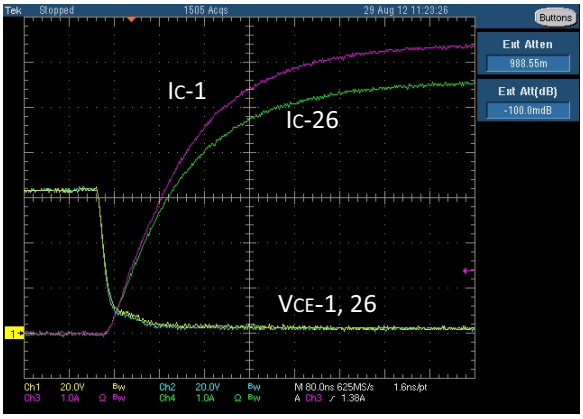

Figure 15. Turn-on Waveform for Mismatched Devices

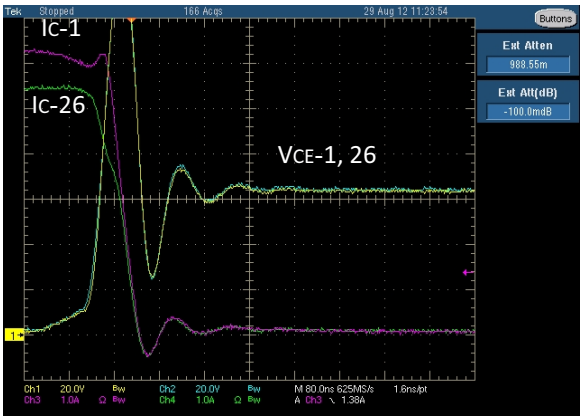

Figure 16. Turn-off Waveform for Mismatched Devices

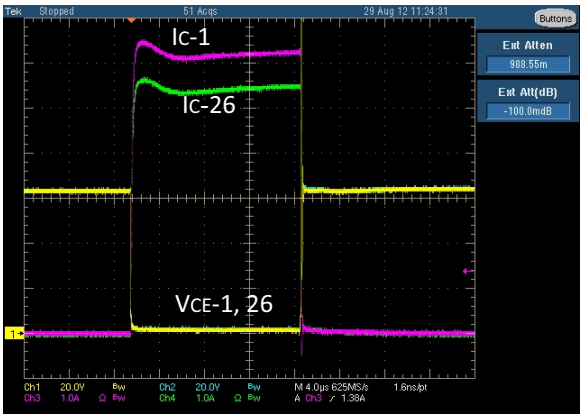

Figure 17. Pulsed Waveform for Mismatched Devices

For the mismatched IGBTs, the turn-on and turn-off follow similar paths; however the conduction current shows a significant difference which exists throughout the duration of the pulse.

While it is desirable to have closely matched parts, some amount of variation in parameters can be tolerated. The thermal management system must be designed with these differences in mind. The $V_{CE(sat)}$ parameter has the greatest affect on the difference in power loss between the two (or more) devices.

All of the above waveforms use a common gate resistor of 11 Ω.

Test Board

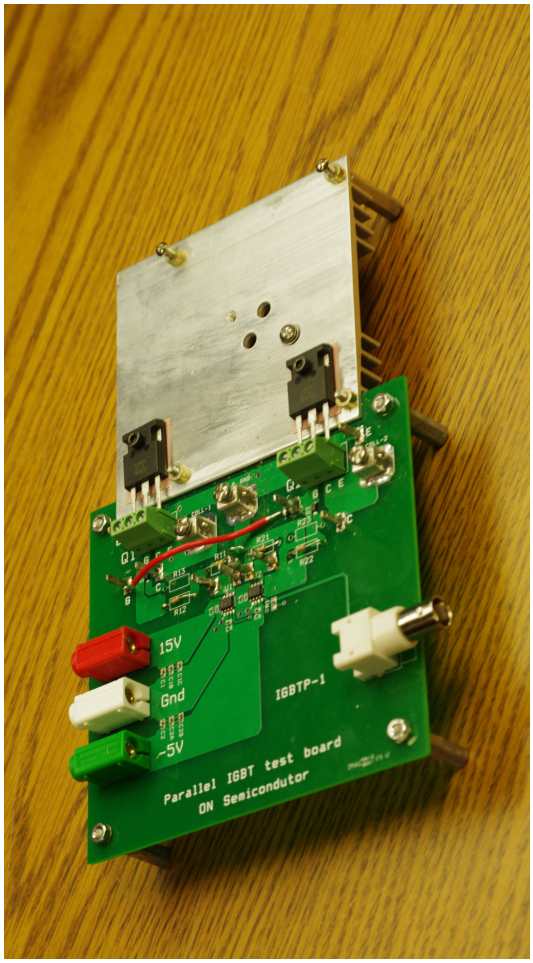

Figure 18. Test Board and Heat Sink for Parallel Testing

This setup was used to test the IGBTs and generate the waveforms used in this application note. Every effort was made to match the trace impedances between the two IGBTs. Two drivers are installed but only one was used so there are no timing differences due to the drivers.

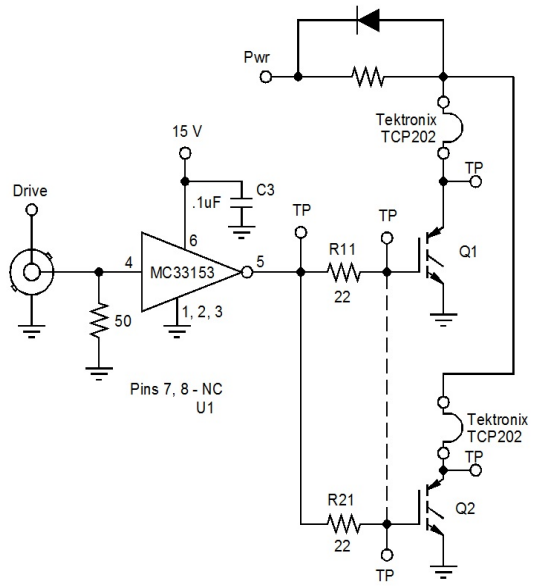

Figure 19. Schematic of Test Circuit

Check List for Paralleled Devices

- Match electrical impedances as closely as possible.
- Match thermal impedances as closely as possible.
- Keep the gate drive voltage high.
- Use a common gate resistor unless oscillations occur.

Summary

This application note has discussed several issues associated with paralleled IGBTs. Selecting a high gate drive voltage and proper gate resistor configuration are as important to equalizing current sharing as is matched thermal and electrical layout. Using the information described here will help to assure a reliable design.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊