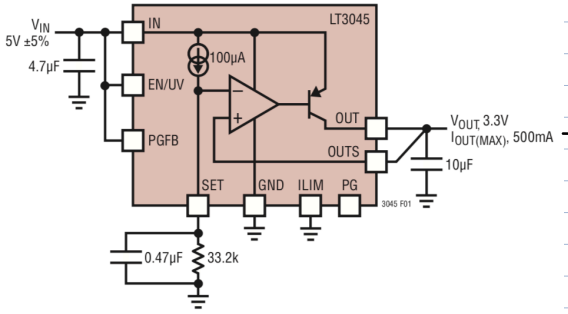
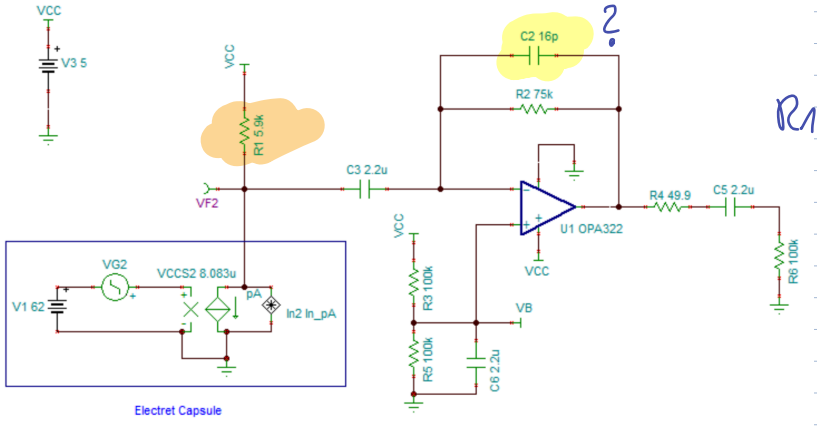


Figure 1. Basic Adjustable Regulator

3,3V



3,3V Version

$R_1 = \frac{3,3V - 2V}{0,5mA} = 2,6k\Omega$

Analog Out

Mic

Figure 18: A 5V version of the microphone pre-amplifier circuit.

The internal JFET of the electret microphone is biased by resistor R1. The value of this resistor can be calculated from the desired supply voltage (V_{CC}), and the microphone operating voltage (V_{MIC}) and current consumption (I_S) given in Table 2:

$$R_1 = \frac{V_{CC} - V_{MIC}}{I_S} = \frac{9V - 2V}{0.5mA} = 14k\Omega \rightarrow 13.7k\Omega \quad (9)$$

A value for R1 slightly less than the calculated value (13.7kΩ as opposed to 14kΩ) is used to accommodate variation in the supply voltage.

The feedback capacitor C2 compensates for parasitic capacitance at the op amp inverting input which can cause instability. Capacitor C2 also forms a pole with resistor R2 in the response of the pre-amplifier. The frequency of this pole must be high enough to not affect the microphone transfer function within the audible bandwidth. For this design, a response deviation of -0.1dB at 20kHz is acceptable. The location of the pole can be calculated using the relative gain at 20kHz:

$$f_p = \frac{f}{\sqrt{\left(\frac{G_0}{G_f}\right)^2 - 1}} = \frac{20kHz}{\sqrt{\left(\frac{1}{0.989}\right)^2 - 1}} = 133725Hz \quad (7)$$

In the above equation, G_0 and G_f are the gains at low frequency and the gain at frequency "f" respectively. Inserting 20kHz for "f", and 0.989 (-0.1dB) for G_f, gives a pole frequency of 133725Hz. The feedback capacitor value can then be calculated:

$$C_2 = \frac{1}{2\pi f_p R_2} = \frac{1}{2\pi(133725Hz)(75k\Omega)} = 15.87pF \rightarrow 15pF \quad (8)$$

A.1 Electrical Schematic

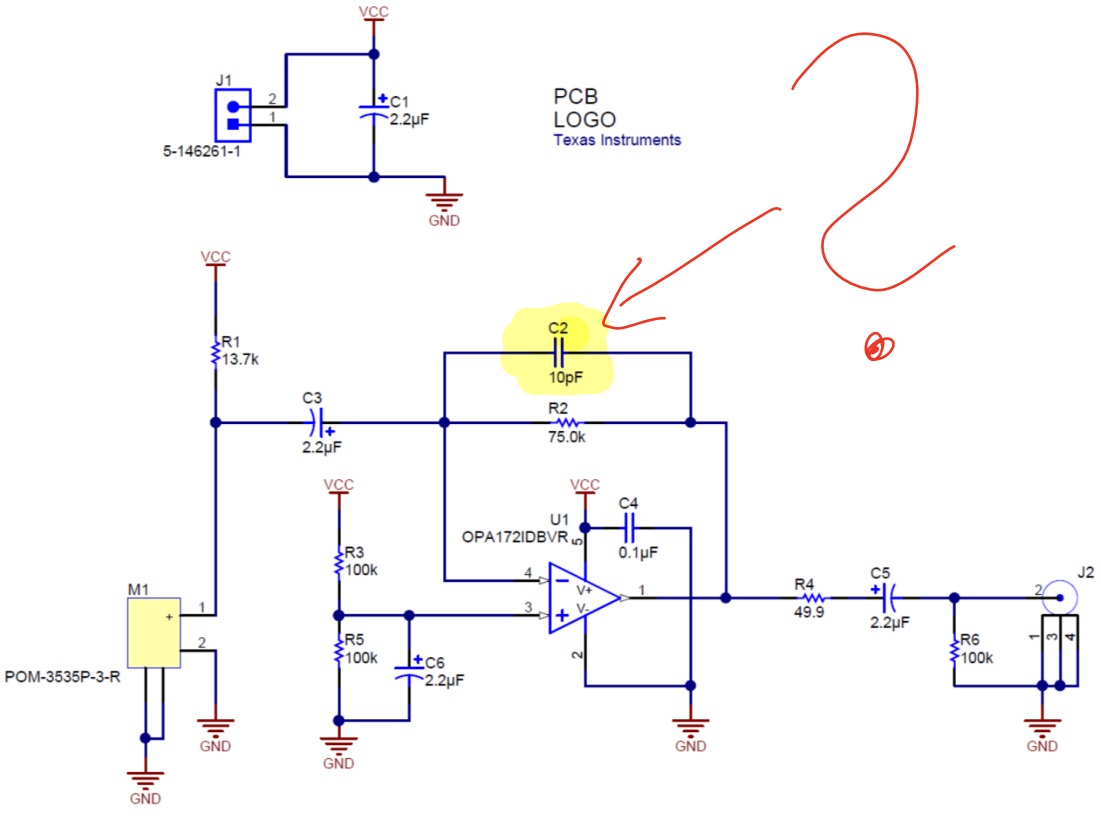


Figure A-1: Electrical Schematic

3 Component Selection

3.1 Passive Components

1% Thick film resistors in 0603 surface mount packages were used for this design. It should be noted that no additional distortion was observed due to these resistors. Distortion due to resistor non-linearity is typically seen at higher signal levels. Capacitor C2 must be a NP0/C0G type ceramic capacitor or film capacitor. High-K ceramic capacitors (X7R, Y5V, etc.) will produce distortion if installed at C2. Capacitors C3 and C5 are tantalum capacitors selected to avoid microphonic behavior associated with high-k ceramics[3]. Because these capacitors are polarized, correct polarity must be observed when they are installed in the circuit. Furthermore, there is minimal ac voltage drop across these capacitors and therefore they do not contribute distortion to the signal path.

A.2 Bill of Materials

Item	Qty	Value	Designator	Description	Manufacturer	Part Number
1	4	2.2uF	C1, C3, C5, C6	CAP, TA, 2.2uF, 16V, +/-10%, 5.9 ohm, SMD	Vishay-Sprague	293D225X9016A2TE3
2	1	10pF	C2	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A100JAT2A
3	1	0.1uF	C4	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A
4	1		J1	Header, 100mil, 2x1, Gold, TH	TE Connectivity	5-146261-1
5	1		J2	RCA Jack, Metal, Right Angle	CUI Inc	RCJ-011
6	1		M1	Electret capsule microphone	PUI Audio	POM-3535P-3-R
7	1	13.7k	R1	RES, 13.7k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060313K7FKEA
8	1	75.0k	R2	RES, 75.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060375K0FKEA
9	3	100k	R3, R5, R6	RES, 100k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA
10	1	49.9	R4	RES, 49.9 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060349R9FKEA
11	1		U1	36V 10MHz, CMOS Operational Amplifier	Texas Instruments	OPA172IDBVR

Figure A-2: Bill of Materials

Changed to 3.3V Version

opa322 -- OPA322AIDBVT

24.14 Analog-to-Digital Converter (ADC)

Table 24-33. ADC Electrical Characteristics[ab]

Parameter	Parameter Name	Min	Nom	Max	Unit
POWER SUPPLY REQUIREMENTS					
V_{DDA}	ADC supply voltage	2.97	3.3	3.63	V
GNDA	ADC ground voltage	-	0	-	V
VDDA / GNDA VOLTAGE REFERENCE					
C_{REF}	Voltage reference decoupling capacitance	-	1.0 // 0.01[c]	-	µF
ANALOG INPUT					
V_{ADCIN}	Single-ended, full- scale analog input voltage, internal reference[de]	0	-	V_{DDA}	V
	Differential, full-scale analog input voltage, internal reference[df]	$-V_{DDA}$	-	V_{DDA}	V
VIN_{CM}	Input common mode voltage, differential mode[g]	-	-	(VREFP + VREFN) / 2 ± 25	mV
I_L	ADC input leakage current[h]	-	-	2.0	µA
R_{ADC}	ADC equivalent input resistance[h]	-	-	2.5	kΩ
C_{ADC}	ADC equivalent input capacitance[h]	-	-	10	pF
R_S	Analog source resistance[h]	-	-	500	Ω
SAMPLING DYNAMICS					
F_{ADC}	ADC conversion clock frequency[i]	-	16	-	MHz
F_{CONV}	ADC conversion rate		1		Msps
T_S	ADC sample time	-	250	-	ns
T_C	ADC conversion time[j]		1		µs
T_{LT}	Latency from trigger to start of conversion	-	2	-	ADC clocks
SYSTEM PERFORMANCE when using internal reference					
N	Resolution		12		bits

h. As shown in Figure 24-18 on page 1391, R_{ADC} is the total equivalent resistance in the input line all the way up to the sampling node at the input of the ADC.

Figure 24-18. ADC Input Equivalency Diagram

Mic

Analog Out