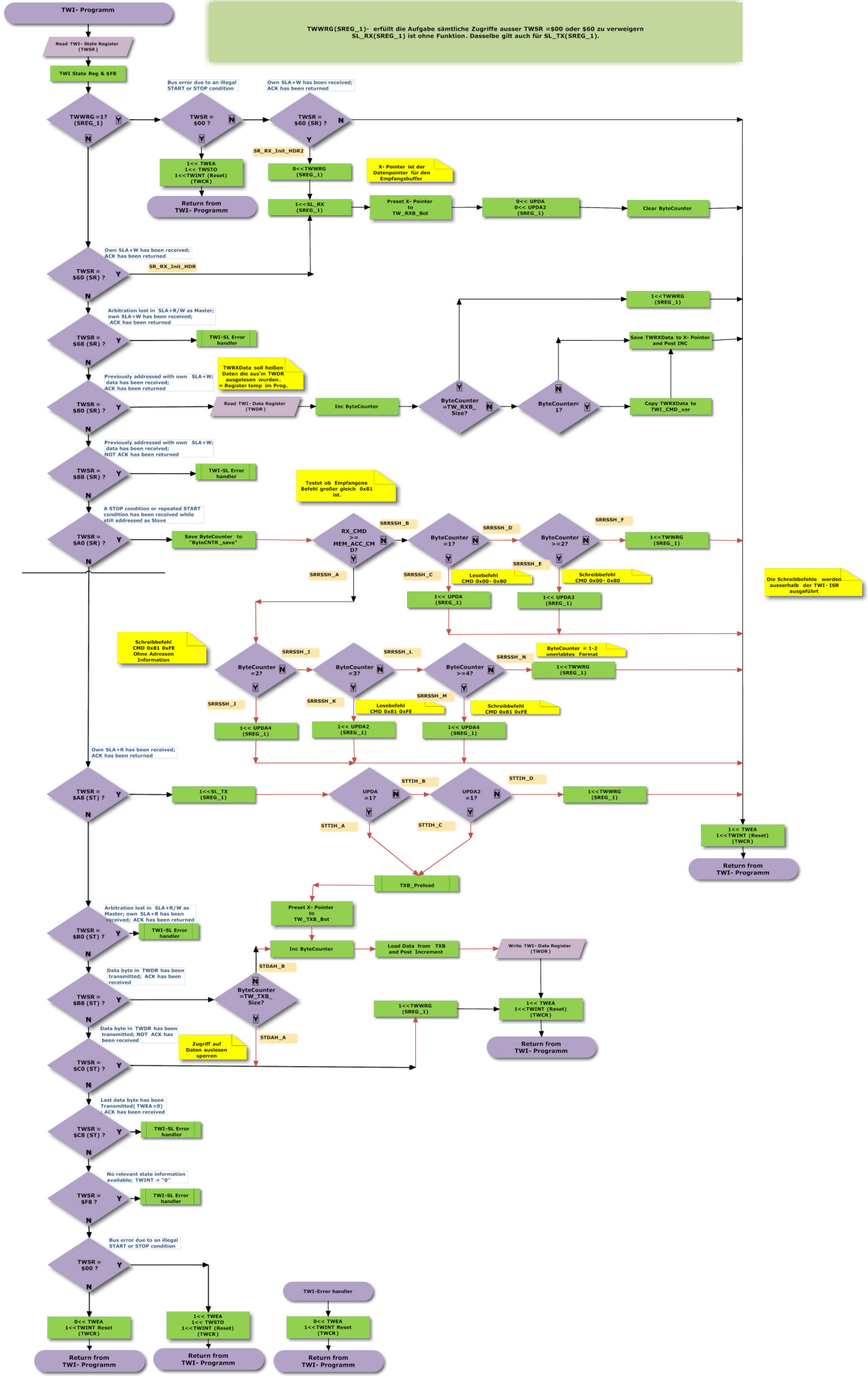
TWI- Programm
TWWRG(SREG_1)- erfüllt die Aufgabe sämtliche Zugriffe ausser TWSR =$00 oder $60 zu verweigern SL_RX(SREG_1) ist ohne Funktion. Dasselbe gilt auch für SL_TX(SREG_1).
Read TWI- State Register (TWSR)
TWI State Reg & $F8
TWWRG =1? (SREG_1)
Bus error due to an illegal START or STOP condition
TWSR = $00 ?
Own SLA+W has been received; ACK has been returned
TWSR = $60 (SR) ?
1<< TWEA 1<< TWSTO 1<<TWINT (Reset) (TWCR)
Return from TWI- Programm
SR_RX_Init_HDR2
0<<TWWRG (SREG_1)
X- Pointer ist der Datenpointer für den Empfangsbuffer
1<<SL_RX (SREG_1)
Preset X- Pointer to TW_RXB_Bot
0<< UPDA 0<< UPDA2 (SREG_1)
Clear ByteCounter
Own SLA+W has been received; ACK has been returned
SR_RX_Init_HDR
TWSR = $60 (SR) ?
1<<TWWRG (SREG_1)
Arbitration lost in SLA+R/W as Master; own SLA+W has been received; ACK has been returned
TWSR = $68 (SR) ?
TWI-SL Error handler
Save TWRXData to X- Pointer and Post INC
TWRXData soll heißen Daten die aus'm TWDR ausgelesen wurden. = Register temp im Prog.
Previously addressed with own SLA+W; data has been received; ACK has been returned
TWSR = $80 (SR) ?
Read TWI- Data Register (TWDR)
Inc ByteCounter
ByteCounter =TW_RXB_ Size?
ByteCounter= 1?
Copy TWRXData to TWI_CMD_var
Previously addressed with own SLA+W; data has been received; NOT ACK has been returned
TWSR = $88 (SR) ?
TWI-SL Error handler
Testet ob Empfangene Befehl großer gleich 0x81 ist.
A STOP condition or repeated START condition has been received while still addressed as Slave
TWSR = $A0 (SR) ?
Save ByteCounter to "ByteCNTR _save"
RX_CMD >= MEM_ACC_CMD?
SRRSSH_B
ByteCounter =1?
SRRSSH_D
ByteCounter >=2?
SRRSSH_F
1<<TWWRG (SREG_1)
SRRSSH_A
SRRSSH_C
Lesebefehl CMD 0x00- 0x80
SRRSSH_E
Schreibbefehl CMD 0x00- 0x80
1<< UPDA (SREG_1)
1<< UPDA3 (SREG_1)
Die Schreibbefehle werden ausserhalb der TWI- ISR ausgeführt
Schreibbefehl CMD 0x81 0xFE Ohne Adressen Information
ByteCounter =2?
SRRSSH_I
ByteCounter =3?
SRRSSH_L
ByteCounter >=4?
SRRSSH_N
ByteCounter = 1-2 unerlabtes Format
1<<TWWRG (SREG_1)
SRRSSH_J
SRRSSH_K
Lesebefehl CMD 0x81 0xFE
SRRSSH_M
Schreibbefehl CMD 0x81 0xFE
1<< UPDA4 (SREG_1)
1<< UPDA2 (SREG_1)
1<< UPDA4 (SREG_1)
Own SLA+R has been received; ACK has been returned
TWSR = $A8 (ST) ?
1<<SL_TX (SREG_1)
UPDA =1?
STTIH_B
UPDA2 =1?
STTIH_D
1<<TWWRG (SREG_1)
STTIH_A
STTIH_C
1<< TWEA 1<<TWINT (Reset) (TWCR)
Return from TWI- Programm
TXB_Preload
Arbitration lost in SLA+R/W as Master; own SLA+R has been received; ACK has been returned
TWSR = $B0 (ST) ?
TWI-SL Error handler
Preset X- Pointer to TW_TXB_Bot
Inc ByteCounter
Load Data from TXB and Post Increment
Write TWI- Data Register (TWDR)
STDAH_B
Data byte in TWDR has been transmitted; ACK has been received
TWSR = $B8 (ST) ?
ByteCounter =TW_TXB_ Size?
1<<TWWRG (SREG_1)
1<< TWEA 1<<TWINT (Reset) (TWCR)
Return from TWI- Programm
Data byte in TWDR has been transmitted; NOT ACK has been received
Zugriff auf Daten ausleseen sperren
STDAH_A
TWSR = $C0 (ST) ?
Last data byte has been Transmitted(TWEA=0) ; ACK has been received
TWSR = $C8 (ST) ?
TWI-SL Error handler
No relevant state information available; TWINT = "0"
TWSR = $F8 ?
TWI-SL Error handler
Bus error due to an illegal START or STOP condition
TWSR = $00 ?
0<< TWEA 1<<TWINT Reset (TWCR)
Return from TWI- Programm
1<< TWEA 1<< TWSTO 1<<TWINT (Reset) (TWCR)
Return from TWI- Programm
TWI-Error handler
0<< TWEA 1<<TWINT Reset (TWCR)
Return from TWI- Programm