Product Summary

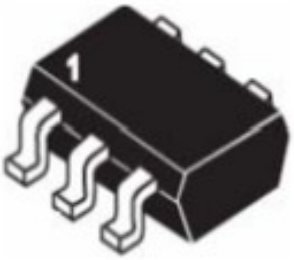
NMOS

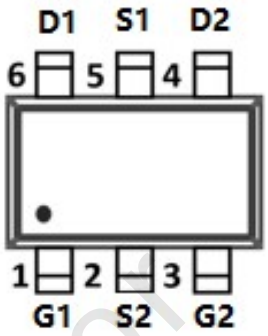
- V_{DS} 30V
- I_D 3A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜95mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜150mohm

PMOS

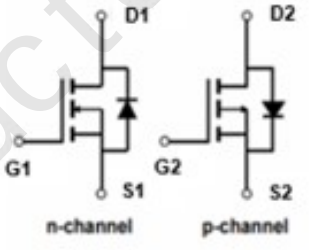
- V_{DS} -30V
- I_D -2.5A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜130mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜220mohm

- 100% ∇V_{DS} Tested





SOT-23-6L



General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

Applications

- Wireless charger
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage	V_{DS}	30	-30	V
Gate-source Voltage	V_{GS}	±20	±20	V
Drain Current	I_D	3	-2.5	A
Pulsed Drain Current [A]	I_{DM}	8	-8	A
Total Power Dissipation	P_D	0.95	0.95	W
Thermal Resistance Junction-to-Ambient [B]	$R_{\theta JA}$	62.5	62.5	℃/ W
Junction and Storage Temperature Range	T_J ,T_{STG}	-55～+150	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
JSM6333C	F2	.333	3000	45000	180000	7“ reel

■ N-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=2.5A		52	95	mΩ
		V_{GS}=4.5V, I_D=2.0A		73	150	
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V,f=1MHZ		303		pF
Output Capacitance	C_{oss}			53		
Reverse Transfer Capacitance	C_{rss}			20		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=5.6A		5.2		nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.2		
Reverse Recovery Chrage	Q_{rr}	I_F=5.6A, di/dt=100A/us		1.28		
Reverse Recovery Time	t_{rr}			16.5		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V, V_{DS}=15V, I_D=1A R_{GEN}=3Ω		4.5		
Turn-on Rise Time	t_r			2.5		
Turn-off Delay Time	$t_{D(off)}$			12.8		
Turn-off fall Time	t_f			3.5		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ P-MOS Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.0	-1.5	-3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-2.0A		65	130	mΩ
		V_{GS}=-4.5V, I_D=-1.7A		95	220	
Diode Forward Voltage	V_{SD}	I_S=-4A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ		320		pF
Output Capacitance	C_{oss}			55		
Reverse Transfer Capacitance	C_{rss}			41		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-3.0A		5.5		nC
Gate-Source Charge	Q_{gs}			1.1		
Gate-Drain Charge	Q_{gd}			1.6		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-15V, R_L=15Ω,I_D=-1A, R_{GEN}=2.5Ω		14		ns
Turn-on Rise Time	t_r			61		
Turn-off Delay Time	$t_{D(off)}$			19		
Turn-off fall Time	t_f			10		

C. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

D. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ N-MOS Typical Performance Characteristics

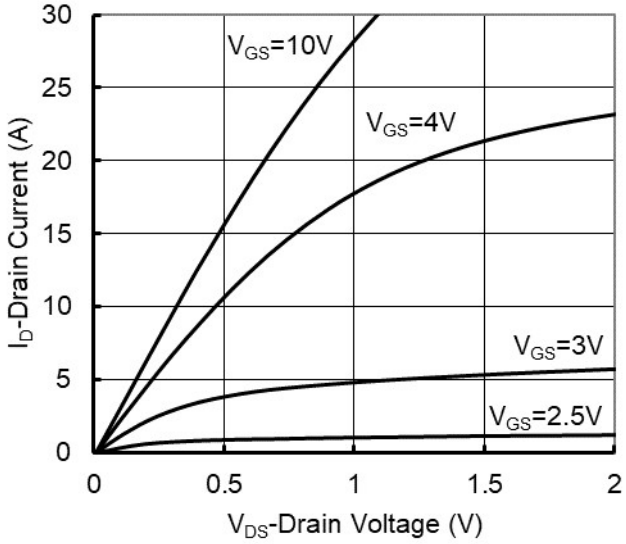


Figure1. Output Characteristics

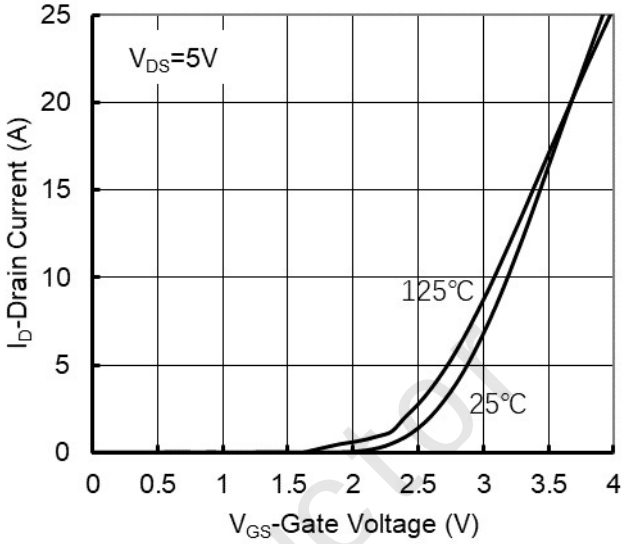


Figure2. Transfer Characteristics

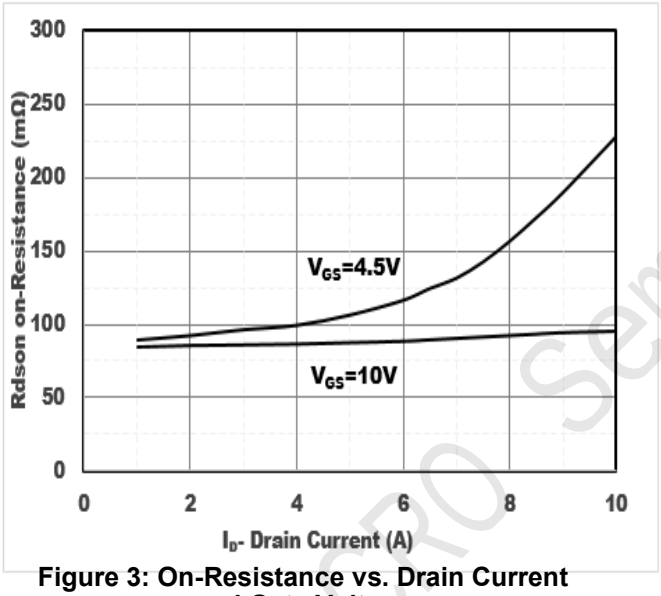


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

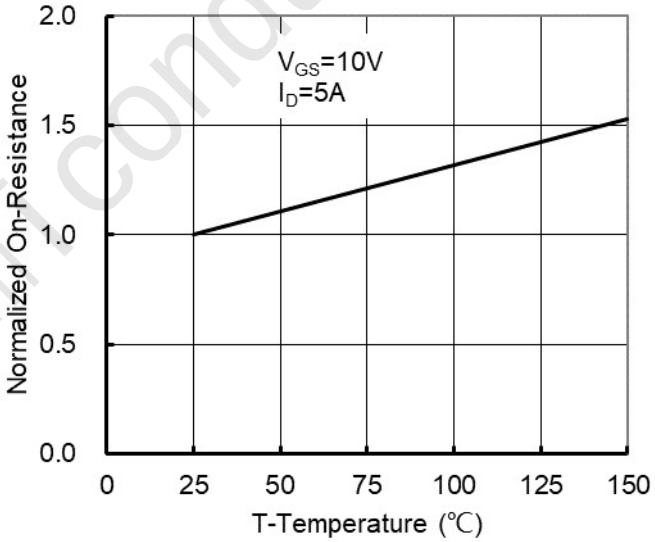


Figure 4: On-Resistance vs. Junction Temperature

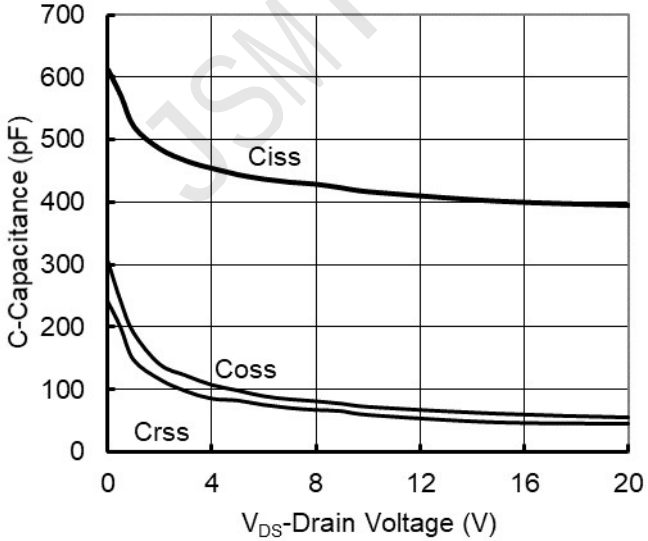


Figure5. Capacitance Characteristics

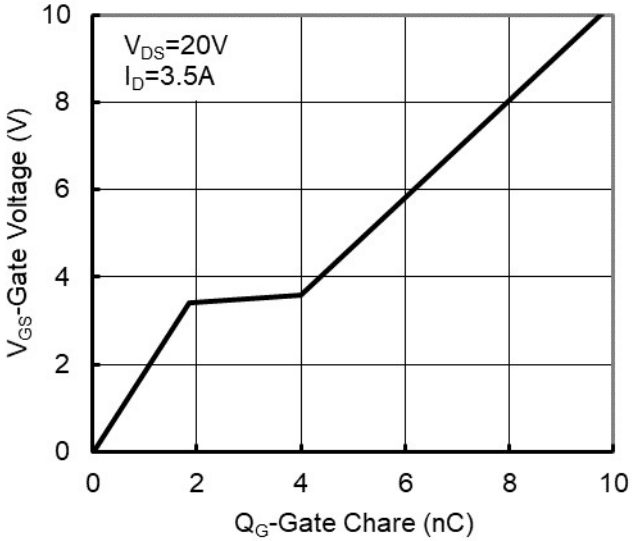


Figure6. Gate Charge

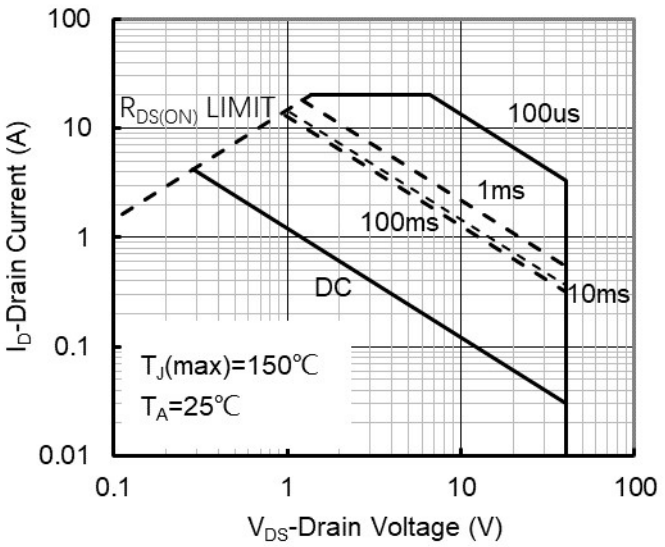


Figure7. Safe Operation Area

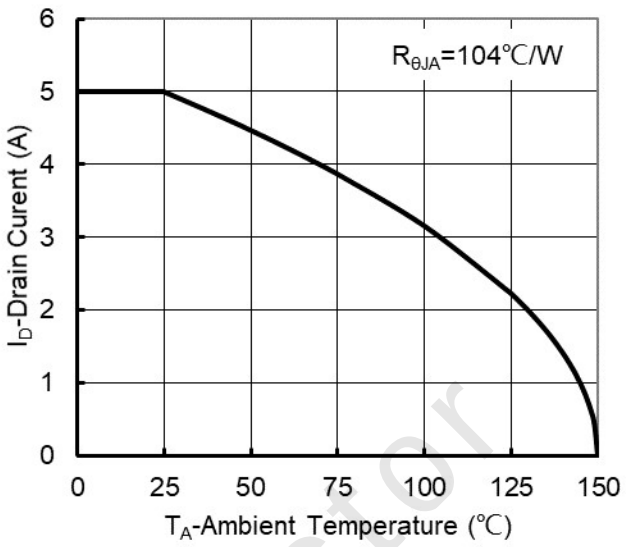


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

■ P-MOS Typical Performance Characteristics

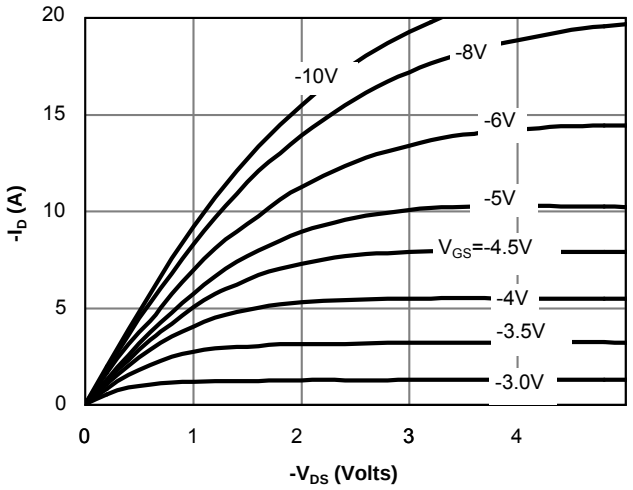


Fig 1: On-Region Characteristics

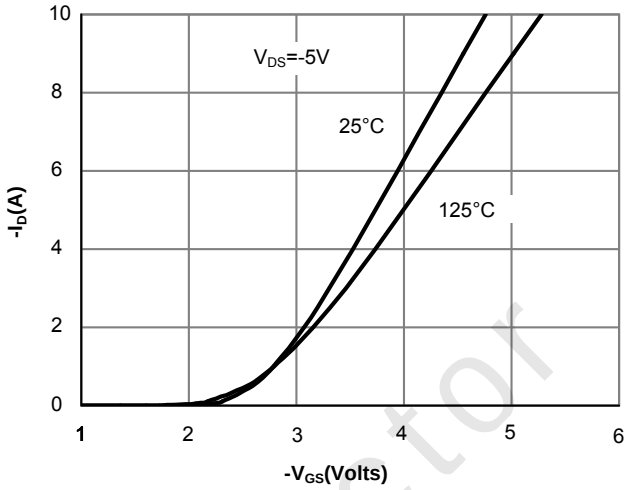


Figure 2: Transfer Characteristics

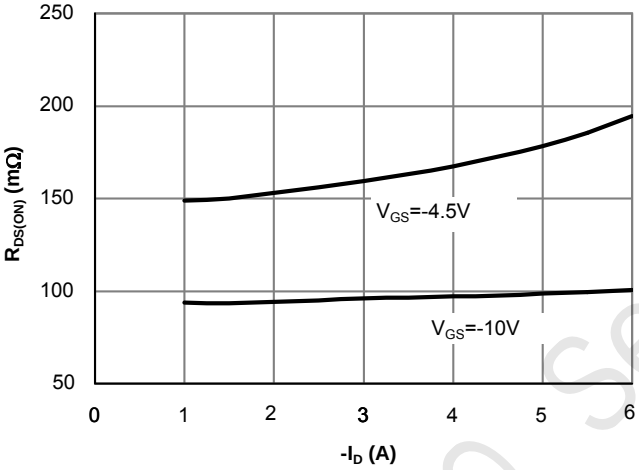


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

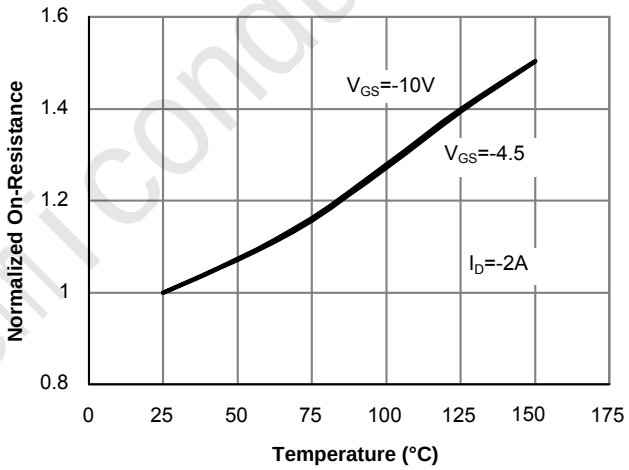


Figure 4: On-Resistance vs. Junction Temperature

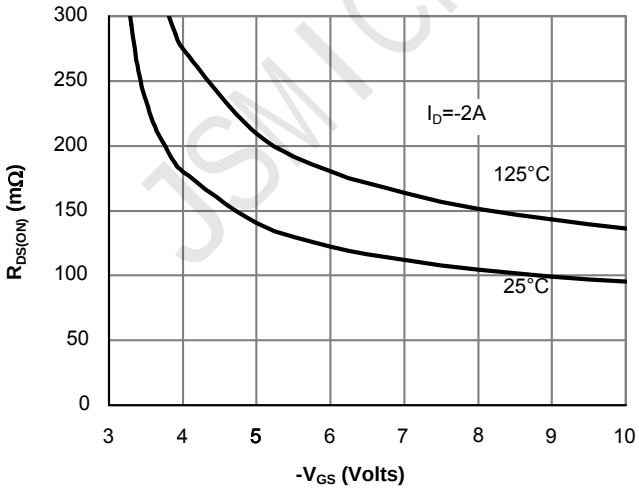


Figure 5: On-Resistance vs. Gate-Source Voltage

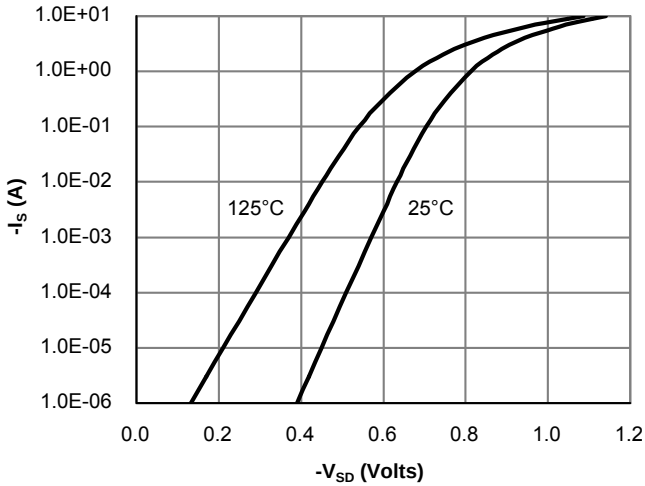


Figure 6: Body-Diode Characteristics

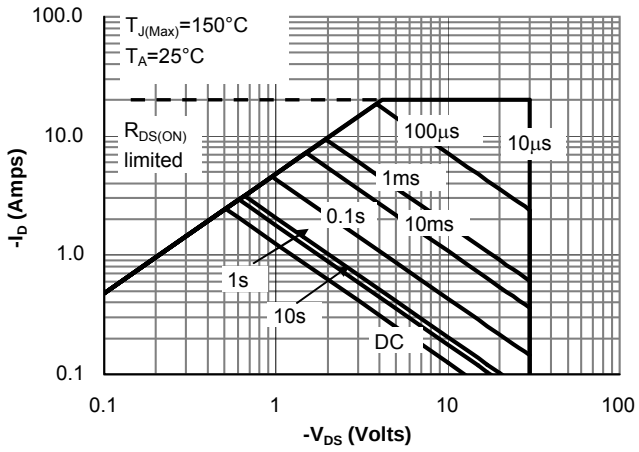


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

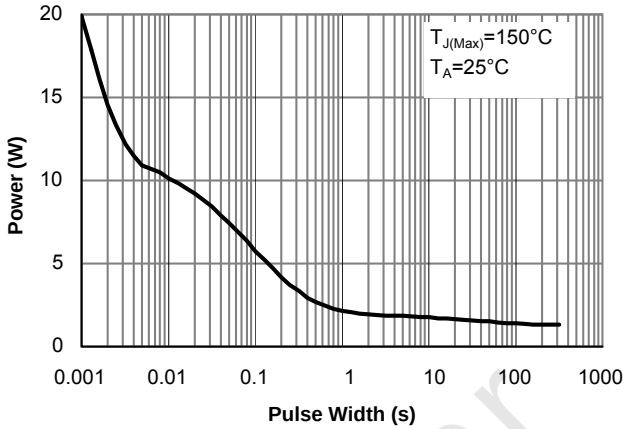
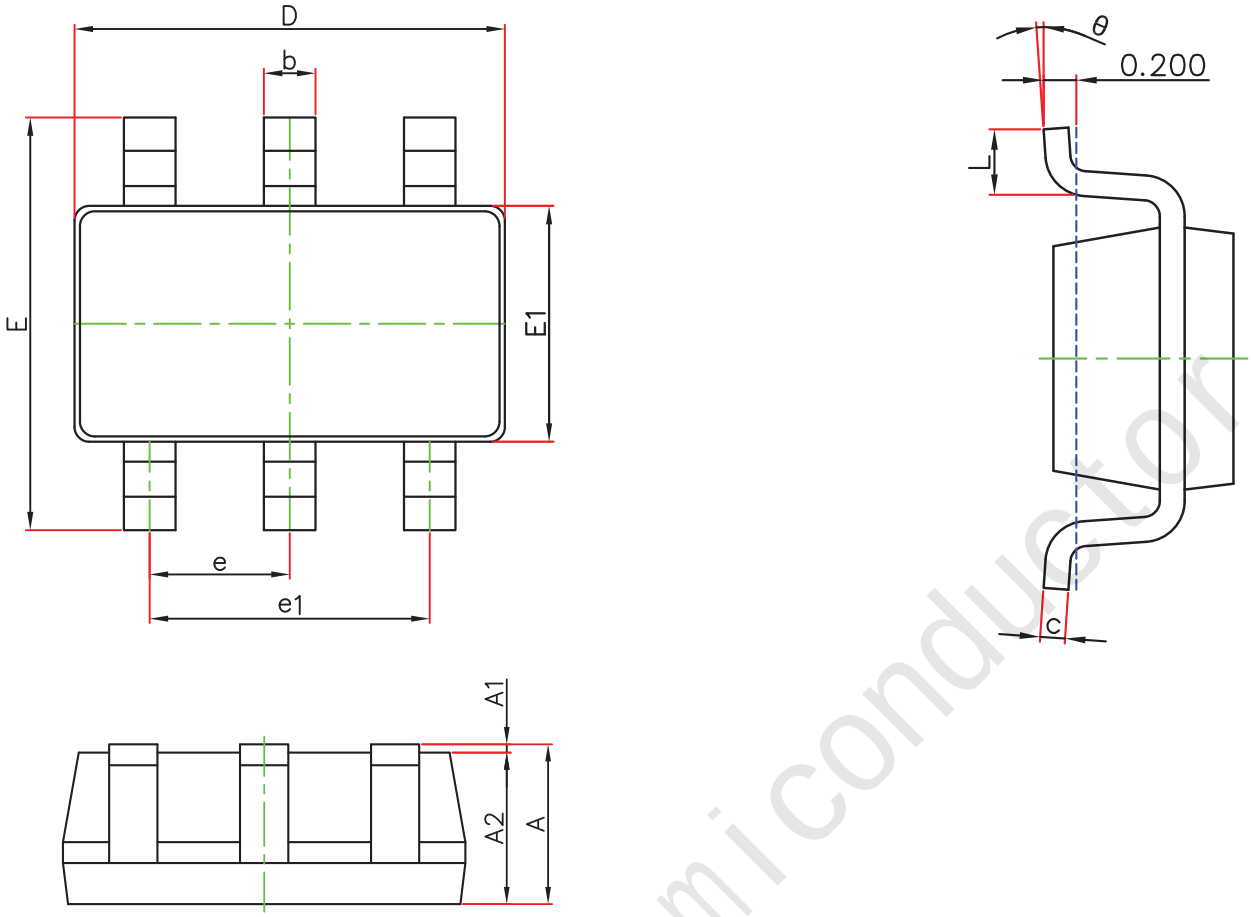


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

■ SOT-23-6L Package information



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.050	1.200
A1	0.000	0.100
A2	1.000	1.200
b	0.300	0.500
c	0.100	0.150
D	2.800	3.000
E1	1.500	1.700
E	2.600	3.000
e	0.950(BSC)	
e1	1.800	2.000
L	0.300	0.600
K	0°	8°