FD6287T

three phase250Vgate driver

overview

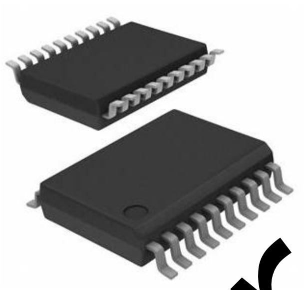
The FD6287T is an integrated three independent half-bridge Gate drive integrated circuit chip, designed for high voltage, high speed drive dynamic MOSFET design,Operates up to +250V.

FD6287T built-in VCC/VBS undervoltage (UVLO) protection Protection function to prevent the power tube from working under too low voltage.

FD6287T built-in shoot-through prevention and dead time, anti- Prevent the driven high and low side MOSFETs from passing through, effectively protecting power component.

FD6287T built-in input signal filter to prevent input noise disturbance.

encapsulation



TSSOP-20

Features

- Suspension absolute voltage +250V
- Power supply voltage range: 7~20V
- Integrates three independent half-bridge drivers
- Output current +1.5A/-1.8A
- 3.3V/5V input logic compatible
- VCC/VBS undervoltage protection (UVLO)
- Built-in shoot-through prevention function
- Built-in 200ns dead time
- Built-in input filter function
- High and low end channel matching
- The high-side output is in phase with the input, and the low-side output is in phase with the input inversion

application

Three-phase motor drive

1. Absolute Maximum Ratings(Unless otherwise specified, all pins areCOMas a reference point)

parameter		symbol	scope	unit
High side floating absolute voltage		$V_{B1,2,3}$	- 0.3~275	V
High Side Floating Offset Voltage		$V_{S1,2,3}$	$V_{B1,2,3}$-25~$V_{B1,2,3}$+0.3	V
High side output voltage		$V_{HO1,2,3}$	$V_{S1,2,3}$-0.3~$V_{B1,2,3}$+0.3	V
Low side supply voltage		V_{CC}	- 0.3~25	V
Low side output voltage		$V_{LO1,2,3}$	- 0.3~V_{CC}+0.3	V
logic input voltage (HIN, LIN*)		V_{IN}	- 0.3~V_{CC}+0.3	V
Offset Voltage Slew Rate Range		dV_S/dt	≤50	V/ns
Power Dissipation@T_A≤25-C	TSSOP-20	$P_{D.}$	≤1.25	W
Thermal Resistance Junction-to-Ambient	TSSOP-20	R_{wxya}	≤100	-C/W
Junction temperature range		T_j	≤150	-C
storage temperature range		T_{stg}	- 55~150	-C

Note1: In any case, do not exceedP_D..

Note2: Voltages exceeding the absolute maximum ratings may damage the chip.

2. Recommended working conditions(all voltages are inCOMas a reference point)

parameter	symbol	minimum value	maximum value	unit
High side floating absolute voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+7	$V_{S1,2,3}$+20	V
Static high-side floating offset voltage	$V_{S1,2,3}$	COM-2(Note1)	250	V
Dynamic high-side floating offset voltage	$V_{S1,2,3}$	- 50(Note2)	250	V
High side output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Low side supply voltage	V_{CC}	7	20	V
Low side output voltage	$V_{LO1,2,3}$	0	V_{CC}	V
logic input voltage (HIN, LIN*)	V_{IN}	0	V_{CC}	V
ambient temperature	T_A	- 40	125	-C

Note1:$V_{S1,2,3}$for(COM-2V)arrive250Vhour,HOnormal work.$V_{S1,2,3}$for(COM-2V)arrive(COM-V_{BS})hour,HOLogical state is maintained.

Note2:$V_{S1,2,3}$for(COM-5V),Width50nsof transient negative voltages, theHOnormal work.

Note3: The chip works above the recommended working conditions for a long time, which may affect its reliability. It is not recommended that the chip work above the recommended working conditions for a long time.

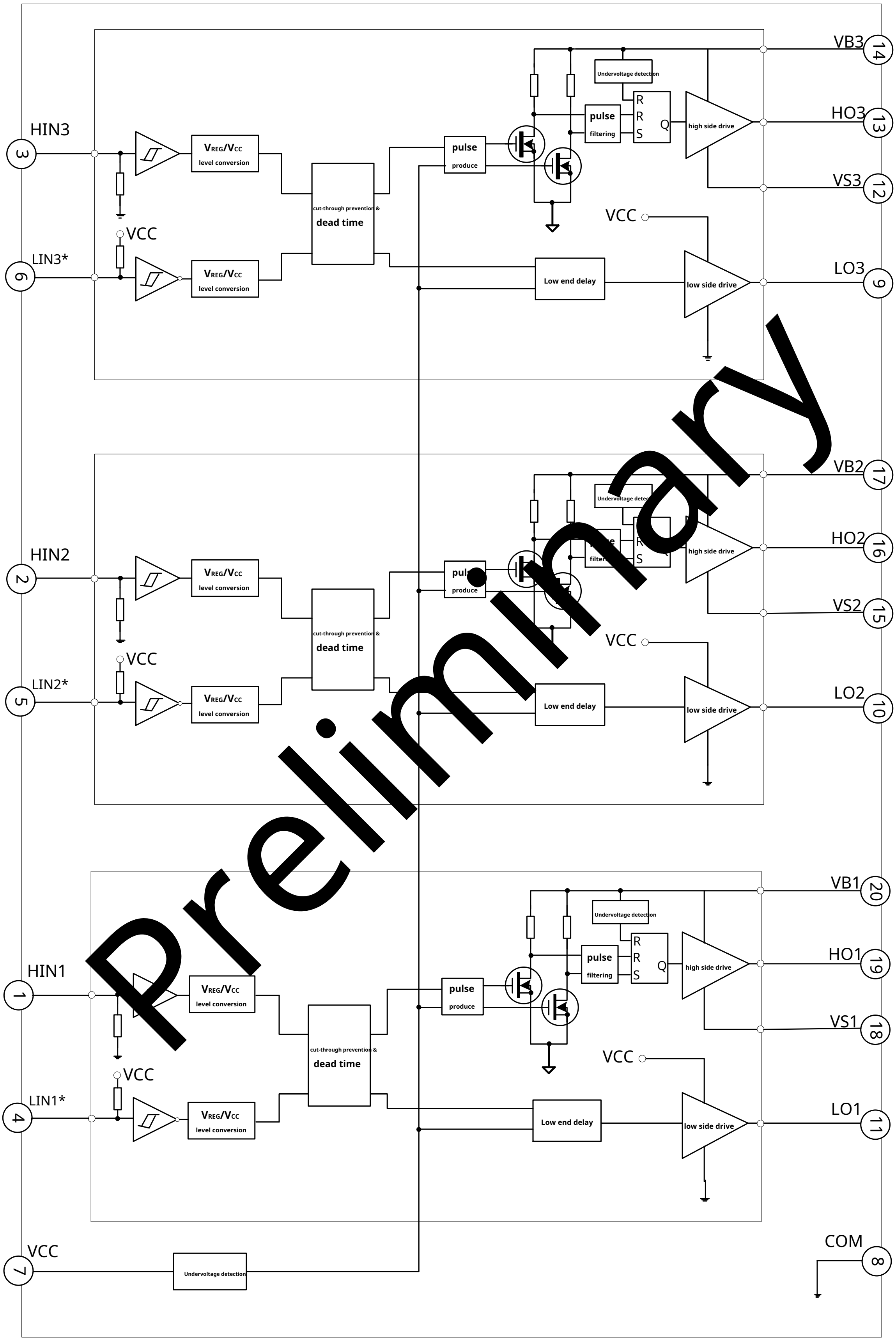
3. Static electrical parameters(unless otherwise notedT_A=25-C,V_{CC}=$V_{BS1,2,3}$=15V,V_S= COM)

parameter	symbol	Test Conditions	minimum value	typical value	maximum value	unit
High Level Input Threshold Voltage	V_{IH}		2.7	- -	- -	V
Low Level Input Threshold Voltage	V_{IL}		- -	- -	0.8	V
V_{CC}Undervoltage protection trip voltage	V_{CCUV+}		5.8	6.4	7.0	V
V_{CC}Brown-out Protection Reset Voltage	V_{CCUV-}		5.4	6.0	6.6	V
V_{CC}Undervoltage Protection Hysteresis Voltage	V_{CCUVH}		0.3	0.4	- -	V
V_{BS}Undervoltage protection trip voltage	V_{BSUV+}		5.8	6.4	7.0	V
V_{BS}Brown-out Protection Reset Voltage	V_{BSUV-}		5.4	6.0	6.6	V
V_{BS}Undervoltage Protection Hysteresis Voltage	V_{BSUVH}		0.3	0.4	- -	V
Suspension Power Leakage Current	I_{LK}	$V_{B1,2,3}$=$V_{S1,2,3}$=250V	- -	0.1	5.0	μA
V_{BS}Quiescent Current	I_{QBS}	V_{IN}=0Vor5V	- -	180	270	μA
V_{BS}dynamic current	I_{PBS}	$f_{HIN1,2,3}$=20kHz	- -	180	270	μA
V_{CC}Quiescent Current	I_{QCC}	V_{IN}=0Vor5V	- -	330	[illegible]	uA
V_{CC}dynamic current	I_{PCC}	$f_{LIN1,2,3}$=20kHz	[illegible]	[illegible]	500	uA
LIN*High level input bias current	I_{LIN+}	V_{LIN}=0V	- -	20	40	μA
LIN*Low level input bias current	I_{LIN-}	V_{LIN}=5V	[illegible]	- -	2	μA
HINHigh level input bias current	I_{HIN+}	V_{HIN}=5V	- -	20	40	μA
HINLow level input bias current	I_{HIN-}	V_{HIN}=0V	- -	- -	2	μA
Input pull-down resistor	R_{IN}		200	260	320	KΩ
High level output voltage	V_{Oh}	I_o=10[illegible]	- -	0.6	0.9	V
Low level output voltage	V_{OL}	I_o[illegible]00mA	- -	0.3	0.45	V
High level output short circuit pulse current	I_{Oh}	V_o=0[illegible]V_{IN}=5V,PWD≤10μs	1.1	1.5	1.9	A
Low level output short circuit pulse current	I_{OL}	V_o[illegible]15V,V_{IN}=0V,PWD≤10μs	1.3	1.8	2.3	A
$V_S$static negative pressure	[illegible]		- -	- 6.0	- -	V

4. Dynamic electrical parameters(unless otherwise notedT_A=25-C,V_{CC}=$V_{BS1,2,3}$=15V,V_S= COM)

parameter	symbol	Test Conditions	minimum value	typical value	maximum value	unit
Output rising edge transfer time	t_{on}		- -	300	450	ns
Output falling edge transfer time	t_{off}		- -	100	160	ns
output rise time	t_r	C_L=1000pF	- -	12	- -	ns
output fall time	t_f	C_L=1000pF	- -	12	- -	ns
High and low side delay matching	MT		- -	- -	50	ns
dead time	DT		100	200	300	ns

5. Circuit diagram



6. Chip pin configuration

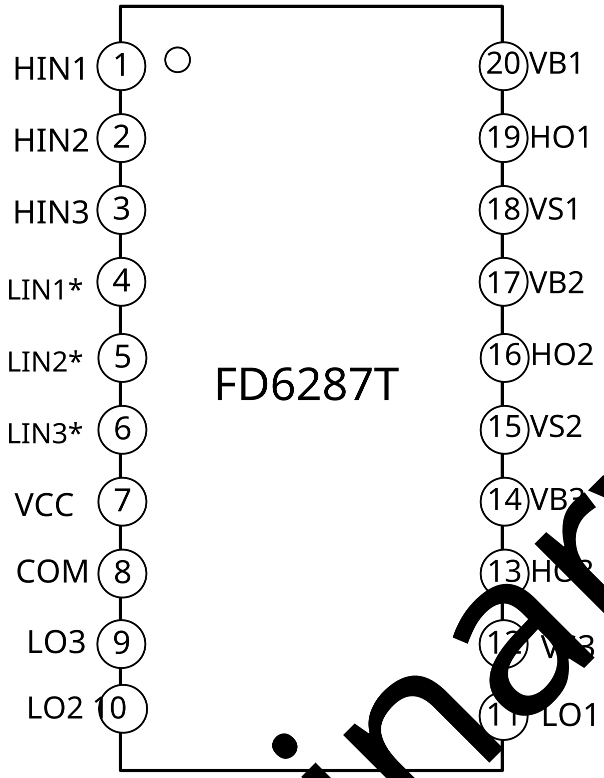
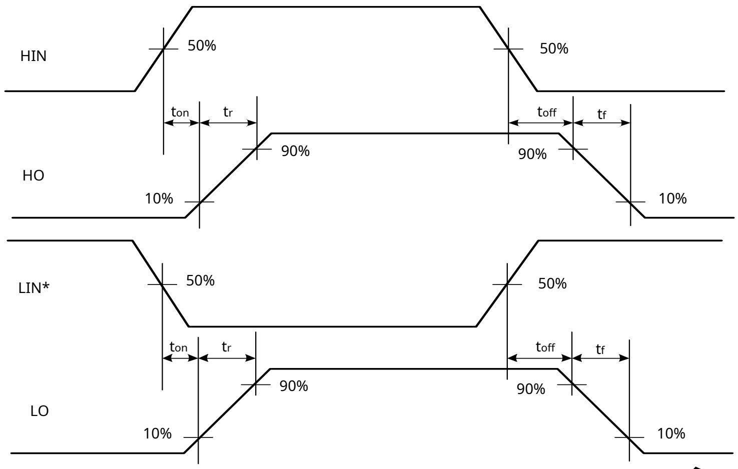


Figure 6-1 Package pin diagram

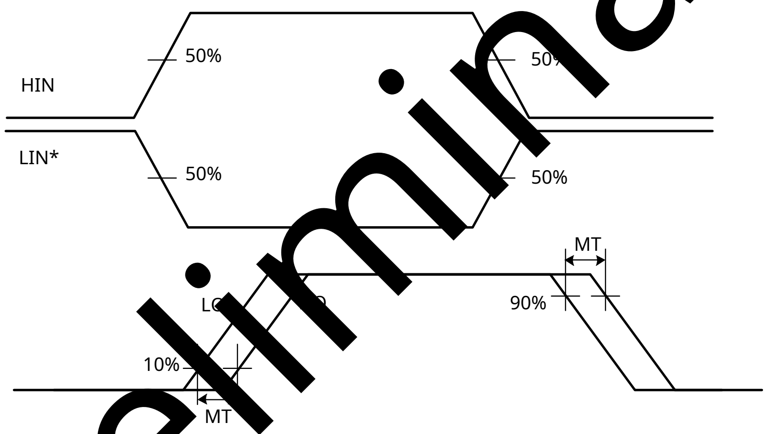
Table 6-1 Pin description

pin number	Pin name	Pin Description
1,2,3	HIN1,HIN2,HIN3	High side input
4,5,6	LIN1*,LIN2*,LIN3*	low side input
7	VCC	Low side supply voltage
8	COM	grounding
9,10,11	LO3, LO2, LO1	low side output
12,15,18	VS3, VS2, VS1	High Side Floating Offset Voltage
13,16,19	HO3, HO2, HO1	high side output
14,17,20	VB3, VB2, VB1	High side floating absolute voltage

7. Switching time test standard

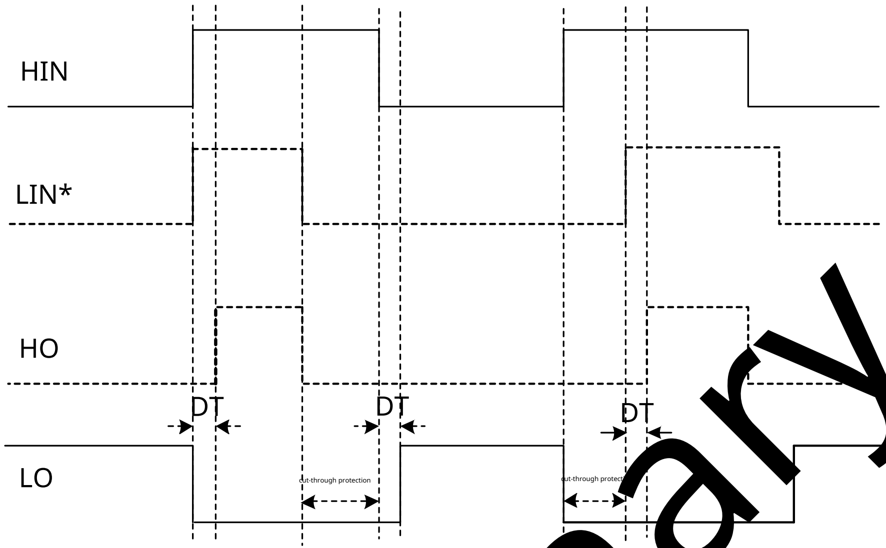


8. Transit Time Matching Test Criteria



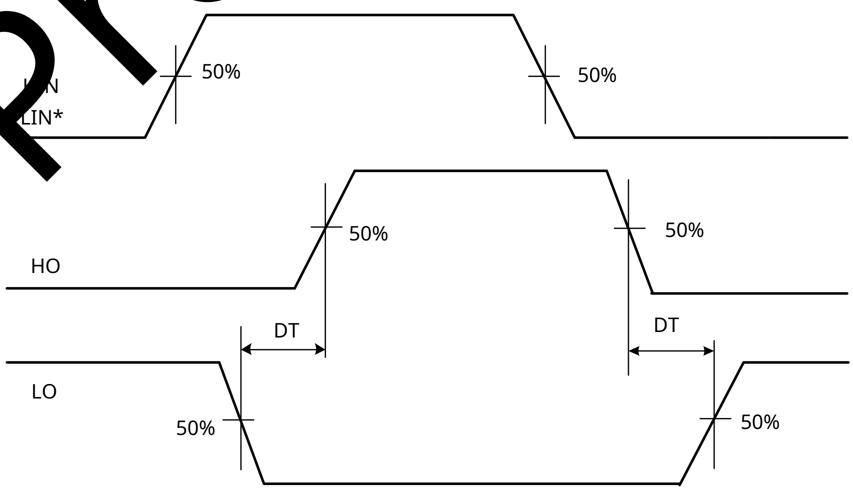
9. Shoot-through prevention function

The internal design of the chip is specially designed to prevent the power tube from passing through the protection circuit, which can effectively prevent the high-side and low-side input signals from being interfered. Power tube through damage caused by interference. The figure below shows how the shoot-through prevention circuit protects the power transistor.

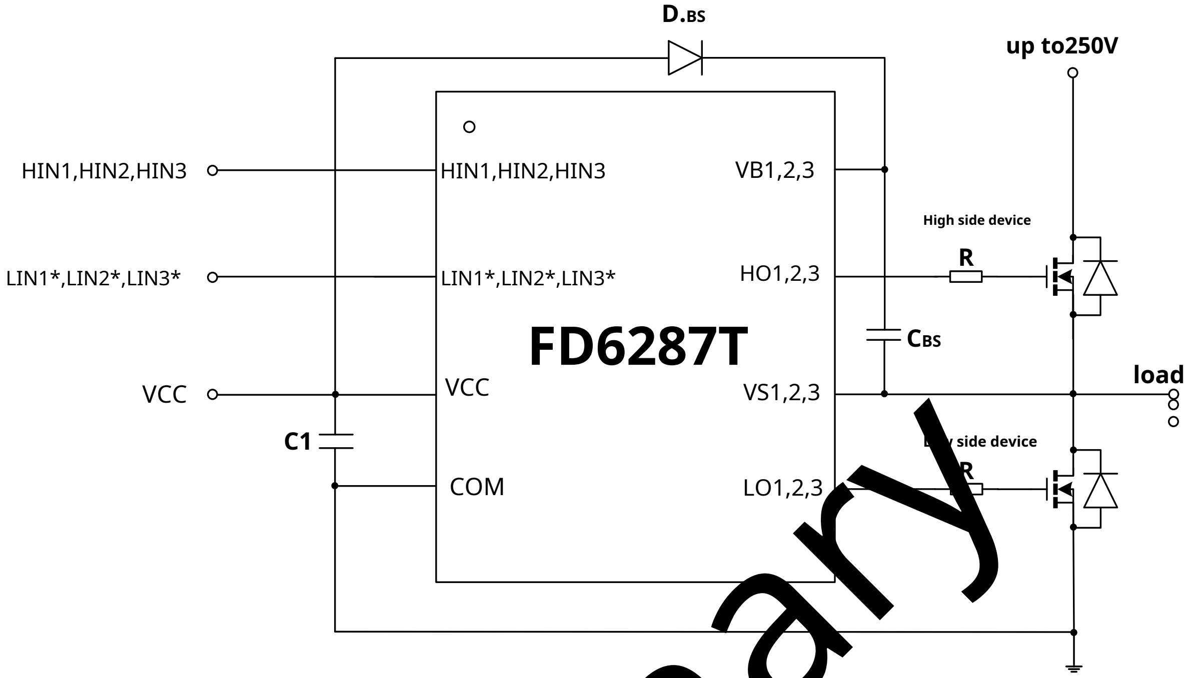


10. Dead zone function

A fixed dead-time protection circuit is set inside the chip. Both high-side and low-side outputs are set low during the dead time. The set dead time must ensure that after one power tube is turned off, another power tube is turned on to effectively prevent the generation of up and down power tubes. Through phenomenon. If the external dead time set by the logic input is greater than the dead time set inside the chip, the dead time set by the logic input The external dead time is the chip output dead time; if the external dead time set by the logic input is less than the dead time set inside the chip , the dead time of the chip output is the dead time set inside the chip. The figure below describes the dead time, input signal and driver The timing relationship of the output signal.



11. Typical application circuit



C1: power supply filter capacitor, according to the circuit conditions, you can choose 10μF~1[illegible]μF, as close as possible to the chip pin.

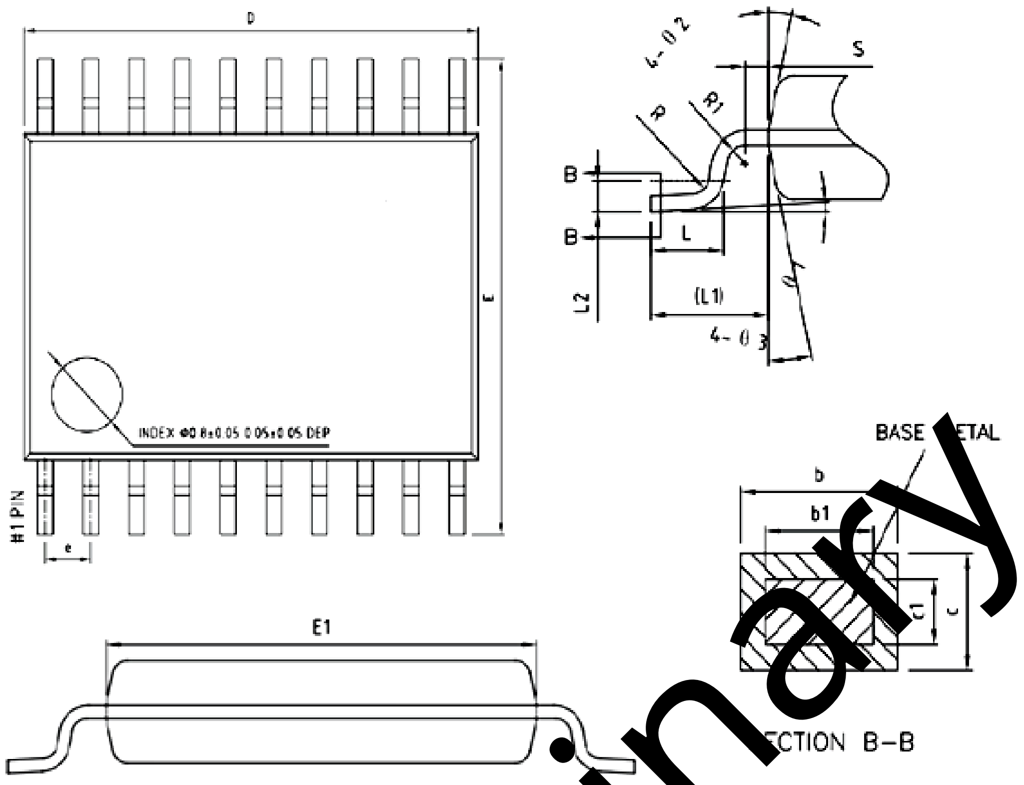
R: Gate drive resistor, the resistance value depends on the driven device and dead time.

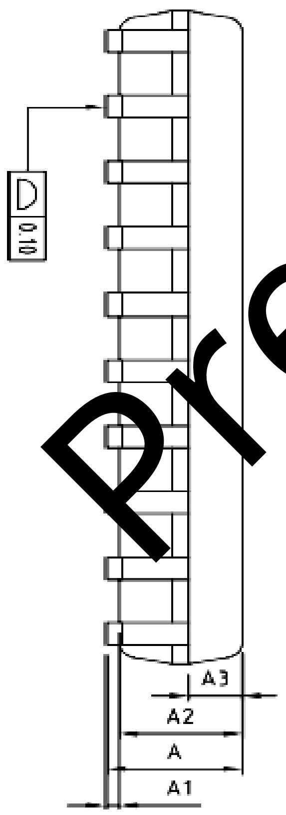
Dbs: Bootstrap diode, Schottky diode with high reverse breakdown voltage and short recovery time should be selected.

Cbs: bootstrap capacitor, should choose ceramic capacitor or tantalum capacitor, can choose 1uF~50μF, as close as possible to the chip pin.

Note: The above circuits and parameters are for reference only, and the actual application circuit sets the parameters according to the actual measurement results.

12. Package size (TSSOP-20)





	MIN(mm)	NOM(mm)	MAX(mm)
A	one	one	1.20
A1	0.05	one	0.15
A2	0.80	1.00	1.05
b	0.19	one	0.30
b1	0.19	0.22	0.25
c	0.09	one	0.20
c1	0.09	one	0.16
D.	6.40	6.50	6.60
E.	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		

Product number	Package form	Marking	Packing	quantity
FD6287T	TSSOP20	FD6287T	Tape&Reel	3000

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Fortior Technology (Shenzhen) Co.,Ltd.

Room203,2/F,Building No.11,Keji Central Road2,
SoftwarePark, High-Tech Industrial Park, Shenzhen, PR China 518057
Tel: 0755-26867710
Fax: 0755-26867715
URL:http://www.fortiortech.com