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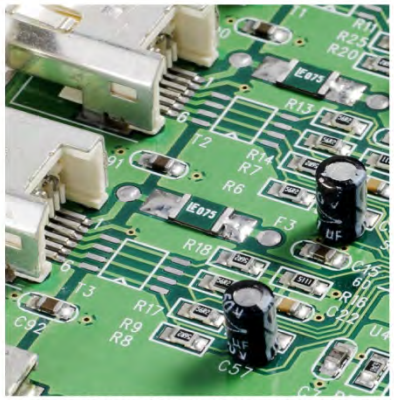
ESD PROTECTION DESIGN GUIDE



A Guide for Protecting
Electronic Circuits and Interfaces
From Electrostatic Discharge (ESD)
Using TVS Diode Arrays

This guide was developed to help electronics designers navigate selection of appropriate TVS Diode Array circuit protection components for equipment interfaces such USB, HDMI, Ethernet, and keypad. This document includes consideration factors, example circuits, applicable standards, and recommended components.

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Introduction:

Designers of today's electronic devices have demanded more functionality with greater flexibility and higher levels of user interaction. These circumstances have helped in driving the development of nanometer chipsets along with a multitude of user interfaces or ports. The confluence of these two has made electronic devices more susceptible to ESD and required the need for a more robust solution.

ESD Standards:

MIL-STD-883, Method 3015

Historically, analog and digital designers have been required to have ESD protection "on-chip" to protect the IC during manufacturing. The most commonly used ESD standard in the manufacturing environment is the MIL-STD-883, Method 3015 and it's also referred to as the Human Body Model (HBM). This model discharges a 100pF capacitor through a 1500Ω resistor into the device under test. The table below points out the four test levels as defined in the standard.

HBM Level	Contact Discharge (kV)	Peak Current (A)
1	±0.5	0.33
2	±1	0.67
3	±2	1.33
4	±4	2.67

The maximum level required for a typical IC had been ±2kV up until 2007, but today that level has been drastically reduced to ±0.5kV. Obviously, this has helped chip designers save valuable silicon area for more functionality, but in turn, it has made the IC much more susceptible to damage from ESD.

IEC61000-4-2

Conversely, equipment manufacturers have traditionally used an ESD standard defined by the IEC (International Electrotechnical Commission) for system or application level testing. This model uses a 150pF capacitor which is discharged through a 330Ω resistor. The table below displays the four test levels as defined in the standard.

IEC Level	Contact Discharge (kV)	Peak Current (A)
1	±2	7.5
2	±4	15
3	±6	22.5
4	±8	30

Most all manufacturers require that their equipment pass Level 4, or ±8kV, as a minimum, however, some are looking for increased reliability and require that their devices pass a much higher level like ±15kV or ±30kV.

Conclusions:

The system level ESD test defined by the IEC produces a substantial increase in peak current compared to the military standard. If an IC is rated for 0.5kV per the MIL-STD and the equipment manufacturer tests this same IC at 8kV per the IEC specification, the chip will see nearly a 100 fold increase in peak current (i.e. 0.33A vs. 30A)!

Ultimately, hardware or board designers must add supplementary ESD devices to protect these sensitive chipsets from the high level ESD threats seen in the field.

Solutions:

Littelfuse TVS Diode Arrays (SPA™ Family) are an ideal choice for suppressing ESD as their speed and clamping levels are essential to protect today's integrated circuits unlike the previous MLV, MOV, and polymer technologies. The SPATM portfolio offers a wide range of devices to suit the majority of application needs available in the market today, and this guide will steer the designer toward the appropriate ESD device for the particular application they're trying to protect.

Some of the applications discussed in this guide are:

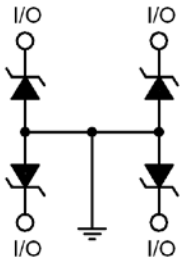
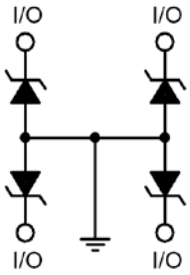
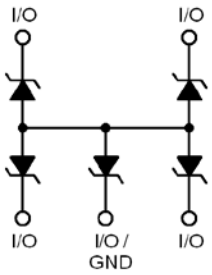
- USB1.1/2.0/3.0
- HDMI
- DisplayPort
- DVI
- 10/100/1000 Ethernet
- Esata
- 1394a/b
- LVDS
- Analog Video
- SIM Sockets
- RS-232
- RS-485
- CAN Bus
- Audio (Speaker/Microphone)
- Keypad/Push button
- LCD/Camera display interfaces

Many of these applications can be found in electronic devices such as:

- PC's
- Portable Medical Devices
- Set Top Boxes
- LCD/PDP TV's
- Portable Navigation Devices
- Keyboards/Mouse
- Mobile Handsets
- MP3/PMP's
- PDA's
- Digital Cameras
- SIM/SD Cards
- External Storage
- Switches/Routers
- Smart Phone

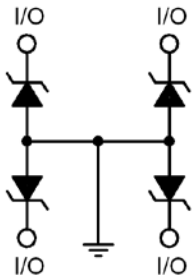
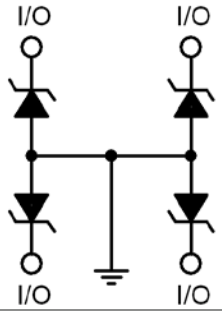
TVS Diode Array (SPA™) Series Descriptions

General Purpose ESD Protection

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V_R= 0V (@ Bias)	V_{RWM}	Lightning (t_P=8/20µs)	Number of Channels	Package Options
SP05		±30kV	50pF (30pF @ 2.5V)	5.5V	N/A	2	SOT23-3 SC70-3
						3	SOT143
						4	SOT23-5 SC70-5
						5	SOT23-6 SC70-6
						6	MSOP-8
SP1001		±15kV	12pF (8pF @ 2.5V)	5.5V	2A	2	SC70-3 SOT553
						4	SC70-5 SOT553
						5	SC70-6 SOT563
SP1002		±8kV	6pF (5pF @ 2.5V)	6V	2A	1	SC70-3
						2	SC70-5
SP1003		±30kV	30pF (17pF @ 2.5V)	5V	7A	1	SOD723 SOD882
SP1004		±8kV	6pF (5pF @ 1.5V)	6V	2A	4	SOT953

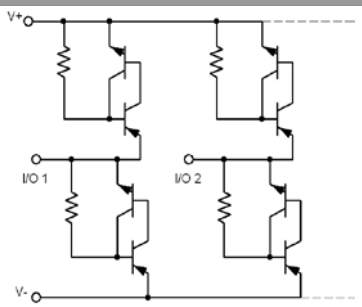
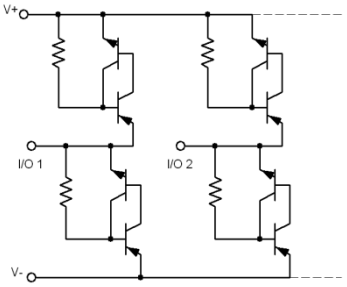
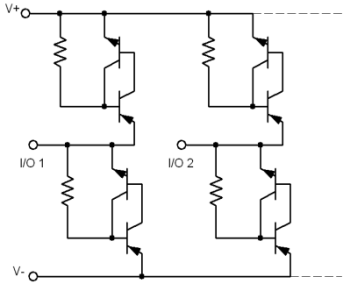
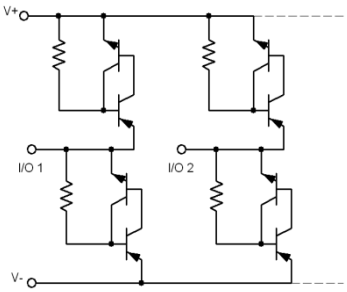
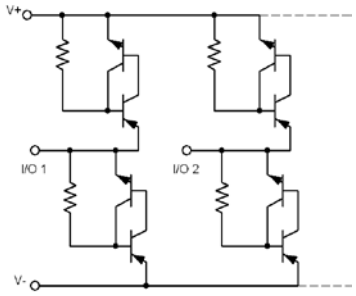
TVS Diode Arrays (SPA™) Series Descriptions

General Purpose ESD Protection *(continued)*

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V_R= 0V (@ Bias)	V_{RWM}	Lightning (t_P=8/20µs)	Number of Channels	Package Options
SP1005		±30kV	30pF (23pF @ 2.5V)	6V	10A	1	0201 Flipchip
SP1006		±30kV	25pF (15pF @ 2.5V)	6V	5A	1	0201 µDFN-2 0.6x0.3mm
SP1007		±8kV	5pF (3.5pF @ 5V)	6V	2A	1	0201 Flipchip
SP1010		±8kV	6pF (3.5pF @ 2.5V)	6V	1A	4	µDFN-6 1.25x1.0mm
SP1011		±15kV	12pF (7pF @ 2.5V)	6V	2A	4	µDFN-6 1.25x1.0mm

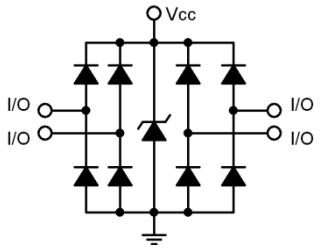
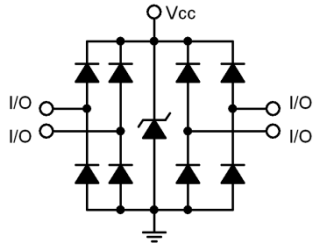
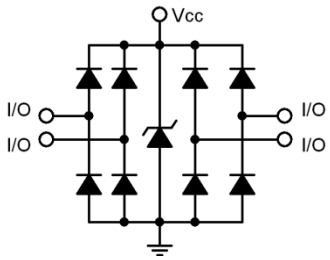
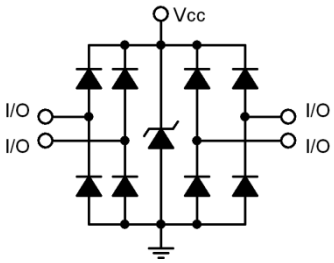
TVS Diode Arrays (SPA™) Series Descriptions

General Purpose ESD Protection *(continued)*

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap	V_{RWM}	Lightning (t_P=8/20µs)	Number of Channels	Package Options
SP720		±4kV	3pF	30V or (±15V)	3A	14	SOIC-16 PDIP-16
SP721		±4kV	3pF	30V or (±15V)	3A	6	SOIC-8 PDIP-8
SP723		±8kV	5pF	30V or (±15V)	7A	6	SOIC-8 PDIP-8
SP724		±8kV	3pF	20V or (±10V)	3A	4	SOT23-6
SP725		±8kV	5pF	30V or (±15V)	14A	4	SOIC-8

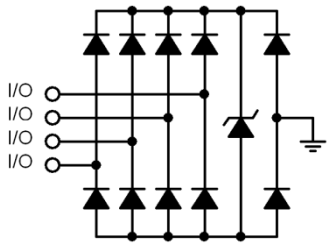
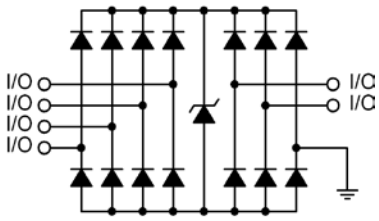
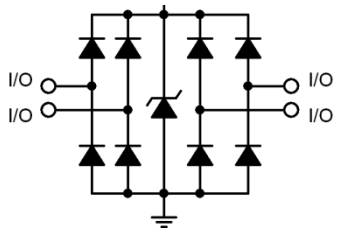
TVS Diode Arrays (SPA™) Series Descriptions

Low Capacitance ESD Protection

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V_R= 1.65V	V_{RWM}	Lightning (t_P=8/20µs)	Number of Channels	Package Options
SP3001		±8kV	0.65pF	6V	2.5A	4	SC70-6
SP3002		±12kV	0.85pF	6V	4.5A	4	SC70-6 SOT23-6 µDFN-6 1.6x1.6mm
SP3003		±8kV	0.65pF	6V	2.5A	2	SC70-5 SOT553
						4	SC70-6 SOT563 MSOP-10
						8	MSOP-10
SP3004		±12kV	0.85pF	6V	4A	4	SOT563

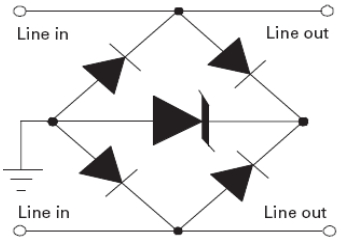
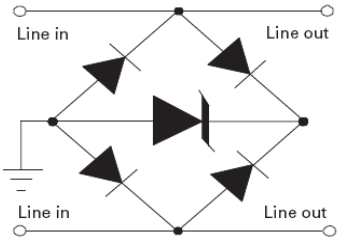
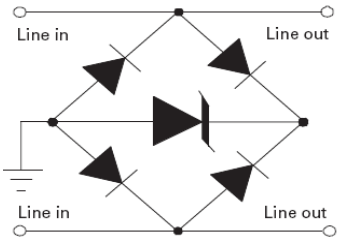
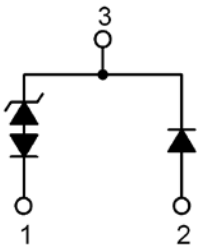
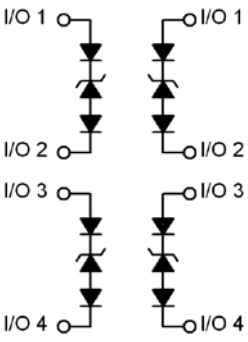
TVS Diode Arrays (SPA™) Series Descriptions

Low Capacitance ESD Protection *(continued)*

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V_R= 0V	V_{RWM}	Lightning (t_P=8/20µs)	Number of Channels	Package Options
SP3010		±8kV	0.45pF	6V	3A	4	µDFN-10 2.5x1.0mm
SP3011		±8kV	0.40pF	6V	3A	6	µDFN-14 3.5x1.35mm
SP3012		±12kV	0.50pF	5V	4A	4	µDFN-10 2.5x1.0mm
SP3021 (2012 release)		±8kV	0.50pF	5V	1A	1	SOD882
SP3031 (2012 release)		±10kV	0.80pF	5V	5A	1	SOD882

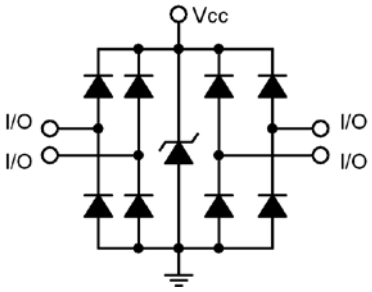
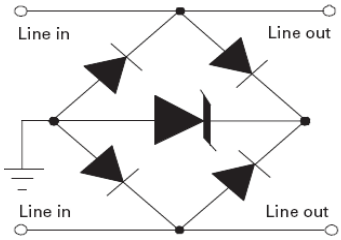
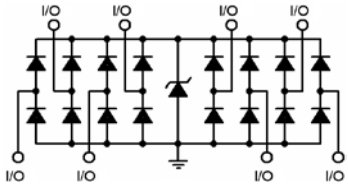
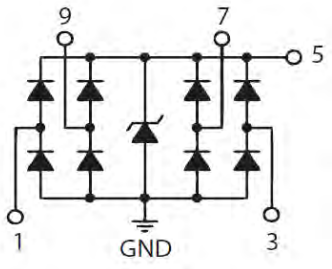
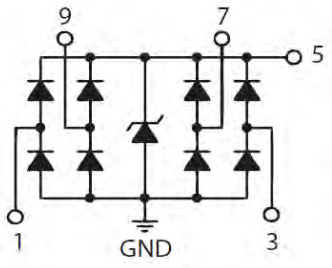
TVS Diode Arrays (SPA™) Series Descriptions

Lightning Surge Protection

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V_R= 0V	V_{RWM}	Lightning (t_P=8/20µs)	Number of Channels	Package Options
SP03-3.3		±30kV	16pF (8pF I/O to I/O)	3.3V	150A	2	SOIC-8
SP03A-3.3		±30kV	9pF (4.5pF I/O to I/O)	3.3V	150A	2	SOIC-8
SP03-6		±30kV	16pF (8pF I/O to I/O)	6V	150A	2	SOIC-8
SPLV2.8		±30kV	2pF	2.8V	40A	1	SOT23-3
SPLV2.8-4		±30kV	2pF	2.8V	40A	4	SOIC-8

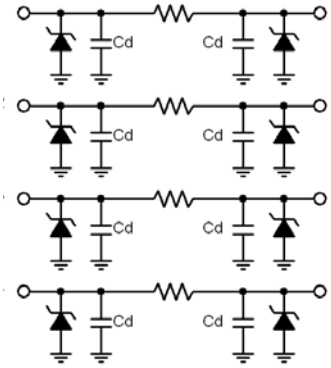
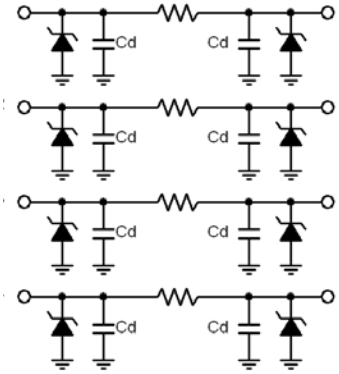
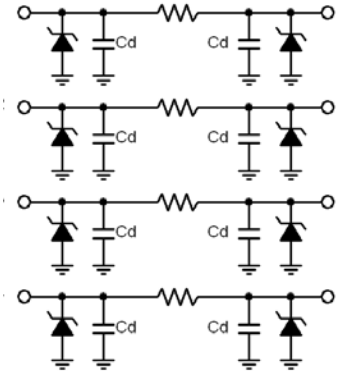
TVS Diode Arrays (SPA™) Series Descriptions

Lightning Surge Protection *(continued)*

Series	Schematic (Example)	ESD Level (Contact)	I/O Cap V_R= 0V	V_{RWM}	Lightning (t_P=8/20µs)	Number of Channels	Package Options
SP3050		±20kV	2.4pF	6V	10A	4	SOT23-6
SP4040		±30kV	5pF (2.5pF I/O to I/O)	3.3V	75A	2	SOIC-8
SP4060		±30kV	4.4pF	2.5V	20A	8	MSOP-10
SP4061		±30kV	3.5pF	2.5V	20A	4	µDFN-10 2.6x2.6mm
SP4062		±30kV	3.5pF	3.3V	20A	4	µDFN-10 2.6x2.6mm

TVS Diode Arrays (SPA™) Series Descriptions

EMI Filter Arrays with ESD Protection

Series	Schematic (Example)	ESD Level (Contact)	Line Cap (V_R=2.5V)	V_{RWM}	Attenuation	Number of Channels	Package Options
SP6001		±30kV	24pF (C_{DIODE}=12pF)	6V	≥ -30dB @ 1GHz	4	µDFN-8 1.7x1.35mm
						6	µDFN-12 2.5x1.35mm
						8	µDFN-16 3.3x1.35mm
SP6002		±30kV	30pF (C_{DIODE}=15pF)	6V	≥ -30dB @ 1GHz	4	µDFN-8 1.7x1.35mm
						6	µDFN-12 2.5x1.35mm
SP6003 (not yet released)		±15kV	14pF (C_{DIODE}=7pF)	6V	≥ -20dB @ 1GHz	4	µDFN-8 1.7x1.35mm
						6	µDFN-12 2.5x1.35mm

TVS Diode Array Ordering Guide

Series	Number of Channels	Package	Orderable Part Number
SP05	2	SOT23-3	SP0502BAHTG
		SC70-3	SP0502BAJTG
	3	SOT143	SP0503BAHTG
	4	SOT23-5	SP0504BAHTG
		SC70-5	SP0504BAJTG
	5	SOT23-6	SP0505BAHTG
		SC70-6	SP0505BAJTG
	6	MSOP-8	SP0506BAATG
SP1001	2	SC70-3	SP1001-02JTG
		SOT553	SP1001-02XTG
	4	SC70-5	SP1001-04JTG
		SOT553	SP1001-04XTG
	5	SC70-6	SP1001-05JTG
		SOT56	SP1001-05XTG
SP1002	1	SC70-3	SP1002-01JTG
	2	SC70-5	SP1002-02JTG
SP1003	1	SOD723	SP1003-01DTG
		SOD882	SP1003-01ETG
SP1004	4	SOT953	SP1004-04VTG
SP1005	1	0201 Flipchip	SP1005-01WTG
SP1006	1	0201 (µDFN-2,0.6x0.3mm)	SP1006-01UTG
SP1007	1	0201 Flipchip	SP1007-01WTG
SP1010	4	µDFN-6 (1.25x1.0mm)	SP1010-04UTG
SP1011	4	µDFN-6 (1.25x1.0mm)	SP1011-04UTG
SP3001	4	SC70-6	SP3001-04JTG
SP3002	4	SOT23-6	SP3002-04HTG
		SC70-6	SP3002-04JTG
		µDFN-6 (1.6x1.6mm)	SP3002-04UTG
SP3003	2	SC70-5	SP3003-02JTG
		SOT553	SP3003-02XTG
	4	SC70-6	SP3003-04JTG
		SOT563	SP3003-04XTG
		MSOP-10	SP3003-04ATG
	8	MSOP-10	SP3003-08ATG
SP3004	4	SOT563	SP3004-04XTG

TVS Diode Array Ordering Guide (continued)

Series	Number of Channels	Package	Orderable Part Number
SP3010	4	µDFN-10 (2.5x1.0mm)	SP3010-04UTG
SP3011	6	µDFN-14 (3.5x1.35mm)	SP3011-06UTG
SP3012	4	µDFN-10 (2.5x1.0mm)	SP3012-04UTG
SP3021	1	SOD882	SP3021-01ETG
SP3031	1	SOD882	SP3031-01ETG
SP3050	4	SOT23-6	SP3050-04HTG
SP4040	2	SOIC-8	SP4040-02BTG
SP4060	8	MSOP-10	SP4060-08ATG
SP4061	4	µDFN-10 (2.6x2.6mm)	SP4061-04UTG
SP4062	4	µDFN-10 (2.6x2.6mm)	SP4062-04UTG
SP03-3.3	2	SOIC-8	SP03-3.3BTG
SP03A-3.3	2	SOIC-8	SP03A-3.3BTG
SP03-6	2	SOIC-8	SP03-6BTG
SPLV2.8	1	SOT23-3	SPLV2.8HTG
SPLV2.8-4	4	SOIC-8	SPLV2.8-4BTG
SP6001	4	µDFN-8 (1.7x1.35mm)	SP6001-04UTG-1
	6	µDFN-12 (2.5x1.35mm)	SP6001-06UTG-1
	8	µDFN-16 (3.3x1.35mm)	SP6001-08UTG-1
SP6002	4	µDFN-8 (1.7x1.35mm)	SP6002-04UTG-1
	6	µDFN-12 (2.5x1.35mm)	SP6002-06UTG-1
SP6003 (not released)	4	µDFN-8 (1.7x1.35mm)	SP6003-04UTG-1
	6	µDFN-12 (2.5x1.35mm)	SP6003-06UTG-1
SP720	14	PDIP-16	SP720APP
	14	SOIC-16	SP720AB*G
SP721	6	PDIP-8	SP721APP
	6	SOIC-8	SP721AB*G
SP723	6	PDIP-8	SP723APP
	6	SOIC-8	SP723AB*G
SP724	4	SOT23-6	SP724AHTG
SP725	4	SOIC-8	SP725AB*G

**Add "T" for Tape and Reel, otherwise parts are packed in tubes*

Application Specific Device Selection

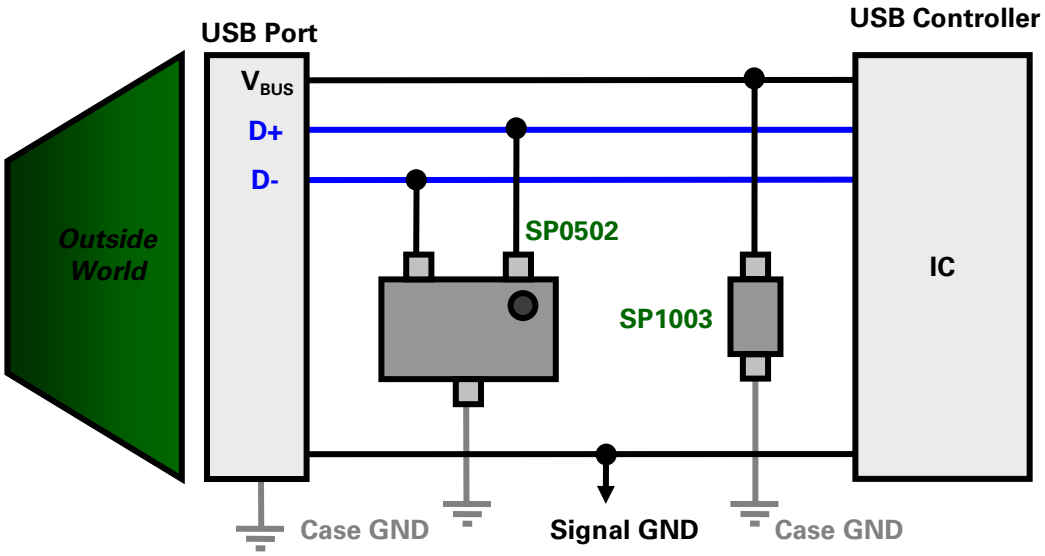
USB1.1

Considerations:

- Each port operates at either 1.5Mbps or 12Mbps (low and full speed respectively)
  - Parasitic capacitance should be taken into account although these relatively slow speeds can tolerate tens of picofarads

- Requires 2 channels of data line protection per port (i.e. D±)
  - A 4 channel device can be useful if protecting a USB stack of 2 ports to make the ESD footprint as small as possible
  - V_{BUS} can be protected separately with a single channel device in an 0402 or 0201 form factor (0402 shown)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=2.5V	# of Channels	V_{RWM}	Packaging
SP0502BAJTG	±30kV	30pF	2	5.5V	SC70-3
SP1001-02XTG	±15kV	8pF	2	5.5V	SOT553
SP1003-01ETG	±30kV	17pF	1	5.0V	0402 (SOD882)
SP1003-01DTG	±30kV	17pF	1	5.0V	0402 (SOD723)
SP1006-01UTG	±30kV	15pF	1	5.0V	0201 (µDFN-2)

Application Specific Device Selection

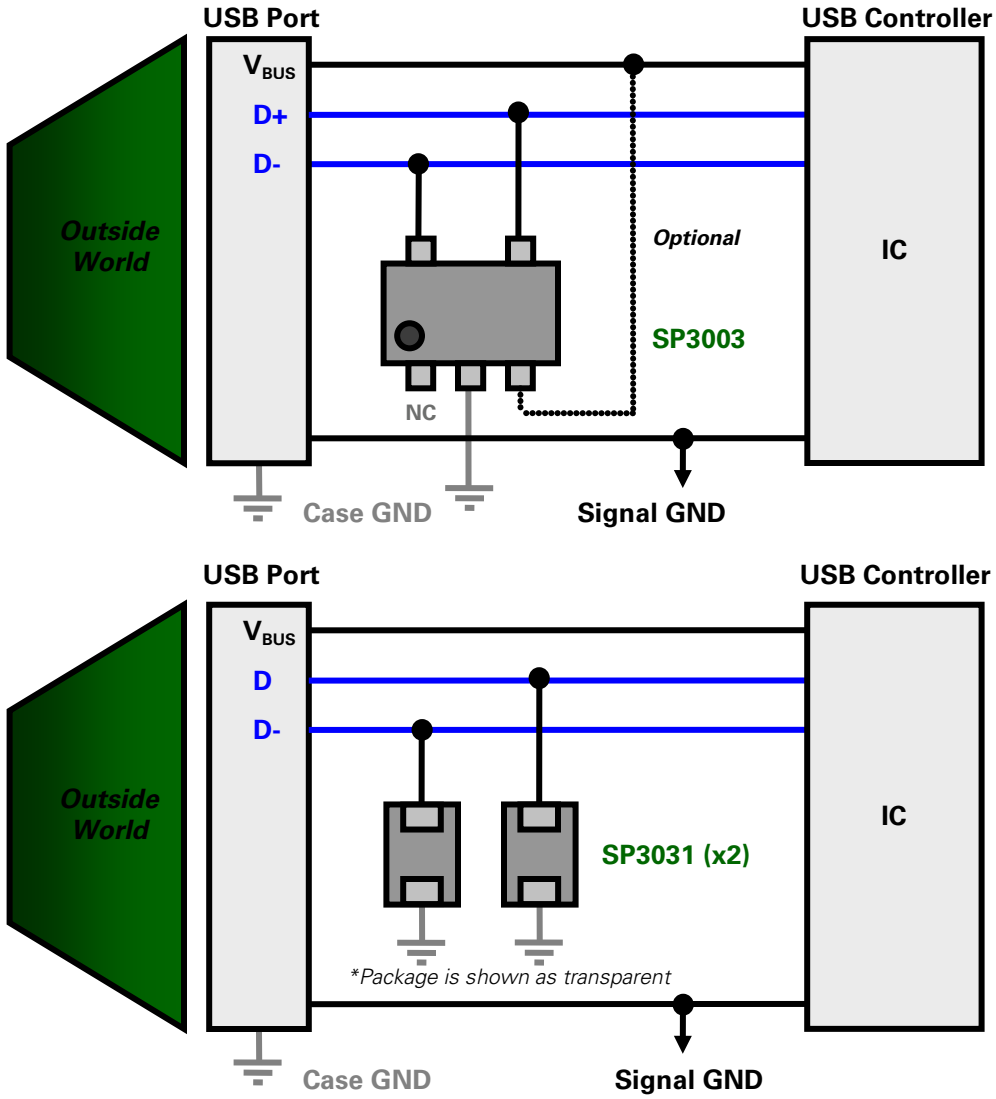
USB2.0

Considerations:

- Each port can operate up to 480Mbps
  - The high data rate requires a low capacitance device to preserve signal integrity

- Requires 2 channels of data line protection per port (i.e. D±) which can be done via array or discretely
  - A 4 channel device such as the SP3002-04 can be useful if protecting a USB stack of 2 ports to make the ESD footprint as small as possible
  - V_{BUS} can be protected by connecting it to the V_{CC} pin on the diode array or by using a separate single channel device like the SP1003

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3003-02XTG	±8kV	0.65pF	2	6V	SOT553
SP3003-02JTG	±8kV	0.65pF	2	6V	SC70-5
SP3031-01ETG (2012 release)	±10kV	0.80pF	1	5V	SOD882

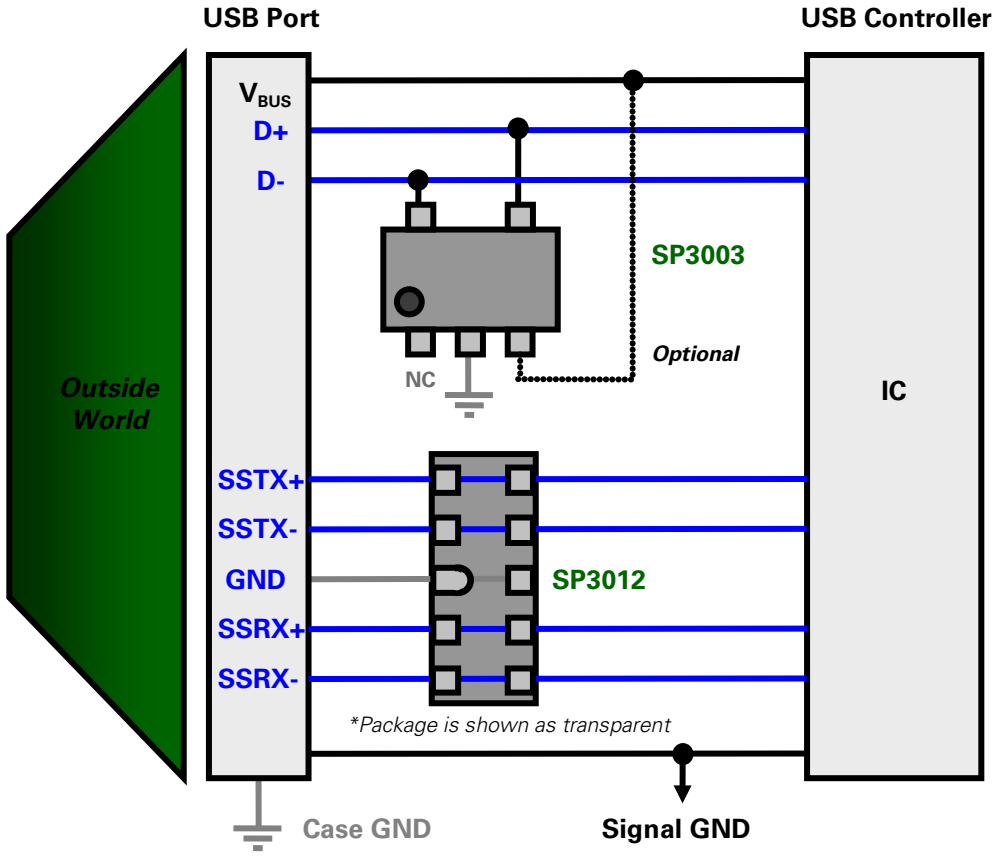
Application Specific Device Selection

USB3.0 (Two Device Solution)

Considerations:

- Each port depending upon what it's connected to can operate:
  - Up to 5Gbps over the new super-speed data pairs, SSTX± and SSRX±
  - Up to 480Mbps on the legacy data pair, D±
- Requires 4 channels of ultra-low capacitance protection for the super-speed data pair (i.e. SSTX± and SSRX±)
- Requires 2 channels of protection for the legacy D± data pair
  - V_{BUS} can be protected by connecting it to the V_{CC} pin on the SPA or by using a separate single channel device

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3003-02XTG	±8kV	0.65pF	2	6V	SOT553
SP3012-04UTG	±12kV	0.50pF	4	5V	µDFN-10 (2.5x1.0mm)

Application Specific Device Selection

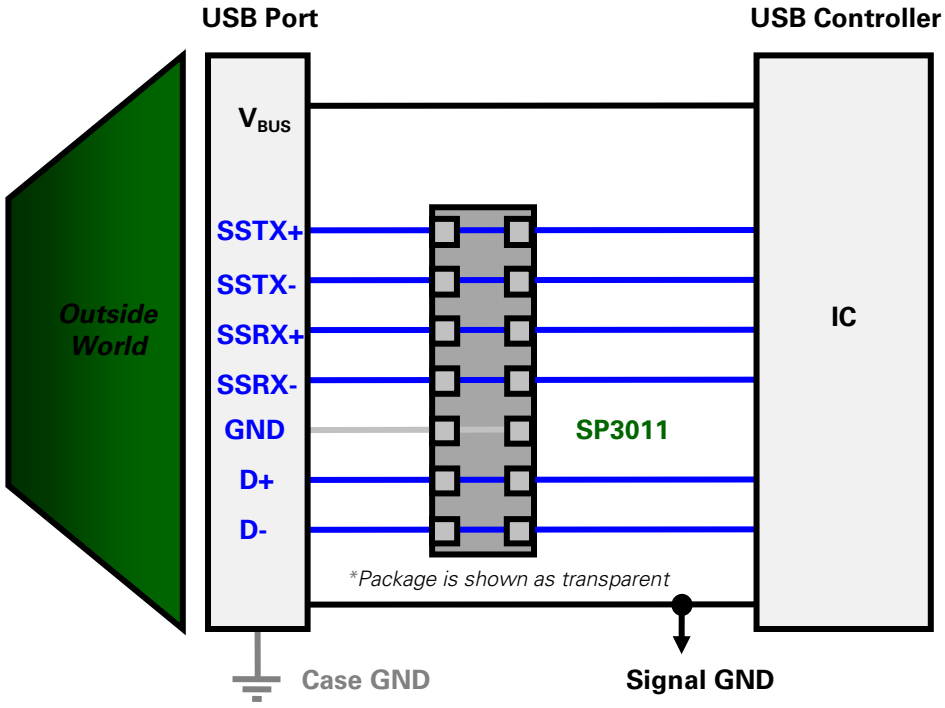
USB3.0 (Fully Integrated Solution)

Considerations:

- Each port depending upon what it's connected to can operate:
  - Up to 5Gbps over the new super-speed data pairs, SSTX± and SSRX±
  - Up to 480Mbps on the legacy data pair, D±

- Requires 4 channels of ultra-low capacitance protection for the super-speed data pair (i.e. SSTX± and SSRX±) and 2 channels of protection for the legacy D± data pair. The SP3011 shown below integrates all 6 channels of protection into a small form factor µDFN-14 package.

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=0V	# of Channels	V_{RWM}	Packaging
SP3011-06UTG	±8kV	0.40pF	6	6V	µDFN-14 (3.5x1.35mm)

Application Specific Device Selection

HDMI

Considerations:

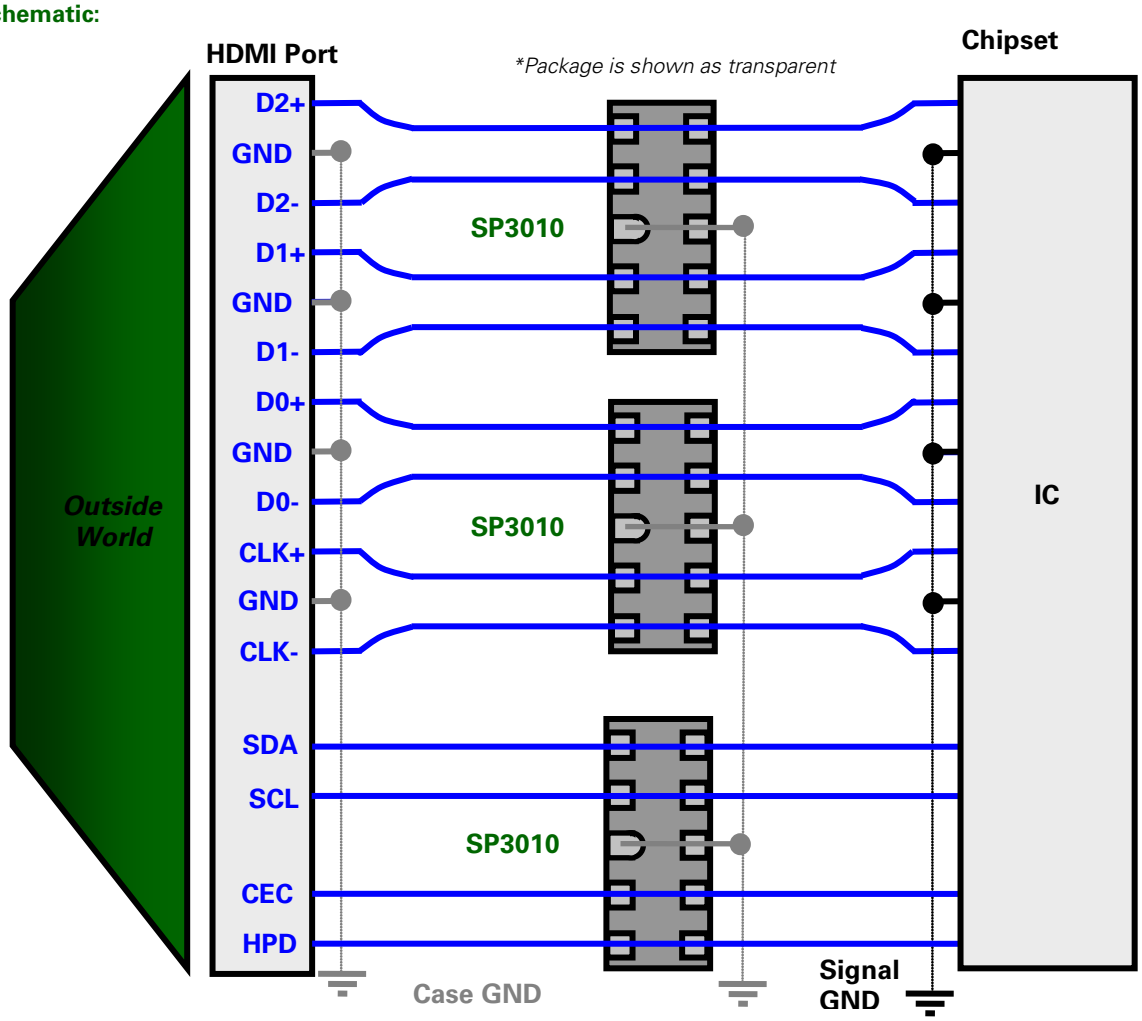
- Each port has 3 differential pairs of data (i.e. D0±, D1±, D2±) plus a clock (CLK±)
  - For HDMI 1.1-1.2 the throughput is a total of 4.95Gbps (1.65Gbps per lane)
  - For HDMI 1.3-1.4 the throughput is a total of 10.2Gbps (3.4Gbps per lane)

- To maintain the differential impedance per the HDMI Compliance Test Specification (and consequently signal integrity) a very low capacitance device must be used

- To maintain the differential impedance the designer should avoid using 90° angles and vias
  - This can be accomplished by the use of an ESD device that offers a "straight-through" routing scheme

- Requires 12 channels of protection : 8 TMDS data pairs, SDA, SCL, CEC, and HPD

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3010-04UTG	±8kV	0.45pF	4	6V	µDFN-10 (2.5x1.0mm)
SP3012-04UTG)	±12kV	0.50pF	4	5V	µDFN-10 (2.5x1.0mm)

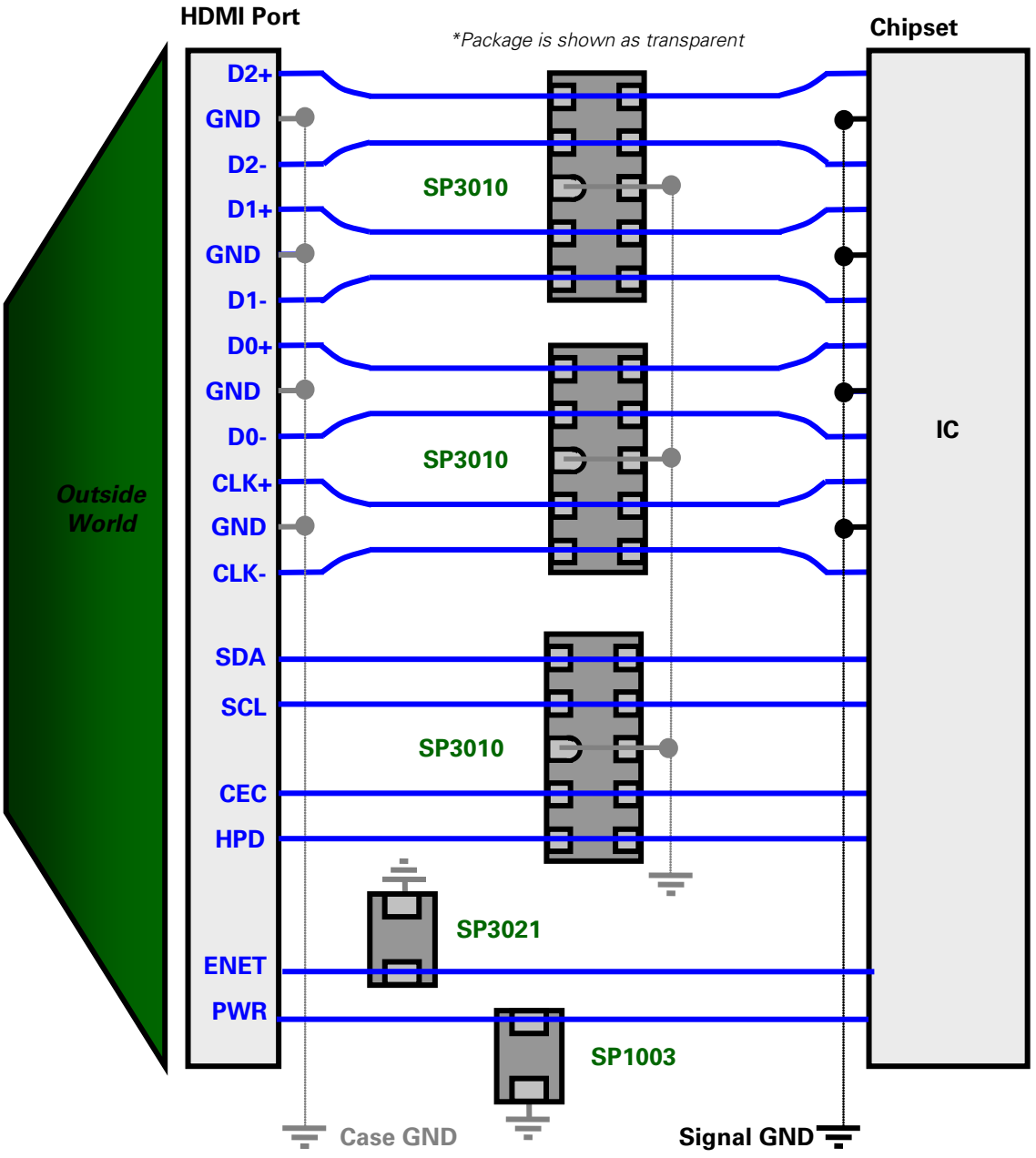
Application Specific Device Selection

HDMI (includes protection for Ethernet and 5V power)

Considerations:

- Same as noted on previous page except the protection scheme below includes options for protecting additional Ethernet and 5V power pins.
- Other combinations exist such as using 2, 6 channel SP3011 devices along with 2, single channel discrete

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=2.5V	# of Channels	V_{RWM}	Packaging
SP3010-04UTG	±8kV	0.45pF	4	6V	µDFN-10 (2.5x1.0mm)
SP3012-04UTG)	±12kV	0.50pF	4	5V	µDFN-10 (2.5x1.0mm)
SP3021-01ETG (2012 release)	±8kV	0.50pF	1	5V	0402 (SOD882)
SP1003-01ETG (SP1003)	±30kV	17pF	1	6V	0402 (SOD882)

Application Specific Device Selection

Display Port

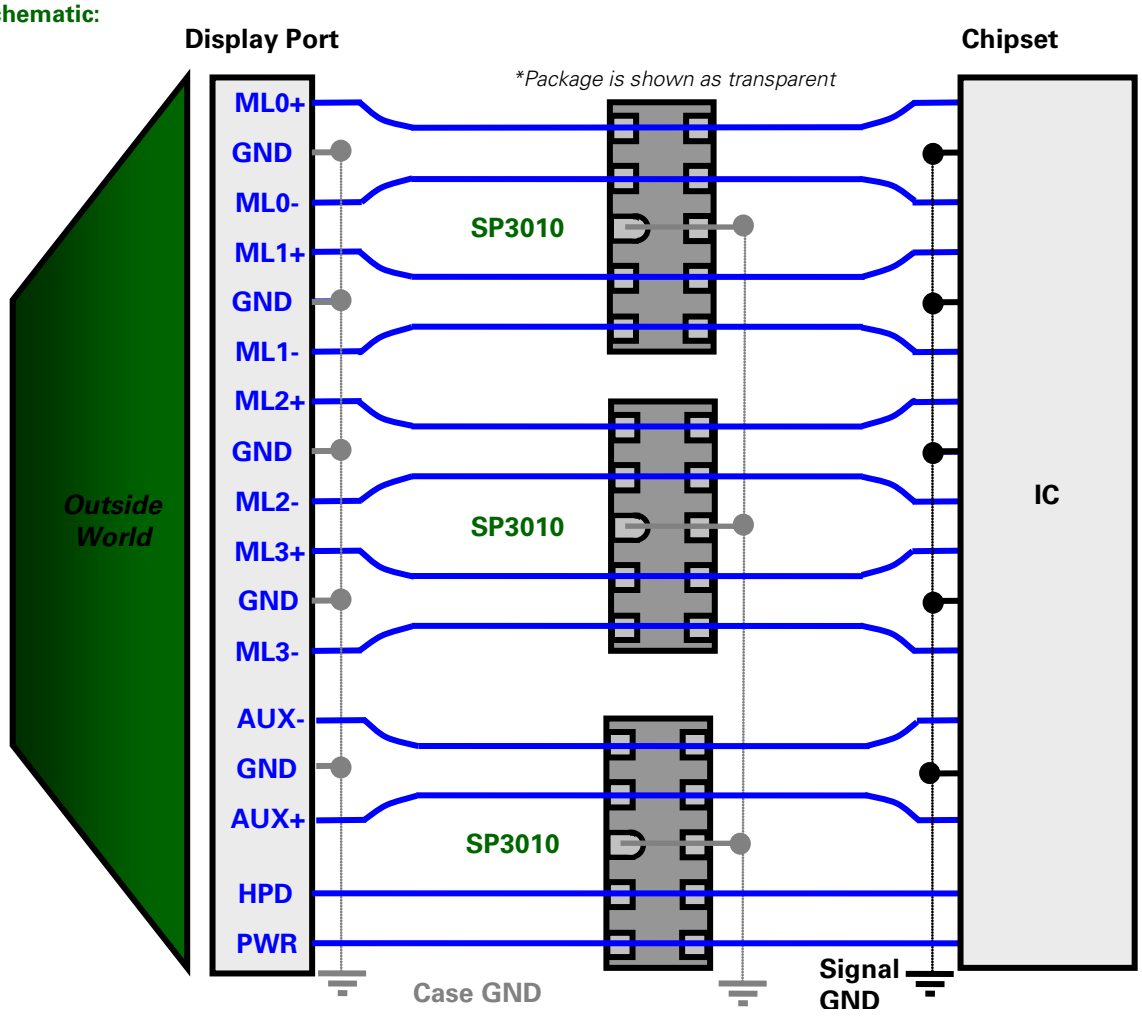
Considerations:

- Each port has a main link which contains 4 differential pairs or lanes (i.e. ML0±, ML1±, ML2±, and ML3±)
  - The total throughput is 10.8Gbps or 2.7Gbps per lane
  - The clock signal is embedded in the lanes and does not exist separately as in HDMI
  - There is also an auxiliary channel (AUX±), hot plug detect (HPD), and power pin (PWR) as well.

- To maintain the differential impedance (and consequently signal integrity) a very low capacitance device must be used
  - To maintain the differential impedance the designer should avoid using 90° angles and vias
  - This can be accomplished by the use of an ESD device that offers a "straight-through" routing scheme

- Requires 12 channels of protection per port (ML0±, ML1±, ML2±, ML3±, AUX±, HPD, and PWR)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3010-04UTG	±8kV	0.45pF	4	6V	µDFN-10 (2.5x1.0mm)
SP3012-04UTG	±12kV	0.50pF	4	5V	µDFN-10 (2.5x1.0mm)

Application Specific Device Selection

DVI

Considerations:

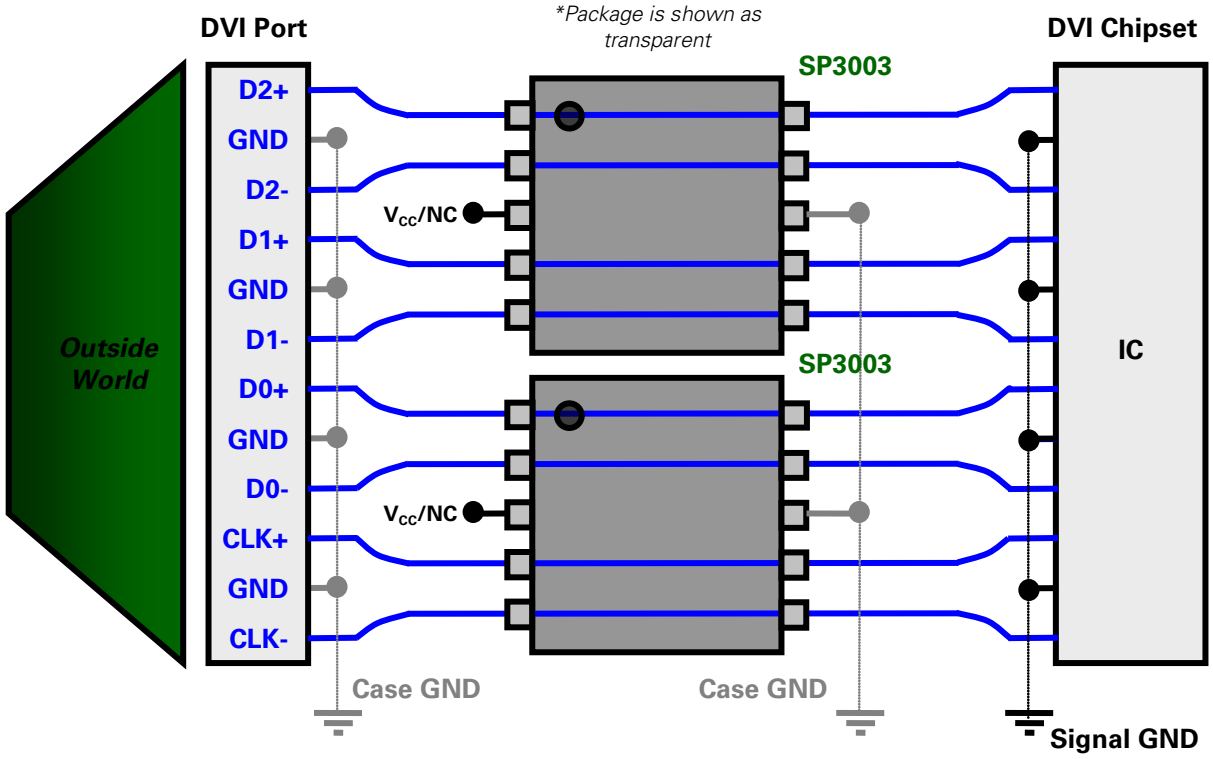
- A DVI port may have single or dual link capability
  - Each link has 3 differential lanes of data (i.e. D0±, D1±, D2±) plus a clock (CLK±)
  - For single link, the maximum throughput can approach a total of 4.95Gbps or 1.65Gbps per lane
  - For dual link, the maximum throughput can approach a total of 8Gbps or 2.67Gbps per lane

- To maintain signal integrity a very low capacitance device must be used

- To maintain the differential impedance the designer should avoid using 90° angles and vias
  - This can be accomplished by the use of an ESD device that offers a "straight-through" routing scheme

- Requires 8 channels of protection per port (D0±, D1±, D2±, CLK±)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3003-04ATG	±8kV	0.65pF	4	6V	MSOP-10
SP3010-04UTG	±8kV	0.45pF	4	6V	µDFN-10 (2.5x1.0mm)

Application Specific Device Selection

10/100/1000 Ethernet, Intra-building Lightning Immunity (GR-1089)

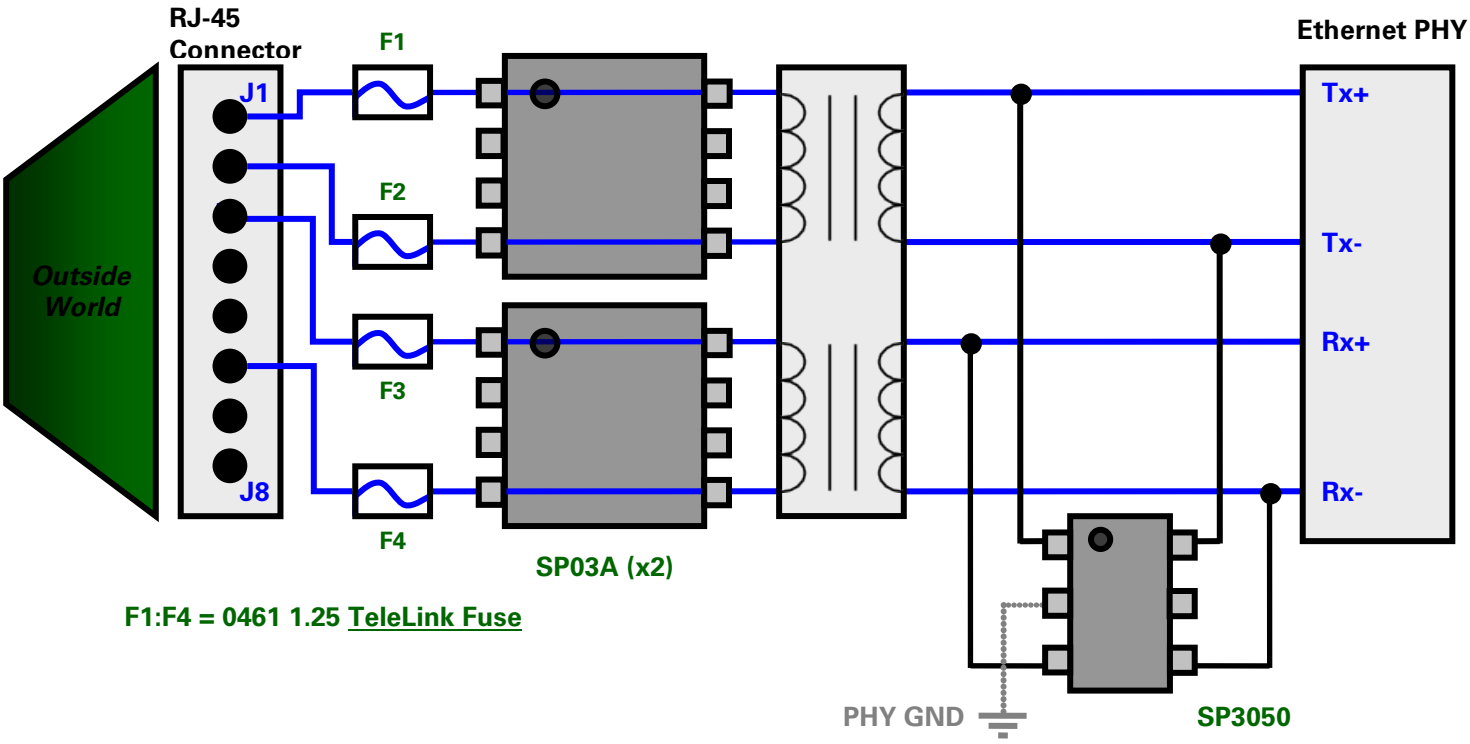
Considerations:

- 10/100/1000 relates to the data rate in Mbps (i.e. 10Mbps, 100Mbps, and 1000Mbps)
  - For 10 Base-T, data is transmitted over 2 UTP (unshielded twisted pairs) using a 10MHz clock
  - For 100 Base-TX, data is transmitted over 2 UTP using a 125MHz clock
  - For 1000 Base-T data is transmitted over 4 UTP using a 125MHz clock
  - For these data rates the parasitic capacitance needs to be taken into account to preserve signal integrity

- The 4 data lines below (Tx± and Rx±) are being protected against intra-building (i.e. 100A, t_P=2/10µs) lightning transients by a two-stage protection scheme

- 1000Mbps Ethernet (or 1GbE) will require 8 channels of protection for the 4 differential pair so the below scheme should be replicated for the remaining 2 data pair

Application Schematic:



F1:F4 = 0461 1.25 TeleLink Fuse

Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=0V	# of Channels	V_{RWM}	Packaging
SP03A-xBTG	±30kV	150A	4.5pF (I/O to I/O)	2	3.3V	SOIC-8
SP03-3.3BTG	±30kV	150A	8pF (I/O to I/O)	2	3.3V,6V	SOIC-8
SP3050-04HTG	±20kV	10A	2.4pF	4	6V	SOT23-6

Application Specific Device Selection

10/100/1000 Ethernet, Inter-building Lightning Immunity (GR-1089)

Considerations:

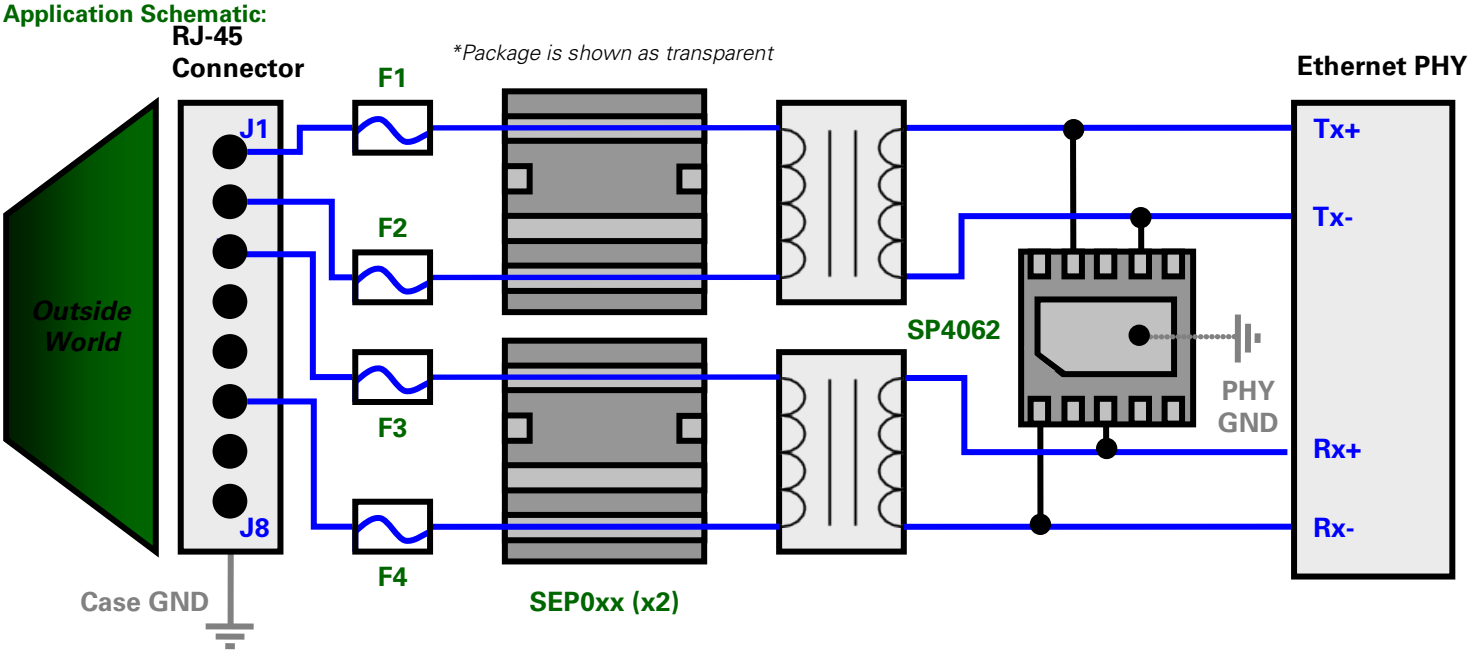
- 10/100/1000 relates to the data rate in Mbps (i.e. 10Mbps, 100Mbps, and 1000Mbps)
  - For 10 Base-T, data is transmitted over 2 UTP (unshielded twisted pairs) using a 10MHz clock
  - For 100 Base-TX, data is transmitted over 2 UTP using a 125MHz clock
  - For 1000 Base-T data is transmitted over 4 UTP using a 125MHz clock
  - For these data rates the parasitic capacitance needs to be taken into account to preserve signal integrity

- The 4 data lines below are being protected against inter-building (i.e. 500A, t_P=2/10µs) lightning transients by a two-stage protection scheme. The 4 channel, SP4061 or SP4062 should be selected based on the operating voltage of the PHY.

- The standoff voltage of the SEP Series device will be dictated by the use of PoE. If PoE is present the SEP0640 should be used; otherwise, the SEP0080 is ok for non-PoE applications. *Note: Higher voltage options are available for atypical PoE voltages.*

- 1000Mbps Ethernet (or 1GbE) will require 8 channels of protection for the 4 differential pair so the below scheme should be replicated for the remaining 2 data pair

Application Schematic:



F1:F4 = 0461 1.25 TeleLink Fuse

Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=0V	# of Channels	V_{RWM}	Packaging
SEP0080Q38CB	±30kV	400A	See datasheet	2	6V	QFN
SEP0640Q38CB	±30kV	400A	See datasheet	2	58V	QFN
SP4061-04UTG	±30kV	20A	3.5pF	4	2.5V	µDFN-10 (2.6x2.6mm)
SP4062-04UTG	±30kV	20A	3.5pF	4	3.3V	µDFN-10 (2.6x2.6mm)

Application Specific Device Selection

10/100/1000 Ethernet, Tertiary Only Lightning Immunity (General)

Considerations:

- 10/100/1000 relates to the data rate in Mbps (i.e. 10Mbps, 100Mbps, and 1000Mbps)
  - For 10 Base-T, data is transmitted over 2 UTP (unshielded twisted pairs) using a 10MHz clock
  - For 100 Base-TX, data is transmitted over 2 UTP using a 125MHz clock
  - For 1000 Base-T data is transmitted over 4 UTP using a 125MHz clock
  - For these data rates the parasitic capacitance needs to be taken into account to preserve signal integrity

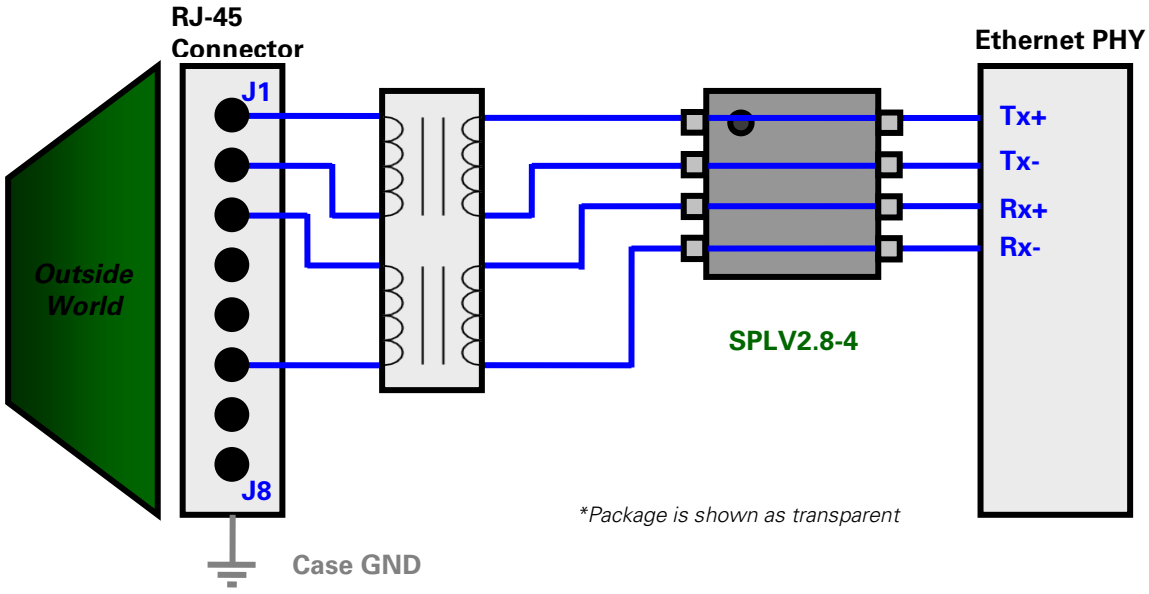
- Some designers choose to use a robust transformer in their design to act as the first line of protection against an incoming surge event. This is usually done to minimize the parasitic capacitance on the data line and to save on the cost of the primary protector

- Using such a technique will require a robust PHY side protection device and one such option is the SPLV2.8-4 shown below. It should be noted that this device will only provide differential protection between the data pairs.

- If longitudinal and differential protection are required, the SP3050-04HTG (with 2 I/O's tied per line) or SP4060/SP4061/SP4062 can be considered as alternatives

- Protection for 100Mbps Ethernet (or Fast Ethernet) is shown below. For 1000Mbps (or 1GbE) interfaces two, SPLV2.8-4BTG are required

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=0V	# of Channels	V_{RWM}	Packaging
SPLV2.8-4BTG	±30kV	40A	2.0pF	4	2.8V	SOIC-8
SP3050-04HTG	±20kV	10A	2.4pF	4	6V	SOT23-6
SP4060-08ATG	±30kV	20A	4.4pF	8	2.5V	MSOP-8
SP4061-04UTG	±30kV	20A	3.5pF	4	2.5V	µDFN-10 (2.6x2.6mm)
SP4062-04UTG	±30kV	20A	3.5pF	4	3.3V	µDFN-10 (2.6x2.6mm)

Application Specific Device Selection

10/100/1000 Ethernet (ESD only)

Considerations:

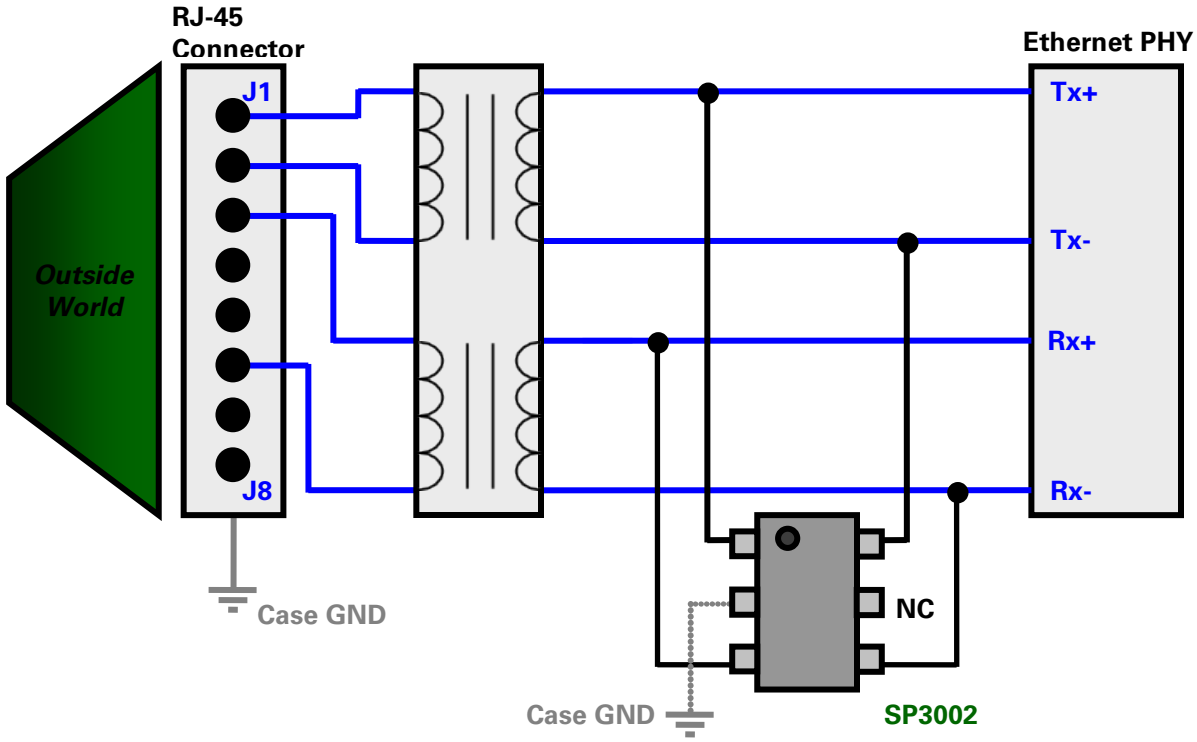
- Some Ethernet ports only need be protected for ESD and not for lightning induced transients
  - These are sometimes referred to as "2M" ports or 2 Meter ports that have very short CAT5 cable installations

- Parasitic capacitance should be taken into account especially for 1GbE

- The 4 data lines below (Tx± and Rx±) are being protected against ESD by a low capacitance SP3002 which is suitable for all Ethernet data rates
  - In fact, any low capacitance SP30xx device is suitable for any "ESD only" Ethernet application

- 1000Mbps Ethernet (or 1GbE) will require 8 channels of protection for the 4 differential pair so the below scheme can be replicated or the 8 channel SP3003-08ATG can be used.

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3002-04JTG	±12kV	4.5A	0.85pF	4	6V	SC70-6
SP3003-04XTG	±8kV	2.5A	0.65pF	4	6V	SOT563
SP3004-04XTG	±12kV	4A	0.85pF	4	6V	SOT563
SP3003-08ATG	±8kV	2.5A	0.65pF	8	6V	MSOP-10

Application Specific Device Selection

eSATA

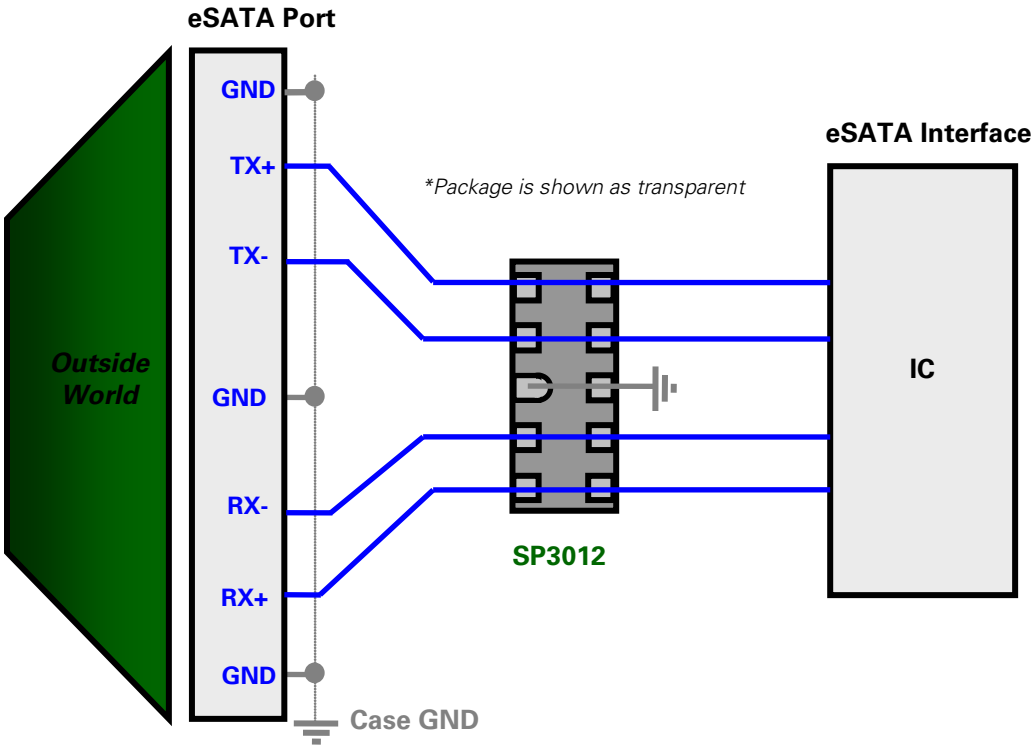
Considerations:

- eSATA is a subset of the SATA protocol that uses 2 differential pairs for communication
  - Four lines need to be protected per port (i.e. TX± and RX±)
  - Currently eSATA is capable of running raw data rates of 1.5Gbps (Gen 1) and 3.0Gbps (Gen 2)

- These high bus speeds require very low capacitance devices to prevent signal degradation

- To maintain the line impedance the designer should avoid using 90° angles and vias

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3012-04UTG	±12kV	0.50pF	4	5V	µDFN-10 (2.5x1.0mm)
SP3010-04UTG	±8kV	0.45pF	4	6V	µDFN-10 (2.5x1.0mm)
SP3003-02XTG	±8kV	0.65pF	2	6V	SOT553
SP3003-04JTG	±8kV	0.65pF	4	6V	SC70-6

Application Specific Device Selection

1394a/b

Considerations:

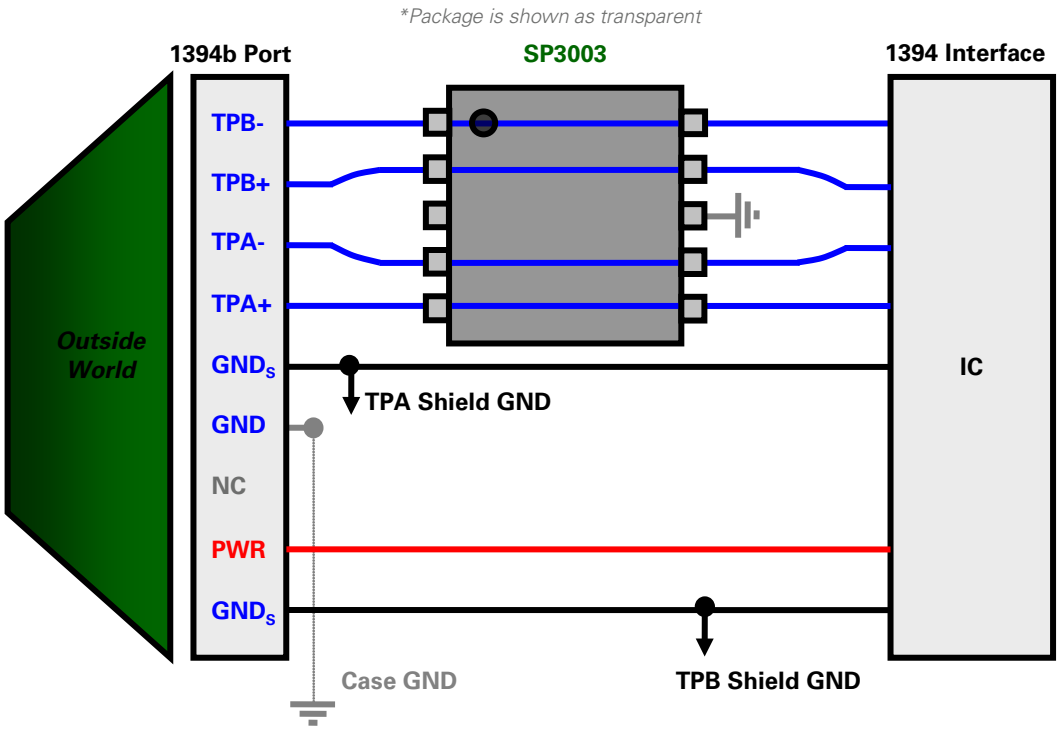
- 1394a (FireWire 400 or S400) was the original (1st generation) implementation
  - Allowed for two connectors, powered (6 pin) and unpowered (4 pin)
  - Data rates up to 400Mbps using 2 differential pair

- 1394b (FireWire 800 or S800) was the 2nd generation
  - Required a new 9 pin connector but was backwards compatible to S400
  - Data rates up to 800Mbps using 2 differential pair

- 1394b also had provisions for 1600Mbps and 3200Mbps (or S1600 and S3200)
  - Uses same 9 pin connector as S800

- S800, S1600, and S3200 require very low capacitance devices for the high speed data rates
  - Protection of 4 data lines is needed (i.e. TPB± and TPA±) and can be done with an array or with discrete low capacitance devices

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3003-04ATG	±8kV	0.65pF	4	6V	MSOP-10
SP3010-04UTG	±8kV	0.45pF	4	6V	µDFN-10
SP3012-04UTG	±12kV	0.50pF	4	5V	µDFN-10 (2.5x1.0mm)
SP3021-01ETG (2012 release)	±8kV	0.50pF	1	5V	SOD882

Application Specific Device Selection

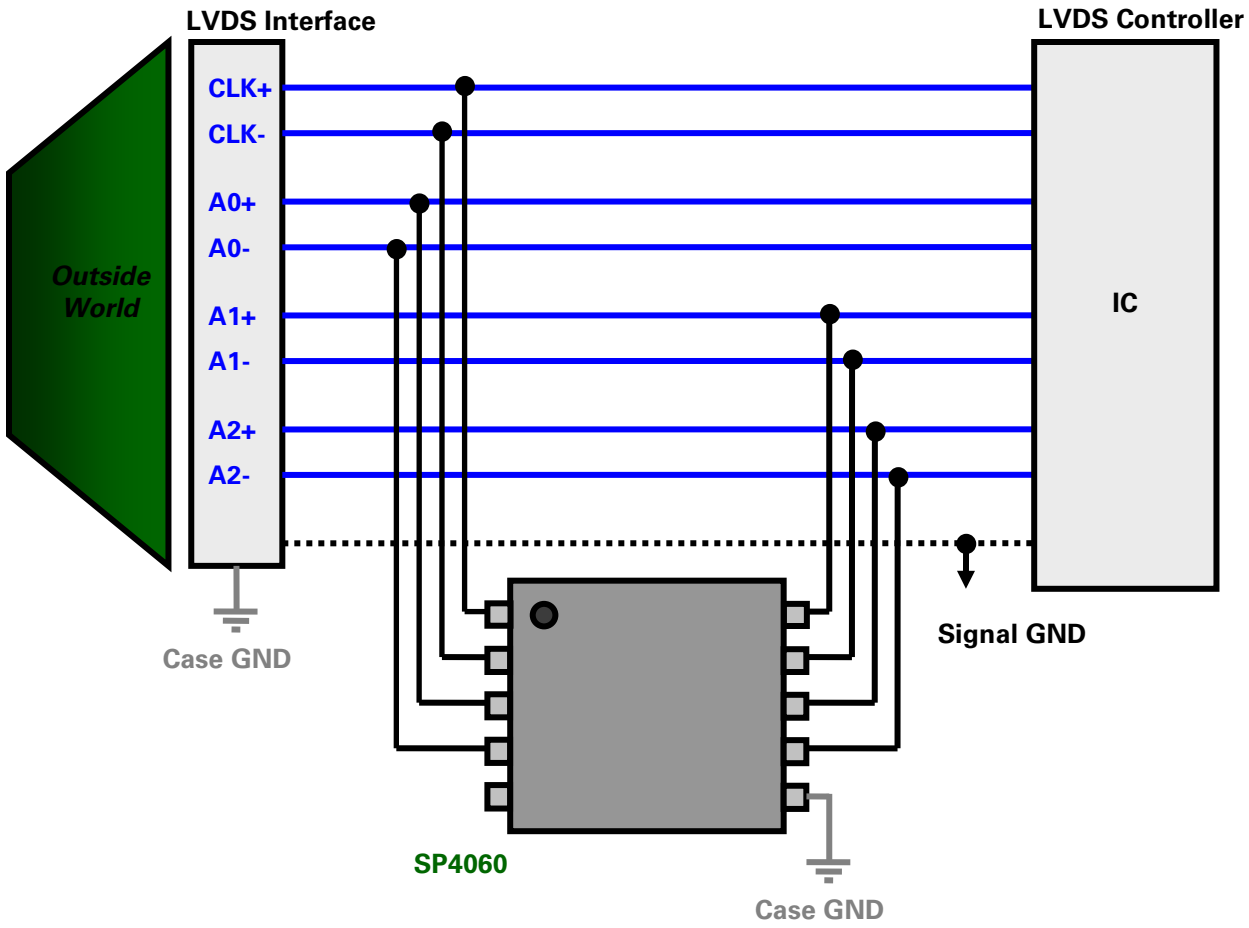
LVDS (Low Voltage Differential Signaling)

Considerations:

- LVDS is a low noise, low-voltage signal scheme that uses a small current (typically 3.5mA) to generate a voltage drop across a 100Ω resistor to convey information or data
  - Data rates can vary per application but the ANSI/TIA/EIA-644-A standard recommends a maximum of 655Mbps

- The medium/high speed bus requires a low capacitance device in 1-6pF range (typically)
  - LVDS schemes will vary in terms of the total number of channels used
  - Protection of 8 data lines is shown below (i.e. CLK± and Ax±)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=0V	# of Channels	V_{RWM}	Packaging
SP4060-08ATG	±30kV	20A	4.4pF	8	2.5V	MSOP-10
SP3050-04HTG	±20kV	10A	2.4pF	4	6V	SOT23-6
SP4061-04UTG	±30kV	20A	3.5pF	4	2.5V	µDFN-10 (2.6x2.6mm)

Application Specific Device Selection

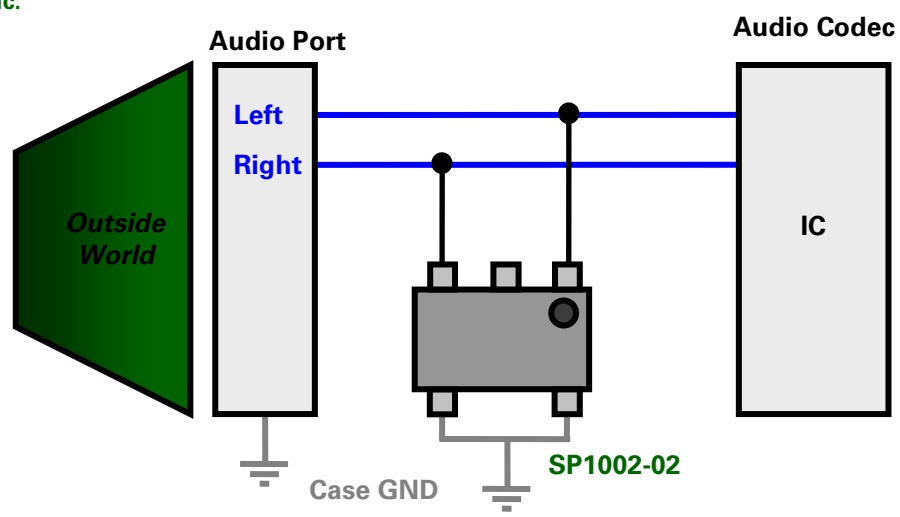
Audio (Speaker/Microphone)

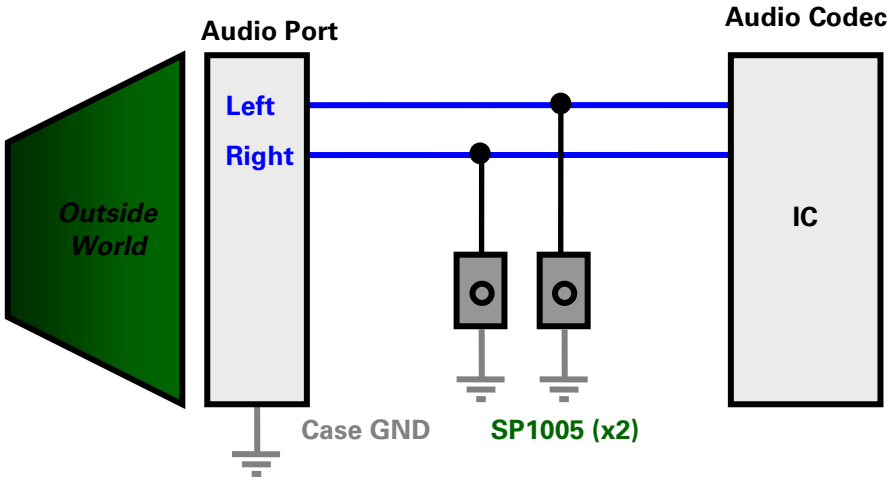
Considerations:

- Audio ports typically have signals that swing above and below GND (i.e. ±2.5V)
  - If no DC bias is applied, a bidirectional protection device should be used as these devices will not clip the analog signal
  - Protection of 2 data lines is shown below (i.e. Left and Right) with an array and with discrete 0201s

- Some audio ports will bias the data bus so that the signal never swings below GND (i.e. 0-5V)
  - If a bias is applied, a unidirectional OR bidirectional protection device could be used as neither device would clip the analog signal
  - The SP1001-02XTG is a good option in this case (not shown for Left and Right but is listed below)

Application Schematic:





Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=2.5V	# of Channels	V_{RWM}	Packaging
SP1002-02JTG	±8kV	2A	5pF	2	6V	SC70-5
SP1005-01WTG	±30kV	10A	23pF	1	6V	0201 Flipchip
SP1001-02XTG	±15kV	2A	8pF	2	5.5V	SOT553

Application Specific Device Selection

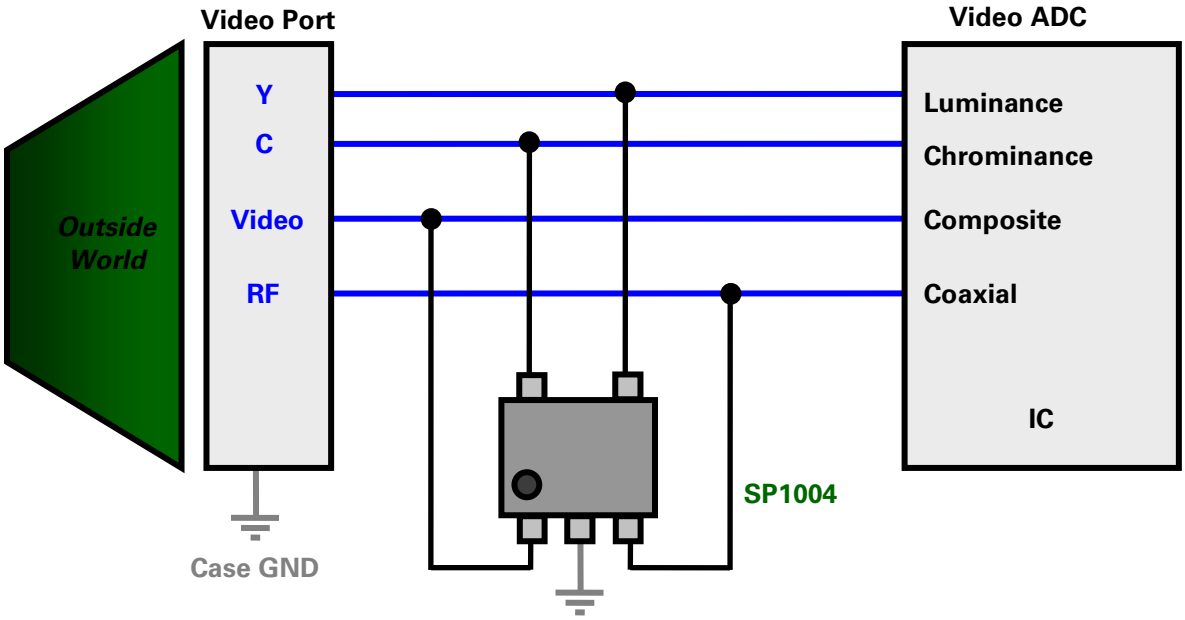
Analog Video

Considerations:

- Analog video ports typically have signals that swing above and below GND (i.e. ±2V)
  - A bidirectional protection device should be used as these devices will not clip the analog signal

- S-Video, Composite, and RF/Coaxial are a few of the common low-speed analog video signals in use today
  - Typical bus speeds will not exceed 5MHz so capacitance is not much of a concern
  - Protection of the three are shown below (Y, C, Video, and RF)

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=2.5V	# of Channels	V_{RWM}	Packaging
SP1004-04VTG	±8kV	2A	4.5pF	4	6V	SOT953
SP1002-02JTG	±8kV	2A	5pF	2	6V	SC70-5
SP1005-01WTG	±30kV	10A	23pF	1	6V	0201 Flipchip
SP1007-01WTG	±8kV	2A	3.5pF	1	6V	0201 Flipchip

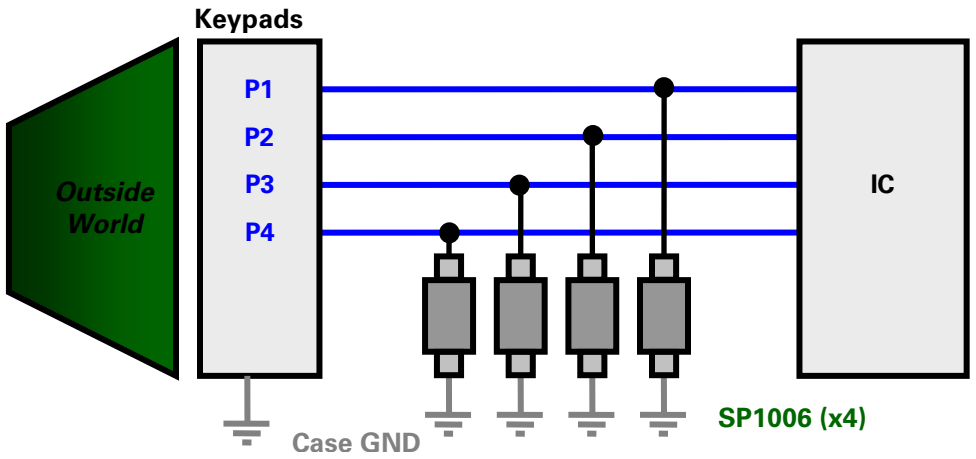
Application Specific Device Selection

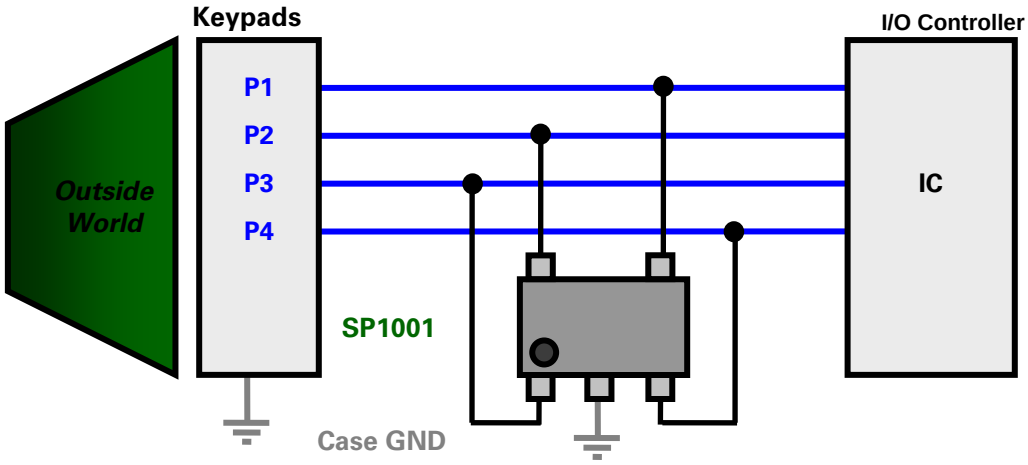
Keypad/Push Buttons

Considerations:

- Keypads and push buttons on electronic devices are particularly susceptible to ESD due to constant human interaction
  - Most are DC switches that operate at less than 5V, and for most applications capacitance will not be a concern
- The number of ports will vary with the particular application, but as an example, 4 data lines are shown below (i.e.Px)
- For space constrained applications the SP1003 or SP1005 may be considered as they are 0402 and 0201 footprints, respectively

Application Schematics:





Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=2.5V	# of Channels	V_{RWM}	Packaging
SP1001-04XTG	±15kV	2A	8pF	4	6V	SOT553
SP1003-01ETG	±30kV	7A	17pF	1	5V	0402 (SOD882)
SP1005-01WTG	±30kV	10A	23pF	1	6V	0201 Flipchip
SP1006-01UTG	±30kV	5A	15pF	1	6V	0201 (µDFN-2)

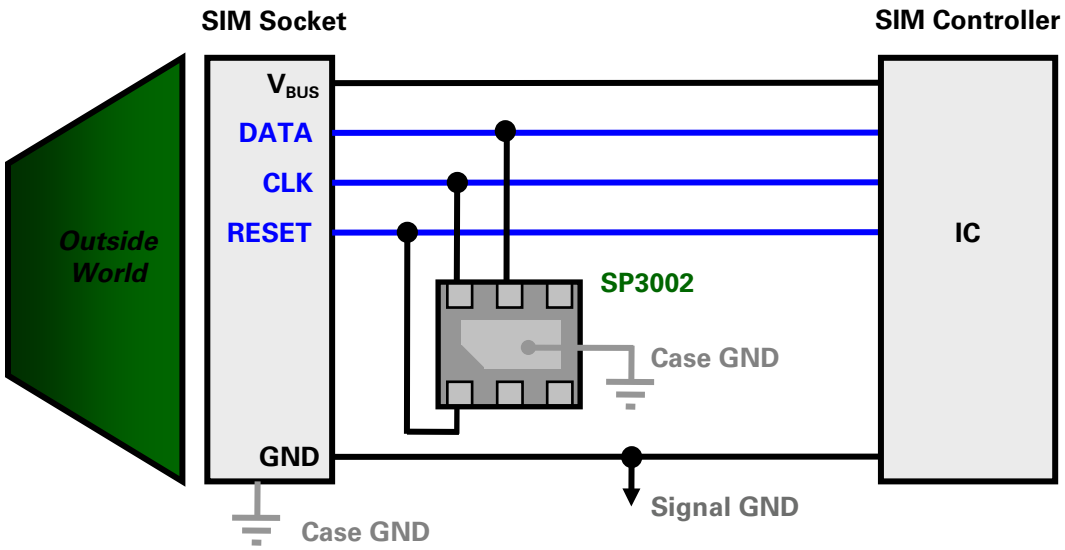
Application Specific Device Selection

SIM Socket

Considerations:

- The SIM (Subscriber Identification Module) card has 3 data lines that are low-speed and low-voltage
  - Given the low speed of the signals, the capacitance will not be a concern
- The low-voltage signal lines are best protected by a device which has a low standoff voltage or V_{RWM}
- Protection of the 3 data lines is shown below (i.e. CLK, DATA, and RESET)

Application Schematics:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP3002-04UTG	±12kV	4.5A	0.85pF	4	6V	µDFN-6 (1.6x1.6mm)
SP1011-04UTG	±15kV	2A	7pF	4	6V	µDFN-6 (1.25x1.0mm)
SP1005-01WTG	±30kV	10A	23pF	1	6V	0201 Flipchip
SP1006-01UTG	±30kV	5A	15pF	1	6V	0201 (µDFN-2)

Application Specific Device Selection

RS-232

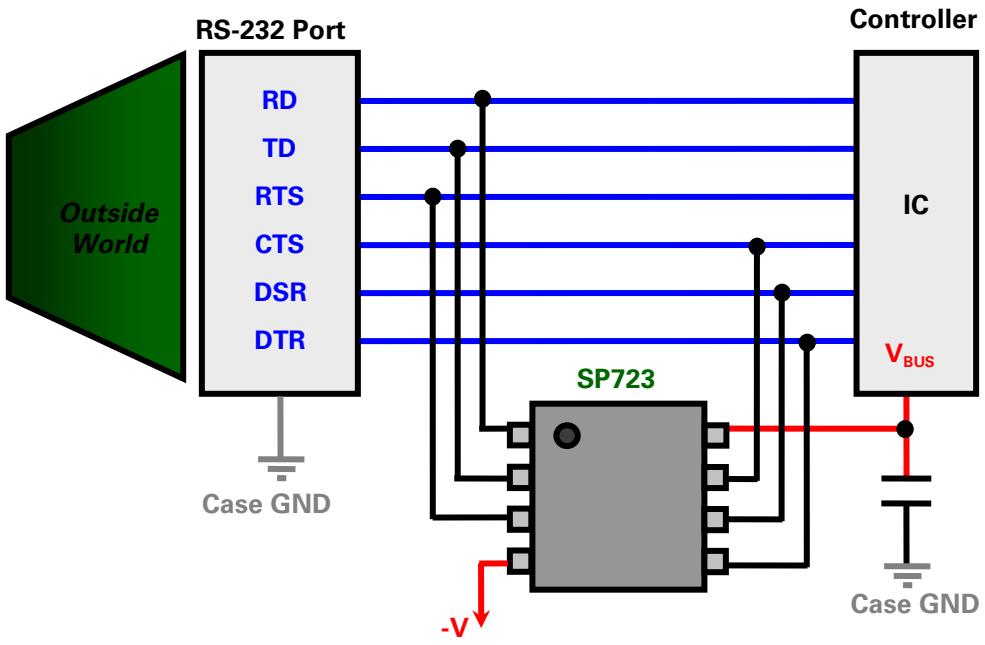
Considerations:

- There are numerous implementations of RS-232
  - Most involve 6 wires (as shown below) though some may only include 2, 3, or 5 wires
  - The maximum data rate is 20kbps
  - Typically bus voltages are bipolar and can swing as high as ±24V though most installations are limited to ±12V or even lower
  - For ±12V systems the SP72x Series is recommended and shown below

- Some implementations are a unipolar (i.e. 0-3.3V or 0-5V) or use bus voltages generally below 6V
  - In this event the SP1001 Series can be used for ESD protection or the SP03 Series could be used if lightning is the primary threat

- Every application should be evaluated thoroughly before using the recommended devices below

Application Schematics:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=1.65V	# of Channels	V_{RWM}	Packaging
SP721ABTG	±4kV	3A	3pF	6	30V	SOIC-8
SP723ABTG	(±8kV	7A	5pF	6	30V	SOIC-8
SP724AHTG	±8kV	3A	3pF	4	20V	SOT23-6
SP725ABTG	±8kV	14A	5pF	4	30V	SOIC-8

Application Specific Device Selection

RS-485

Considerations:

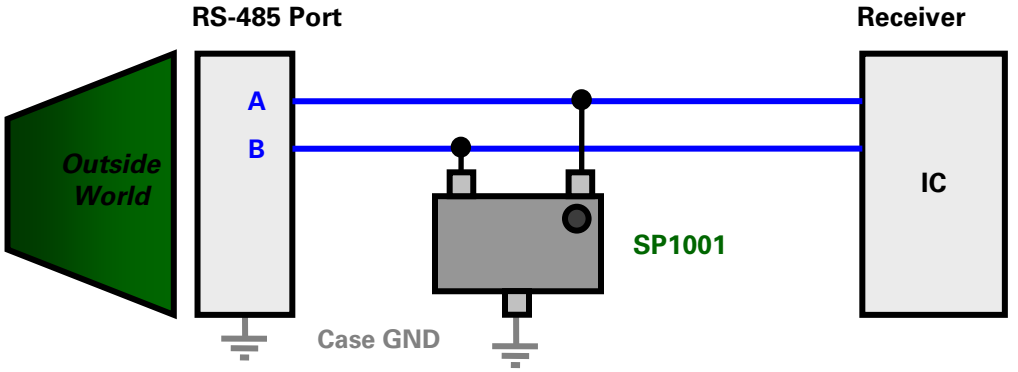
- There are numerous implementations and applications of RS-485
  - Most applications involve two wires (i.e. A and B) while a few are four wire (i.e. full duplex)
  - Depending on cable length, data rates can vary from 100kbps-10Mbps
  - Bus voltages can be unipolar (i.e. 0-6V) or bipolar (i.e. ±3V) and every application should be evaluated thoroughly before using the recommended devices below

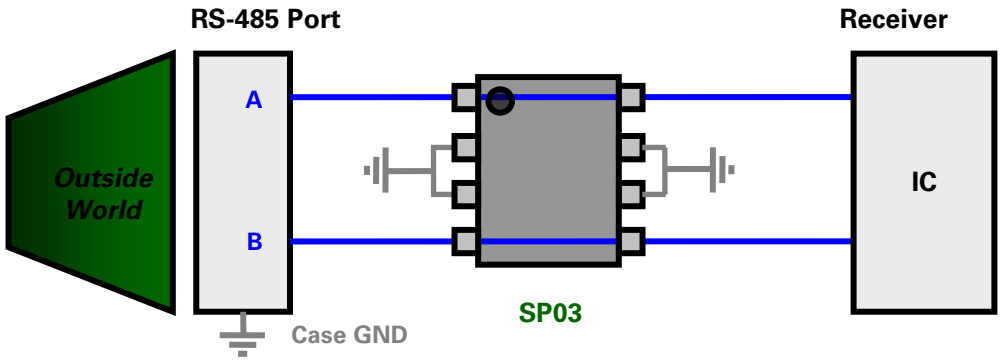
- For a unipolar bus with a voltage ≤ 6V (MAX):
  - The SP1001 Series is shown for ESD protection only
  - The SP03 Series is shown for lightning/surge protection

- For differential protection between A and B, the GND connection can be removed from the schematics below

- For a bipolar bus with a maximum voltage swing of ±3V:
  - The SP1002 or SP1004 Series can be used ESD protection only
  - The SP03 Series (x2) can still be used for lightning/surge protection with one I/O tied to GND

Application Schematic:





Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=2.5V/0V	# of Channels	V_{RWM}	Packaging
SP1001-02JTG	±15kV	2A	8pF	2	6V	SC70-3
SP03-xBTG	±30kV	150A	8pF (I/O to I/O)	2	3.3V, 6V	SOIC-8
SP03A-3.3BTG	±30kV	150A	4.5pF (I/O to I/O)	2	3.3V	SOIC-8

Application Specific Device Selection

CAN Bus

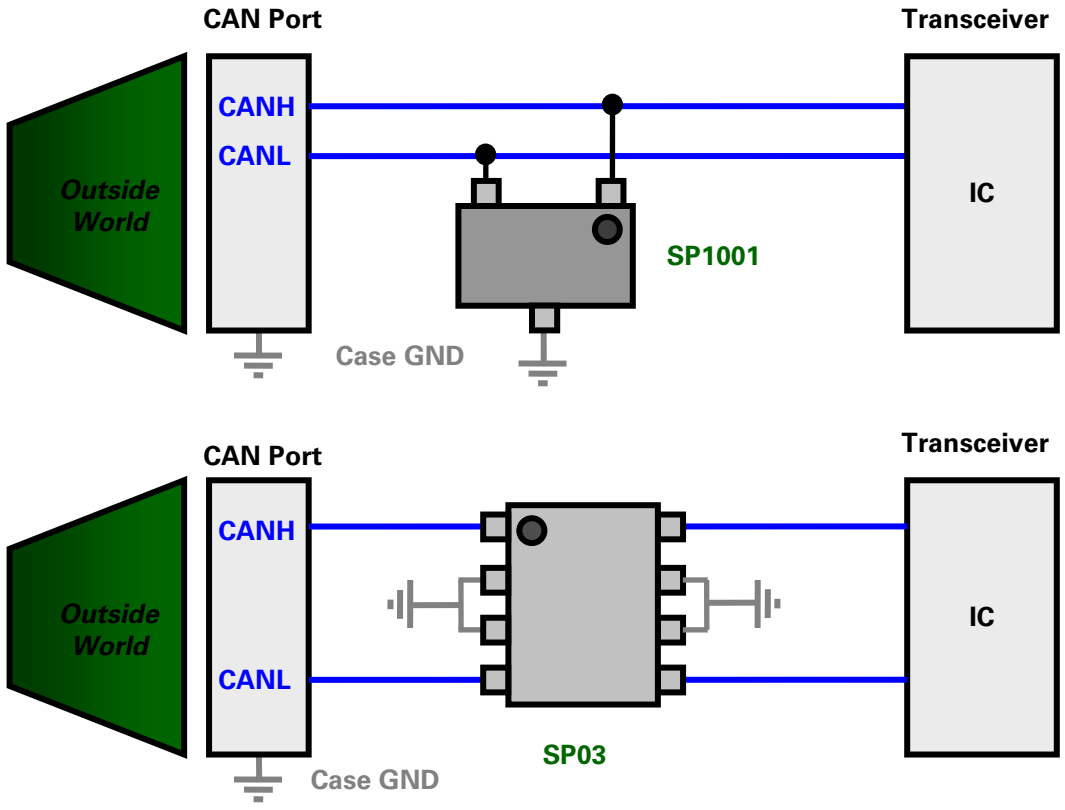
Considerations:

- There are numerous implementations and applications of a CAN bus
  - Most applications involve two wires (i.e. CANH and CANL)
  - Depending on cable length, data rates can vary from 10kbps-1Mbps
  - Most applications do not exceed 0-5V to transmit a Low/High signal, however, every application should be evaluated thoroughly before using the recommended devices below

- For the described application of unipolar bus with voltages between 0 and 5V:
  - The SP1001 Series is shown for ESD protection only
  - The SP03 Series is shown for lightning/surge protection

- For differential protection between CANH and CANL, the GND connection can be removed from the schematics below

Application Schematic:



Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Lightning (t_P=8/20µs)	I/O Capacitance @ V_R=2.5V/0V	# of Channels	V_{RWM}	Packaging
SP1001-02JTG	±15kV	2A	8pF	2	6V	SC70-3
SP03-xBTG	±30kV	150A	8pF (I/O to I/O)	2	3.3V, 6V	SOIC-8
SP03A-3.3BTG	±30kV	150A	4.5pF (I/O to I/O)	2	3.3V	SOIC-8

Application Specific Device Selection

LCD and Camera Interfaces (Mobile)

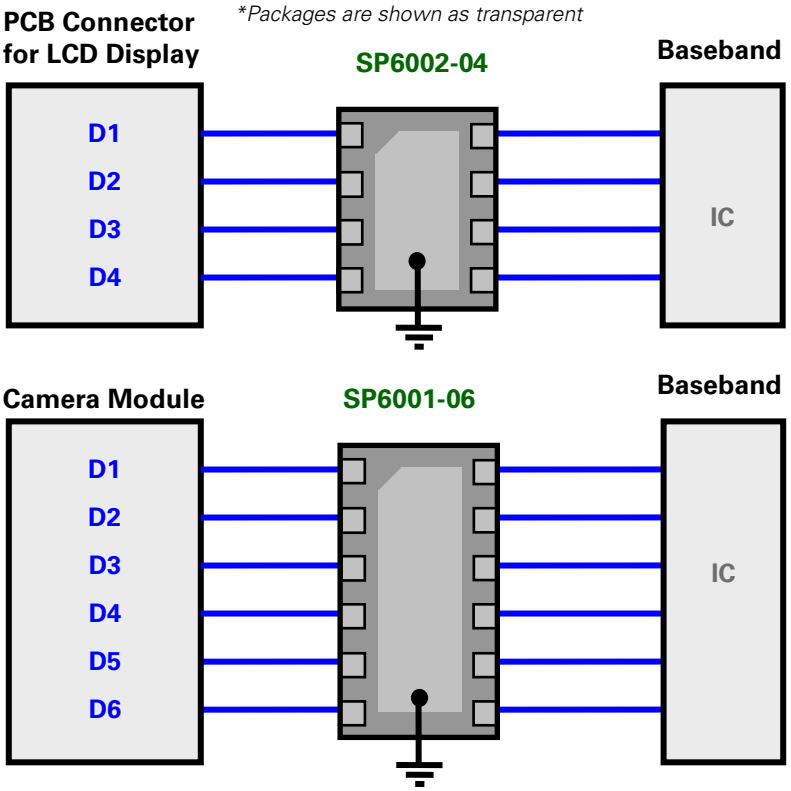
Considerations:

- LCD and camera interfaces in mobile devices are vulnerable to EMI from the cellular band
  - Frequencies between 800-3000MHz should be attenuated to prevent distortion on the display

- The pixel clocks vary depending upon the display size but the frequency will typically fall between 5-65MHz
  - This corresponds to data rates between 10-60Mbps and with these speeds line capacitances need to be considered
  - In the majority of applications line capacitances of 20-40pF will not cause signal integrity issues

- The protection schemes below for data lines Dx are only examples and will vary with the particular application

Application Schematic:

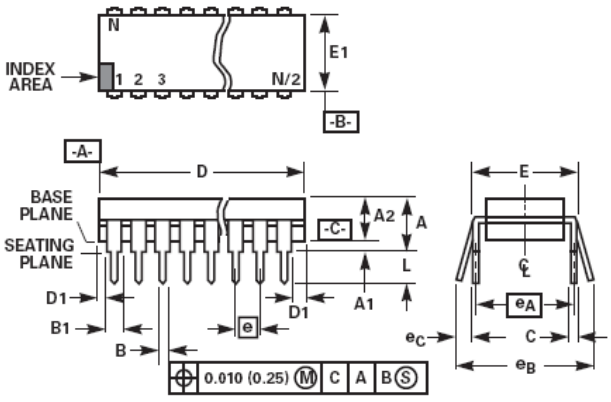


Recommended SPA Devices:

Ordering Number	ESD Level (Contact)	Cut-off Frequency	Line Capacitance @ V_R=2.5V	# of Channels	V_{RWM}	Packaging
SP6001-0xUTG-1	±30kV	115MHz	24pF	4/6/8	6V	µDFN-8/12/16
SP6002-0xUTG-1	±30kV	100MHz	30pF	4/6	6V	µDFN-8/12
SP6003-0xUTG-1 (not released yet)	±15kV	175MHz	14pF	4/6	6V	µDFN-8/12

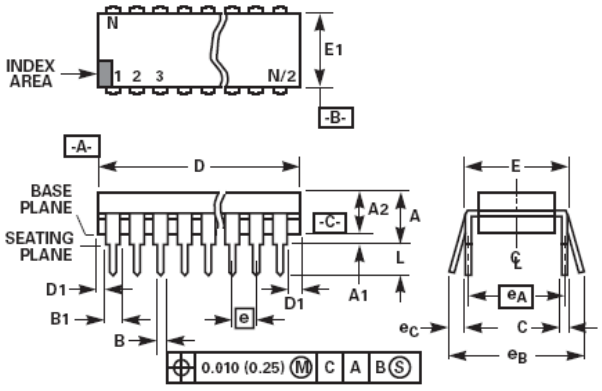
Appendix A
SPA Package Outlines

PDIP-8



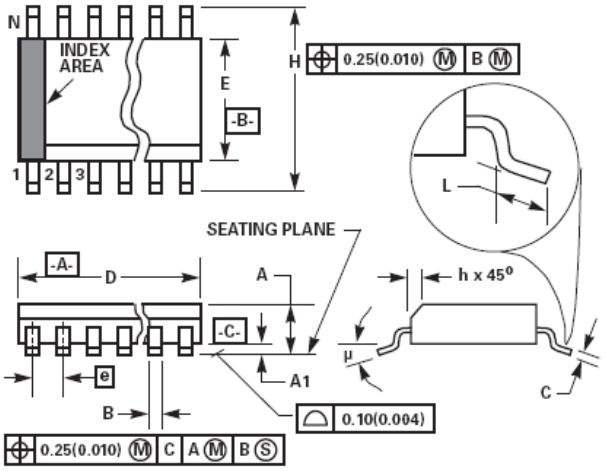
Package	PDIP				
Pins	8				
JEDEC	E8.3 (JEDEC MS-001-BA Issue D)				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	-	5.33	-	0.210	4
A1	0.39	-	0.015	-	4
A2	2.93	4.95	0.115	0.195	-
B	0.356	0.558	0.014	0.022	-
B1	1.15	1.77	0.045	0.070	8, 10
C	0.204	0.355	0.008	0.014	-
D	9.01	10.16	0.355	0.400	5
D1	0.13	-	0.005	-	5
E	7.62	8.25	0.300	0.325	6
E1	6.1	7.11	0.240	0.280	5
e	2.54 BSC		0.100 BSC		-
e_A	7.62 BSC		0.300 BSC		6
e_B	-	10.92	-	0.430	7
L	2.93	3.81	0.115	0.150	4
N	8		8		9

PDIP-16



Package	PDIP				
Pins	16 Lead Dual-in-Line				
JEDEC	E16.3 MS-001-BB Issue D				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	-	5.33	-	0.210	4
A1	0.39	-	0.015	-	4
A2	2.93	4.95	0.115	0.195	-
B	0.356	0.558	0.014	0.022	-
B1	1.15	1.77	0.045	0.070	8, 10
C	0.204	0.355	0.008	0.014	-
D	18.66	19.68	0.735	0.775	5
D1	0.13	-	0.005	-	5
E	7.62	8.25	0.300	0.325	6
E1	6.10	7.11	0.240	0.280	5
e	2.54 BSC		0.100 BSC		-
e_A	7.62 BSC		0.300 BSC		6
e_B	-	10.92	-	0.430	7
L	2.93	3.81	0.115	0.150	4
N	16		16		9

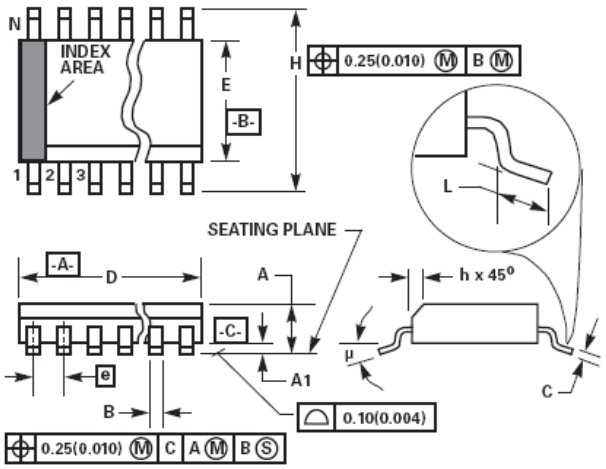
SOIC-8



Package	SOIC				
Pins	16				
JEDEC	M16.15 (JEDEC MS-012-AC Issue C)				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	9.80	10.00	0.3859	0.3937	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	16		16		7
μ	0°	8°	0°	8°	-

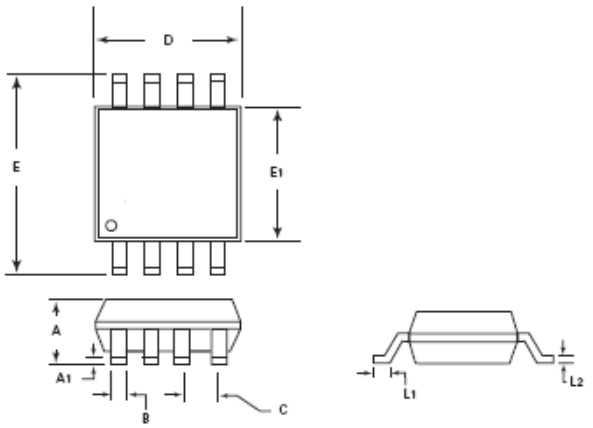
SPA Package Outlines (continued)

SOIC-16



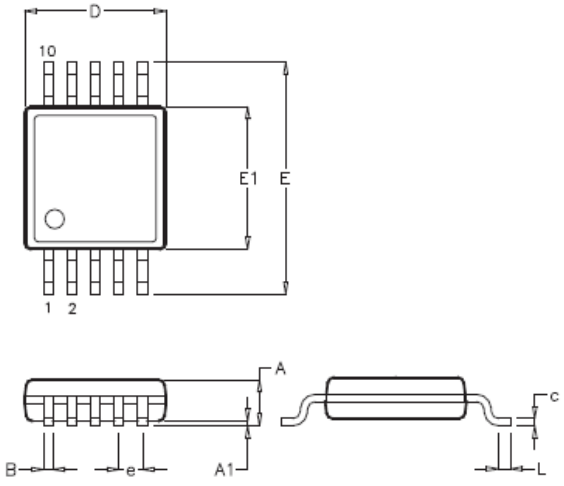
Package	SOIC				
Pins	16				
JEDEC	M16.15 (JEDEC MS-012-AC Issue C)				
	Millimeters		Inches		Notes
	Min	Max	Min	Max	
A	1.35	1.75	0.0532	0.0688	-
A1	0.10	0.25	0.0040	0.0098	-
B	0.33	0.51	0.013	0.020	9
C	0.19	0.25	0.0075	0.0098	-
D	9.80	10.00	0.3859	0.3937	3
E	3.80	4.00	0.1497	0.1574	4
e	1.27 BSC		0.050 BSC		-
H	5.80	6.20	0.2284	0.2440	-
h	0.25	0.50	0.0099	0.0196	5
L	0.40	1.27	0.016	0.050	6
N	16		16		7
μ	0°	8°	0°	8°	-

MSOP-8



Package	MSOP-8			
Pins	8			
	Millimeters		Inches	
	Min	Max	Min	Max
D	2.90	3.10	0.114	.122
E	4.78	4.98	.188	.196
E1	2.90	3.10	.114	.122
A	0.87	1.17	.034	.046
A1	0.05	0.25	.002	0.010
B	-	0.30TYP	-	0.012TYP
C	-	0.65TYP	-	0.026TYP
L1	0.52	0.54	0.020	0.021
L2	-	0.18TYP	-	.007TYP
F	-	5.28	-	.208
F1	-	4.24	-	.167
G	-	0.65	-	0.026
H	-	0.38	-	.015
I	-	1.04	-	.041

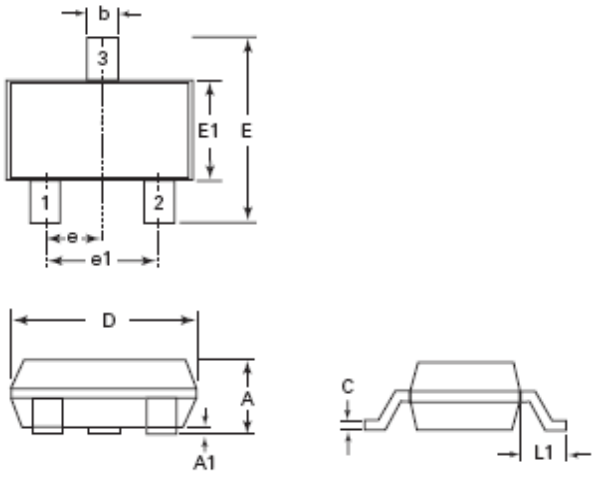
MSOP-10



Package	MSOP10			
Pins	10			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
B	0.17	0.27	0.007	0.011
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
E	4.67	5.10	0.184	0.200
E1	2.90	3.10	0.114	0.122
e	0.50 BSC		0.020 BSC	
HE	0.40	0.80	0.016	0.031

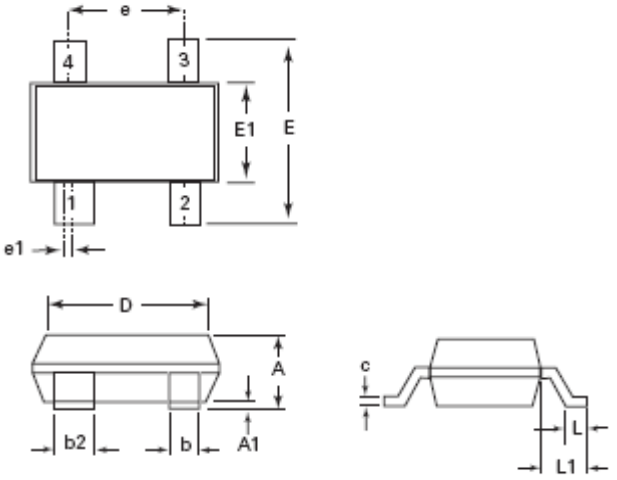
SPA Package Outlines (continued)

SOT23-3



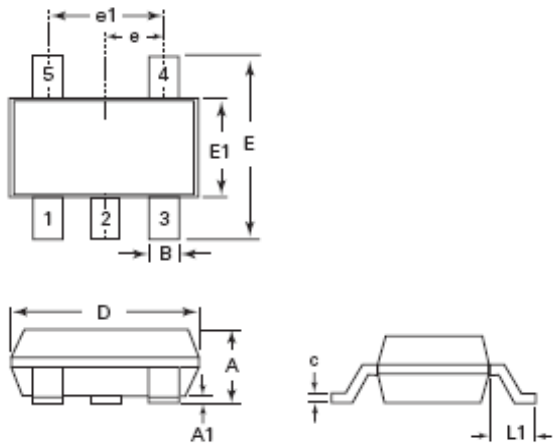
Package	SOT23-3			
Pins	3			
JEDEC	TO-236			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A1	0.01	0.1	0.0004	0.004
b	0.3	0.5	0.012	0.020
c	0.08	0.2	0.003	0.008
D	2.8	3.04	0.110	0.120
E	2.1	2.64	0.083	0.104
E1	1.2	1.4	0.047	0.055
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L1	0.54 REF		0.021 REF	
M		2.29		.090
N		0.95		0.038
O		0.78		.030TYP
P		0.78		.030TYP

SOT143



Package	SOT143-4			
Pins	4			
JEDEC	TO-253			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.08	1.22	0.003	0.048
A1	0.05	0.15	0.002	0.006
b	0.30	0.50	0.012	0.020
b2	0.76	0.89	0.030	0.035
c	0.08	0.20	0.003	0.008
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.082	0.104
E1	1.20	1.40	0.047	0.055
e	1.92 BSC		0.076 BSC	
e1	0.20 BSC		0.008 BSC	
L	0.4	0.6	0.016	0.024
L1	0.550 REF		0.022 REF	

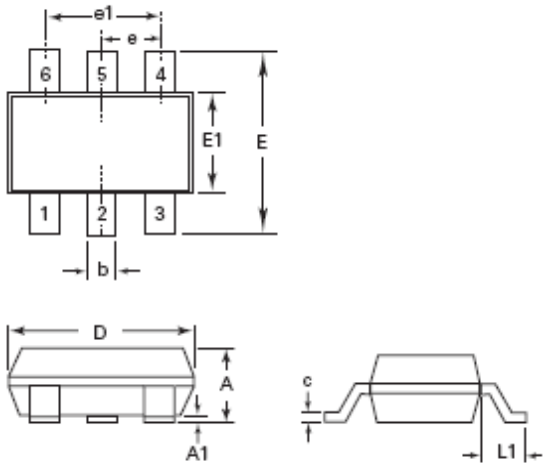
SOT23-5



Package	SOT23-5			
Pins	5			
JEDEC	MO-178			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.45	-	0.057
A1	0	0.15	0	0.006
b	0.3	0.5	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.75	3.05	0.108	0.120
E	2.6	3.0	0.102	0.118
E1	1.45	1.75	0.057	0.069
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L1	0.60 REF		0.024 REF	
M		2.59		.102
N		0.95		.038
O		0.69		.027TYP
P		0.99		.039TYP

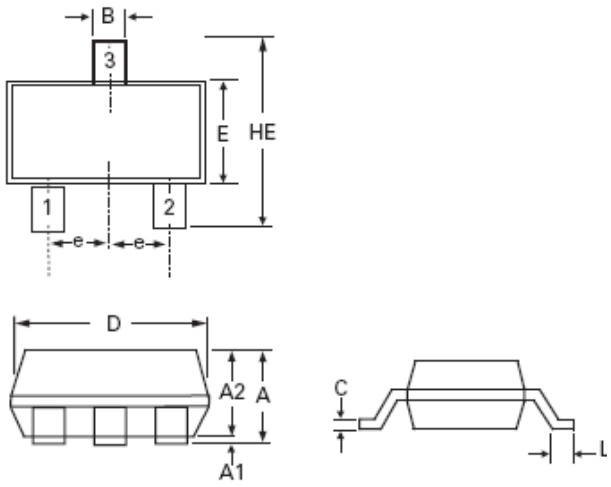
SPA Package Outlines (continued)

SOT23-6



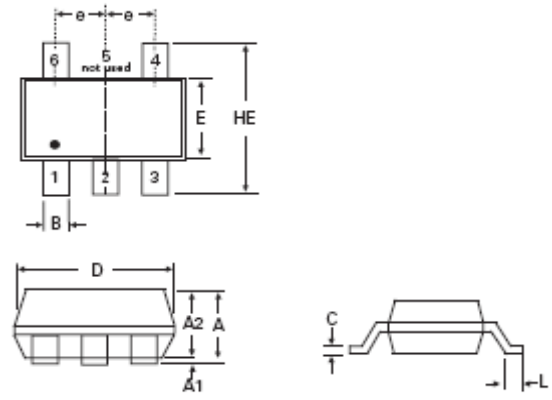
Package	SOT23-6			
Pins	6			
JEDEC	MO-178			
	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.45	-	0.057
A1	0	0.15	0	0.006
b	0.3	0.5	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.75	3.05	0.108	0.120
E	2.6	3.0	0.102	0.118
E1	1.45	1.75	0.057	0.069
e	0.95 BSC		0.038 BSC	
e1	1.90 BSC		0.075 BSC	
L1	0.60 REF		0.024 REF	
M		2.59		.102
N		0.95		0.038
O		0.69		.027TYP
P		0.99		.039TYP

SC70-3



Package	SC70-3			
Pins	3			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.66 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

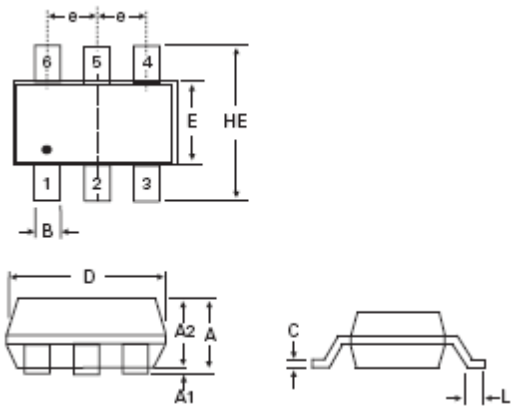
SC70-5



Package	SC70-5			
Pins	5			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

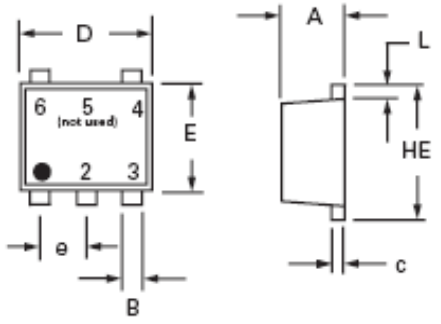
SPA Package Outlines (continued)

SC70-6



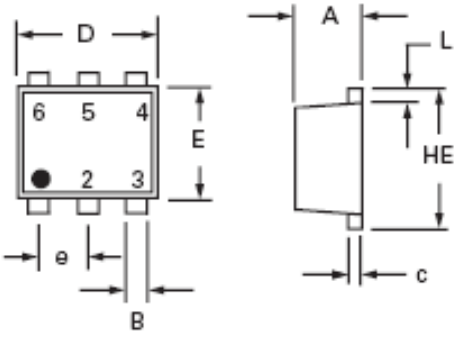
Package	SC70-6			
Pins	6			
JEDEC	MO-203 Issue A			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.70	1.00	0.028	0.039
B	0.15	0.30	0.006	0.012
c	0.08	0.25	0.003	0.010
D	1.85	2.25	0.073	0.089
E	1.15	1.35	0.045	0.053
e	0.65 BSC		0.026 BSC	
HE	2.00	2.40	0.079	0.094
L	0.26	0.46	0.010	0.018

SOT553



Package	SOT 553			
Pins	5			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

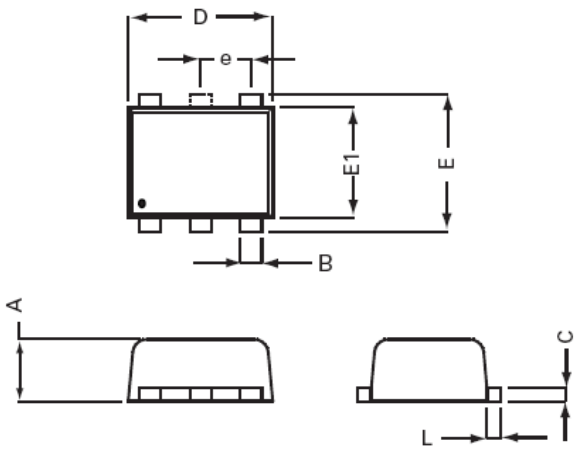
SOT563



Package	SOT 563			
Pins	6			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.50	0.60	0.020	0.024
B	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.059	0.067
E	1.10	1.30	0.043	0.051
e	0.50 BSC		0.020 BSC	
L	0.10	0.30	0.004	0.012
HE	1.50	1.70	0.059	0.067

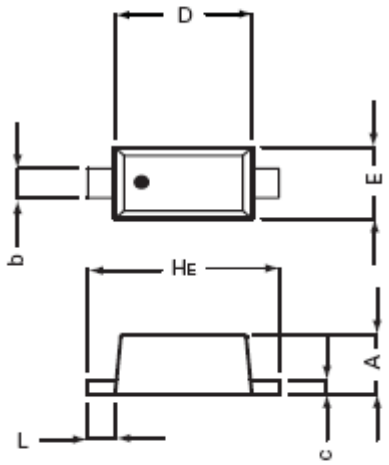
SPA Package Outlines (continued)

SOT953



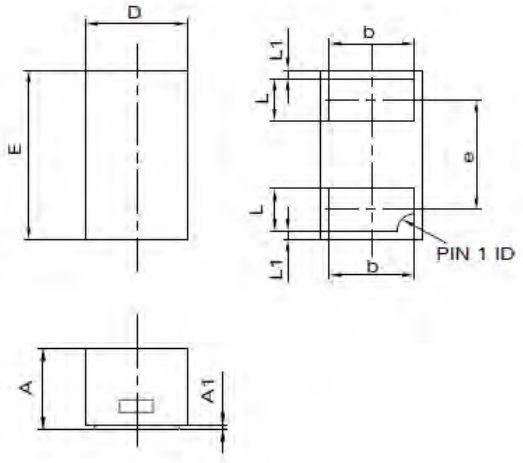
Symbol	SOT953			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.44	0.5	0.170	0.020
B	0.10	0.20	0.004	0.008
c	0.05	0.15	0.002	0.006
D	0.95	1.05	0.037	0.041
E	0.95	1.05	0.037	0.041
E1	0.75	0.85	0.029	0.033
e	0.35 BSC		0.014 BSC	
L	0.05	0.15	0.002	0.006

SOD723



Symbol	SOD723			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.46	0.51	0.018	0.020
b	0.23	0.28	0.009	0.011
c	0.08	0.13	0.003	0.005
D	0.99	1.04	0.039	0.041
E	0.58	0.64	0.023	0.025
HE	1.37	1.47	0.054	0.058
L	0.15	0.25	0.006	0.010

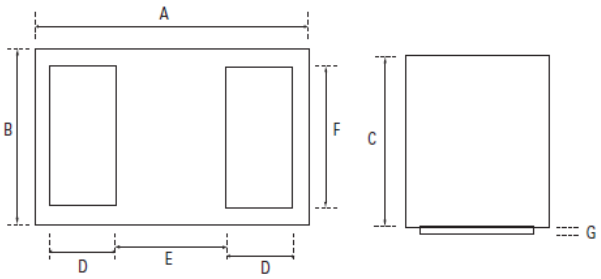
SOD882



Symbol	SOD882			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.40	0.50	0.016	0.02
A1	0.00	0.05	0.000	0.002
D	0.55	0.65	0.022	0.026
E	0.95	1.05	0.037	0.041
b	0.40	0.60	0.016	0.024
e	0.65 TYP		0.026 TYP	
L	0.15	0.35	0.006	0.014
L1	0.05 REF		0.002 REF	

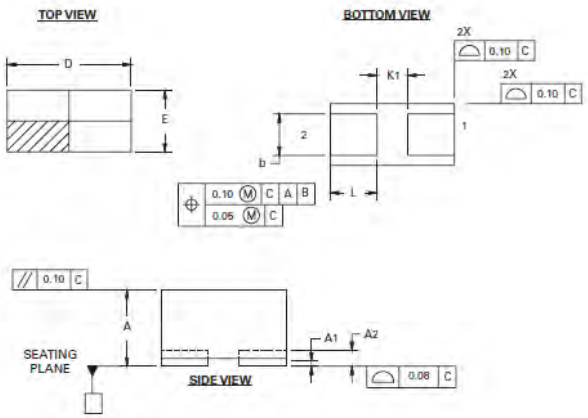
SPA Package Outlines (continued)

0201
Flip chip
(0.62x0.32)



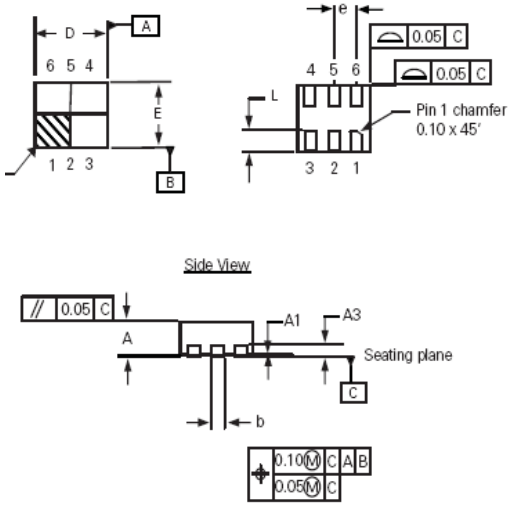
Symbol	0201 Flipchip					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.595	0.620	0.645	0.0234	0.0244	0.0254
B	0.295	0.320	0.345	0.0116	0.0126	0.0136
C	0.245	0.275	0.305	0.0096	0.0108	0.0120
D	0.145	0.150	0.155	0.0057	0.0059	0.0061
E	0.245	0.250	0.255	0.0096	0.0098	0.0100
F	0.245	0.250	0.255	0.0096	0.0098	0.0100
G	0.005	0.010	0.015	0.0002	0.0004	0.0006

0201
µDFN-2
(0.60x0.30)



Symbol	uDFN-2			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.34	0.40	0.014	0.016
A1	0.00	0.05	0.000	0.002
A2	0.075 REF		0.003 REF	
b	0.20 REF		0.008 REF	
D	0.55	0.65	0.022	0.026
E	0.25	0.35	0.010	0.014
L	0.175	0.275	0.007	0.011
K1	0.15 REF		0.006 REF	

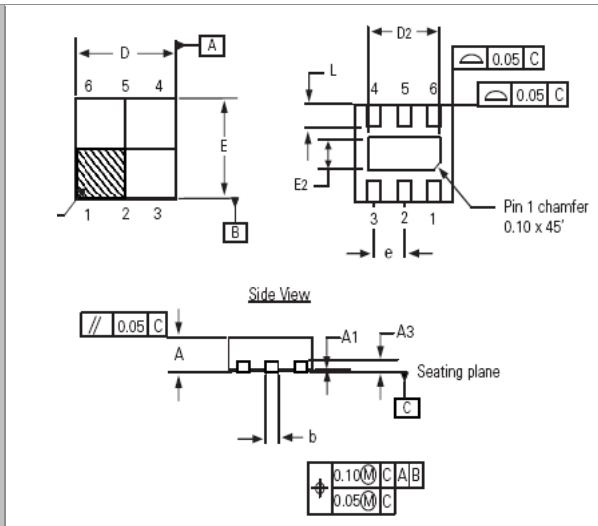
µDFN-6
(1.25x1.0)



uDFN-6 (1.25x1.0x0.5mm)				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.15	0.25	0.006	0.010
D	1.20	1.30	0.047	0.051
D2	-	-	-	-
E	0.95	1.05	0.037	0.041
E2	-	-	-	-
e	0.4 REF		0.016 REF	
L	0.25	0.35	0.010	0.014

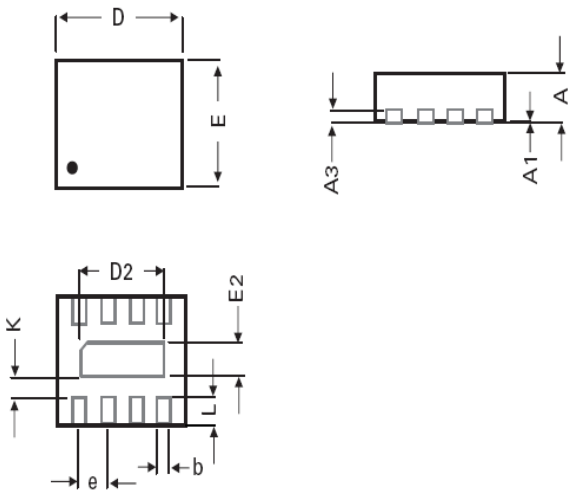
SPA Package Outlines (continued)

µDFN-6 (1.6x1.6)



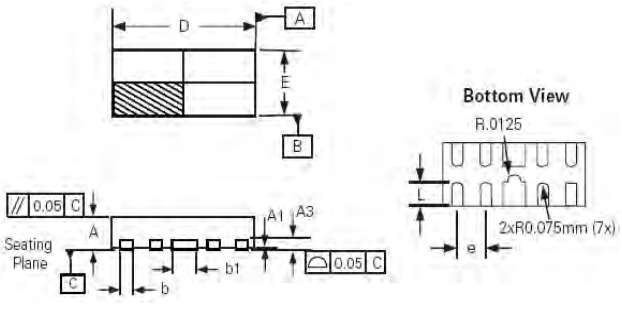
Symbol	uDFN (1.6x1.6x0.5mm)			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.45	0.55	0.018	0.022
A1	0.00	0.05	0.000	0.002
A3	0.127 Ref		0.005 Ref	
b	0.20	0.30	0.008	0.012
D	1.50	1.70	0.060	0.067
D2	1.05	1.30	0.042	0.052
E	1.50	1.70	0.060	0.067
E2	0.40	0.65	0.016	0.026
e	0.50 Ref		0.020 Ref	
L	0.100	0.600	0.004	0.023

µDFN-8 (1.7x1.35)



Symbol	UDFN-08			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.150	0.250	0.006	0.010
D	1.600	1.800	0.063	0.071
D2	1.100	1.300	0.043	0.051
E	1.250	1.450	0.049	0.057
E2	0.300	0.500	0.012	0.020
e	0.400 BSC		0.016 BSC	
K	0.200		0.008	0.000
L	0.150	0.350	0.006	0.014

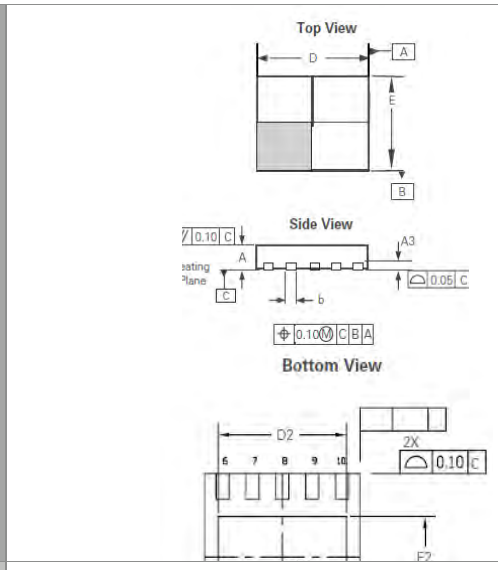
µDFN-10 (2.5x1.0)



Symbol	uDFN-10 (2.5x1.0x0.5mm)					
	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.48	0.515	0.55	0.019	0.020	0.021
A1	0.00	--	0.05	0.000		0.022
A3	0.125 Ref			0.005 Ref		
b	0.15	0.20	0.25	0.006	0.008	0.012
b1	0.35	0.40	0.45	0.014	0.016	0.018
D	2.40	2.50	2.60	0.094	0.098	0.102
E	0.90	1.00	1.10	0.035	0.039	0.043
e	0.50 BSC			0.020 BSC		
L	0.30	0.365	0.43	0.012	0.014	0.016

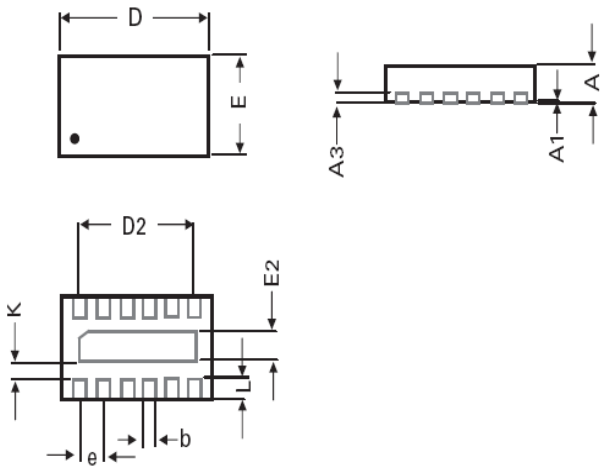
SPA Package Outlines (continued)

µDFN-10 (2.6x2.6)



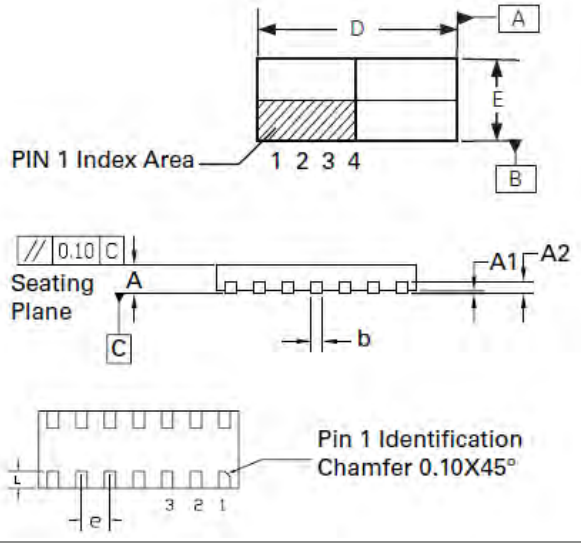
uDFN-10 (2.6x2.6mm)						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A3		0.130 Ref			0.005 Ref	
b	0.17	0.22	0.27	0.006	0.008	0.010
D	2.50	2.60	2.70	0.097	0.101	0.105
D2	2.10	2.15	2.20	0.081	0.083	0.085
E	2.50	2.60	2.70	0.097	0.101	0.105
E2	1.21	1.26	1.31	0.046	0.049	0.051
e		0.50 BSC			0.020 BSC	
L	0.35	0.40	0.45	0.014	0.016	0.018

µDFN-12 (2.5x1.35)



Symbol	UDFN-12			
	Millimeters		Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A3	0.127 REF		0.005 REF	
b	0.150	0.250	0.006	0.010
D	2.400	2.600	0.094	0.102
D2	1.900	2.100	0.075	0.083
E	1.250	1.450	0.049	0.057
E2	0.300	0.500	0.012	0.020
e	0.400 BSC		0.016 BSC	
K	0.200		0.008	0.000
L	0.150	0.350	0.006	0.014

µDFN-14 (3.5x1.35)



uDFN-14 (3.5x1.35x0.5mm)						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2		0.203 Ref			0.008 Ref	
b	0.15	0.20	0.25	0.006	0.008	0.012
D	3.40	3.50	3.60	0.134	0.138	0.142
D2	-	-	-	-	-	-
E	1.25	1.35	1.45	0.050	0.054	0.058
E1	-	-	-	-	-	-
e		0.500 BSC			0.020 BSC	
L	0.25	0.30	0.35	0.010	0.012	0.014

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Semiconductor Business Unit

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