1024 x 4-BIT STATIC RAM

GENERAL DESCRIPTION

The PCD5114 is a low-power, high-speed 4096-bit static CMOS RAM, organized as 1024 words of 4 bits each. The IC is suitable for low power and high speed applications, for battery operation and where battery backup is required. Inputs R/$\overline{W}$ and $\overline{CE}$ control the read/write operation and standby mode respectively. The PCD5114 is pin compatible with the SBB2114 types.

Features

- Operating supply voltage — 2,5 V to 5,5 V
- Low data retention voltage — min. 1,0 V
- Low standby current — max. 5 μA
- Cycle time = access time — max. 200 ns
- Static operation requiring no clock or timing strobe
- Low power consumption
- 3-state common data input/output interface
- All inputs and outputs directly TTL compatible
- Pin compatible with SBB2114 variants
- 18-lead DIL package
- 20-lead SO package

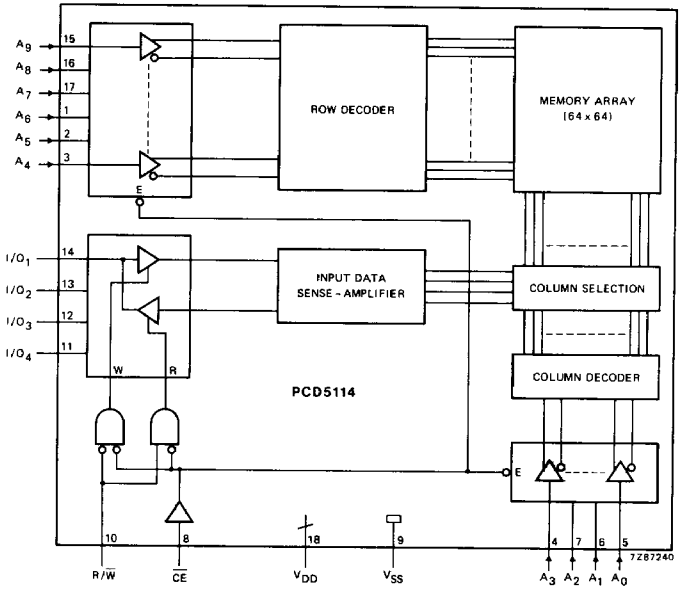

Fig. 1 Block diagram.

PACKAGE OUTLINES

PCD5114P: 18-lead DIL; plastic (SOT102G).
PCD5114T: 20-lead mini-pack; plastic (SO20; SOT163A).

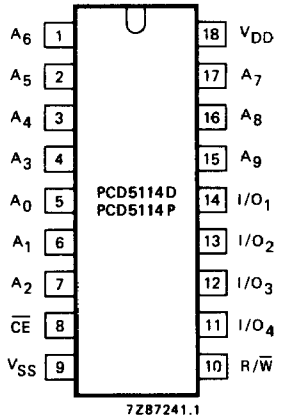

Fig. 2 Pinning diagram: PCD5114D; PCD5114P.

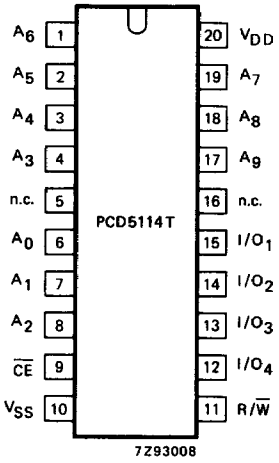

Fig. 3 Pinning diagram: PCD5114T.

A_0 to A_3	column address inputs
A_4 to A_9	row address inputs
$\overline{CE}$	chip enable input
$R/\overline{W}$	read/write input
I/O_1 to I/O_4	data input/output
V_{SS}	negative supply (ground)
V_{DD}	positive supply (+ 5 V)

Table 1 Mode selection

$\overline{CE}$	$R/\overline{W}$	mode	output	power
H	H	not selected	high impedance	standby
H	L	not selected	high impedance	standby
L	H	read	active	active
L	L	write	high impedance	active

H = HIGH logic level (the most positive voltage)
L = LOW logic level (the most negative voltage)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,3 to + 8 V
Input voltage range (any pin)	V_I	V_{SS}−0,3 to V_{DD} + 0,3 V
Storage temperature range	T_{stg}	−55 to + 125 °C
Operating ambient temperature range	T_{amb}	−25 to + 70 °C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS Devices").

DEVELOPMENT DATA

D.C. CHARACTERISTICS

V_{DD} = 5 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 1 MHz; outputs open	I_{DD}	–	10	17	mA
at V_I = 0,8 V/2,0 V; f = 5 MHz; outputs open	I_{DD}	–	12	20	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 2 mA	V_{OH}	2,4	–	–	V
Output voltage LOW					
at I_{OL} = 4 mA	V_{OL}	–	–	0,4	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

D.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply current					
at $V_I = V_{DD}/V_{SS}$; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
at V_I = 0,4 V/1,6 V; f = 1 MHz; outputs open	I_{DD}	–	5	8	mA
Standby current					
at $\overline{CE} = V_{DD}$	I_{SB}	–	0,02	5	μA
Input voltage HIGH	V_{IH}	1,6	–	V_{DD} + 0,3	V
Input voltage LOW	V_{IL}	−0,3	–	+0,4	V
Input leakage current					
at $V_I = V_{SS}$ to V_{DD}	$\pm I_{IL}$	–	–	0,1	μA
Output voltage HIGH					
at $-I_{OH}$ = 1 mA	V_{OH}	1,7	–	–	V
Output voltage LOW					
at I_{OL} = 1 mA	V_{OL}	–	–	0,3	V
Output leakage current					
at $V_O = V_{SS}$ to V_{DD}; $\overline{CE}$ = HIGH	$\pm I_{OL}$	–	–	0,5	μA

A.C. CHARACTERISTICS

V_{DD} = 5 V ±0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C; measured in Fig. 4, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	200	–	–	ns
Address access time	t_{AA}	–	–	200	ns
Chip select access time	t_{AC}	–	–	200	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	80	ns
Write cycle					
Write cycle time	t_{WC}	200	–	–	ns
Chip selection to end of write	t_{CW}	120	–	–	ns
Address set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	140	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	80	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	60	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 4)

Input pulse levels	0,8 V to 2,0 V
Input rise and fall times	5 ns
Input timing reference levels	1,5 V
Output timing levels	1,5 V
Output timing levels for high/low impedance	1,2 V and 2,8 V
Output load	2 TTL gates and C_L = 100 pF

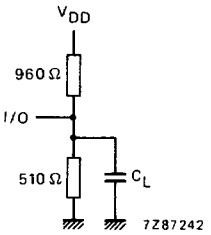

Fig. 4 Load for a.c. test conditions (V_{DD} = 5 V ± 0,5 V).

DEVELOPMENT DATA

A.C. CHARACTERISTICS

V_{DD} = 3 V ± 0,5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70°C; measured in Fig. 5, C_L = 100 pF; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Read cycle					
Read cycle time	t_{RC}	500	–	–	ns
Address access time	t_{AA}	–	–	500	ns
Chip select access time	t_{AC}	–	–	500	ns
Output hold from address change	t_{OHA}	20	–	–	ns
Output hold from chip select	t_{OHC}	20	–	–	ns
Output to low impedance from chip selection at C_L = 5 pF	t_{CLZ}	20	–	–	ns
Output to high impedance from chip deselection at C_L = 5 pF	t_{CHZ}	–	–	200	ns
Write cycle					
Write cycle time	t_{WC}	500	–	–	ns
Chip selection to end of write	t_{CW}	300	–	–	ns
Adress set-up time	t_{AS}	0	–	–	ns
Write pulse duration	t_{WP}	350	–	–	ns
Write recovery time	t_{WR}	0	–	–	ns
Data set-up time	t_{DS}	200	–	–	ns
Data hold time	t_{DH}	0	–	–	ns
Output to high impedance from write enabled at C_L = 5 pF	t_{WZ}	–	–	150	ns
Output active from end of write at C_L = 5 pF	t_{RZ}	20	–	–	ns

A.C. TEST CONDITIONS (see Fig. 5)

Input pulse levels	0,4 V to 1,6 V
Input rise and fall times	5 ns
Input timing reference levels	1,0 V
Output timing levels	1,0 V
Output timing levels for high/low impedance	0,7 V and 1,7 V
Output load	2 TTL gates and C_L = 100 pF

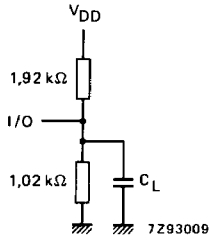

Fig. 5 Load for a.c. test conditions (V_{DD} = 3 V ± 0,5 V).

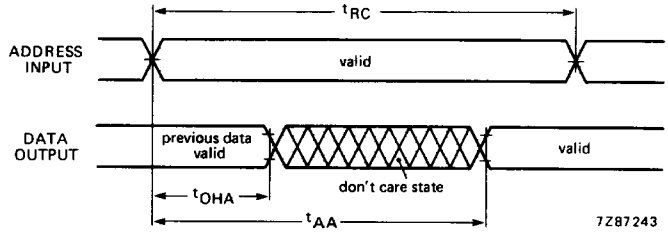

Fig. 6 Read cycle timing (1): R/$\overline{W}$ is HIGH; $\overline{CE}$ is LOW for a read cycle.

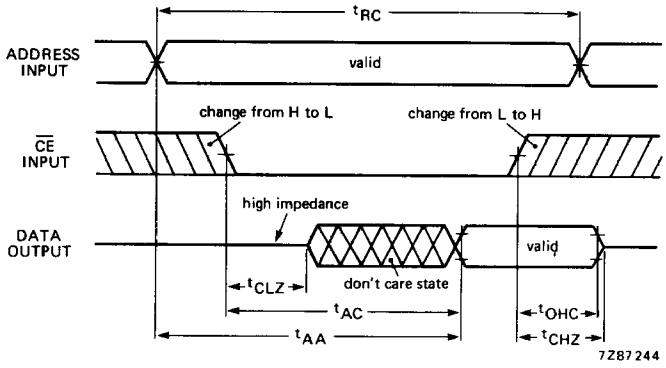

Fig. 7 Read cycle timing (2): R/$\overline{W}$ is HIGH for a read cycle.

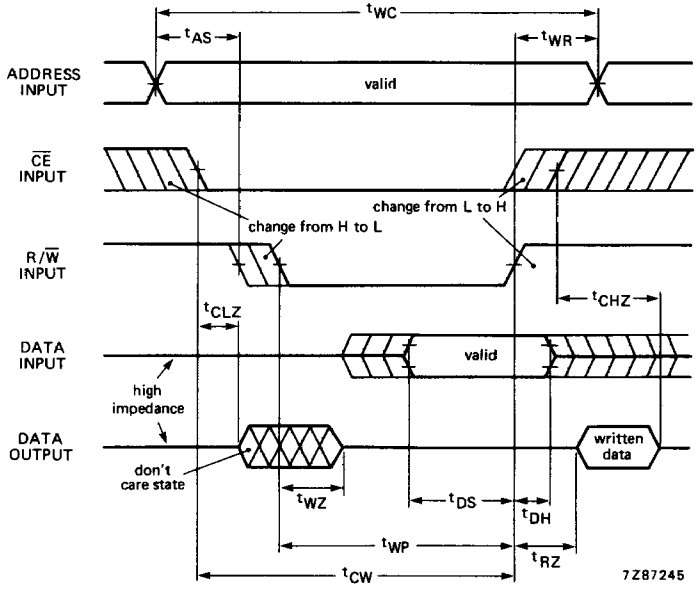

Fig. 8 Write cycle (1): R/$\overline{W}$ controlled.

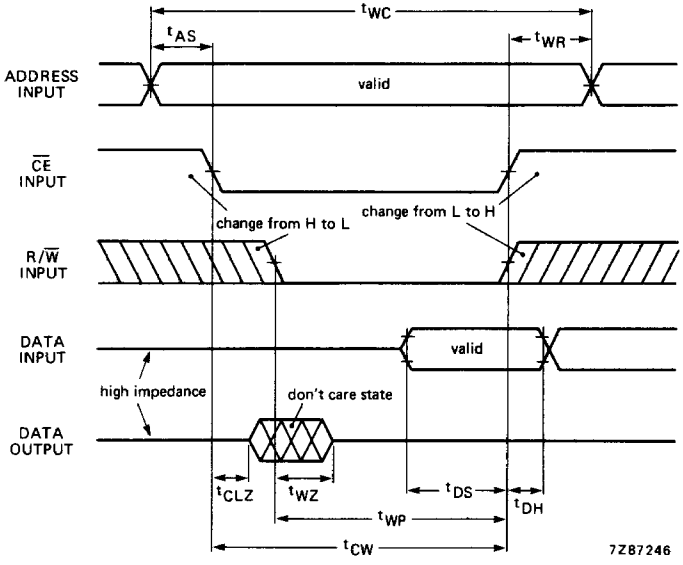

Fig. 9 Write cycle (2): $\overline{CE}$ controlled.

Note : If the $\overline{CE}$ low transition occurs after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.

CAPACITANCE

$f = 1$ MHz; $T_{amb} = 25\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
Input capacitance at $V_I = V_{SS}$	C_I	–	–	5	pF
Output capacitance at $V_O = V_{SS}$	C_O	–	–	5	pF

LOW V_{DD} DATA RETENTION CHARACTERISTICS

$T_{amb} = -25$ to $+70\ ^{o}C$

parameter	symbol	min.	typ.	max.	unit
V_{DD} for data retention at $\overline{CE} = V_{DDR} \pm 0{,}2$ V; $V_I = V_{DDR}$ to V_{SS}	V_{DDR}	1	–	5,5	V
Data retention current at $V_{DDR} = 1{,}5$ V	I_{DDR}	–	0,02	2	μA
Chip deselect to data retention time	t_{CR}	0	–	–	ns
Operation recovery time	t_R	0	–	–	ns

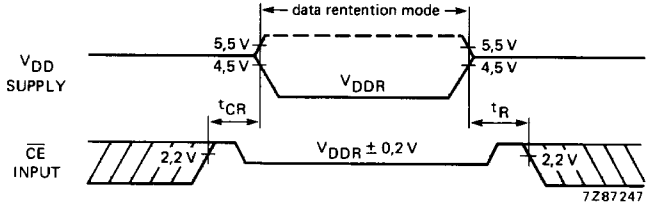

Fig. 10 LOW V_{DD} data retention.