D8575N

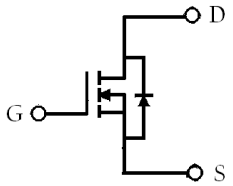
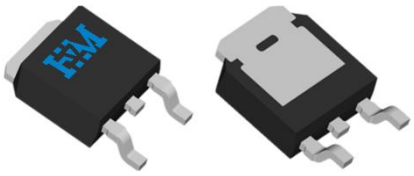
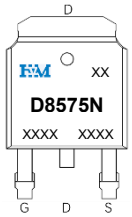
BV_{DSS}	**30**		V
I_D@V_{GS}=10V, T_C=25°C	**60**		A
R_{DSON}, T_C=25°C	Typ	Max	
@V_{GS}=10V, I_D=15A	**6.7**	**8.0**	mΩ
@V_{GS}=4.5V, I_D=10A	**9.5**	**12**	

100% ΔV_{ds} TESTED!

100% UIS TESTED!

Features

- Super Low Gate Charge
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced Trench technology

Equivalent Circuit	TO-252	Marking & Pin Assignment
		

Package Marking and Ordering Information

Device Name	Marking	Device Package	Quantity
HMD8575N	D8575N	TO-252	2500/Reel

Table 1. Absolute Maximum Ratings (TA=25℃)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS}=0V)	30	V
V_{GS}	Gate-Source Voltage (V_{DS}=0V)	±20	V
$I_{D\ (DC)}$	Drain Current-Continuous (Tc =25℃) [1]	60	A
	Drain Current-Continuous (Tc =100℃) [1]	38	A
$I_{DM\ (pulse)}$	Drain Current-Continuous@ Current-Pulsed [2]	240	A
P_D	Maximum Power Dissipation (Tc=25℃) [4]	58	W
E_{AS}	Single Pulse Avalanche Energy [3]	72	mJ
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	℃

Table 2. Thermal Characteristic

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Thermal Resistance Junction-Case [1]	2.6	℃/W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V I_D=250μA	30			V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=30V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V, V_{DS}=0V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	1.5	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance [2]	V_{GS}=10V, I_D=15A		6.7	8.0	mΩ
		V_{GS}=4.5V, I_D=10A		9.5	12	mΩ
Dynamic Characteristics						
R_G	Gate Resistance	V_{DS}=0V, V_{GS}=0V f=1.0MHz		1.4		Ω
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V f=1.0MHz		1148		PF
C_{oss}	Output Capacitance			120		PF
C_{rss}	Reverse Transfer Capacitance			104		PF
Switching Times						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=15V, V_{GS}=10V, I_D=10A, R_G=2.0Ω		5.0		nS
t_r	Turn-on Rise Time			9.5		nS
$t_{d(off)}$	Turn-Off Delay Time			28.0		nS
t_f	Turn-Off Fall Time			8.0		nS
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=10A		24.4		nC
Q_{gs}	Gate-Source Charge			2.9		nC
Q_{gd}	Gate-Drain Charge			5.0		nC
Source-Drain Diode Characteristics						
I_{SD}	Source-Drain Current (Body Diode)[1.5]				60	A
V_{SD}	Forward On Voltage [2]	I_{SD}=20A, V_{GS}=0V, T_J=25℃			1.2	V
t_{rr}	Reverse Recovery Time	T_J=25℃ I_F=10A, di/dt=100A/μs		10		nS
Q_{rr}	Reverse Recovery Charge			2.6		nC
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS +LD)				

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width≦300us , duty cycle≦2%.

3. The test condition is V_{DD} =20V, V_{GS} =10V, L=0.5mH, I_{AS}=17A.

4.The power dissipation is limited by 175℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

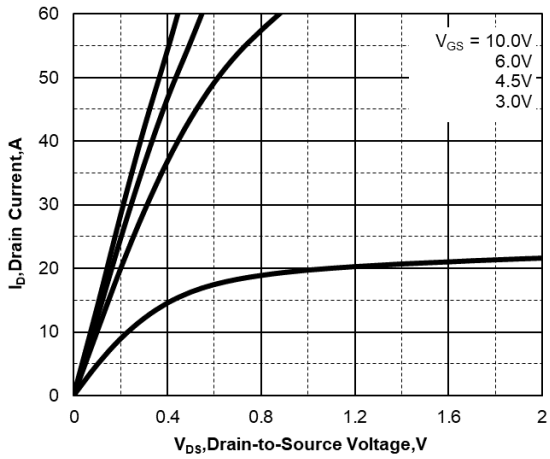


Fig1: Typical Output Characteristics

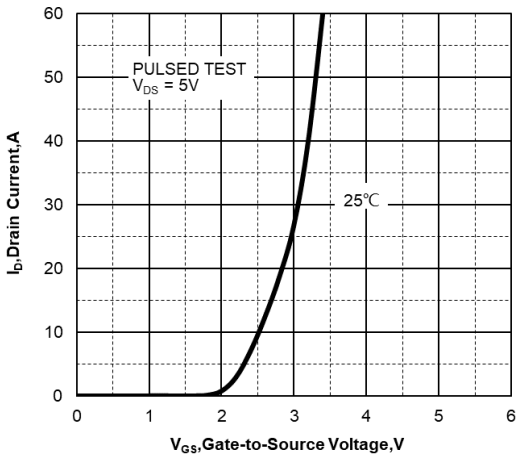


Fig 2: Typical Transfer Characteristics

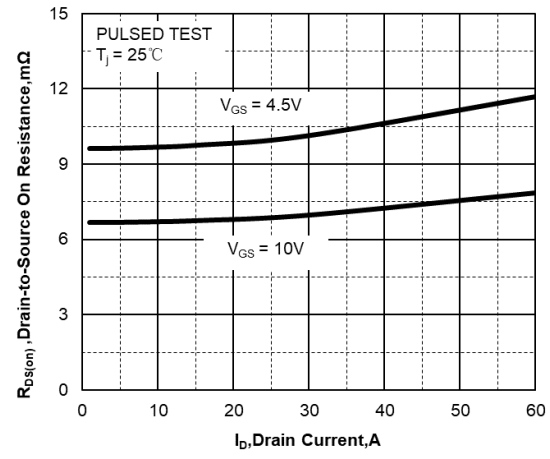


Fig 3: On-Resistance VS. Drain Current

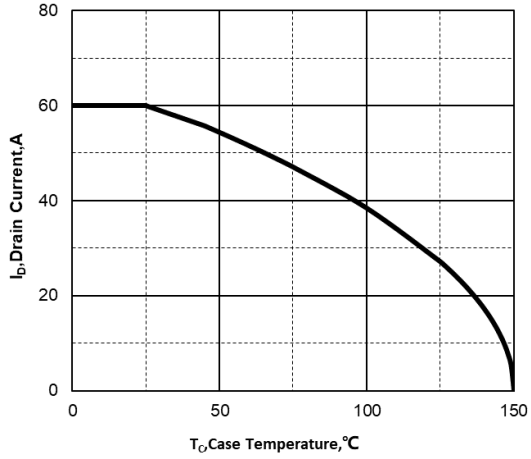


Fig 4: Maximum Continuous Drain Current VS. Case Temperature

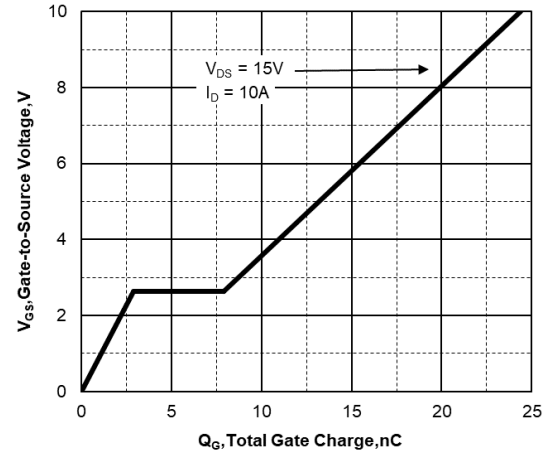


Fig 5: Gate Charge Characteristics

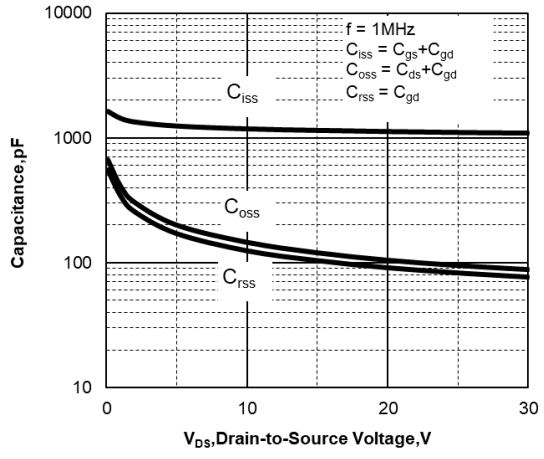


Fig 6: Capacitance Characteristics

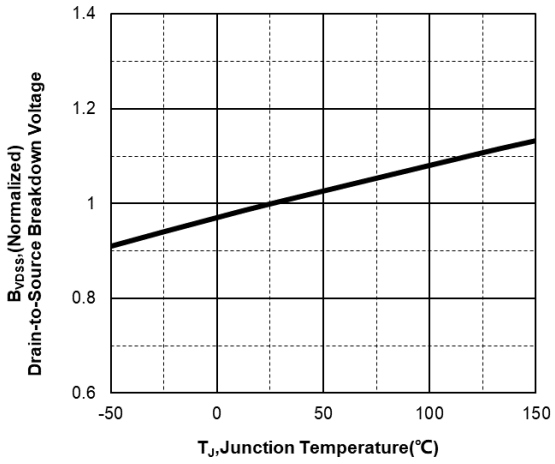


Fig 7: Normalized Breakdown Voltage VS. Junction Temperature

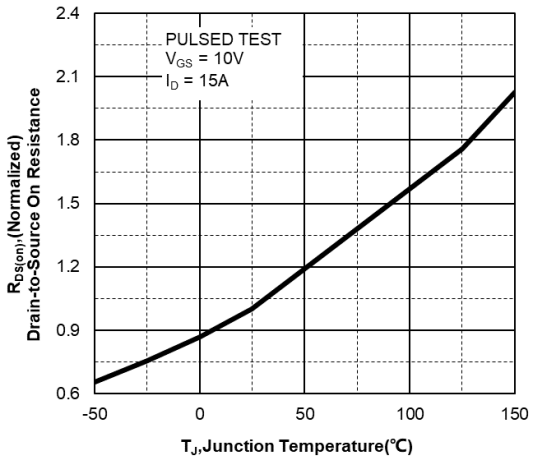


Fig 8: Normalized on Resistance VS. Junction Temperature

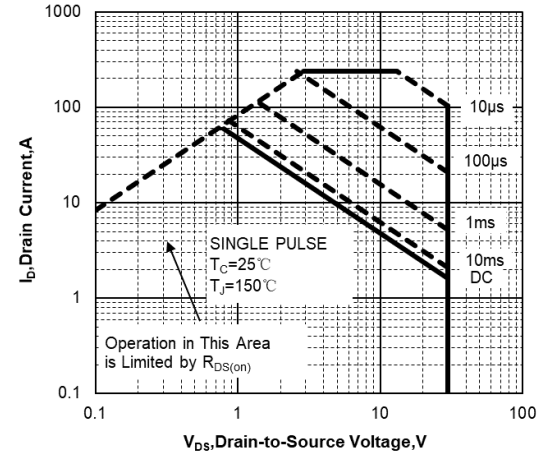


Fig 9: Maximum Safe Operating Area

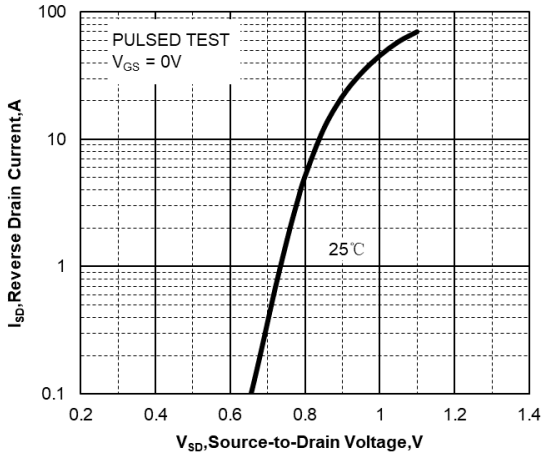


Fig 10: Body Diode Forward Characteristics

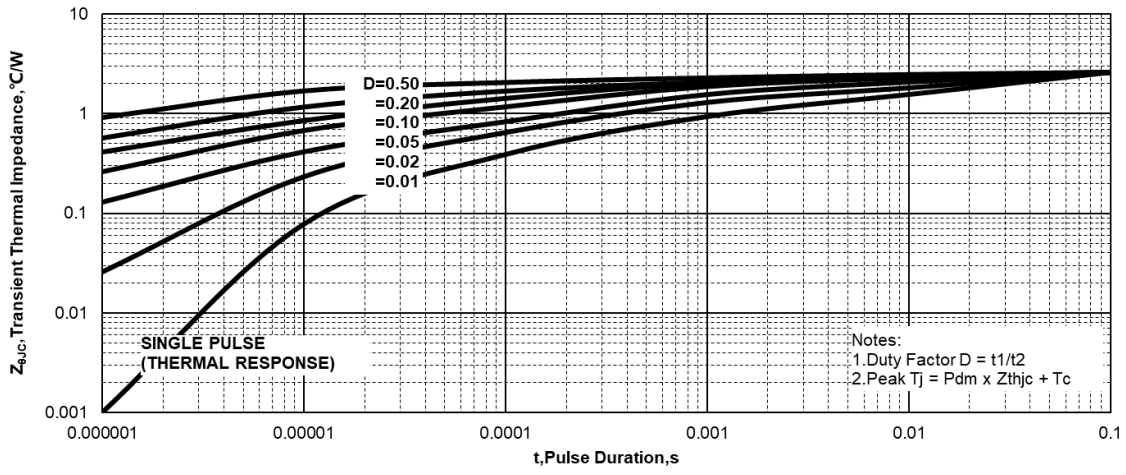


Fig.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

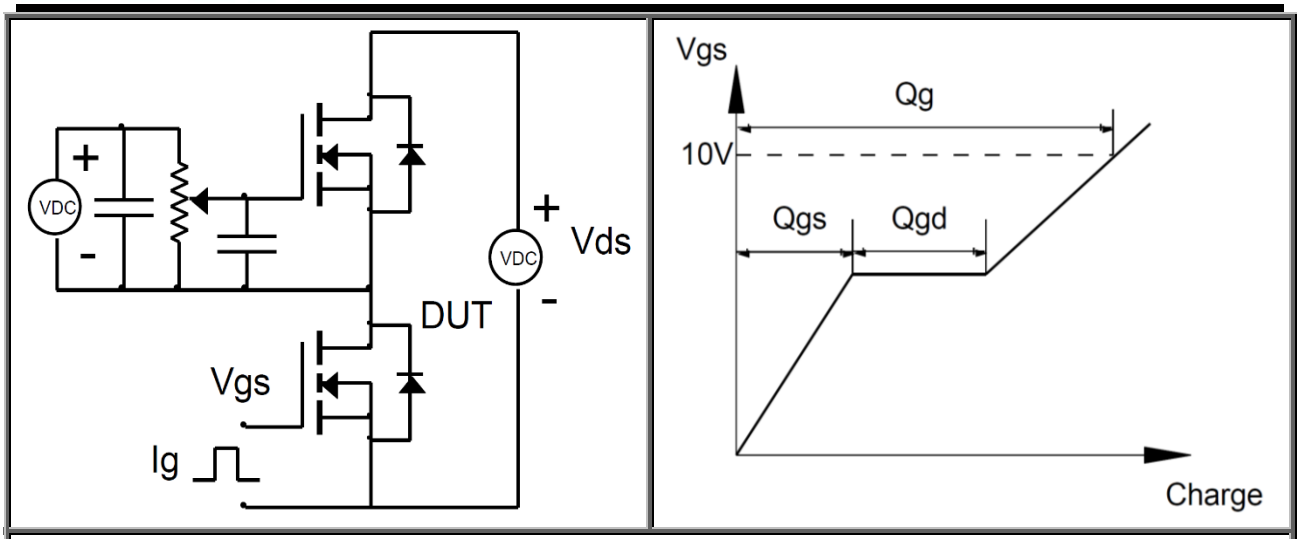


Fig 12: Gate Charge Test Circuit and Waveforms

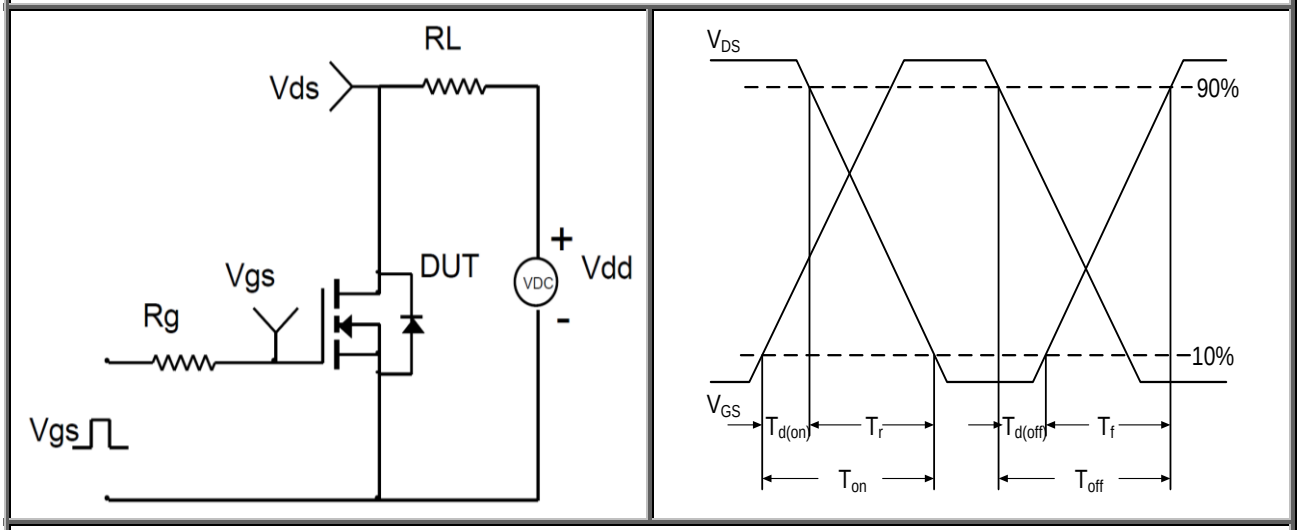


Fig 13: Resistive Switching Test Circuit and Waveforms

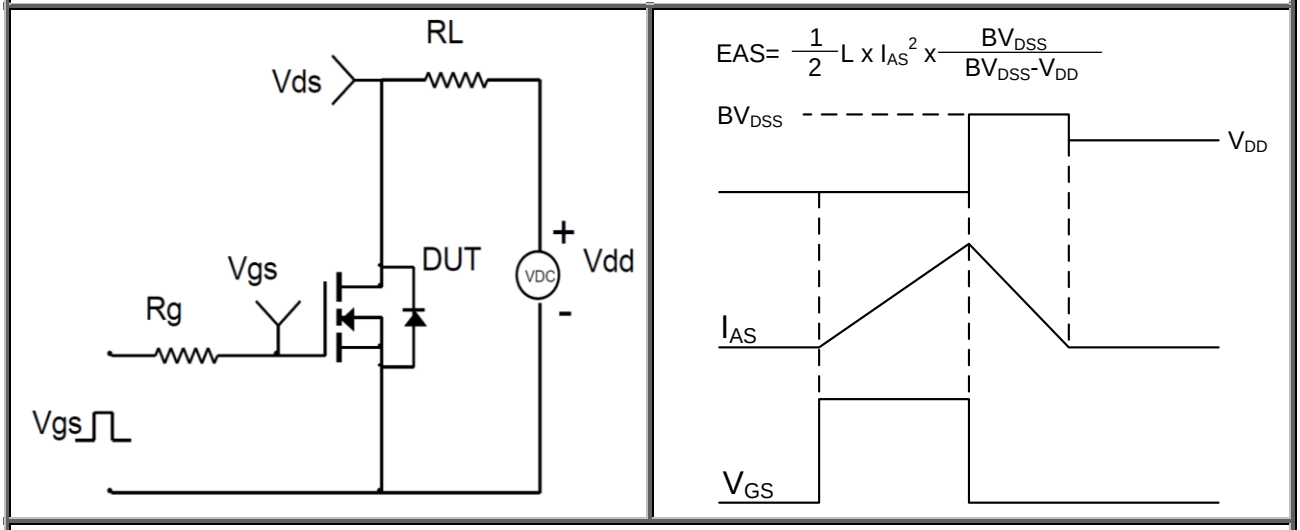
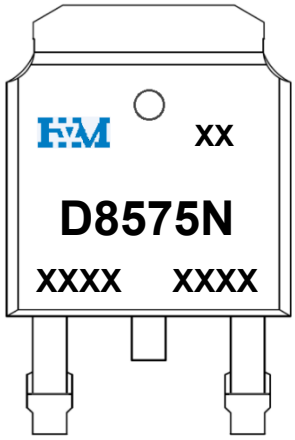


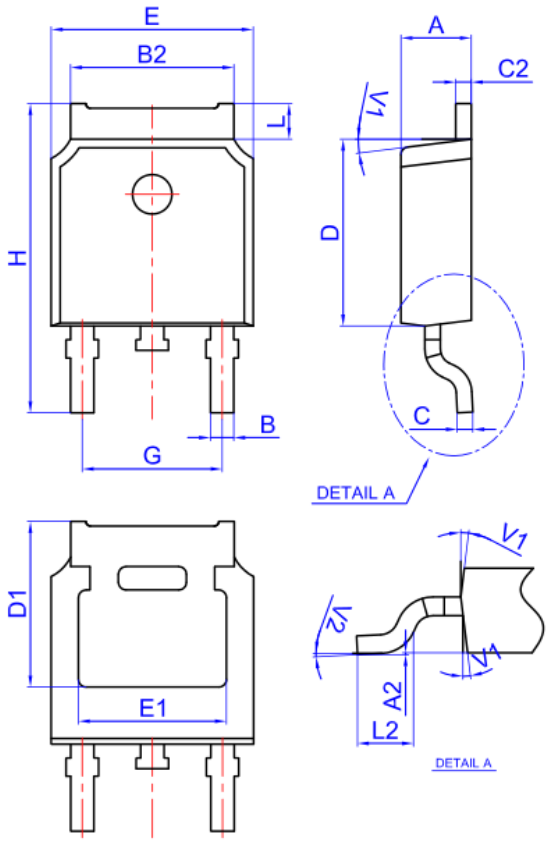
Fig 14: Unclamped Inductive Switching Test Circuit and Waveforms

Marking Information



1st line： HM Logo（left） Coding（right）Changed with Machine Table
2nd line： Device Package and Part Number and Channel and Version
3rd line： Lot number And Date code（XXXX XXXX）
① XXXX： Wafer Lot Number Code Changed with Lot Number
② XXXX： Date code changed with Date Number，Factory Number

TO-252 Dimension



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

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