SHARP

TECHNICAL LITERATURE

MODEL NO. **LM038QB1R10**

DOC.NO. LC99555

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** The technical literature is subject to be changed without notice **

SHARP CORPORATION

PRESENTED BY M. Ise

M.ISE
DEPARTMENT GENERAL MANAGER
ENGINEERING DEPARTMENT I
DUTY LCD DEVELOPMENT CENTER
DUTY LIQUID CRYSTAL DISPLAY GROUP
SHARP CORPORATION

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[Precautions]

1) Industrial (Mechanical) design of the product in which this LCD module will be incorporated must be made so that the viewing angle characteristics of the LCD may be optimized.
This module's viewing angle is illustrated in Fig.1.

θ y MIN. < viewing angle < θ y MAX.

(For the specific values of θ y MIN., and θ y MAX., refer to the Table 9.)

Please consider the optimum viewing conditions according to the purpose when installing the module.

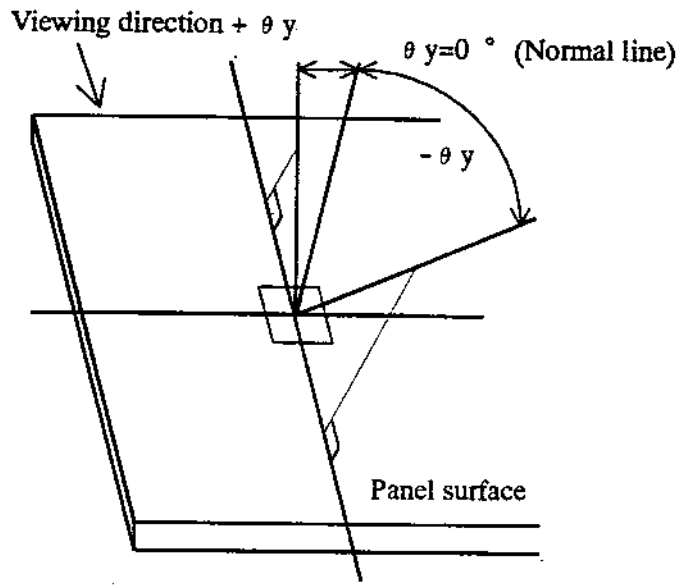

Fig.1 Definition of viewing angle

2) When installing the module, pay attention and handle carefully not to allow any undue stress such as twist or bend.

3) Since the front polarizer is easily damaged. Please pay attention not to scratch on its face.
It is recommended to use a transparent acrylic resin board or other type of protective panel on the surface of the LCD module to protect the polarizer, LCD panel, etc..

4) If the surface of the LCD panel is required to be cleaned, wipe it swiftly with cotton or other soft cloth. If it is not still clear completely, blow on and wipe it.

5) Water droplets, etc. must be wiped off immediately since they may cause color changes, staining, etc., if it remained for a long time.

6) Since LCD is made of glass substrate, dropping the module or banging it against hard objects may cause cracking or fragmentation.

7) Since CMOS LSIs are equipped in this module, following countermeasures must be taken to avoid electrostatics charge.

1. Operator

Electrostatic shielding clothes shall be had because it is feared that the static electricity is electrified to human body in case that operator have a insulating garment.

2. Equipment

There is a possibility that the static electricity is charged to equipment which have a function of peeling or mechanism of friction(EX: Conveyer, soldering iron, working table), so the countermeasure (electrostatic earth:$1\times10^{8}\Omega$) should be made.

3. Floor

Floor is an important part to leak static electricity which is generated from human body or equipment. There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth:$1\times10^{8}\Omega$) should be made.

4. Humidity

Humidity of working room may lower electrostatics generating material's resistance and have something to prevent electrifying. So, humidity should be kept over 50% because humidity less than 50 % may increase material's electrostatic earth resistance and it become easy to electrify.

5. Transportation/storage

The measure should be made for storage materials because there is a possibility that the static electricity, which electrify to human body or storage materials like container by friction or peeling, cause the dielectric charge.

6. Others

The laminator is attached on the surface of LCD module to prevent from scratches, fouling and dust. It should be peeled off unhurriedly with using static eliminator.

And also, static eliminator should be installed to prevent LCD module from electrifying at assembling line.

8) Don't use any materials which emit gas from epoxy resin(amines' hardener) and silicon adhesive agent (dealcohol or deoxym) to prevent change polarizer color owing to gas.

9) Avoid to expose the module to the direct sun-light, strong ultraviolet light, etc. for a long time.

10) If stored at temperatures under specified storage temperature, the LC may freeze and be deteriorated. If storage temperature exceed the specified rating, the molecular orientation of the LC may change to that of a liquid, and they may not revert to their original state. Therefore, the module should be always stored at normal room temperature.

11) Disassembling the LCD module can cause permanent damage and should be strictly avoided.

12) Procedure insert mating connector

When the mating connector is inserted, it should be parallel to the used connector of LCD module and it should be inserted on horizontal firm base. When the mating connector is attempted to be fixed to LCD connector, it should be inserted properly in order not to create a gap as shown "A".

Please insert the connector as both edge is placed to the connect position of LCD connector.

1)Method of correct insert

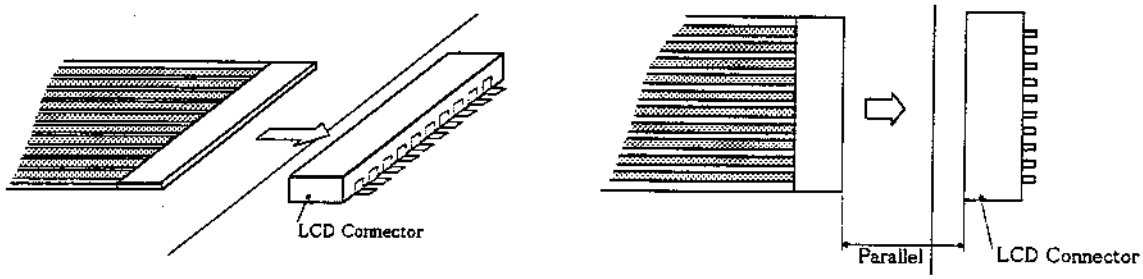

Fig.2

2)Method of wrong insert

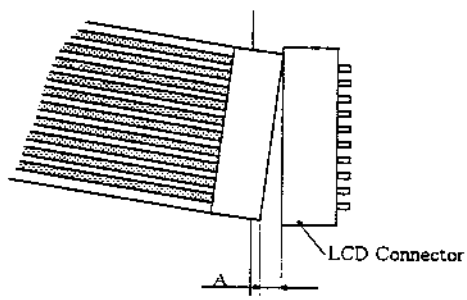

Fig.3

13) This specification describes display quality in case of no gray scale. Since display quality can be affected by gray scale methods, display quality shall be carefully evaluated for the usability of LCD module in case gray scale is displayed on the LCD module.

14) The module should be driven according to the specified ratings to avoid permanent damage.
DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Especially the power ON/OFF sequence shown on Page 21 should be kept to avoid latch-up of drive LSI and application of DC voltage to LCD panel

15) It is a characteristic of LCD to maintain the displaying pattern when the pattern is applied for a long time.(Image retention) To prevent image retention, please do not apply the fixed pattern for along time by pre-installing such programs at your side.

16) This phenomena (image retention) is not deterioration of LCD. If it happens, you can remove it by applying different patterns.

WARNING

Don't use any materials which emit following gas from epoxy resin (amines' hardener) and silicone adhesive agent (dealcohol or deoxym) to prevent change polarizer color owing to gas.

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1. Application

This data sheet is to introduce the specification of LM038QB1R10, Passive matrix type monochrome LCD module.

2. Construction and Outline

Construction: 320× 240 dots monochrome display module consisting of an LCD panel, PWB (printed wiring board) with electric components mounted onto, TCP (tape carrier package) to connect the LCD panel and PWB electrically, and bezel to fix them mechanically.

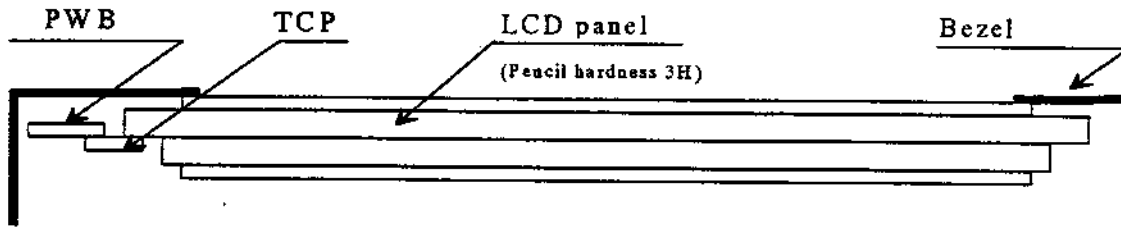


Fig.4

Outline :See Fig. 16

Connection :See Fig. 16 and Table 6

3. Mechanical Specification

Table1

Parameter	Specifications	Unit
Outline dimensions	96.6±0.5(W)×72.4±0.5(H)×4 MAX(D *1)	mm
Active area	76.79(W) × 57.59(H)	mm
Display format	320(W) × 240(H)	mm
Dot size	0.23(W) × 0.23(H)	-
Dot spacing	0.01	mm
*2 Base color	Normally white *3	-
Weight	approx.35	g

*1 4 MAX value is not including connector area.

*2 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*3 Positive-type display

Display data "H" : ON → Black

Display data "L" : OFF → White

4. Absolute Maximum Ratings

4-1. Electrical absolute maximum ratings

Table 2

Parameter	Symbol	Min	Max	Unit	Remark
Logic supply voltage	VDD-VSS	0	6.0	V	Ta=25℃
	VDD-VSL	-0.3	47.0	V	Ta=25℃
	VSS-VSL	-0.3	47.0	V	Ta=25℃
Input signal voltage	VIN-VSS	-0.3	VDD+0.3	V	Ta=25℃
LCD supply voltage	VSH-VSL	-0.3	85.0	V	Ta=25℃
	VBH-VSS	-0.3	7.0	V	Ta=25℃
	VC-VSS	-0.3	VBH+0.3	V	Ta=25℃
	VBL-VSS	-0.3	VBH+0.3	V	Ta=25℃

4-2. Environment Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperature	-25 ℃	+60 ℃	0 ℃	+40 ℃	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)				3 directions(X/Y/Z)
Shock					6 directions(±X±Y±Z)

Note 1) Ta≦40 ℃.....95 % RH Max.

Ta＞40 ℃.....Absolute humidity shall be less than Ta=40 ℃ /95 % RH.

Note 2) Since this module does not have enough mounting mechanism , it is impossible to conduct vibration and shock test at SHARP side. Therefore ,assemble it to your cabinet and then these test shall be conducted to be satisfied the necessary condition in according with (1) and (2) condition (Non operating).

(1)Vibration test

Table 4

Frequency	10 Hz～57 Hz	57 Hz～500 Hz
Vibration level	-	9.8 m/s^2
Vibration width	0.075 mm	-
Interval	10 Hz～500 Hz～10 Hz/11.0 min	

2 hours for each direction of X/Y/Z (6 hours as total)

(2)Shock test

Acceleration : 490 m/s2

Pulse width : 11 ms

3 times for each directions of ±X/±Y/±Z

Note 4) As opto-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 ℃ and it becomes stable.

5. Electrical Specifications

5-1. Electrical characteristics

Table 5-1

Ta=25 ℃ VDD= 3.3 V±10 % 1/tFRM=75 Hz Duty ratio:1/244

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Remark
Supply voltage(Logic)	V_{DD}	Ta=0～40℃	3.0	3.3	3.6	V	
Supply voltage(LCD) (for optimum contrast)	V_{SH}	Ta=0℃	-	T.B.D.	T.B.D.	V	Note 1
		Ta=25℃	(15.5)	(16.4)	(17.3)	V	
		Ta=40℃	T.B.D.	T.B.D.	-	V	
	V_C	Ta=0～	-	$V_{SH}/12$	-	V	
	$\lvert V_C - V_{SL}\rvert$ (V_{SL})	Ta=0～40℃	$\lvert V_{SH}-V_C\rvert$ (-0.1)	$\lvert V_{SH}-V_C\rvert$	$\lvert V_{SH}-V_C\rvert$ (+0.1)	V	
	V_{BH}	Ta=0～40℃	V_C x 2 (-0.02)	V_C x 2	V_C x 2 (+0.02)	V	
	V_{BL}	Ta=0～40℃	0	0	0	V	
Input voltage	V_{IN}	Ta=0～40℃ "High" level	0.8 V_{DD}	—	V_{DD}	V	
		Ta=0～40℃ "Low" level		—	0.2 V_{DD}	V	
Supply current (Logic)	I_{DD1}	Ta=25℃ VDD=3.3V	—	(0.15)	(0.2)	mA	Note 2
Supply current (Logic)	I_{DD2}		—	(0.18)	(0.25)	mA	Note 3
Supply current (LCD)	I_{SH1}	Ta=25℃ VDD=3.3V	—	(0.08)	(0.12)	mA	Note 2
	I_{SL1}		—	(-0.08)	(-0.12)	mA	
	I_{BH1}		—	(0.2)	(0.3)	mA	
	I_{BL1}		—	(-0.2)	(-0.3)	mA	
	I_{C1}		—	(±0.2)	(±0.3)	mA	Note 4
	I_{SL2}	Ta=25℃ VDD=3.3V	—	(0.08)	(0.12)	mA	Note 3
	I_{SL2}		—	(-0.08)	(-0.12)	mA	
	I_{BH2}		—	(1.5)	(2.0)	mA	
	I_{BL2}		—	(-1.5)	(-2.0)	mA	
	I_{C2}		—	(±1.5)	(±2.0)	mA	Note 4

5-2. Input capacitance

Table 5-2

Parameter	Symbol	Input signal	Typ.	Unit
Input capacitance	C_{in1}	YD	50	pF
	C_{in2}	XCK	100	pF
	C_{in3}	LP,M,D0-3	120	pF
	C_{in4}	DISP	150	pF

Note 1) Under the following conditions;

Fixed as V_{BL} =0V

For the adjustment of the LCD contrast, change the each voltage under the condition mentioned below.

$|V_{SH}-V_C| = |V_C-V_{SL}|$,

$|V_{BH}-V_C| = |V_C-V_{BL}|$

$V_{SH} > V_{BH} > V_C > V_{BL} \geqq V_{SS} > V_{SL}$

V_{SH}/V_C=12

(See Fig.5)

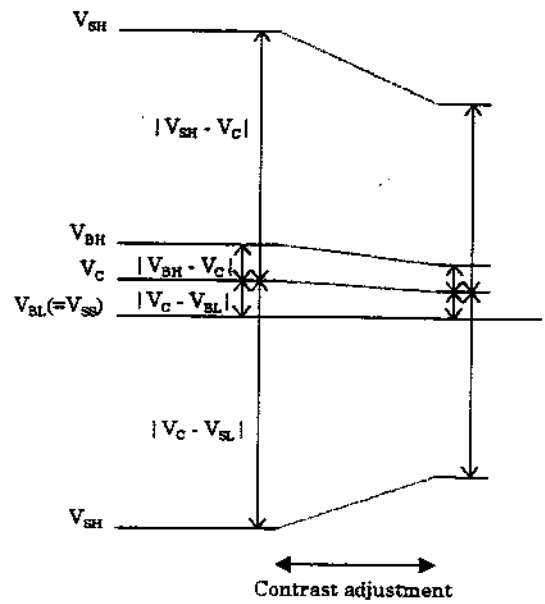
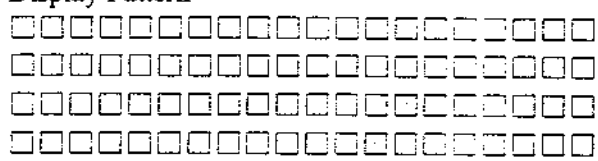


Fig.5

Note 2) Frame Frequency = 75 Hz , Supply voltage(LCD) is typ.value at 25℃.

Display pattern = all digits ON (D0-4 = "H")

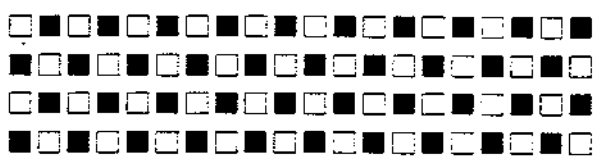
Display Pattern



Note 3) Frame Frequency = 75 Hz , Supply voltage(LCD) is typ.value at 25℃.

Display pattern = black/white checkerboard pattern

Display Pattern



Note 4) This current capacity is needed in the electric power supply for Vc voltage ,because AC current (the amount of positive current and negative current is the same) runs actually, although the average Ic value is almost 0.

5-3. Interface signals

<LCD>

Table 6

Pin No.	Symbol	Description	Level
1	VSS	Ground potential	-
2	LP	Input data latch signal	"H" -> "L"
3	VDD	Power supply for logic	-
4	D0	Display data signal	"H"(ON),"L"(OFF)
5	D1	Display data signal	"H"(ON),"L"(OFF)
6	D2	Display data signal	"H"(ON),"L"(OFF)
7	D3	Display data signal	"H"(ON),"L"(OFF)
8	V_C	Power supply for LCD (center voltage)	-
9	DISP	Display control signal	"H"(ON),"L"(OFF)
10	VSS	Ground potential	-
11	XCK	Data input clock signal	"H" -> "L"
12	V_{BL}	Power supply for LCD (for segment)	-
13	NC	No connection	-
14	NC	No connection	-
15	NC	No connection	-
16	NC	No connection	-
17	V_{BH}	Power supply for LCD (for segment)	-
18	M	Alternating signal	-
19	YD	Scan Start-up signal	"H"
20	V_{SH}	Power supply for LCD (for common)	-
21	VSS	Ground potential	-
22	V_{SL}	Power supply for LCD (for common)	-
23	NC	No connection	-
24	NC	No connection	-

Used connector : FH12-24S-0.5SH (HIROSE)

Correspondence connector : FFC/FPC(0.5mm pitch 24pin)

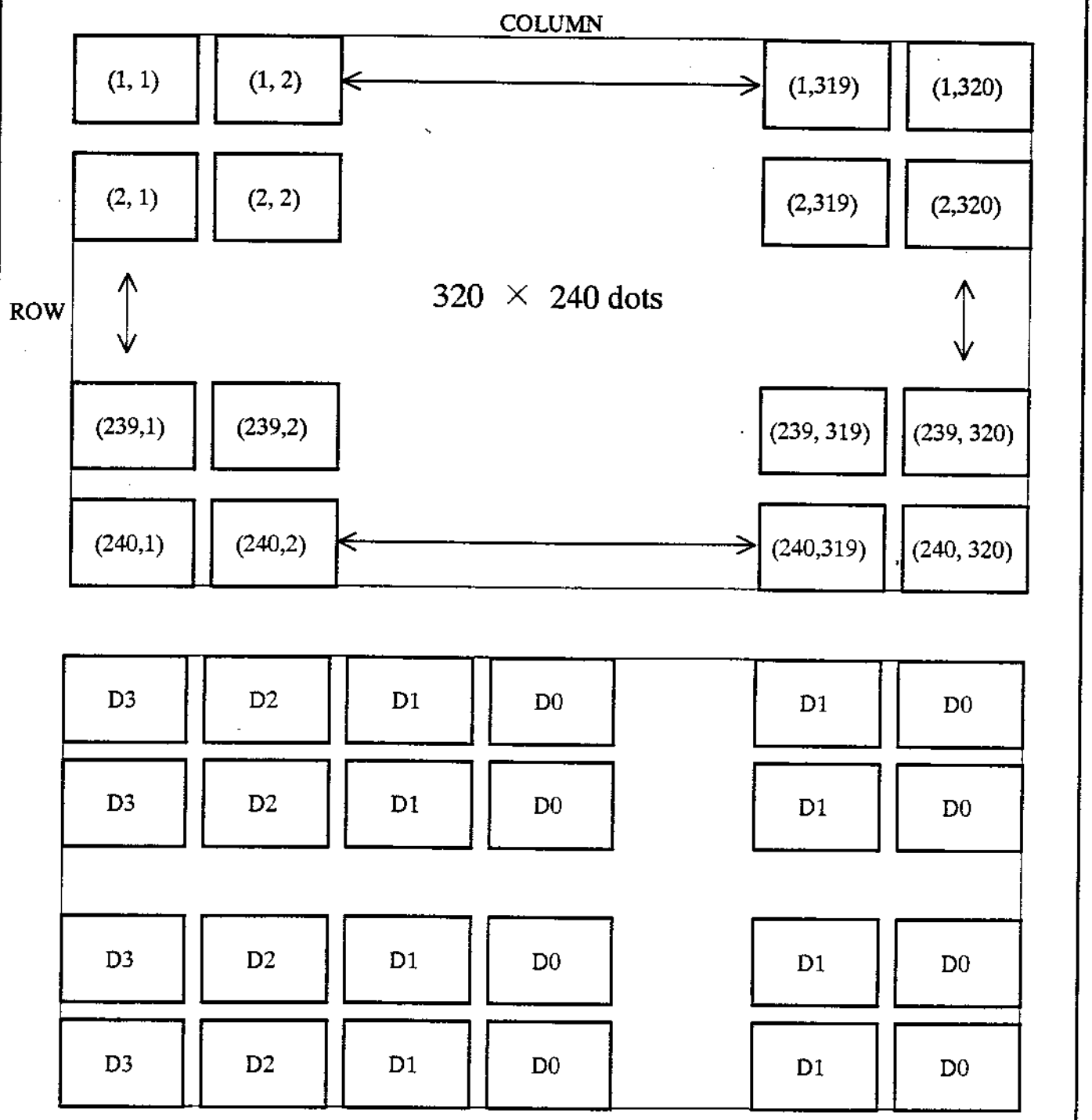
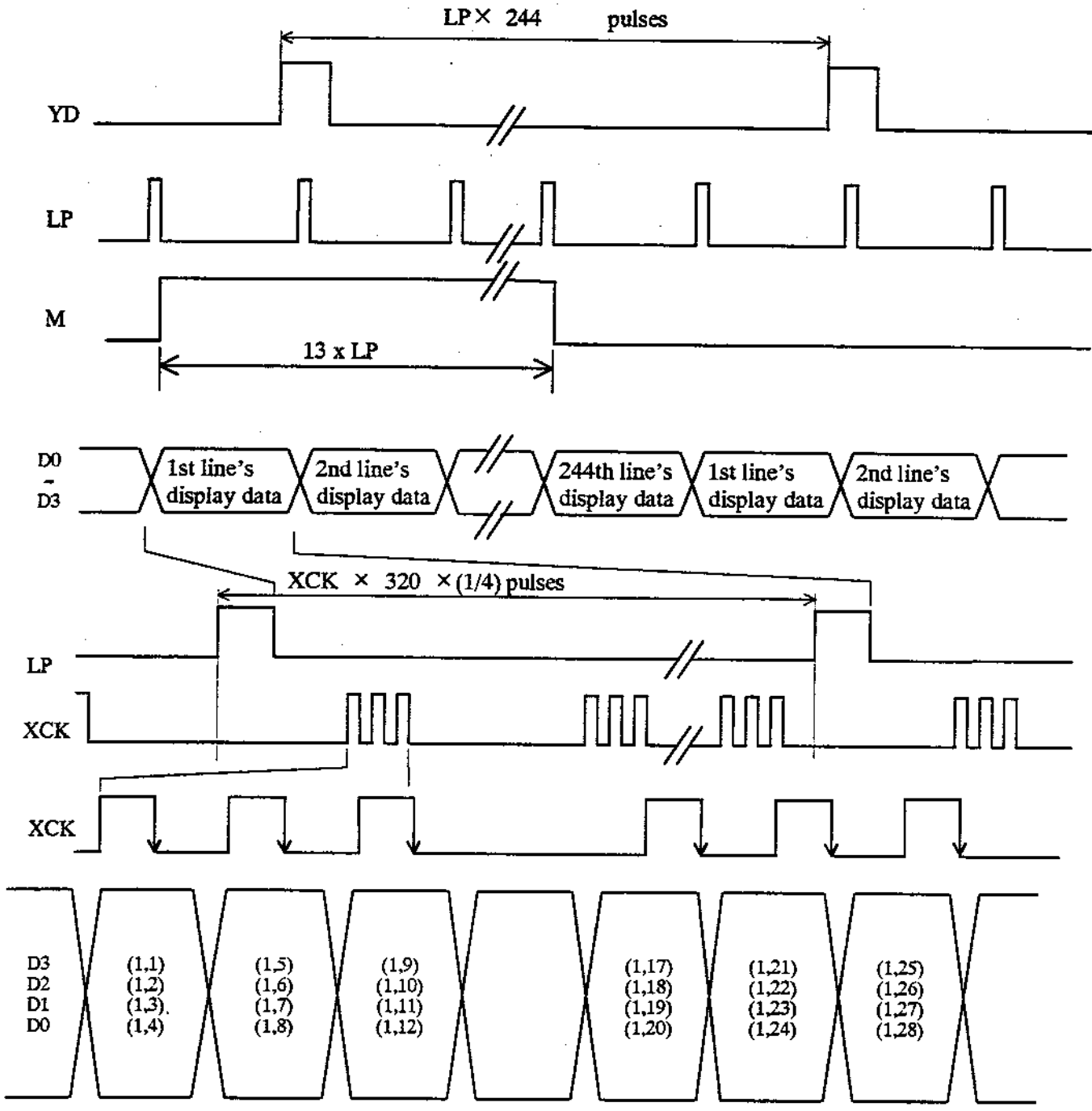


Fig.6 Dot chart of display area



*Electrical and optical characteristics are specified by above condition.

Fig. 7 Data input timing chart

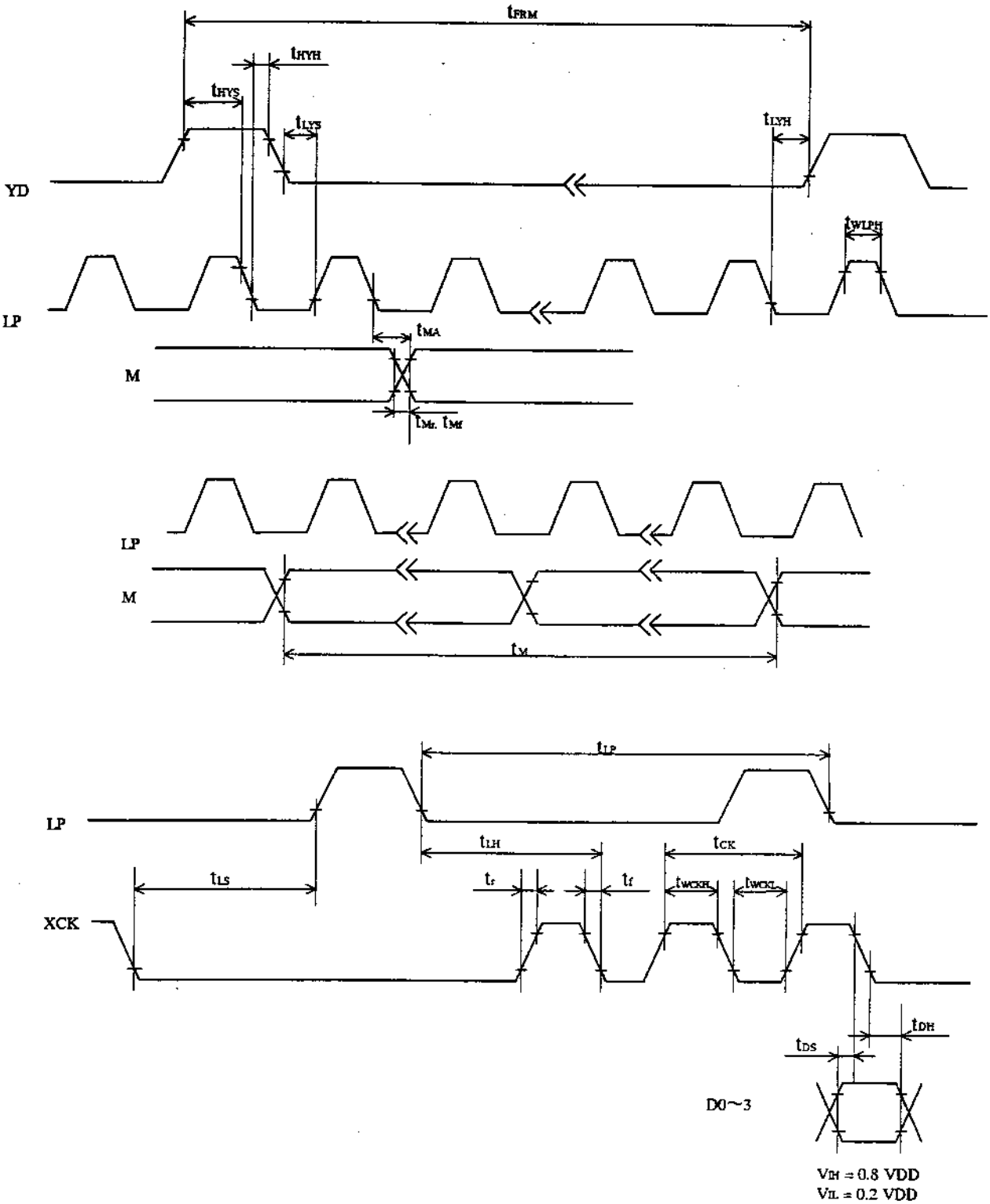


Fig.8 Interface timing chart

5-4. Interface timing ratings

Table 8

Ta=25 ℃,VDD=3.3±10% V

Item	Symbol	Rating			Unit
		MIN.	TYP.	MAX.	
Frame cycle *2 *3	t_{FRM}	8.33		16.94	ms
XCK signal clock cycle	t_{CK}	82			ns
"H" level clock width	t_{WCKH}	30			ns
"L" level clock width	t_{WCKL}	30			ns
LP signal clock cycle *4	t_{LP}			75	μs
LP signal "H" level pulse width	t_{WLPH}	250			ns
Data set up time	t_{DS}	25			ns
Data hold time	t_{DH}	30			ns
YD signal "H" level set up time	t_{HYS}	125			ns
"H" level hold time	t_{HYH}	125			ns
"L" level set up time	t_{LYS}	100			ns
"L" level hold time	t_{LYH}	100			ns
LP ↑ allowance time from XCK ↓	t_{LS}	200			ns
XCK ↑ allowance time from LP ↓	t_{LH}	200			ns
M signal clock cycle	t_M	13×2×LP ↓			pulses
M ↑ ↓ allowance time from LP ↓	t_{MA}			50	ns
M signal rise/fall time	t_{Mr},t_{Mf}			50	ns
Input signal rise/fall time *1	t_r,t_f			20	ns

*1 When LCD module is operated by high speed of XCK(Shift clock), (t_{CK} - t_{WCKH} -t_{WCKL}) /2 is maximum.

*2 LCD module functions at the minimum frame cycle of 8.33 ms(Maximum frame frequency of 120 Hz).
Owing to the characteristics of LCD module, "shadowing" will become more eminent as frame frequency goes up, while flicker will be reduced.

*3 According to our experiments, frame cycle of 8.33 ms Min. or frame frequency of 120 Hz Max. will demonstrate optimum display quality in terms of flicker and "shadowing". But since judgment of display quality is subjective and display quality such as "shadowing" is pattern dependent, it is recommended that decision of frame frequency, to which power consumption of the LCD module is proportional, be made based on your own through testing on the LCD module with every possible patterns displayed on it

*4 The intervals of one LP fall and next must be always the same, and LPs must be input continuously.

6. Module Driving Method

6-1. Circuit configuration

Fig. 13 shows the block diagram of the module's circuitry.

6-2. Display face configuration

The display consists of 320×240 dots as shown in Fig.6.

The interface is single panel with double drive to be driven at 1/244 duty ratio.

6-3. Input data and control signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (320 dots) will be sequentially transferred in the form of 4 bit parallel data through shift registers from top left of the display together with clock signal (XCK).

When input of one row (320 dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP) then, the corresponding drive signals will be transmitted to the 320 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.
While the data of 1st row are being displayed, the data of 2nd row are entered.
When data for 320 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 244th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage. if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-form shall be inverted at every display frame to prevent the generation of such DC voltage. Control signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.

To minimize data transfer speed of XCK clock the LSI has the system of transferring 4 bit parallel data through the 4 lines of shift registers.

Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 4 bit display data shall input to data input pins of D0-3 .

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the right end of the display face is first selected, and the adjacent driver LSI left next side is selected when data of 80 dot (20XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the left end of the display face.

Thus data input will be made through 4 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static display.

The timing chart of input signals are shown in Fig.8 and Table 8.

7. Optical Characteristics

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction($\theta x = \theta y = 0°$) will be MAX..

Table 9 Ta = 25 ℃, V_{DD}= 3.3 V, V_{SH}-V_{SS} = Vmax

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	Co>2.0	$\theta y = 0°$	(-20)	-	(25)		Note 1)
		θy		$\theta x = 0°$	(-20)	-	(25)		
Contrast ratio		Co	$\theta x = \theta y = 0°$		(6)	(10)	-	-	Note2)
Response time	Rise	τr	$\theta x = \theta y = 0°$		-	(250)	(300)	ms	Note3)
	Decay	τd	$\theta x = \theta y = 0°$		-	(250)	(300)	ms	

Note 1) The viewing angle range is defined as shown Fig.9.

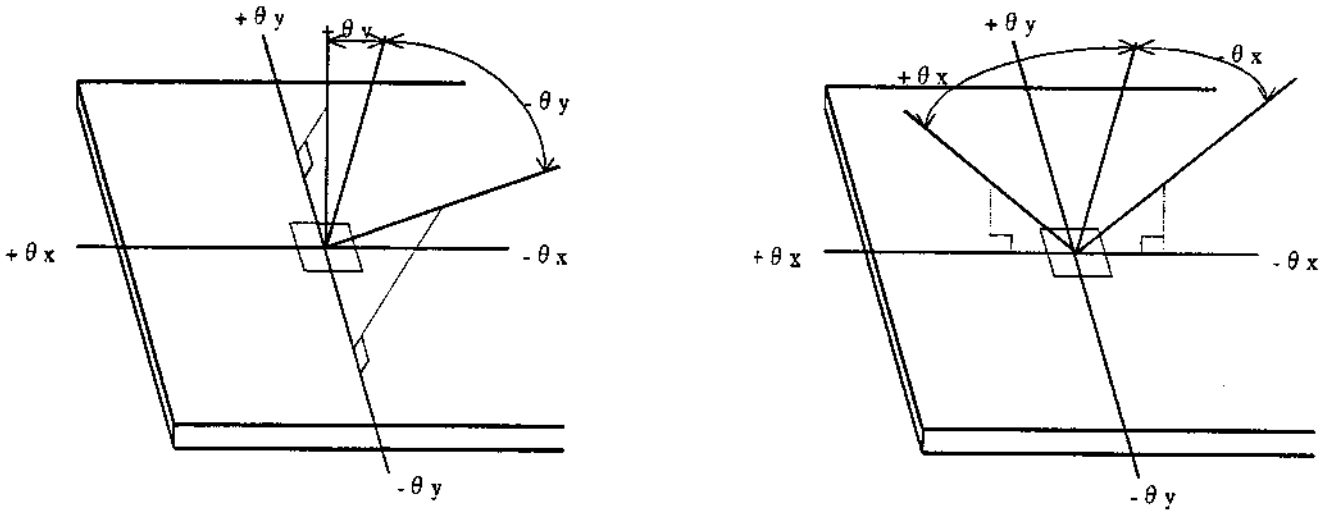


Fig.9 Definition of Viewing Angle

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixes "White" at Vmax}}{\text{Luminance(brightness) all pixes "dark" at Vmax}}$$

(measured as shown in Fig.10.)

Vmax is defined in Fig.11.

Note 3) The response characteristics of photo-detector output are measured as shown in Fig.12, assuming that input signals are applied so as to select and deselect the dot to be measured, in the optical characteristics test method shown in Fig.10.

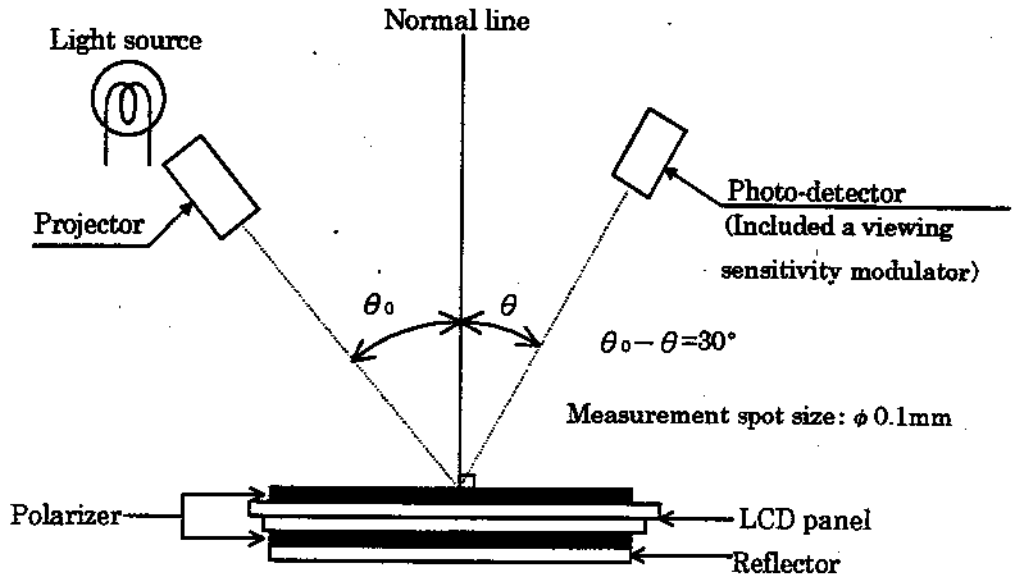


Fig.10 Optical Characteristics Test Method

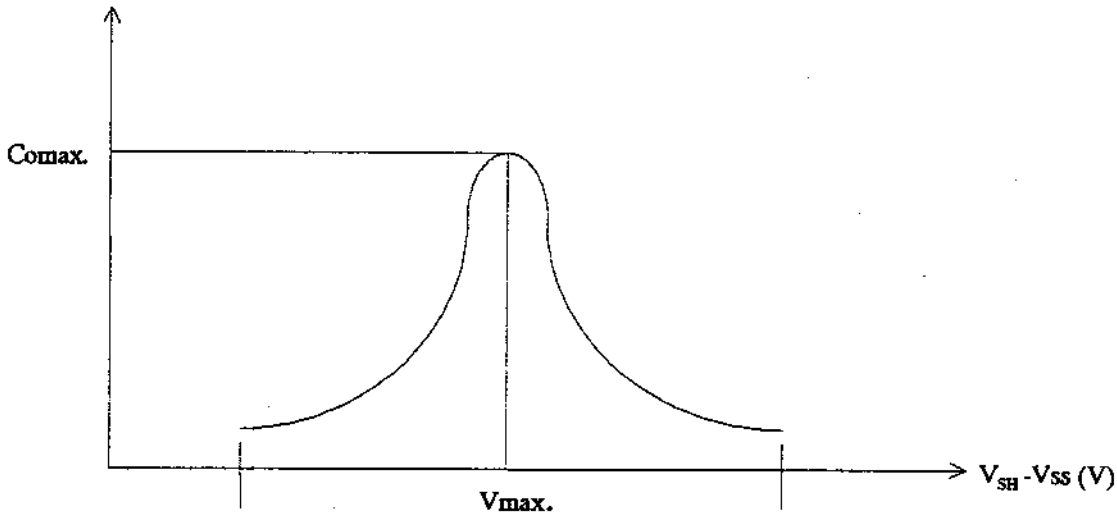
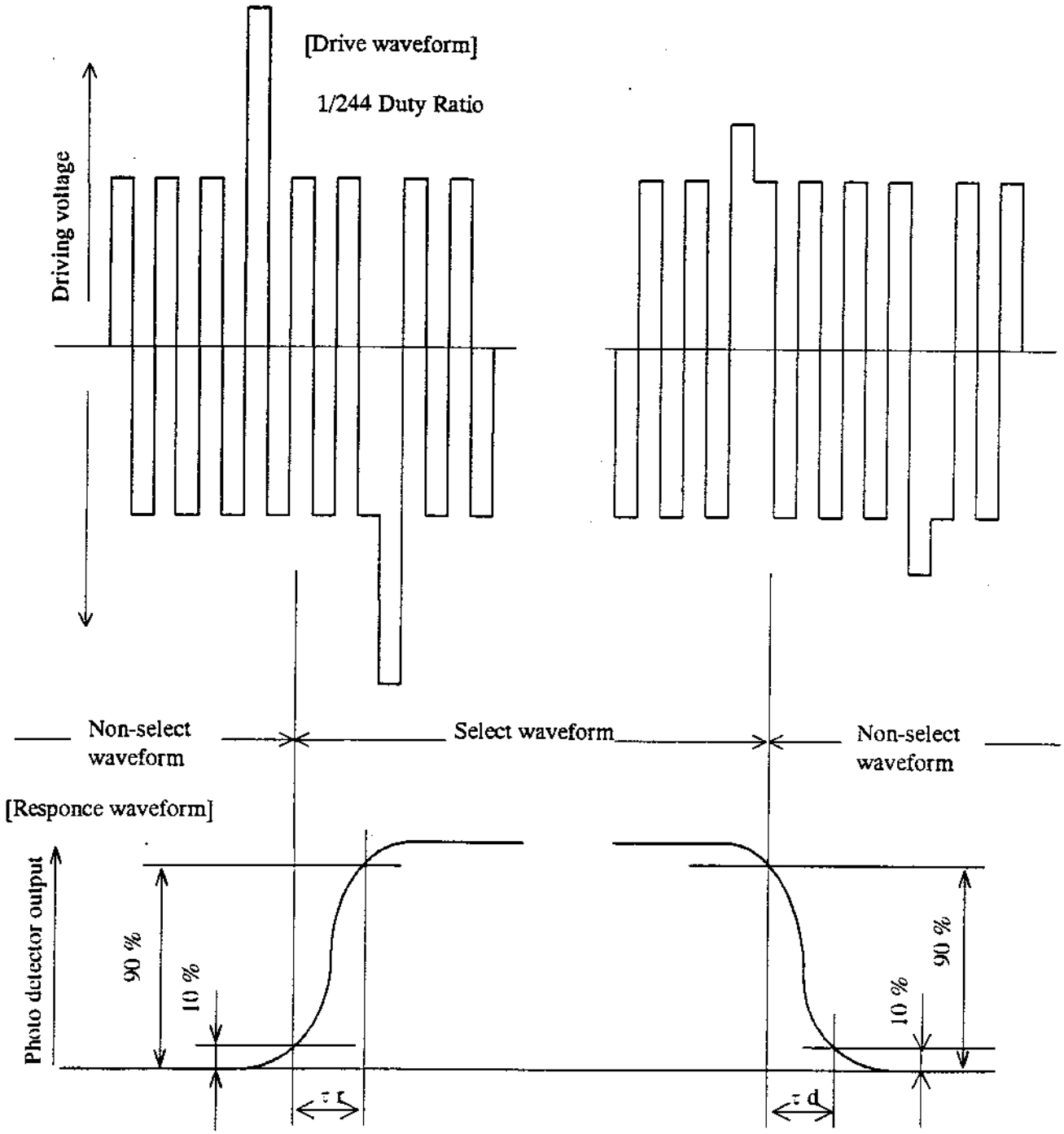


Fig.11 Definition of Vmax



τ r : Rise time

τ d : Decay time

Fig.12 Definition of Response time

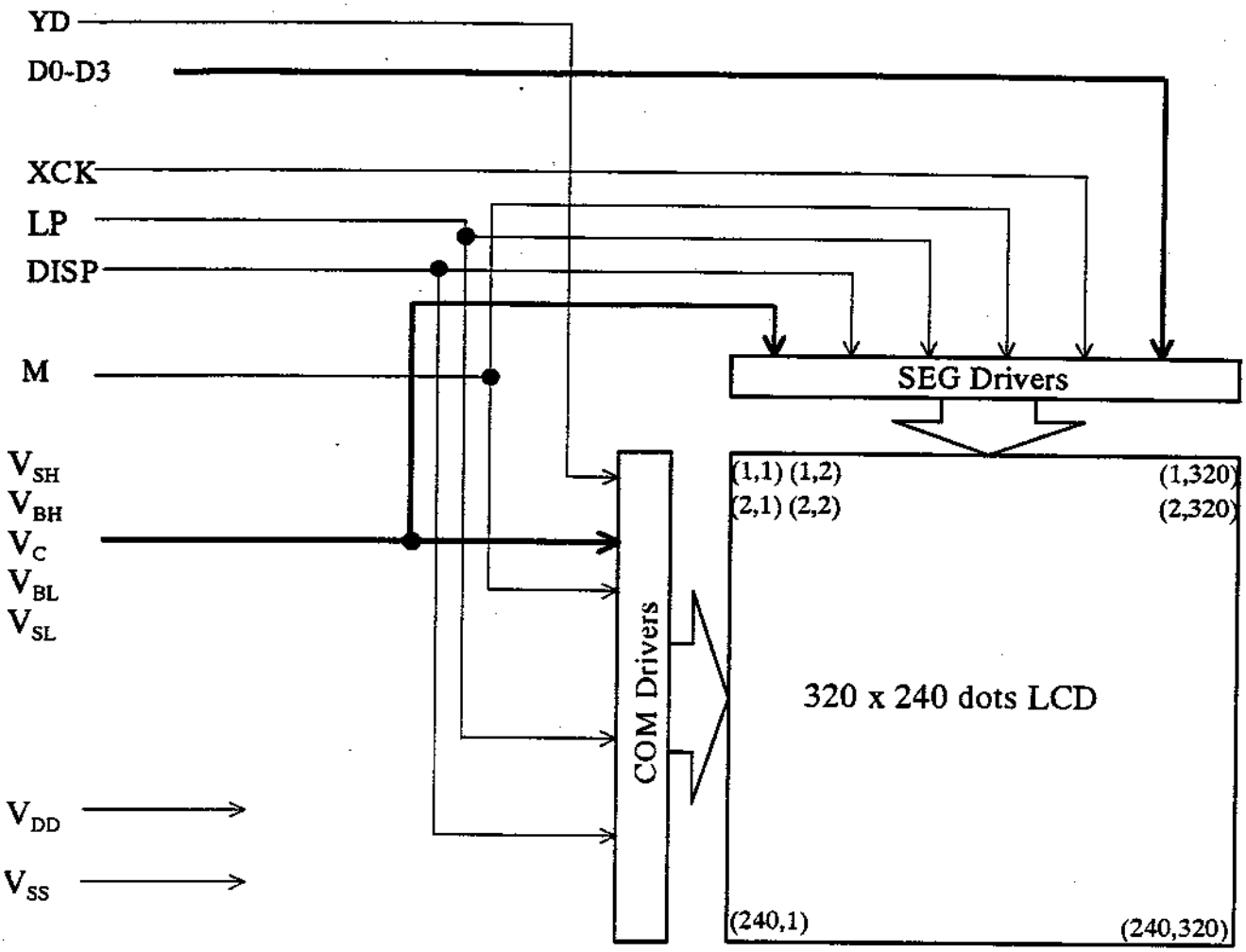


Fig. 13 Circuit block diagram

8. Supply voltage sequence condition

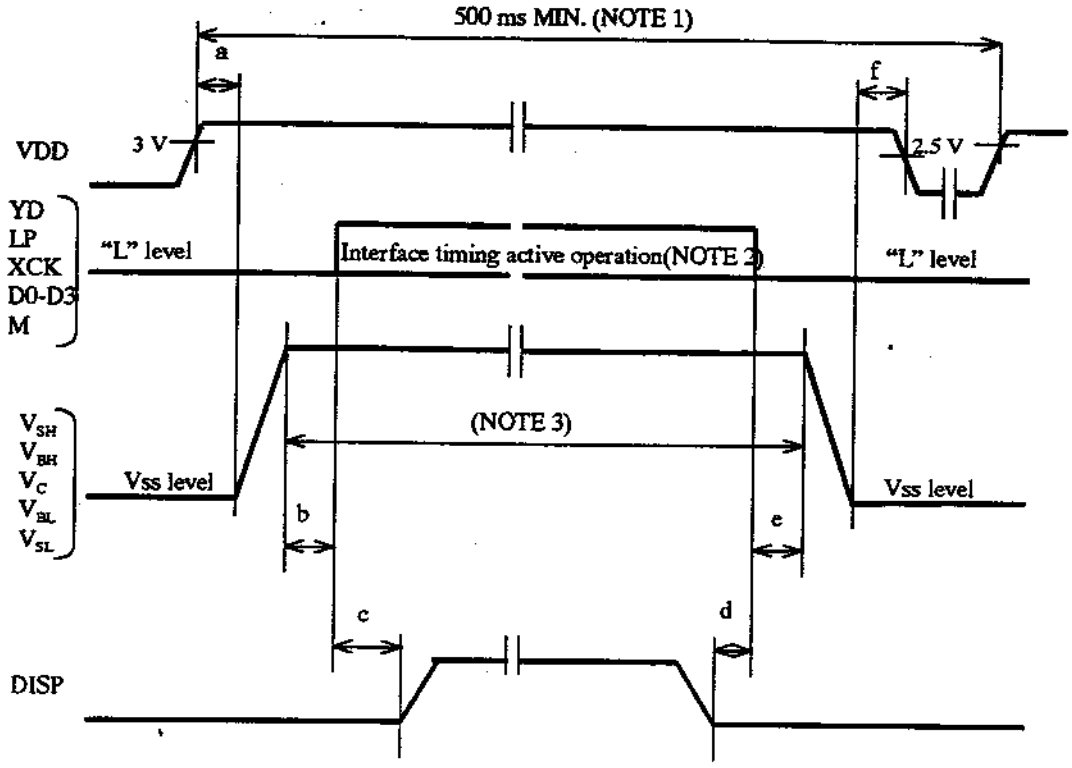


Fig.14 Supply voltage sequence condition

	POWER ON	
Symbol	Allowable value	
a	0 ms MIN.	50ms MAX
b	0 ms MIN.	-
c	50 ms MIN	-

	POWER OFF	
Symbol	Allowable value	
d	0 ms MIN.	-
e	0 ms MIN.	-
f	0 ms MIN	50ms MAX

(NOTE 1) Power ON/OFF cycle time. All signals and power line shall be in accordance with above sequence in case of power ON/OFF.

Keep the following condition for all the periods

$V_{SH} \geqq V_{BH} \geqq V_C \geqq V_{BL} \geqq V_{SS} \geqq V_{SL}$

(NOTE 2) The signals which comply with the interface timing in Fig. 7, Fig.8, and Table 8, must be input.

(NOTE 3) The power supply voltages which comply with the electrical characteristics in Table 5-1 must be input.

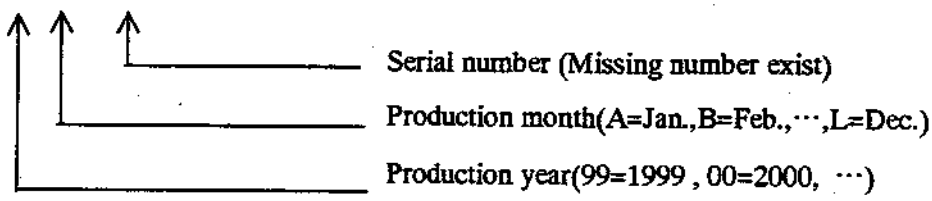
9. Applicable inspection standard

The LCD module shall meet the following inspection standard : S-U-(T.B.D.)

10.Lot Number

Lot number is shown at the position mentioned in Fig.13 in accordance with the following numbering rule.

(Example) 99 E 00001



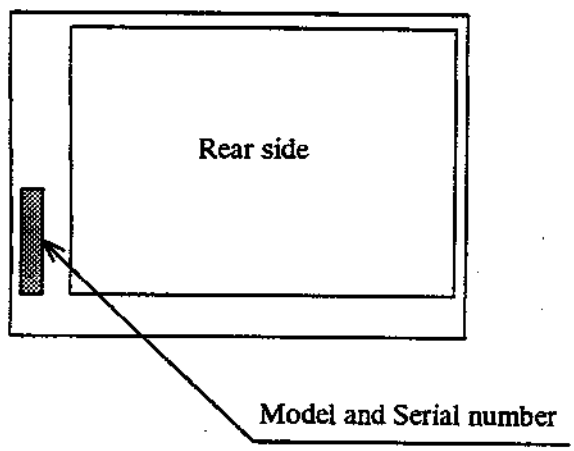
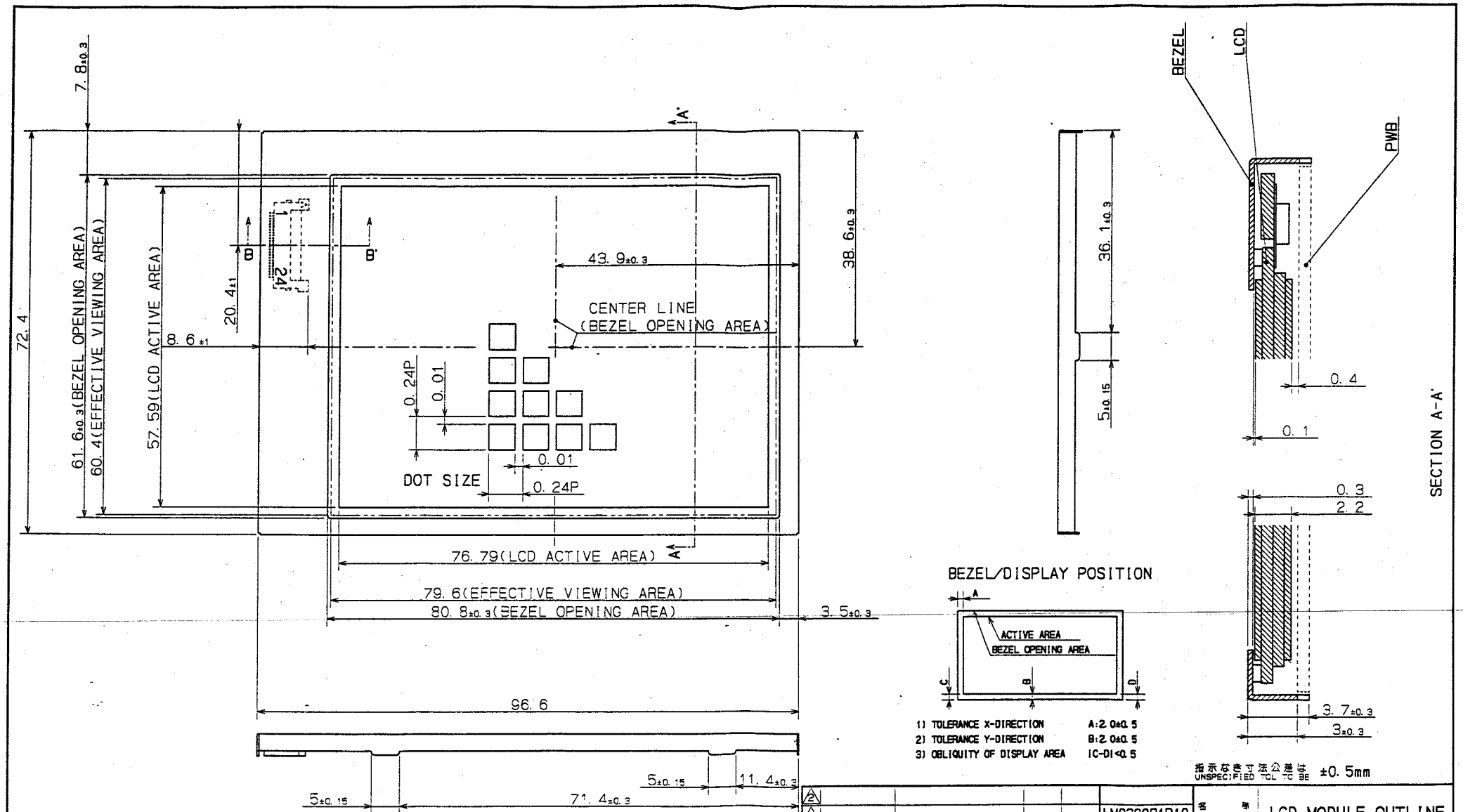


Fig. 15



指示なき寸法公差は UNSPECIFIED TOL TO BE ±0.5mm

2					LM038QB1R10	名称 NAME: LCD MODULE OUTLINE DIMENSIONS
1	年月日 DATE	改定記事 RIVISE	整理No	担当 PREPA	適用機種 MODEL	
	材質 MATERIAL	板厚 THICKNESS	仕上 FINSH		尺度 SCALE: 1.5/1	記号 SYMBOL: 320×240
						部品コード PARTS CODE
設計 DESIGN: E.Horisaki	写図 TRACE	検図 CHECK	検図 CHECK	承認 APPROVE	SHARP CORPORATION	作成日付 DATE: 1999・06・01・
					シャープ株式会社 液晶奈良(事本)	図番 DRAWING. No
					発行部門 デューティー開発センター第1技術部	